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1-Gbit Double-Date-Rate-Three SDRAM
DDR3 SDRAM
EU RoHS HF Compliant Products

Data Sheet

Rev. 1

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	Initial version

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1 Overview

This chapter gives an overview of the 1-Gbit Double-Data-Rate-Three SDRAM product family and describes its main characteristics.

1.1 Features

The 1-Gbit Double-Data-Rate-Three SDRAM offers the following key features:

- 1.5 V ±0.075 V Power Supply
  1.5 V ±0.075 V (SSTL_15) compatible I/O
- DRAM organizations with 8/16 data in/outputs
- Double Data Rate architecture:
  – two data transfers per clock cycle
  – eight internal banks for concurrent operation
- Programmable CAS Latency: 6, 7, 8, 9, 10, 11, 12, 13 and 14 supported
- Programmable Burst Length: 4/8 with both nibble sequential and interleave mode.
- Differential clock inputs (CK and $\overline{CK}$)
- Bi-directional, differential data strobes (DQS and $\overline{DQS}$) are transmitted / received with data. Edge aligned with read data and center-aligned with write data.
- DLL aligns DQ and DQS transitions with clock
- DQS can be disabled for single-ended data strobe operation
- Commands entered on each positive clock edge, data and data mask are referenced to both edges of DQS
- Data masks (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality
- Auto-Precharge operation for read and write bursts
- Auto-Refresh, Self-Refresh and power saving Power-Down modes
- Operating temperature range 0°C to 85°C for standard use.
- Operating temperature range -40°C to 85°C for industrial use.
- Average Refresh Period 7.8 μs at a T_{CASE} lower than 85 °C, 3.9 μs between 85 °C and 95 °C
- Asynchronous RESET pin supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported • 1KB page size for x8; 2KB page size for x16
- Packages: PG-TFBGA-78(×8)；PG-TFBGA-96(×16)
- RoHS Compliant, HF Products[1)]
- All Speed grades faster than DDR3–400 comply with DDR3–400 timing specifications when run at a clock rate of 200 MHz.

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.
For more information please visit **http://www.scsemicon.com/**

TABLE 1
Performance Table

SCS Speed Code			–13K	15H	–19F	Unit	Note
DRAM Speed Grade		DDR3	–1600	–1333	–1066		
CAS-RCD-RP latencies			11–11–11	9–9–9	7–7–7	t_{CK}	
Max. Clock Frequency	CL5	f_{CK5}	667	667	667	MHz	
	CL6	f_{CK6}	800	800	800	MHz	
	CL7	f_{CK7}	1066	1066	1066	MHz	
	CL8	f_{CK8}	1066	1066	1066	MHz	
	CL9	f_{CK9}	1333	1333	--	MHz	
	CL10	f_{CK10}	1333	1333	--	MHz	
	CL11	f_{CK11}	1600	--	--	MHz	
	CL12	f_{CK12}	--	--	--	MHz	
	CL13	f_{CK13}	--	--	--	MHz	
	CL14	f_{CK14}	--	--	--	MHz	
Min. RAS-CAS-Delay		t_{RCD}	13.125	12.5	15	ns	
Min. Row Precharge Time		t_{RP}	13.125	12.5	15	ns	
Min. Row Active Time		t_{RAS}	45	45	45	ns	
Min. Row Cycle Time		t_{RC}	58.125	57.5	60	ns	
Precharge-All (8 banks) command period		t_{PREA}	15	15	18	ns	1)2)

1) This t_{PREA} value is the minimum value at which this chip will be functional.
2) *Precharge-All command for an 4 bank device will equal to t_{RP} + 1 × t_{CK} or t_{nRP} + 1 × nCK, depending on the speed bin, where t_{nRP} = RU{ t_{RP} / $t_{CK(avg)}$ } and t_{RP} is the value for a single bank precharge.*

1.2 Description

The 1-Gbit DDR3 DRAM is a high-speed Double-Data-Rate-Two CMOS Synchronous DRAM device containing 1,073,741,824 bits and internally configured as an octal bank DRAM.

The 1-Gbit device is organized as 8 Mbit ×16 I/O ×8 banks or 16 Mbit ×8 I/O ×8 banks. These synchronous devices achieve high speed transfer rates starting at 400 Mb/sec/pin for general applications. See **Table 1** for performance figures.

The device is designed to comply with all DDR3 DRAM key features:

1. Posted $\overline{\text{CAS}}$ with additive latency.
2. Write latency = read latency - 1.
3. Normal and weak strength data-output driver.
4. Off-Chip Driver (OCD) impedance adjustment.
5. On-Die Termination (ODT) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{\text{CK}}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS-$\overline{\text{DQS}}$ pair in a source synchronous fashion.

A 17 bit address bus for ×8 organised components and a 16 bit address bus for ×16 components is used to convey row, column and bank address information in a RAS- CAS Multiplexing style.

The DDR3 device operates with a 1.5 V ± 0.075 V power supply. An Auto-Refresh and Self-Refresh mode is provided along with various power-saving power-down modes.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

The DDR3 SDRAM is available in TFBGA package.

TABLE 2
Ordering Information for RoHS Compliant Products

Product Type[1]	Org.	Speed	CAS-RCD-RP Latencies[2][3][4]	Clock (MHz)	Package	Note[5]
Standard Temperature Range (0°C - 85°C)						
DDR3-1600 (11-11-11)						
HXB15H1G800CF-13K	×8	DDR3-1600	11-11-11	800	PG-TFBGA-78	
HXB15H1G160CF-13K	×16	DDR3-1600	11-11-11	800	PG-TFBGA-96	
DDR3-1333 (9-9-9)						
HXB15H1G800CF-15H	×8	DDR3-1333	9-9-9	667	PG-TFBGA-78	
HXB15H1G160CF-15H	×16	DDR3-1333	9-9-9	667	PG-TFBGA-96	
DDR3-1066 (7-7-7)						
HXB15H1G800CF-19F	×8	DDR3-1066	5-5-5	533	PG-TFBGA-78	
HXB15H1G160CF-19F	×16	DDR3-1066	5-5-5	533	PG-TFBGA-96	
Industrial Temperature Range (-40°C - 85°C)						
DDR3-1600 (11-11-11)						
HXB15H1G800CF-13K	×8	DDR3-1600	11-11-11	800	PG-TFBGA-78	
HXB15H1G160CF-13K	×16	DDR3-1600	11-11-11	800	PG-TFBGA-96	
DDR3-1333 (9-9-9)						
HXB15H1G800CF-15H	×8	DDR3-1333	9-9-9	667	PG-TFBGA-78	
HXB15H1G160CF-15H	×16	DDR3-1333	9-9-9	667	PG-TFBGA-96	
DDR3-1066 (7-7-7)						
HXB15H1G800CF-19F	×8	DDR3-1066	5-5-5	533	PG-TFBGA-78	
HXB15H1G160CF-19F	×16	DDR3-1066	5-5-5	533	PG-TFBGA-96	

1) For detailed information regarding product type of SCSemicon please see chapter "Product Nomenclature" of this data sheet.
2) CAS: Column Address Strobe
3) RCD: Row Column Delay
4) RP: Row Precharge
5) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

2 Configuration

This chapter contains the chip configuration.

2.1 Configuration for PG-FBGA-78

The chip configuration of a DDR3 SDRAM is listed by function in **Table 3**. The abbreviations used in the Ball#/Buffer Type columns are explained in **Table 4** and **Table 5** respectively.

TABLE 3
Configuration

Ball#	Name	Ball Type	Buffer Type	Function
Clock Signals ×8 Organization				
F7	CK	I	SSTL	**Clock Signal CK, CK**
G7	$\overline{\text{CK}}$	I	SSTL	
G9	CKE	I	SSTL	**Clock Enable**
Control Signals ×8 Organization				
F3	$\overline{\text{RAS}}$	I	SSTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
G3	$\overline{\text{CAS}}$	I	SSTL	
H3	$\overline{\text{WE}}$	I	SSTL	
H2	$\overline{\text{CS}}$	I	SSTL	**Chip Select**
Address Signals ×8 Organization				
J2	BA0	I	SSTL	**Bank Address Bus 2:0**
K8	BA1	I	SSTL	
J3	BA2	I	SSTL	
K3	A0	I	SSTL	**Address Signal 13:0, Address Signal 10/Autoprecharge**
L7	A1	I	SSTL	
L3	A2	I	SSTL	
K2	A3	I	SSTL	
L8	A4	I	SSTL	
L2	A5	I	SSTL	
M8	A6	I	SSTL	
M2	A7	I	SSTL	
N8	A8	I	SSTL	
M3	A9	I	SSTL	
H7	A10	I	SSTL	
	AP	I	SSTL	
M7	A11	I	SSTL	
K7	A12	I	SSTL	
N3	A13	I	SSTL	

Ball#	Name	Ball Type	Buffer Type	Function
Data Signals ×8 Organization				
B3	DQ0	I/O	SSTL	**Data Signal Lower Byte 7:0**
C7	DQ1	I/O	SSTL	
C2	DQ2	I/O	SSTL	
C8	DQ3	I/O	SSTL	
E3	DQ4	I/O	SSTL	
E8	DQ5	I/O	SSTL	
D2	DQ6	I/O	SSTL	
E7	DQ7	I/O	SSTL	
Data Strobe ×8 Organization				
C3	DQS	I/O	SSTL	**Data Strobe Byte**
D3	$\overline{\text{DQS}}$	I/O	SSTL	
B7	DM/TDQS	I/O	SSTL	
A7	NU/$\overline{\text{TDQS}}$	I/O	SSTL	
Reset ×8 Organization				
N2	$\overline{\text{RESET}}$	I	SSTL	**Active Low Asynchronous Reset**
Power Supplies ×8 Organization				
E1	V_{REFDQ}	AI	–	**Reference voltage for DQ**
J8	V_{REFCA}	AI	SSTL	**Reference voltage for CA**
B9, C1, E2, E9,	V_{DDQ}	PWR	–	**I/O Driver Power Supply**
A2, A9, D7, G2, G8, K1, K9, M1, M9	V_{DD}	PWR	–	**Power Supply**
B2, B8, C9, D1,D9	V_{SSQ}	PWR	–	**Power Supply**
A1, A8, B1, D8, F2, F8, J1, J9, L1, L9, N1, N9	V_{SS}	PWR	–	**Power Supply**
H8	ZQ	PWR	–	**Reference Pin for ZQ calibration**
Not Connected ×8 Organization				
A3, F1, F9, H1, H9, J7, N7	NC	NC	–	**Not Connected**
Other Balls ×8 Organization				
G1	ODT	I	SSTL	**On-Die Termination Control**

TABLE 4
Abbreviations for Ball Type

Abbreviation	Description
I	Standard input-only ball. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 5
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_15)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding ball has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

FIGURE 1
Chip Configuration for x8 Components in TFBGA–78 (Top view)

1	2	3	4	5	6	7	8	9
Vss	V_{DD}	NC		A		NU/$\overline{\text{TDQS}}$	V_{SS}	V_{DD}
Vss	V_{SSQ}	DQ0		B		DM/TDQS	V_{SSQ}	V_{DDQ}
V_{DDQ}	DQ2	DQS		C		DQ1	DQ3	V_{SSQ}
V_{SSQ}	DQ6	$\overline{\text{DQS}}$		D		V_{DD}	V_{SS}	V_{SSQ}
V_{REFDQ}	V_{DDQ}	DQ4		E		DQ7	DQ5	V_{DDQ}
NC	V_{SS}	$\overline{\text{RAS}}$		F		CK	V_{SS}	NC
ODT	V_{DD}	$\overline{\text{CAS}}$		G		$\overline{\text{CK}}$	V_{DD}	CKE
NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$		H		A10/AP	ZQ	NC
Vss	BA0	BA2		J		NC	V_{REFCA}	V_{SS}
V_{DD}	A3	A0		K		A12/$\overline{\text{BC}}$	BA1	V_{DD}
Vss	A5	A2		L		A1	A4	V_{SS}
V_{DD}	A7	A9		M		A11	A6	V_{DD}
V_{SS}	$\overline{\text{RESET}}$	A13		N		NC	A8	V_{SS}

2.2 Configuration for PG-FBGA-96

The chip configuration of a DDR3 SDRAM is listed by function in **Table 6**. The abbreviations used in the Ball#/Buffer Type columns are explained in **Table 7** and **Table 8** respectively.

TABLE 6
Configuration

Ball#	Name	Ball Type	Buffer Type	Function
Clock Signals ×16 Organization				
J7	CK	I	SSTL	**Clock Signal CK, CK**
K7	$\overline{CK}$	I	SSTL	
K9	CKE	I	SSTL	**Clock Enable**
Control Signals ×16 Organization				
J3	$\overline{RAS}$	I	SSTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
K3	$\overline{CAS}$	I	SSTL	
L3	$\overline{WE}$	I	SSTL	
L2	$\overline{CS}$	I	SSTL	**Chip Select**
Address Signals ×16 Organization				
M2	BA0	I	SSTL	**Bank Address Bus 2:0**
N8	BA1	I	SSTL	
M3	BA2	I	SSTL	
N3	A0	I	SSTL	**Address Signal 12:0, Address Signal 10/Autoprecharge**
P7	A1	I	SSTL	
P3	A2	I	SSTL	
N2	A3	I	SSTL	
P8	A4	I	SSTL	
P2	A5	I	SSTL	
R8	A6	I	SSTL	
R2	A7	I	SSTL	
T8	A8	I	SSTL	
R3	A9	I	SSTL	
L7	A10	I	SSTL	
	AP	I	SSTL	
R7	A11	I	SSTL	
N7	A12/$\overline{BC}$	I	SSTL	

Ball#	Name	Ball Type	Buffer Type	Function
Data Signals ×16 Organization				
D7	DQU0	I/O	SSTL	**Data Signal Lower Byte 7:0**
C3	DQU1	I/O	SSTL	
C8	DQU2	I/O	SSTL	
C2	DQU3	I/O	SSTL	
A7	DQU4	I/O	SSTL	
A2	DQU5	I/O	SSTL	
B8	DQU6	I/O	SSTL	
A3	DQU7	I/O	SSTL	
E3	DQL0	I/O	SSTL	**Data Signal Upper Byte 15:8**
F7	DQL1	I/O	SSTL	
F2	DQL2	I/O	SSTL	
F8	DQL3	I/O	SSTL	
H3	DQL4	I/O	SSTL	
H8	DQL5	I/O	SSTL	
G2	DQL6	I/O	SSTL	
H7	DQL7	I/O	SSTL	
Data Strobe ×16 Organization				
F3	DQSL	I/O	SSTL	**Data Strobe Upper Byte**
G3	$\overline{\text{DQSL}}$	I/O	SSTL	
C7	DQSU	I/O	SSTL	**Data Strobe Lower Byte**
B7	$\overline{\text{DQSU}}$	I/O	SSTL	
Reset ×16 Organization				
T2	$\overline{\text{RESET}}$	I	SSTL	**Active Low Asynchronous Reset**
Data Mask ×16 Organization				
D3	DMU	I	SSTL	**Data Mask Upper Byte**
E7	DML	I	SSTL	**Data Mask Lower Byte**
Power Supplies ×16 Organization				
H1	V_{REFDQ}	AI	–	**Reference voltage for DQ**
M8	V_{REFCA}	AI	–	**Reference voltage for CA**
A1, A8, C1, C9, D2, E9, F1, H2, H9	V_{DDQ}	PWR	–	**I/O Driver Power Supply**
B2, D9, G7, K2, K8, N1, N9, R1, R9	V_{DD}	PWR	–	**Power Supply**
B1, B9, D1, D8, E2, E8, F9, G1, G9	V_{SSQ}	PWR	–	**Power Supply**
A9, B3, E1, J2, J8, M1, M9, P1, P9, T1, T9	V_{SS}	PWR	–	**Power Supply**
L8	ZQ	PWR	–	**Reference Pin for ZQ calibration**

Not Connected ×16 Organization				
Ball#	**Name**	**Ball Type**	**Buffer Type**	**Function**
J1, J9, L1, L9, M7, T3, T7	NC	NC	–	**Not Connected**
Other Balls ×16 Organization				
K1	ODT	I	SSTL	**On-Die Termination Control**

TABLE 7
Abbreviations for Ball Type

Abbreviation	Description
I	Standard input-only ball. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 8
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_15)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding ball has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

FIGURE 2
Chip Configuration for x16 Components in TFBGA–96 (Top view)

1	2	3	4	5	6	7	8	9
V_{DDQ}	DQU5	DQU7		A		DQU4	V_{DDQ}	V_{SS}
V_{SSQ}	V_{DD}	V_{SS}		B		$\overline{\text{DQSU}}$	DQU6	V_{SSQ}
V_{DDQ}	DQU3	DQU1		C		DQSU	DQU2	V_{DDQ}
V_{SSQ}	V_{DDQ}	DMU		D		DQU0	V_{SSQ}	V_{DD}
V_{SS}	V_{SSQ}	DQL0		E		DML	V_{SSQ}	V_{DDQ}
V_{DDQ}	DQL2	DQSL		F		DQL1	DQL3	V_{SSQ}
V_{SSQ}	DQL6	$\overline{\text{DQSL}}$		G		V_{DD}	V_{SS}	V_{SSQ}
V_{REFDQ}	V_{DDQ}	DQL4		H		DQL7	DQL5	V_{DDQ}
NC	V_{SS}	$\overline{\text{RAS}}$		J		CK	V_{SS}	NC
ODT	V_{DD}	$\overline{\text{CAS}}$		K		$\overline{\text{CK}}$	V_{DD}	CKE
NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$		L		A10/AP	ZQ	NC
V_{SS}	BA0	BA2		M		NC	V_{REFCA}	V_{SS}
V_{DD}	A3	A0		N		A12/$\overline{\text{BC}}$	BA1	V_{DD}
V_{SS}	A5	A2		P		A1	A4	V_{SS}
V_{DD}	A7	A9		R		A11	A6	V_{DD}
V_{SS}	$\overline{\text{RESET}}$	NC		T		NC	A8	V_{SS}

2.3 Addressing

This chapter describes the DDR3 addressing.

TABLE 9
Addressing

Configuration	128 Mb x 8[1)]	64 Mb x 16[1)]	Note
Bank Address	BA[2;0]	BA[2;0]	
Number of Banks	8	8	
Auto Precharge	A10	A10	
Row Address	A[13:0]	A[12:0]	
Column Address	A[9:0]	A[9:0]	
Number of Column Address Bits	10	10	3)
Number of I/Os	8	16	
Page Size [Bytes]	1024 (1 K)	2048 (2 K)	4)

1) Referred to as 'org'
2) Referred to as 'org'
3) Referred to as 'colbits'
4) PageSize = $2^{colbits} \times org/8$ [Bytes]

3 Electrical Characteristics

This chapter describes the Electrical Characteristics.

3.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device listed in **Table 18** at any time.

TABLE 10
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–0.4	+1.975	V	1) 3)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.4	+1.975	V	1) 3)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	+1.975	V	1)
T_{STG}	Storage Temperature	–55	+100	°C	1)2)

1). Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2). Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

3). VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 11
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{OPER}	Normal Operating Temperature Range	0	+85	°C	1)2)
	Extended Temperature Range (Optional)	-40	+85	°C	1) 3)

1). Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.

2). The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85oC under all operating conditions.

3). Some applications require operation of the DRAM in the Extended Temperature Range between 85oC and 95oc case temperature. Full specifications are supported in this range, but the following additional conditions apply:

a, Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability

b, If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

3.2 DC Characteristics

TABLE 12
Recommended DC Operating Conditions (SSTL_15)

Symbol	Parameter	Rating			Unit	Note
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.425	1.500	1.575	V	1) 2)
V_{DDQ}	Supply Voltage for Output	1.425	1.500	1.575	V	1) 2)

1) Under all conditions, VDDQ must be less than or equal to VDD.
2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

3.3 Input / Output Capacitance

This chapter contains the Input / Output Capacitance.

TABLE 13
Input / Output Capacitance

Symbol	Parameter	DDR3-1600		DDR3-1333		DDR3-1066		Unit
		Min	Max	Min.	Max.	Min.	Max.	
CCK	Input capacitance, CK and $\overline{CK}$	0.8	1.4	0.8	1.4	0.8	1.6	pF
CDCK	Input capacitance delta, CK and $\overline{CK}$	0	0.15	0	0.15	0	0.15	pF
CDDQS	Input capacitance delta, DQS and $\overline{DQS}$	0	0.15	0	0.15	0	0.20	pF
CI	Input capacitance, all other input-only pins	0.75	1.3	0.75	1.3	0.75	1.35	pF
CDI_CTRL	Input capacitance delta, All CTRL input-only pins	-0.4	0.2	-0.4	0.2	-0.5	0.3	pF
CDI_ADD_CMD	Input capacitance delta, All ADD/CMD input-only pins	-0.4	0.4	-0.4	0.4	-0.5	0.5	pF
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	1.5	2.3	1.5	2.5	1.5	2.7	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF
CZQ	Input/output capacitance of ZQ pin	--	3	--	3	--	3	pF

4 Currents Measurement Conditions

This chapter describes the Current Measurement, Specifications and Conditions.

TABLE 19
I_{DD} Measurement Conditions

Parameter	Symbol	Note
Operating One Bank Active-Precharge Current CKE: High; External clock: On; BL: 8a); AL: 0; /CS: High between ACT and PRE; Command, Address, Bank Address Inputs: Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0;	I_{DD0}	
Operating One Bank Active-Read-Precharge Current CKE: High; External clock: On; BL: 8a); AL: 0; /CS: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0;	I_{DD1}	
Precharge Standby Current CKE: High; External clock: On; BL: 8a); AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0;	I_{DD2N}	
Precharge Standby ODT Current CKE: High; External clock: On; BL: 8a); AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registersb);	I_{DD2NT}	
Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; BL: 8a); AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0; Precharge Power DownMode: Slow Exitc)	I_{DD2P0}	
Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; BL: 8a); AL: 0; /CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exitc)	I_{DD2P1}	
Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8a); AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0	I_{DD2Q}	
Active Standby Current CKE: High; External clock: On; BL: 8a); AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0;	I_{DD3N}	
Active Power-Down Current CKE: Low; External clock: On; BL: 8a); AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0	I_{DD3P}	

Parameter	Symbol	Note
Operating Burst Read Current CKE: High; External clock: On; BL: 8a); AL: 0; /CS: High between RD; Command, Address, Bank Address Inputs; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0;	I_{DD4R}	
Operating Burst Write Current CKE: High; External clock: On; BL: 8a); AL: 0; /CS: High between WR; Command, Address, Bank Address Inputs: Data IO: seamless read data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at HIGH;	I_{DD4W}	
Burst Refresh Current CKE: High; External clock: On; BL: 8a); AL: 0; /CS: High between REF; Command, Address, Bank Address Inputs; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: REF command every nREC ; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0;	I_{DD5B}	
Self-Refresh Current: Normal Temperature Range **TCASE**: 0 - 85 oC; Auto Self-Refresh (ASR): Disabledd);Self-Refresh Temperature Range (SRT): Normale); CKE: Low; External clock: Off; CK and /CK: LOW; CL:; BL: 8a); AL: 0; /CS, Command, Address, Bank Address Inputs, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: MID-LEVEL	I_{DD6}	
Self-Refresh Current: Extended Temperature Range **TCASE**: 0 - 95 oC; Auto Self-Refresh (ASR): Disabledd);Self-Refresh Temperature Range (SRT): Extendede); CKE: Low; External clock: Off; CK and /CK: LOW; CL; BL: 8a); AL: 0; /CS, Command, Address, Bank Address Inputs, Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: MIDLEVEL	I_{DD6ET}	
Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL; BL: 8a)f); AL: CL-1; /CS: High between ACT and RDA; Command, Address, Bank Address Inputs: Data IO: read data burst with different data between one burst and the next one ; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, Output Buffer and RTT: Enabled in Mode Registersb); ODT Signal: stable at 0;	I_{DD7}	

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit
d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range
f) Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

TABLE 15
Definition for I_{DD}

Parameter	Description
LOW	Defined as $V_{IN} \leq V_{IL.AC.MAX}$
HIGH	Defined as $V_{IN} \geq V_{IH.AC.MIN}$
STABLE	Defined as inputs are stable at a HIGH or LOW level
FLOATING	Defined as inputs are $V_{REF} = V_{DDQ} / 2$
SWITCHING	Defined as: Inputs are changing between high and low every other clock (once per two clocks) for address and control signals, and inputs changing between high and low every other clock (once per clock) for DQ signals not including mask or strobes

TABLE 16
I_{DD} Specification

Symbol	-13K	-15H	-19F	Unit	Note
	DDR3 - 1600	DDR3 - 1333	DDR3 - 1066		
	Max.	Max.	Max.		
I_{DD0}	52	50	48	mA	
I_{DD1}	68	65	62	mA	
I_{DD2N}	26	25	22	mA	
I_{DD2NT}	32	30	26	mA	
I_{DD2P0}	12	12	12	mA	
I_{DD2P1}	15	15	15	mA	
I_{DD2Q}	26	25	22	mA	
I_{DD3N}	40	38	35	mA	
I_{DD3P}	26	25	22	mA	
I_{DD4R}	165	145	120	mA	
I_{DD4W}	145	125	110	mA	
I_{DD5B}	110	105	100	mA	
I_{DD6}	12	12	12	mA	
I_{DD6ET}	15	15	15	mA	
$I_{DD6\ low\ power}$	TBD	TBD	TBD	mA	
I_{DD7}	225	215	210	mA	

1) $0\,°\leq T_{CASE} \leq 85\,$℃.

5 Speed Grade Definitions

TABLE 17
Speed Grade Definition - DDR3–1600

Speed Grade			**DDR3–1600**		**Unit**	**Note**
SCS Sort Name			**–13k**			
CAS-RCD-RP latencies			**11–11–11**		t_{CK}	
Parameter		**Symbol**	**Min.**	**Max.**	**—**	
Clock Period	@ CL = 5	t_{CK}	3.0	3.3	ns	1)2)3)4)8)9)
	@ CL = 6	t_{CK}	2.5	3.3	ns	1)2)3)8)
	@ CL = 7	t_{CK}	1.875	<2.5	ns	1)2)3)4)8)
	@ CL = 8	t_{CK}	1.875	<2.5	ns	1)2)3)8)
	@ CL = 9	t_{CK}	1.5	<1.875	ns	1)2)3)4)8)
	@ CL = 10	t_{CK}	1.5	<1.875	ns	1)2)3)8)
	@ CL = 11	t_{CK}	1.25	<1.5	ns	1)2)3)
Row Active Time		t_{RAS}	35	9*tREFI	ns	
Row Cycle Time		t_{RC}	48.75	—	ns	
RAS-CAS-Delay		t_{RCD}	13.75	—	ns	
Row Precharge Time		t_{RP}	13.75	—	ns	

TABLE 18
Speed Grade Definition - DDR3–1333/1066

Speed Grade			DDR3–1333		DDR3–1066		Unit	Note
SCS Sort Name			–15H		–19F			
CAS-RCD-RP latencies			9–9–9		7–7–7		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Period	@ CL = 5	t_{CK}	3.0	3.3	3.0	3.3	ns	1)2)3)4)6)7)9)
	@ CL = 6	t_{CK}	2.5	3.3	2.5	3.3	ns	1)2)3)6)7)
	@ CL = 7	t_{CK}	1.875	<2.5	1.875	<2.5	ns	1)2)3)4)7)
	@ CL = 8	t_{CK}	1.875	<2.5	1.875	<2.5	ns	1)2)3)7)
	@ CL = 9	t_{CK}	1.5	<1.875	—	—	ns	1)2)3)4)
	@ CL = 10	t_{CK}	1.5	<1.875	—	—	ns	1)2)3)
Row Active Time		t_{RAS}	36	9*tREFI	37.5	9*tREFI	ns	
Row Cycle Time		t_{RC}	49.5	—	50.625	—	ns	
RAS-CAS-Delay		t_{RCD}	13.5	—	13.125	—	ns	
Row Precharge Time		t_{RP}	13.5	—	13.125	—	ns	

Absolute Specification (TOPER; VDDQ = VDD = 1.5V +/- 0.075 V);

1) The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2) tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
3) tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4) 'Reserved' settings are not allowed. User must program a different value.
5) 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature.
6) Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7) Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8) Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9) DDR3 SDRAM devices supporting optional down binning to CL=7, 9 and CL=11, and tAA/ tRCD/tRP must be 13.125 ns. SPD settings must be programmed to match. For example, DDR3-1866 RD devices supporting down binning to DDR3-1600K or DDR3-1333 H9 or 1066 G7 should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333 H9 and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600 PB.
10) For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.

6 Package Outline

This chapter contains the package dimension figures.

Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

FIGURE 3
Package Outline PG-FBGA-78

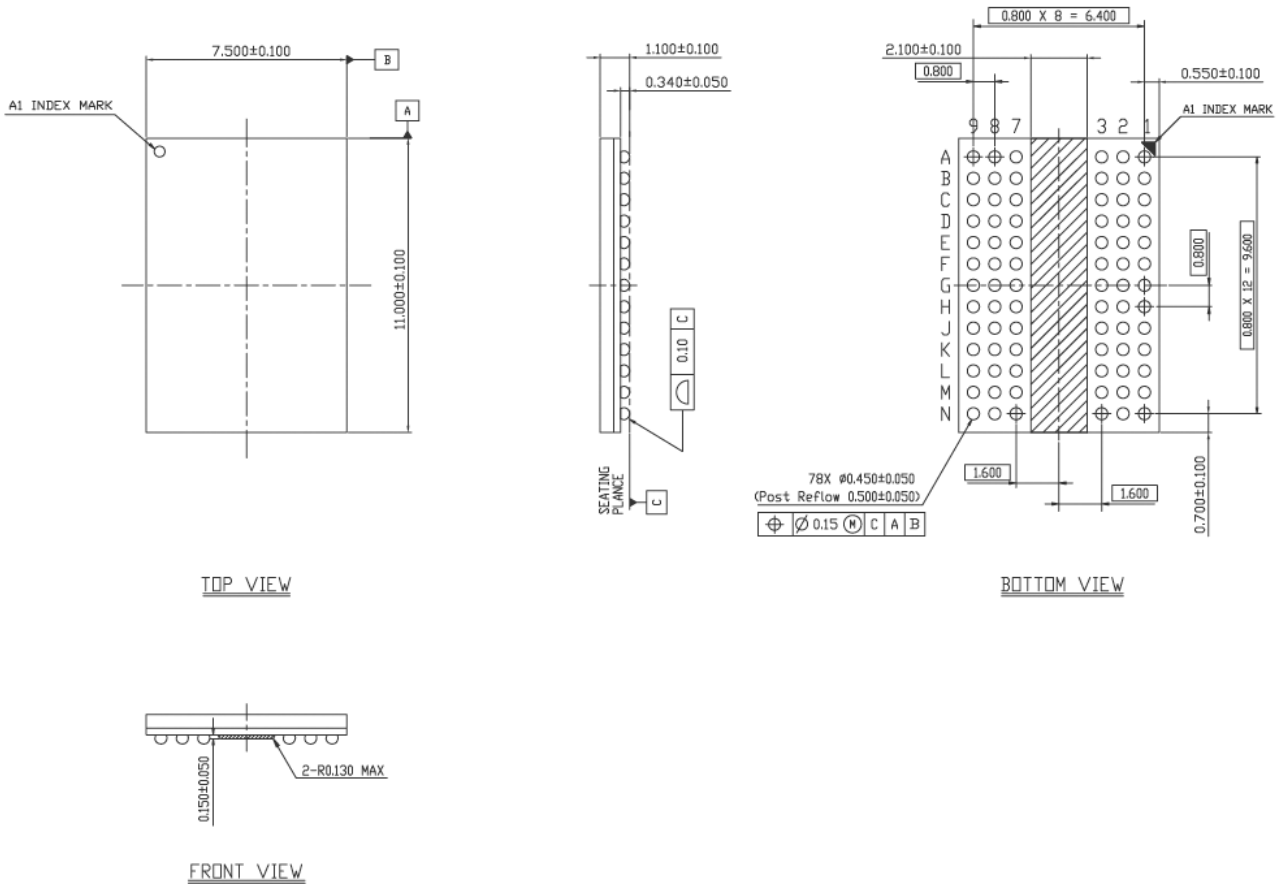
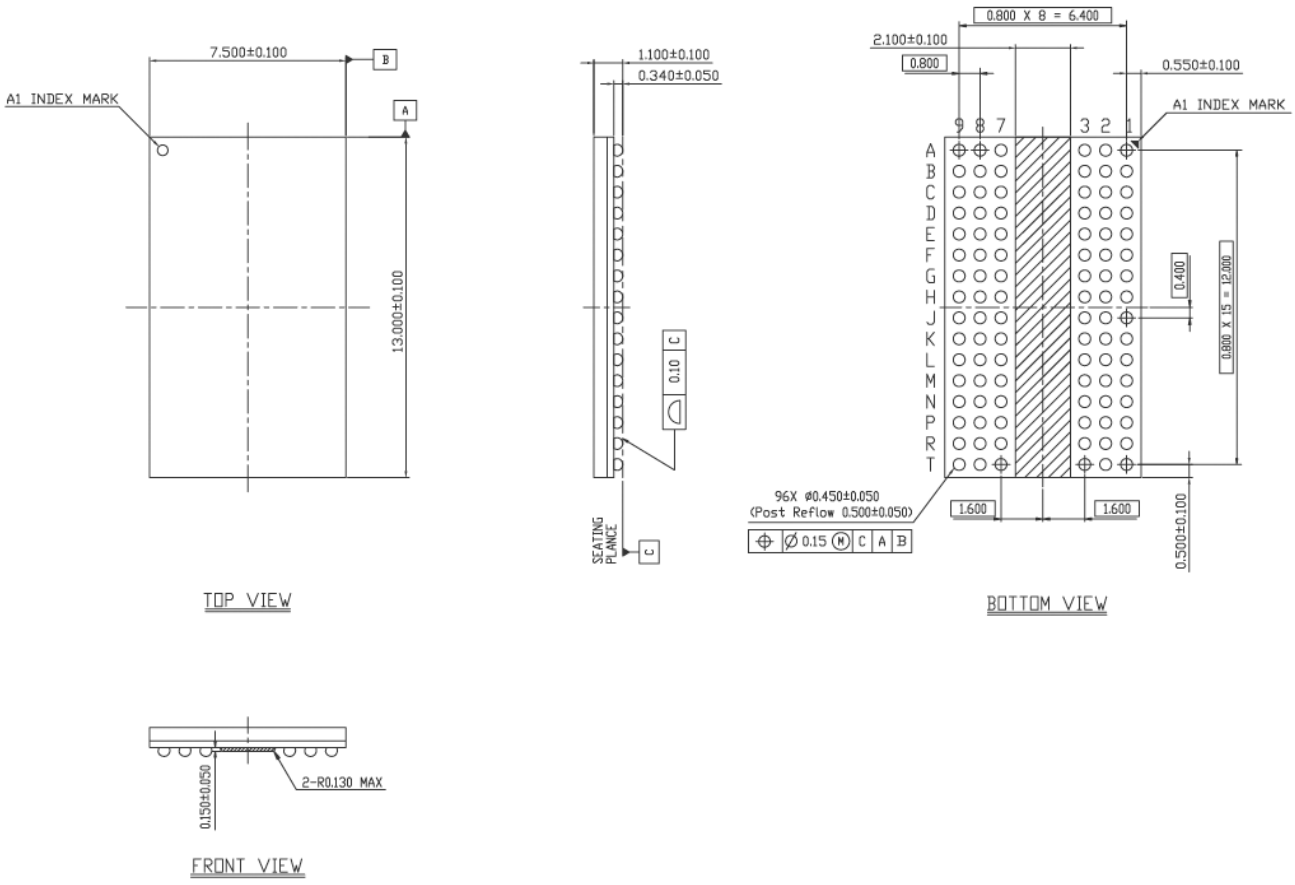


FIGURE 11
Package Outline PG-FBGA-96



7 Product Nomenclature

For reference the SCSemicon SDRAM component nomenclature is enclosed in this chapter.

TABLE 19
Examples for Nomenclature Fields

Example for	Field Number									
	1	2	3	4	5	6	7	8	9	10
DDR3 DRAM	HXB	15	H	1G	16	0	A	F	-	25D

TABLE 20
DDR3 Memory Components

Field	Description	Values	Coding
1	SCSemicon Component Prefix	HXB	Memory components, standard temperature range (0°C – +85 °C)
		HXI	Memory components, industrial temperature range (-40°C – +95 °C)
2	Interface Voltage [V]	18	SSTL_18, + 1.8 V (± 0.1 V)
		15	SSTL_15, + 1.5 V (± 0.075 V)
3	DRAM Technology	T	DDR3
		H	DDR3
4	Component Density [Mbit]	32	32 Mbit
		64	64 Mbit
		128	128 Mbit
		256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
		4G	4 Gbit
5	Number of I/Os	40	× 4
		80	× 8
		16	× 16
6	Product Variant	0 .. 9	–
7	Die Revision	A	First
		B	Second
		C	Third
8	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
9	Power	–	Standard power product
		L	Low power product

Field	Description	Values	Coding
10	Speed Grade	–13K	DDR3–1600 11–11–11
		–13J	DDR3–1600 10–10–10
		–15H	DDR3–1333 9–9–9
		–15G	DDR3–1300 8–8–8
		–19F	DDR3–1066 7–7–7
		–19E	DDR3–1066 6–6–6
		–25D	DDR3–800 5–5–5
		–25E	DDR3–800 6–6–6
		–3C	DDR3–667 4–4–4
		–3D	DDR3–667 5–5–5

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