HY10P40
Datasheet

8-Bit RISC-like Mixed Signal Microcontroller

Embedded 18-Bit ΣΔADC

Table of Contents

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1. Features

- 8-bit RISC-like, 46 high performance instructions included (H08B instruction set).
- 24-Bit ΣΔADC Analog-to-Digital Converter
  - Comb filter conversion rate up to 1.95Ksps
  - Sampling frequency: 250KHz
  - Over-sampling rate configurations: 128~32768
  - Fully differential input signal and zero adjust of measurement range
  - Signal amplification, x1/4, x1/2, x1, x2, x4, x8, x16
  - Measurement signal input: 8-ch
  - Low temp. drift
- Internal Power System
  - Built-in LDO linear power regulator, VDDA
    - Internal analog circuit or external sensor voltage source
    - 2.4V//2.7/3.0V configurable output, can use external voltage input
    - Low consumption and low temp. drift
  - Built-in reference voltage, ACM
    - Analog circuit voltage reference source (1.2V)
    - Low consumption and low temp. drift
- Timer
  - Watch Dog
    - Reset and interrupt event
  - 8-bit Timer
    - Interrupt event
  - 16-bit Timer
    - 16-Bit PWM output
    - 2 8-Bit PWM output
    - Interrupt event
- Operation Voltage and Temperature Range
  - V_{REGIN}: 4V ~ 24V
  - V_{DD}: 2.2V ~ 3.6V
  - - 40°C ~ 85°C
- Operation Frequency
  - Built-in high resolution HAO oscillator 2MHz/4MHz/8MHz
  - Built-in low power oscillator,14KHz LPO
- Memory Type
  - 2KW OTP program memory
  - 128B data memory
  - 6-layer stack
  - Built-in EPROEM
    - VPP operation voltage 6.0V
    - 64W EPROM memory
- Pin Features
  - Equipped with 10mA driving power
  - Self-define function module output pin
- Reset Function
  - Power On Reset
  - Brown Out Reset
  - Watch Dog Reset
- I^2C Interface

2. Pin Definition

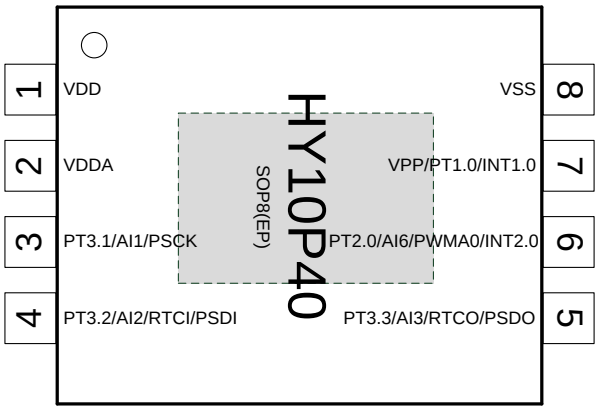


Figure 2-1 HY10P40 SOP8(EP) Pin Diagram

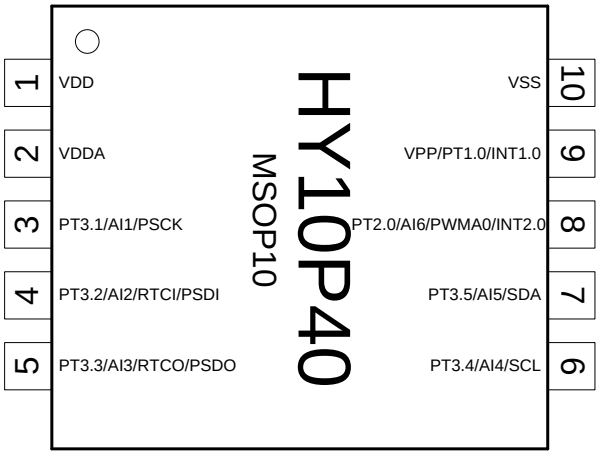


Figure 2-2 HY10P40 MSOP10 Pin Diagram

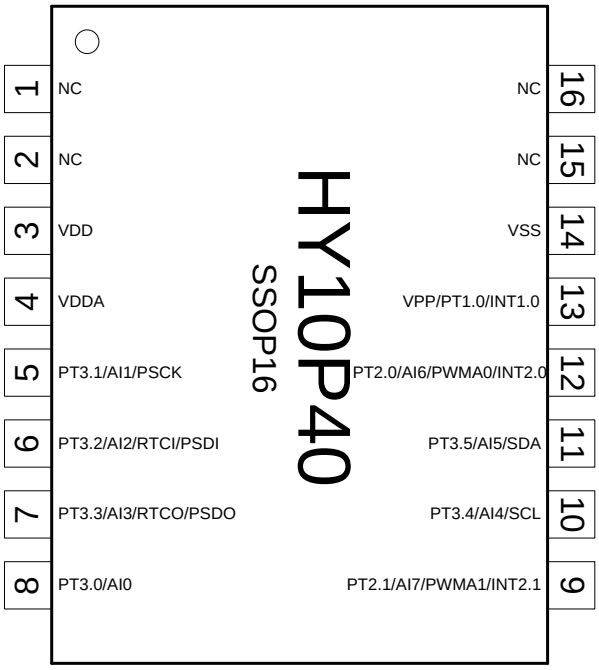


Figure 2-4 HY10P40 SSOP16 Pin Diagram

2.1. Pinout I/O Description

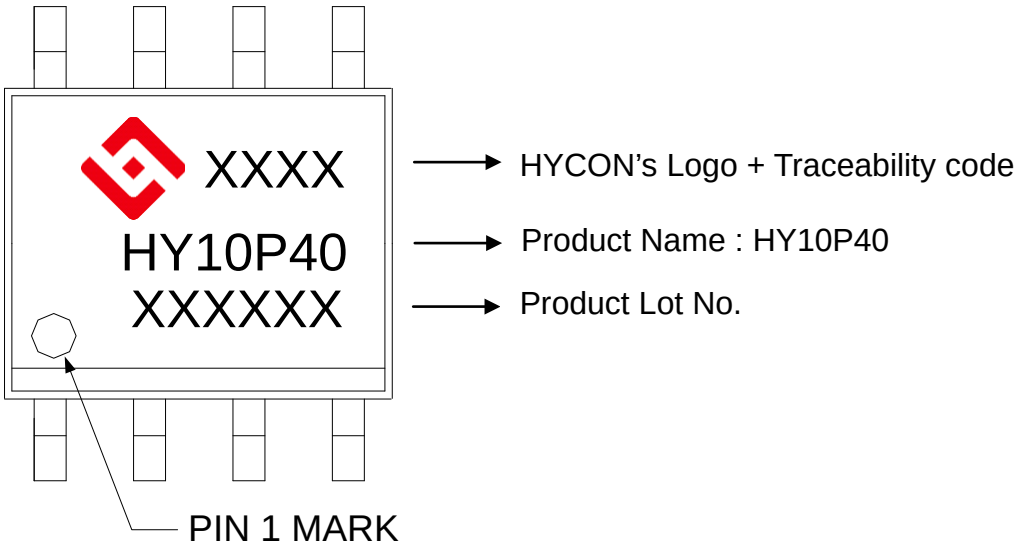
"I": input, "O": output, "A"" Analog, "S": Smith Trigger, "C": CMOS I/O,"P": Power Source,"/" or, "X": can be omitted

Package				Pin	Design		Description
SSOP16	SSOP16	MSOP10	SOP8(EP)		Type	Buffer	
1	-	-	-	REGIN	P	P	Power Supply Connect a 1uF ceramic capacitor to VSS
2	-	-	-	REG33	P	P	Regulated Power Output A 3.3V regulated voltage output. Only for device use Connect a 4.7uF ceramic capacitor to VSS
3	3	1	1	VDD	P	P	Chip operation power source pin
4	4	2	2	VDDA	P	P	LDO linear regulator power output pin
5	5	3	3	PT3.1	I/O	S/C	Digital input/output pin
				AI1	A	A	Analog input channel
				PSCK	I	S	OTP read/write interface, PSCK pin
6	6	4	4	PT3.2	I/O	C	Digital input/output pin
				AI2	A	A	Analog input channel
				RTCI	C	C	External RTC oscillator connect pin
				PSDI	I	S	OTP read/write interface, PSDI pin
7	7	5	5	PT3.3	I/O	C	Digital input/output pin
				AI3	A	A	Analog input channel
				RTCO	C	C	External RTC oscillator connect pin
				PSDO	I/O	S	OTP read/write interface, PSDO pin
8	8	-	-	PT3.0	I/O	C	Digital input/output pin
				AI0	A	A	Analog input channel
9	9	-	-	PT2.1	I/O	C	Digital input/output pin
				AI7	A	A	Analog input channel
				PWMA1	O	C	PWM1 output pin of TMB1
				INT2.1	I	S	External Falling Edge Trigger Interrupt
10	10	6	-	PT3.4	I/O	C	Digital input/output pin
				AI4	A	A	Analog input channel
				SCL	I/O	S	I^2C communication interface
11	11	7	-	PT3.5	I/O	C	Digital input/output pin
				AI5	A	A	Analog input channel
				SDA	I/O	S	I^2C communication interface
12	12	8	6	PT2.0	I/O	C	Digital input/output pin
				AI6	A	A	Analog input channel

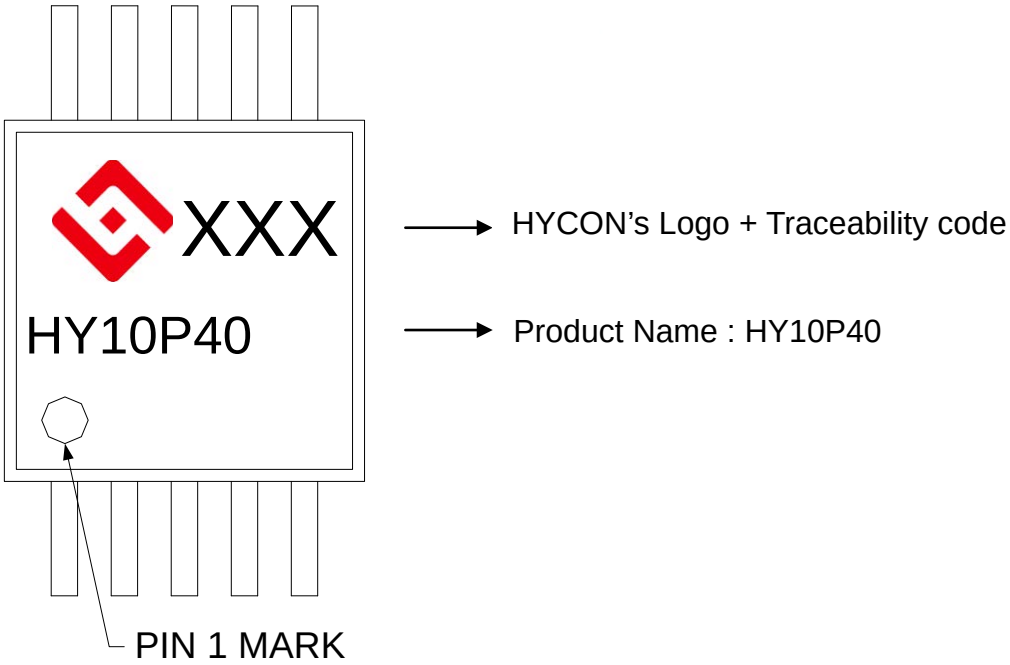
				PWMA0	O	C	PWM0 output pin of TMB1
				INT2.0	I	S	External Falling Edge Trigger Interrupt
13	**13**	**9**	**7**	PT1.0	I	S	Digital input
				VPP	P	P	OTP programming voltage pin
				INT0	I	S	External interrupt source
14	**14**	**10**	**8**	VSS	P	P	Chip operation power source ground pin
15	**-**	**-**	**-**	REGVSS	P	P	Connect to VSS.
16	**-**	**-**	**-**	NC	X	X	-
-	**-**	**-**	**EP**	E-pad	P	P	Chip operation power source ground pin

Table 2-1 Pin Definition and Function Description

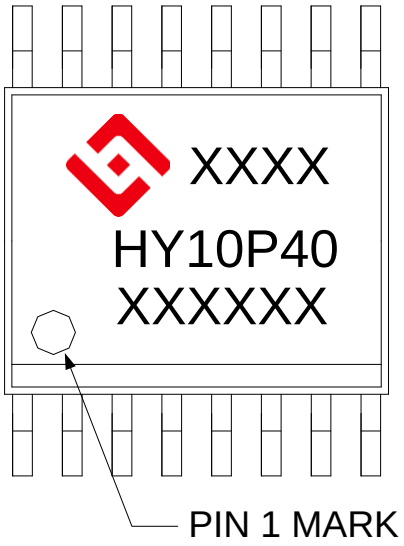
2.1.1. SOP package marker information



2.1.2. MSOP package marker information



2.1.3. SSOP package marker information



→ HYCON's Logo + Traceability code

→ Product Name : HY10P40

→ Product Lot No.

3. Application Circuit

3.1. PIR application (Pyroelectric Infrared-detector)

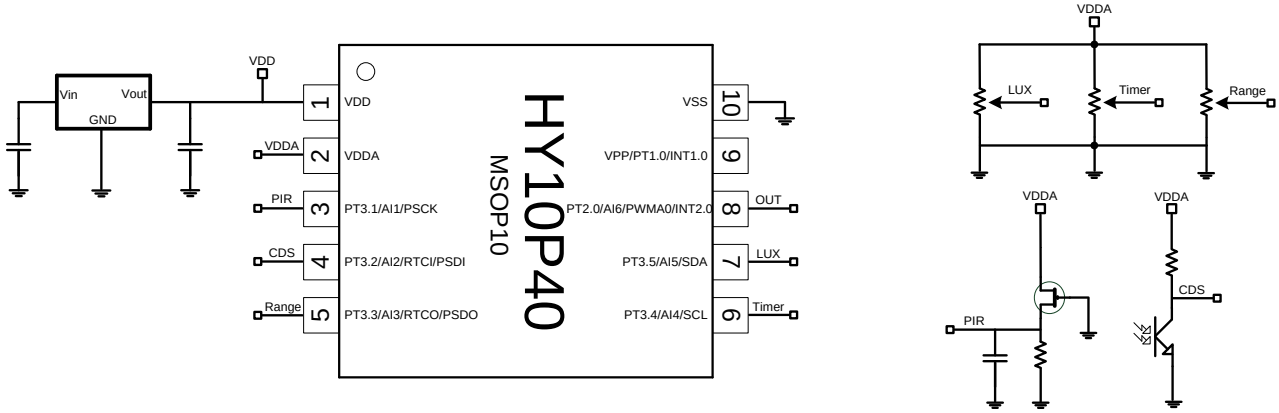


Figure 3-1 PIR Application Circuit

3.2. Smart Pressure Sensor Application

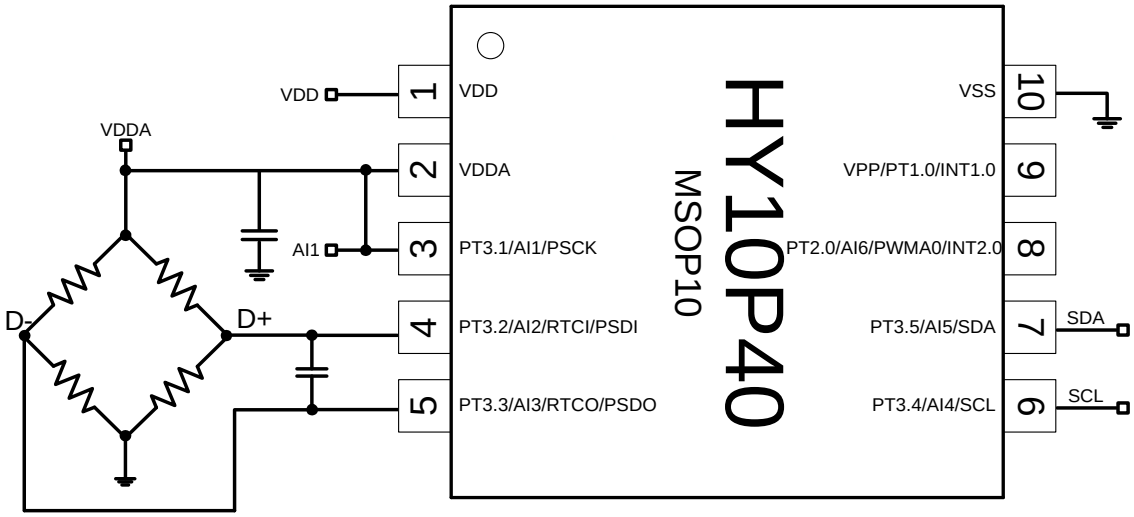


Figure 3-2 Smart Pressure Sensor Application Circuit

4. Function Outline

4.1. Internal Block Diagram

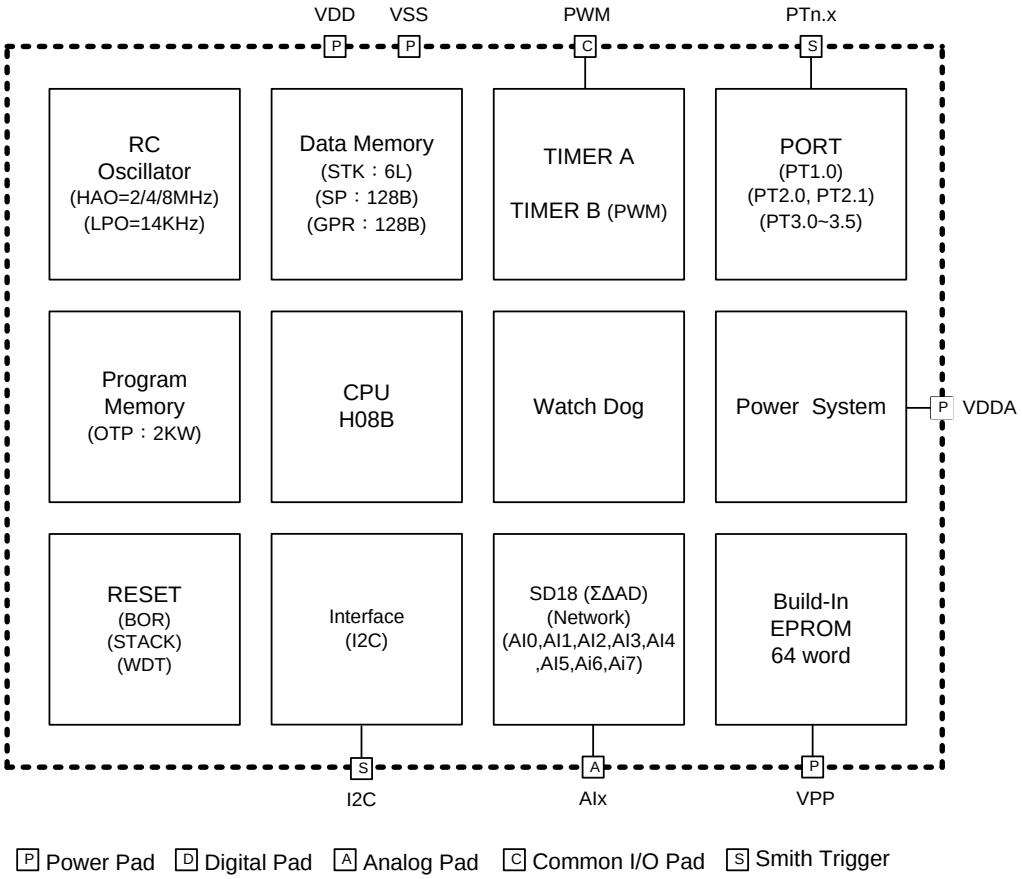


Figure 4-1 HY10P40 Internal Block Diagram

4.2. Related Description and Supporting Document

IC Function Related Operating Instruction

DS-HY10P40 HY10P40 Datasheet

UG-HY10SXX HY10Pxx Series User's Manual

APD-CORE003-Vxx H08B Instruction Description

Development Tool Related Operating Instruction

APD-HYIDE00X-Vxx HY10xxx Development Tool Software Instruction Manual

APD-HYIDE00X-Vxx HY10xxx Development Tool Hardware Instruction Manual

APD-OTP001-Vxx OTP Programming Pin Manual

Product Production Related Operating Instruction

APD-HYIDE004-Vxx HY1xxxx Series Production Tool-Programmer Hardware Instruction Manual

BDI-HY10P40-Vxx HY10P40 Bonding Information

4.3. SD18 Network

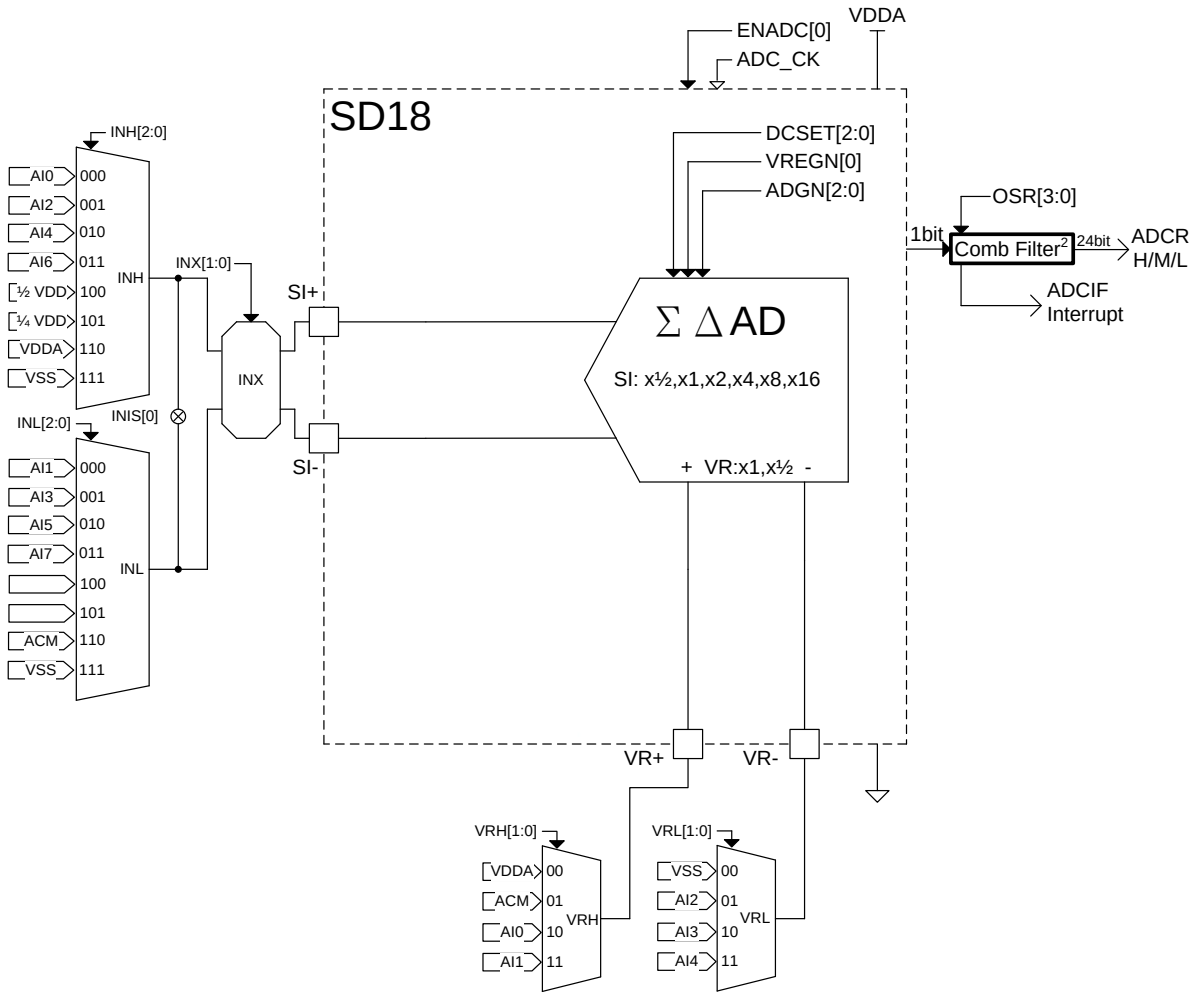


Figure 4-2 SD18 Network

5. Register List

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1

"$"for event status,"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

位址	名稱	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A-RESET	I-RESET	R/W
000h	INDF0	Contents of FSR0 to address data memory - value of FSR0 not changed								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
001h	POINC0	Contents of FSR0 to address data memory - value of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
002h	PODEC0	Contents of FSR0 to address data memory - value of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
003h	PRINC0	Contents of FSR0 to address data memory - value of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
004h	PLUSW0	Contents of FSR0 to address data memory - value of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
010H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
016h	TOSH	-	-	-	-	-	TOS[10]	TOS[9]	TOS[8]	 xxxx	.... uuuu	-,-,-,- -,*,*,*
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
018h	STKPTR	SKFL	SKUN	SKOV	-	-	SKPRT[2:0]			000. .000	u$$. .$$$	rw0,rw0,rw0,- -,*,*,*
01Ah	PCLATH	-	-	-	-	-	PC[10]	PC[9]	PC[8]	.... .0000	 0000	-,-,-,- -,*,*,*
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*,*,*,*,*,*,*,*
023h	INTE0	GIE	ADIE	E21IE	WDTIE	TB1IE	TMAIE	E20IE	E10IE	0000 0000	0uuu uuuu	*,*,-,*,*,*,-,*
024h	INTE1	-	-	-	-	I2CERIE	I2CIE	-	-	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
026h	INTF0	-	ADIF	E21IF	WDTIF	TB1IF	TMAIF	E20IF	E10IF	.000 0000	.uuu uuuu	*,*,-,*,*,*,-,*
027h	INTF1	-	-	-	-	I2CERIF	I2CIF	-	-	0000 0000	uuuu uuuu	*,*,*,* r,r,*,*
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
02Bh	STATUS	-	-	-	C	-	-	-	Z	...x xxxx	...u uuuu	-,-,-,-,*,*,*,*
02Ch	PSTATUS	BOR	PD	TO	IDL	-	SKERR	-	-	$000 $00.	uu$u u$u.	rw0,rw0,rw0,rw0 rw0,rw0,rw0,-
02Eh	BIECN	-	-	-	-	VPPHV	-	BIEWR	BIERD	1... $.00	1... $.uu	r1,-,-,- r,-,*,*
02Fh	BIEARH	ENBIE	-	-	-	-	11-bit look-up Table as BIEAH[2:0]			0... xxxx	u... uuuu	*,-,-,- *,*,*,*
030h	BIEARL	BIE Address Register as BIEAL[5:0] or 11-bit look-up Table as BIEAL[7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
031h	BIEDRH	BIE High Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
032h	BIEDRL	BIE Low Byte Data Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
033h	PWRCN	ENLDO[1:0]		VDDAX[1:0]		-	-	ADRST	CSFON	0000 0000	uuuu u00u	*,*,*,* *,wr0,wr0,*
034h	OSCCN0	OSCS[1:0]		DHS[1:0]		DMS[2:0]			CPUS	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
035h	OSCCN1	-	-	ADCS[2:0]			DTMB[1:0]		TMBS	0000 0000	uuuu uuu.	*,*,*,*,*,*,*,-
036h	OSCCN2	-	-	-	-	HAOM[1:0]		ENHAO	LPO	.000 0011	.uuu uu11	.,*,*,*,*,*,*,r
037h	WDTCN	-	-	-		ENWDT	DWDT[2:0]			0000 0000	uuuu $000	-,*,*,* rw1,*,*,*
038h	TMACN	ENTMA	TMACL	TMAS	DTMA[2:0]			-	-	0000 00..	u0uu uu..	*,rw1,*,*,*,-,-
039h	TMAR	TMA counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0 rw0,rw0,rw0,rw0
041h	CSFCN0	SKRST	-	HAOTR[5:0]						0.10 0000	u.uu uuuu	*,-,*,*,*,*,*,*
043h	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
044h	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r

045h	ADCRL	ADC conversion memory Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
046h	ADCCN1	ENADC	ENHIGN	ENCHP	-	-	ADGN[2:0]			0000 0000	0000 0000	*,*,*,*,*,*,*,*
047h	ADCCN2	-	-	-	-	VREGN	DCSET[2:0]			 0000	 0000	-,-,-,- *,*,*,*
048h	ADCCN3	OSR[3:0]				-	-	-	-	000. ..0.	000. ..0.	*,*,*,- -,-,*,-
049h	AINET1	INH[2:0]			INL[2:0]			INIS	-	0000 000.	0000 000.	*,*,*,*,*,*,*,-
04Ah	AINET2	-	VRH[1:0]		INX[1:0]		VRL[1:0]		-	.000 000.	.000 000.	-,*,*,*,*,*,*,-
04Eh	TB1Flag	-	-	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	..00 0000	..uu uuuu	-,-,r,r r,r,r,r
04Fh	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	-	-	0000 0000	uuuu u0uu	*,*,*,* *,rw1,*,*
050h	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
051h	TB1RH	TimerB1 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
052h	TB1RL	TimerB1 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
053h	TB1C0H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
054h	TB1C0L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
055h	TB1C1H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
056h	TB1C1L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
057h	TB1C2H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
058h	TB1C2L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
061h	CFG	Rsv.					I2CRST	ENI2CT	ENI2C	.... .000	.... .uuu	-,-,-,- -,*,*,*
062h	ACT	SLAVE	-	-	I2CER	START	STOP	I2CINT	ACK	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
063h	STA	MACTF	SACTF	RDBF	RWF	DFF	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	*,*,*,*,*,*,*,*
064h	CRG	CRG[7:0]								0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
065h	TOC	I2CTF	DI2C[2:0]		I2CTLT[3:0]					0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
066h	RDB	RDB[7:1]							RDB[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
067h	TDB0	TDB0[7:1]							TDB[0]	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
068h	SID0	SID[7:1],The corresponding address of the 7-bit mode							SIDV[0]	0000 0000	uuuu uuuu	*,*,*,*,*,*,*,*
070h	PT1	-	-	-	-	-	-	-	PT10	xx.. ..xx	xx.. ..xx	*,*,-,- -,-,*,*
071h	TRISC1	-	-	-	-	-	-	-	-	0000 0000	uuuu uuuu	*,*,-,- -,-,*,*
072h	PT1DA	-	-	-	-	-	-	-	-	0000 0000	uuuu uuuu	-,-,-,- *,-,*,*
073h	PT1PU	-	-	-	-	-	-	-	-	0000 0000	uuuu uuuu	*,*,-,- -,-,*,*
074h	PT1EG	-	-	FPWMA1	FPWMA0	-	-	E0EG[1:0]		 0000	.... uuuu	-,-,-,- *,*,*,*
075h	PT2	-	-	-	-	-	-	PT21	PT20	xx	xx	-,-,-,- -,-,*,*
076h	TRISC2	-	-	-	-	-	-	TC21	TC20	00	.... ..uu	-,-,-,- -,-,*,*
077h	PT2DA	-	-	-	-	-	-	DA21	DA20	00	.... ..uu	-,-,-,- -,-,*,*
078h	PT2PU	-	-	-	-	-	-	PU21	PU20	00	.... ..uu	-,-,-,- -,-,*,*
079h	PT3	-	-	PT35	PT34	PT33	PT32	PT31	PT30	..xx xxxx	..xx xxxx	-,-,*,*,*,*,*,*
07Ah	TRISC3	-	-	TC35	TC34	TC33	TC32	TC31	TC30	..00 0000	..uu uuuu	-,-,*,*,*,*,*,*
07Bh	PT3DA	-	-	DA35	DA34	DA33	DA32	DA31	DA30	..00 0000	..uu uuuu	-,-,*,*,*,*,*,*

07Ch	PT3PU	-	-	PU35	PU34	PU33	PU32	PU31	PU30	..00 0000	..uu uuuu	-,-,*,*,*,*,*,*
080h ~ 0FFh	GPR0	General Purpose Register as 128Byte								uuuu uuuu	uuuu uuuu	*,*,*,*,*,*,*,*

6. Electrical Characteristics

6.1. Recommended Operating Conditions

T_A = -40℃ ~ 85℃, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{REGIN}	Supply Voltage		4		24	V
V_{REG33}	Regulator Output Voltage	$I_L \leqq 3mA$	3.3-1.5%		3.3V+1.5%	V
		$4V \leqq V_{REGIN} \leqq 20V$ $3mA \leqq I_{REGOUT} \leqq 16mA$	3.3-2.5%		3.3V+2.5%	
		$4V \leqq V_{REGIN} \leqq 20V$ $3mA \leqq I_{REGOUT} \leqq 16mA$ T_A= -40℃~ +85℃	3.3-3.5%		3.3V+3.5%	
V_{REGVSS}	Supply Voltage	Connect to VSS	0		0	
V_{DD}	Supply Voltage	All digital peripherals and CPU	2.2		3.6	V
		Analog peripherals	2.4		3.6	
V_{SS}	Supply Voltage		0		0	

6.2. Internal RC Oscillator

T_A = 25℃, V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO(2.0MHz)	High Speed Oscillator frequency	ENHAO[0]=1	1.8	2.0	2.2	MHz
HAO(3.8MHz)	High Speed Oscillator frequency		3.42	3.8	4.18	MHz
HAO(7.0MHz)	High Speed Oscillator frequency		6.3	7.0	7.7	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO		14		KHz

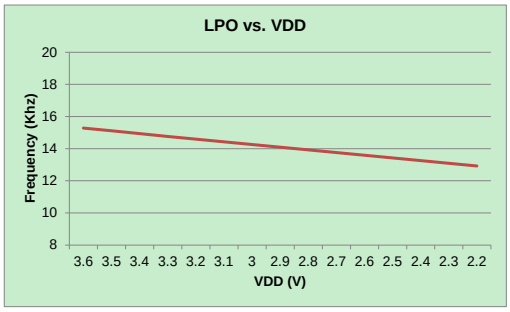


Figure 6.2-1 LPO vs. VDD

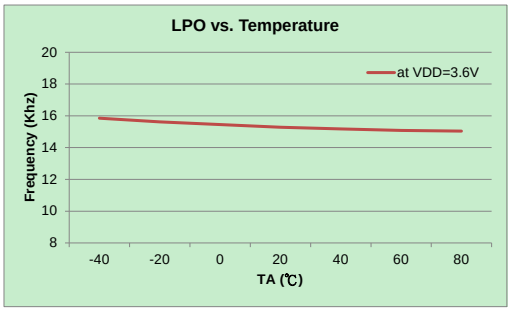


Figure 6.2-2 LPO vs. Temperature

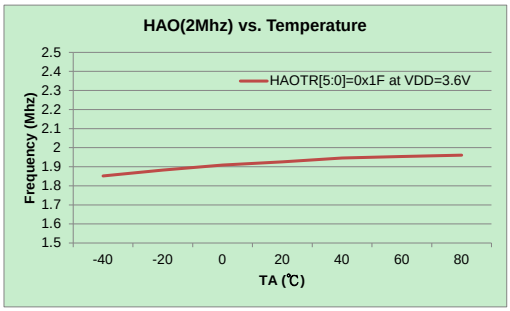


Figure 6.2-3 HAO (2.0MHz) vs. Temperature

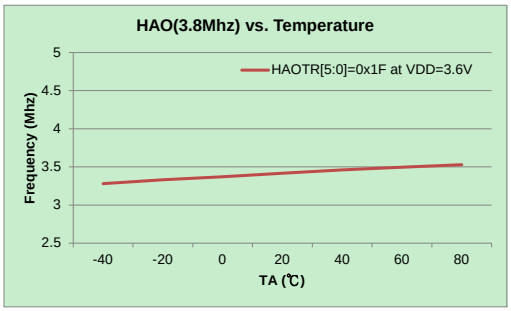


Figure 6.2-4 HAO (3.8MHz) vs. Temperature

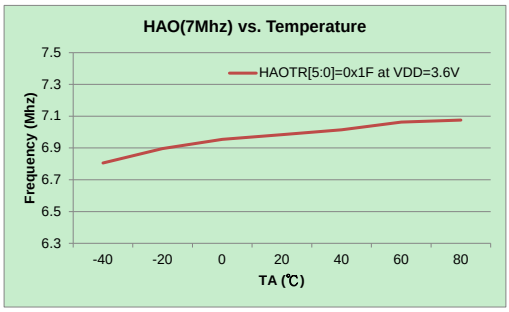


Figure 6.2-5 HAO (7.0MHz) vs. Temperature

6.3. Supply Current into VDD Excluding Peripherals Current

T_A = 25℃,V_{DD} = 3.0V,OSC_LPO = 14KHz, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 8MHz, CPU_CK = 8MHz		0.78		mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO =4MHz, CPU_CK = 4MHz		0.43		mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.24		mA
I_{AM4}	Active mode 4	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.14		mA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO,		2.5		uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.2		uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.6		uA

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

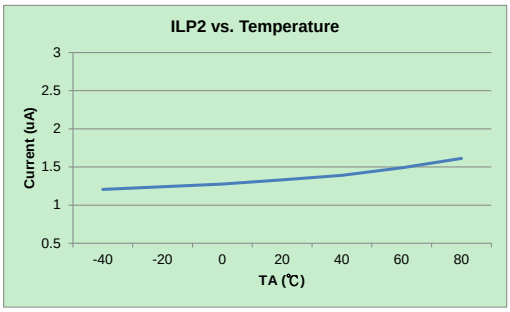


Figure 6.3-1 ILP2 vs. Temperature

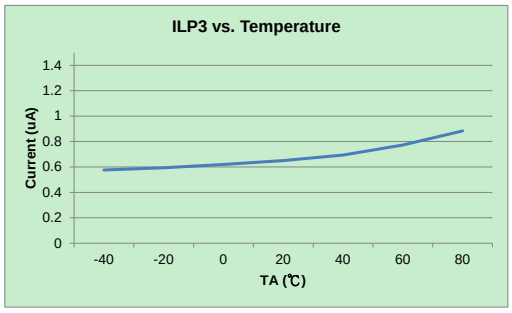


Figure 6.3-2 ILP3 vs. Temperature

6.4. Port 1~3

T_A = 25 °C, V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage		0.7*VDD		VDD	V
V_{IL}	Low-Level input voltage		VSS		0.3*VDD	
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	

6.5. Reset (Brownout)

T_A = 25 ℃, V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, $t_{d\text{-}LVR}$		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H), V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS\text{-}LVR}$			70		mV
BOR：Brownout Reset LVR：Low Voltage Reset of BOR						

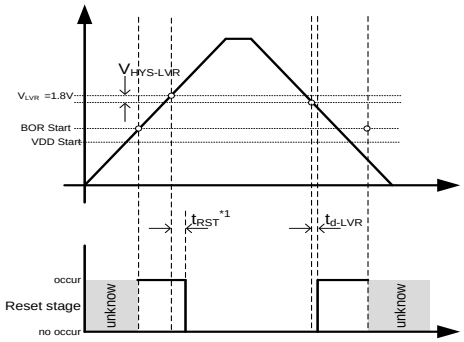


Figure 6.5-1 BOR Reset Diagram

*1 rRST：Please see BOR Introduce of HY10Pxx series User's Guide (UG-HY10S00-Vxx).

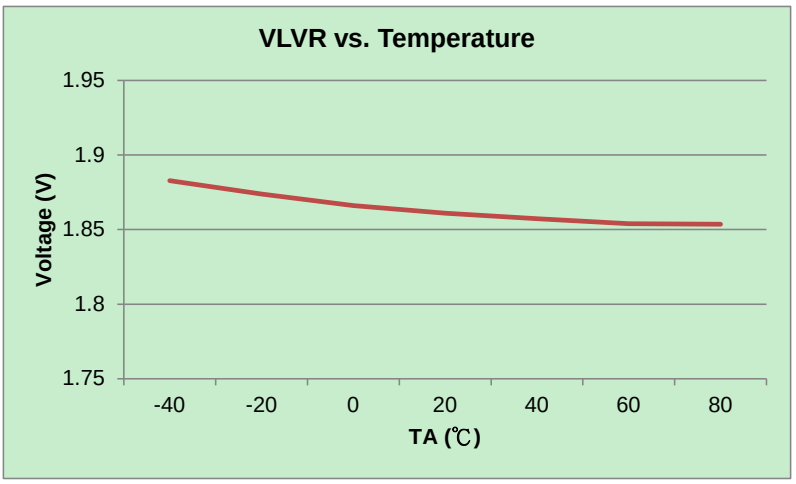


Figure 6.5-3 LVR vs. Temperature

6.6. Power System

TA = 25℃,VDD = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	ENLDO[1:0]=11b		13		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.2V	VDDAX[1:0]=01b		3.0		V
			VDDAX[1:0]=10b		2.7		
			VDDAX[1:0]=11b		2.4		
	Dropout voltage	I_L = 10mA	VDDAX[1:0]=01b		150		mV
			VDDAX[1:0]=10b		165		
			VDDAX[1:0]=11b		180		
	Temperature drift	ENLDO[1:0]=11b, I_L = 0.1mA	T_A=-40℃~85℃		50		ppm/℃
	V_{DD} Voltage drift		V_{DD}=2.5V~3.6V		±0.2		%/V
ACM	Analog Common Mode Voltage ,V_{ACM}	ENADC[0]=1	I_L = 0uA		1.2		V
	Analog Common Mode Voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Temperature drift	ENADC[0]=1, I_L = 10uA	T_A=-40℃~85℃		50		ppm/℃
	VDDA Voltage drift				100		uV/V
VDDA：Adjust Voltage Regulator ACM：Analog Common Mode Voltage							

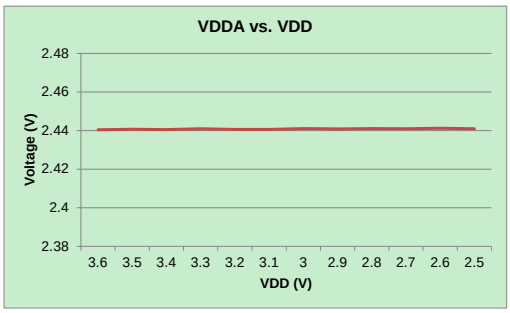


Figure 6.6-1 VDDA vs. VDD

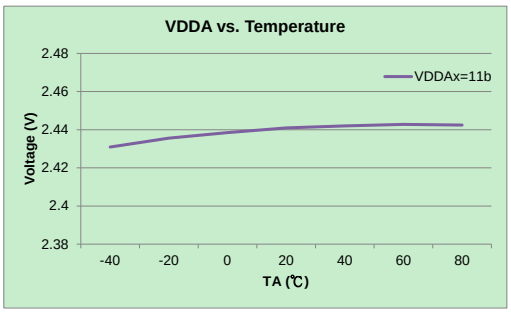


Figure 6.6-2 VDDA vs. Temperature

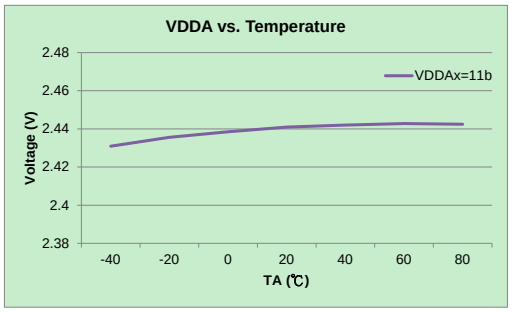


Figure 6.6-2 VDDA vs. Temperature

6.7. SD18, Power Supply and Recommended Operating Conditions

T_A = 25 ℃, V_{DD} = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			128 *1		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1	GAIN =4, ADC_CK=250KHz		120		uA
*1, OSR=128, setting by ADCCN3[OSR[3]] bit. OSR[3:0]=1010, OSR=128; OSR[3:0]=0xxx, OSR=256 ~ 32768							

6.7.1. SD18 Performance (fSD18=250KHz)

T_A = 25℃, V_{DD} = 3.0V, VDDA=3.0V, V_{VR}=1.0V, GAIN=1 without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V, V_{VR}=1.0V, ΔSI=±450mV			±0.003	±0.01	%FSR
	No Missing Codes[3]	ADC_CK=250KHz, OSR[2:0]=010b		23			Bits
G_{SD18}	Temperature drift **Gain 1~x16**		T_A= -40 ℃		5		ppm/ ℃
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper without PGA	ΔAI=0V ΔVR=0.9V DCSET[2:0]=<000> *ΔAI is external short	Gain=2			1	%FSR
	Offset temperature drift with chopper without PGA		GAIN=1		2		uV/ ℃
			GAIN=2		1		
			GAIN=4		0.5		
			GAIN=16		0.15		
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,without PGA	V_{SI}=0V, GAIN=1		90		dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,	V_{SI}=0V, GAIN=16		75		
PSRR	DC power supply rejection	VDDA=3.0V, ΔVDDA=±100mV, V_{VR}=1.0V, V_{SI}=V_{SI-}=1.2V,	GAIN=1 PGA=off		75		dB
			GAIN=16				

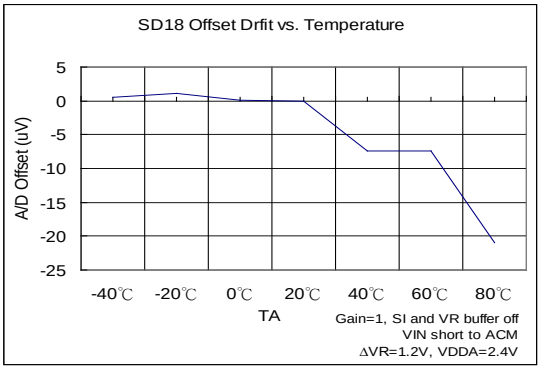


Figure 6.7-1(a) SD18 Offset Temperature Drift

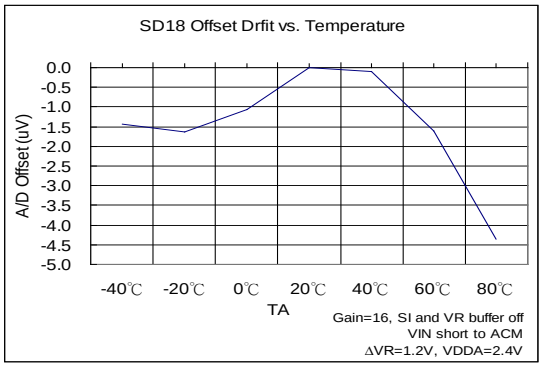


Figure 6.7-1(b) SD18 Offset Temperature Drift

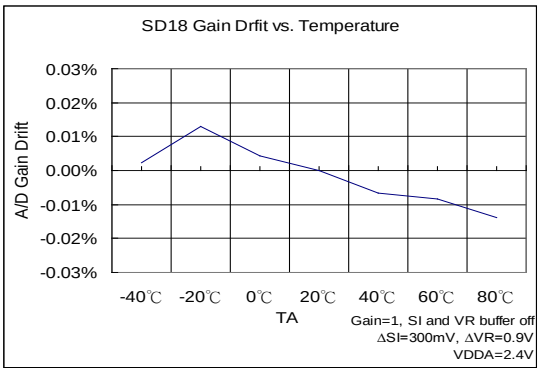


Figure 6.7-2(a) SD18 Gain Drift with Temperature

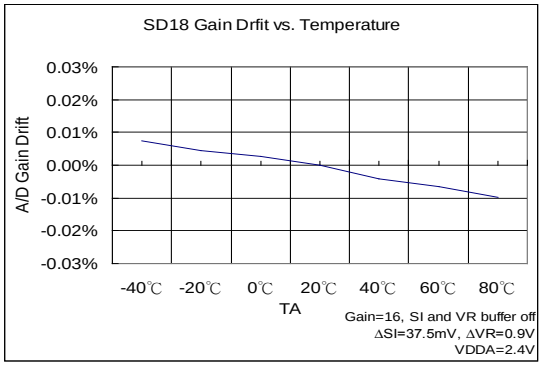


Figure 6.7-2(b) SD18 Gain Drift with Temperature

6.7.2. SD18 Noise Performance

T_A = 25 °C, VDD=3.0V, VDDA=2.4V, unless otherwise noted

HY10P40 provides important input noise specifications for SD18. Below tables list out the relations of typical noise specification, Gain, Output rate and maximum input voltage of single end. Test conditions: external input signal short, ADC voltage reference using external VDDA and VSS as voltage reference network, referred voltage reference: 1.2V and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V														
Max. Vin(mV) =0.9*VREF (1)	OSR					128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					1953	977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN									
±2160	0.5	=	1	×	0.5	14.39	16.14	16.96	17.27	17.44	17.66	18.08	19.52	19.73
±1080	1	=	1	×	1	14.38	16.04	16.85	17.18	17.42	17.76	18.89	19.85	20.22
±540	2	=	1	×	2	14.4	16.01	16.79	17.03	17.31	17.53	18.02	19.55	20.1
±270	4	=	1	×	4	14.42	15.91	16.57	16.94	17.14	17.39	17.69	18.61	19.81
±135	8	=	1	×	8	14.34	15.66	16.24	16.64	17.01	17.4	17.99	19.05	19.52
±68	16	=	1	×	16	14.22	15.3	15.88	16.34	16.85	17.41	17.85	18.53	19.01

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 6.7-4(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V														
Max. Vin(mV) =0.9*VREF	OSR					128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					1953	977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN									
±2160	0.5	=	1	×	0.5	226.11	67.48	38.23	30.84	27.40	23.43	17.59	6.46	5.58
±1080	1	=	1	×	1	113.68	36.14	20.60	16.42	13.86	10.94	5.00	2.58	1.99
±540	2	=	1	×	2	56.28	18.46	10.69	9.06	7.49	6.40	4.58	1.58	1.09
±270	4	=	1	×	4	27.72	9.85	6.25	4.82	4.20	3.53	2.88	1.52	0.66
±135	8	=	1	×	8	14.67	5.85	3.92	2.98	2.30	1.75	1.17	0.56	0.40
±68	16	=	1	×	16	7.95	3.76	2.52	1.83	1.29	0.87	0.64	0.40	0.29

Table 6.7-4(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\mathrm{ENOB(RMS)} = \ln\left(\frac{\mathrm{FSR}}{\mathrm{RMS\,Noise}}\right) \Big/ \ln(2)$$

$$\mathrm{RMS\,Noise} = \left(2 \times \mathrm{VREF} \times \sqrt{\sum_{k=1}^{1024} (\mathrm{ADO[k]} - \mathrm{Average})^2}\right) \Big/ 2^{23}$$

Where FSR (Full - Scale Range) = 2 × VREF/Gain.

$$\text{Average} = \frac{\sum_{k=1}^{1024}(\text{ADO}[k])}{1024}$$

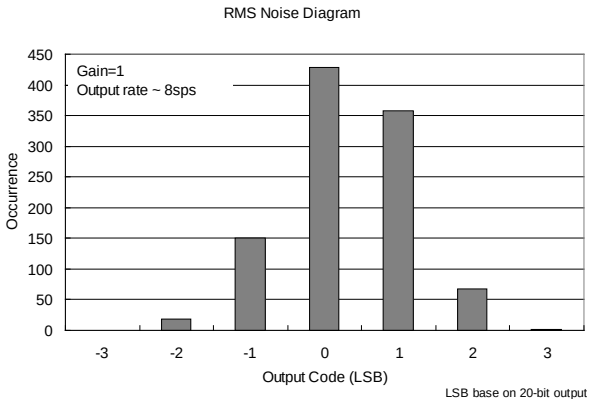


Figure 6.7-4(a) RMS Noise Diagram

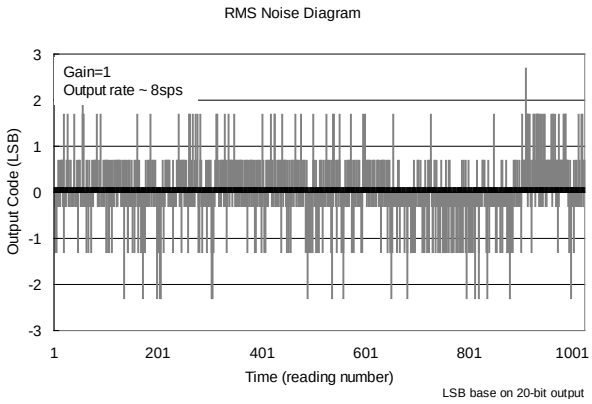


Figure 6.7-4(b) Output Code Diagram

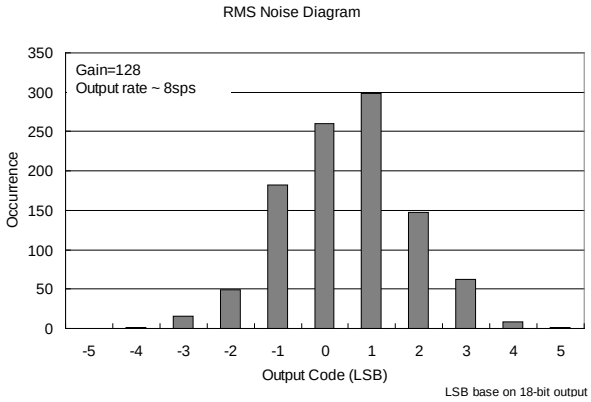


Figure 6.7-4(c) RMS Noise Diagram (Gain=16)

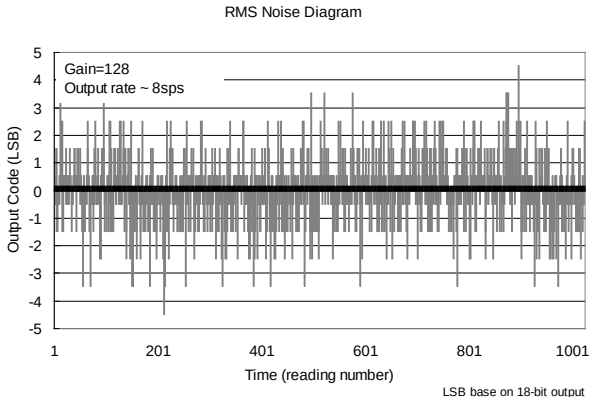


Figure 6.7-4(d) Output Code Diagram (Gain=16)

6.8. Built-in EPROM (BIE)

T_A = 25 °C, V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{BIE}	Supply Voltage			6.0	6.5	V
I_{BIE}	Operation supply current			5		mA
V_{SS}	Supply Voltage			0		V

7. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Programming Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY10P40-D000	Die	-	D	000	000	-	250	Green[4]	-
HY10P40-SE08	SOP8(EP)	9	S	E08	000	Tube	100	Green[4]	MSL-3
HY10P40-SE08	SOP8(EP)	9	S	E08	000	Tape & Reel	2500	Green[4]	MSL-3
HY10P40-M010	MSOP	10	M	010	000	Tube	80	Green[4]	MSL-3
HY10P40-M010	MSOP	10	M	010	000	Tape & Reel	3000	Green[4]	MSL-3
HY10P40-E016	SSOP	16	E	016	000	Tube	100	Green[4]	MSL-3
HY10P40-E016	SSOP	16	E	016	000	Tape & Reel	2500	Green[4]	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code**

(Blank Code/ Standard/ Customized Programming Code)

Ex：Your customized programming code is 007, IC model no. is HY10P40 and you require die shipment. The ordering device no. will be HY10P40-D000-007

Ex：You request blank code in die package, IC model no. is HY10P40.

The ordering device no. will be HY10P40-D000

Ex：You request IC model no. is HY10P40, blank code in SSOP16 package.

The ordering device no. will be HY10P40-E016. If you required the shipment to be packed in Tape & Reel, then please remark the shipment packing type as Tape & Reel.

Ex：Your customized programming code is 008 and you require products in SOP8(EP). The ordering device no. will be HY10P40-SE08-008. If you required the shipment to be packed in Tape & Reel, then please remark the shipment packing type as Tape & Reel.

Ex：Your customized programming code is 009 and you require products in MSOP10. The ordering device no. will be HY10P40-M010-009. If you required the shipment to be packed in Tube, then please remark the shipment packing type as Tube.

[2] **Programming Code:**

"001"~"999" is standard or customized programming code. Blank code does not have these numbers.

[3] **MSL:**

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

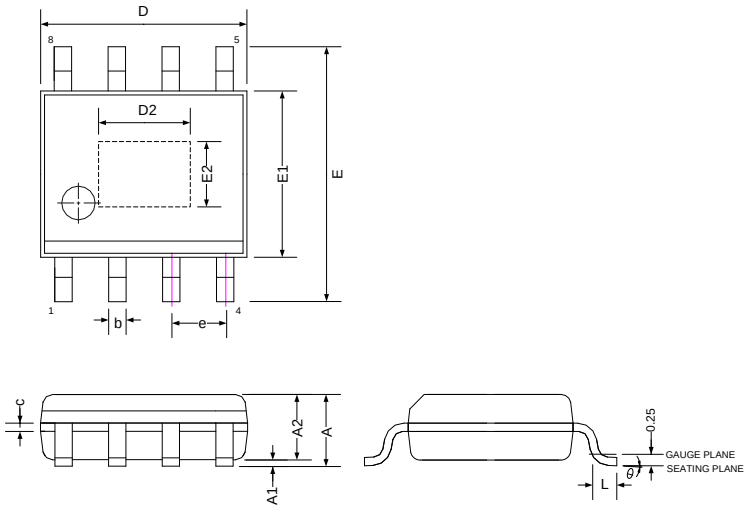
[4] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that are compliant with RoHS directive, SVHC under REACH and Halogen free.

8. Package Information

8.1. SOP8EP(SE08)

8.1.1. Package Dimensions



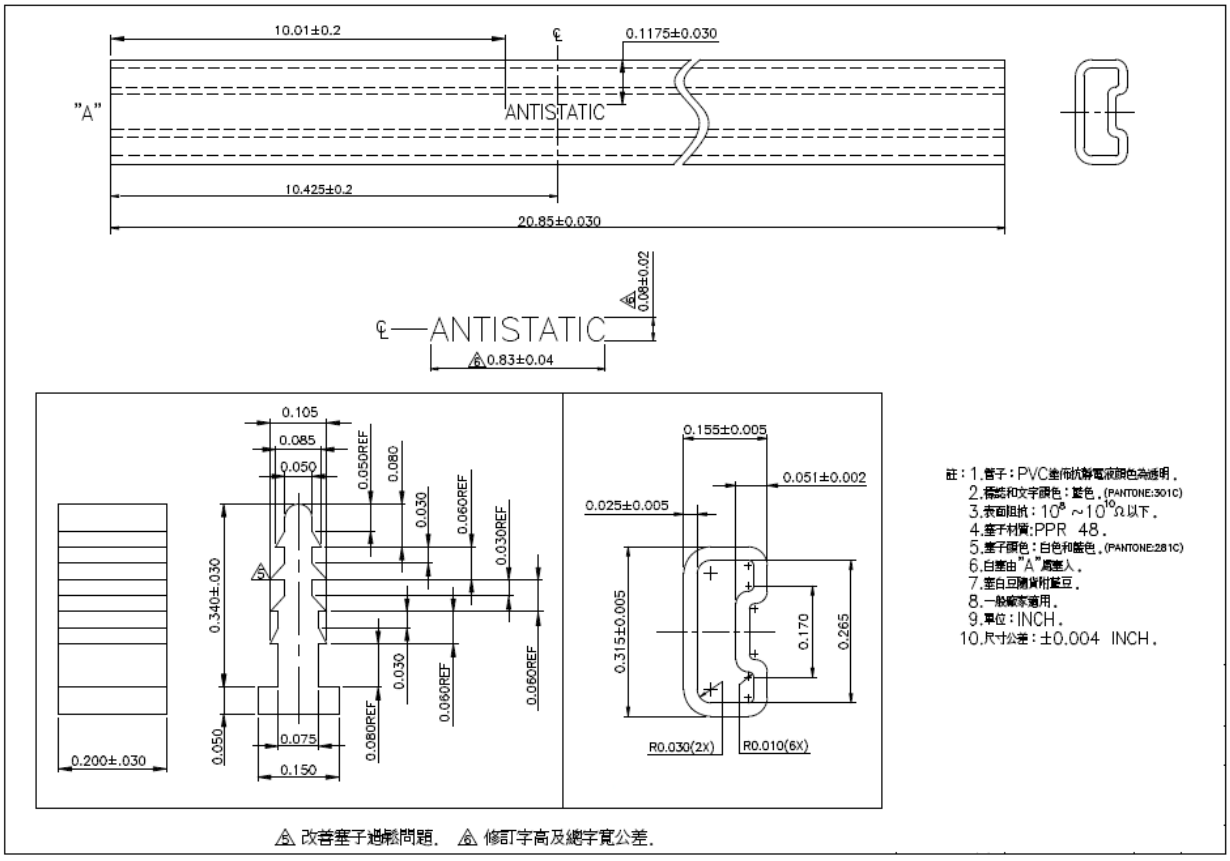
SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.10	-	0.25
D	4.90 BSC		
E1	3.90 BSC		
E	6.00 BSC		
L	0.40	-	1.27
e	1.27 BSC		
θ°	0	-	8

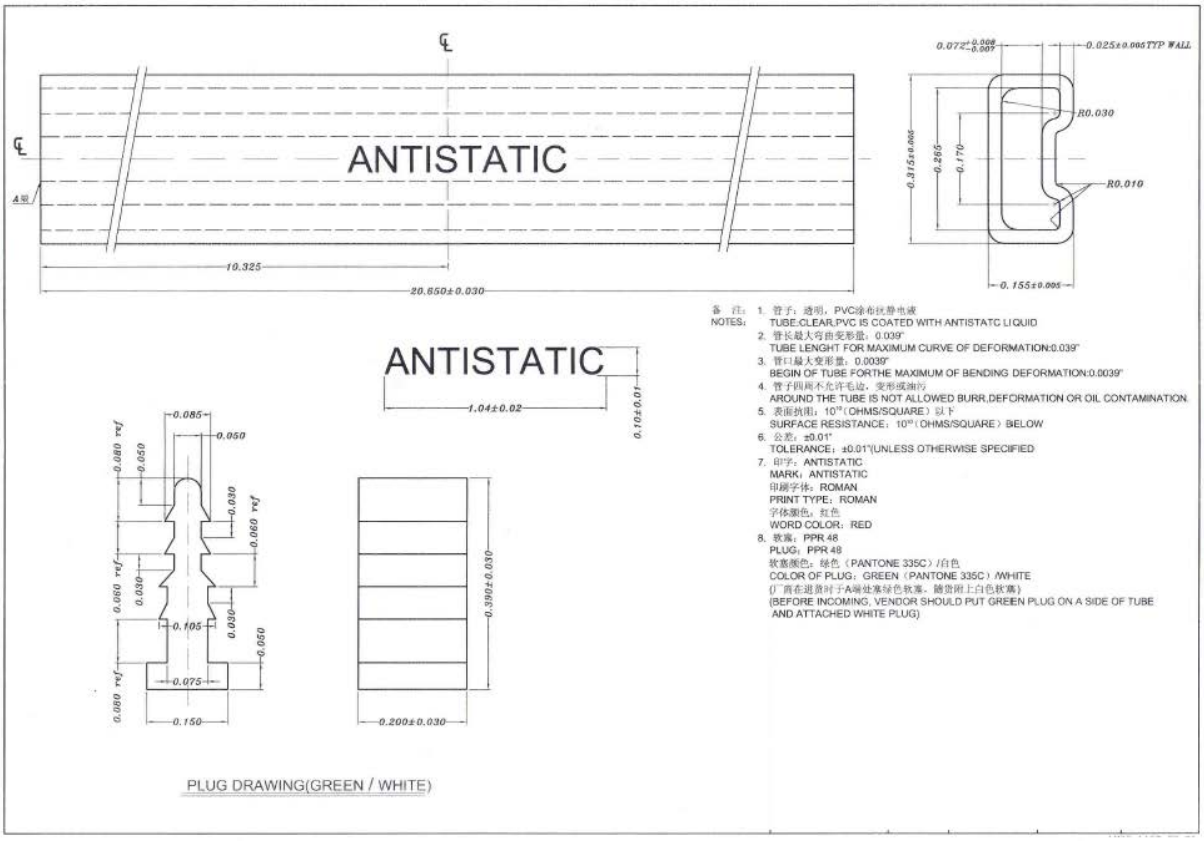
Exposed Pad (E-Pad) Dimension (mm)						
L/F Pad size	D2			E2		
	MIN	NOM	MAX	MIN	NOM	MAX
95*130mil	2.66	-	-	1.77	-	-
90*90mil	1.65	-	-	1.65	-	-

Note:

1. All dimensions refer to JEDEC OUTLINE MS-012.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.1.2. Tube Dimensions

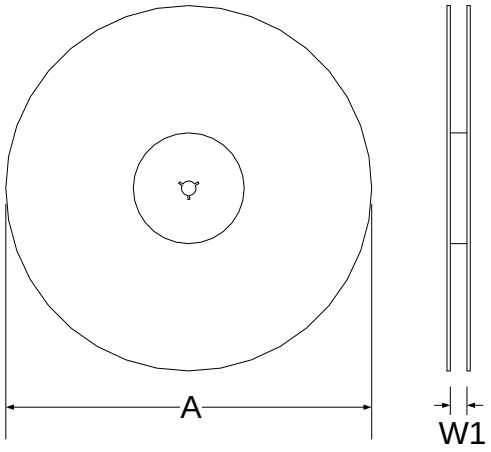




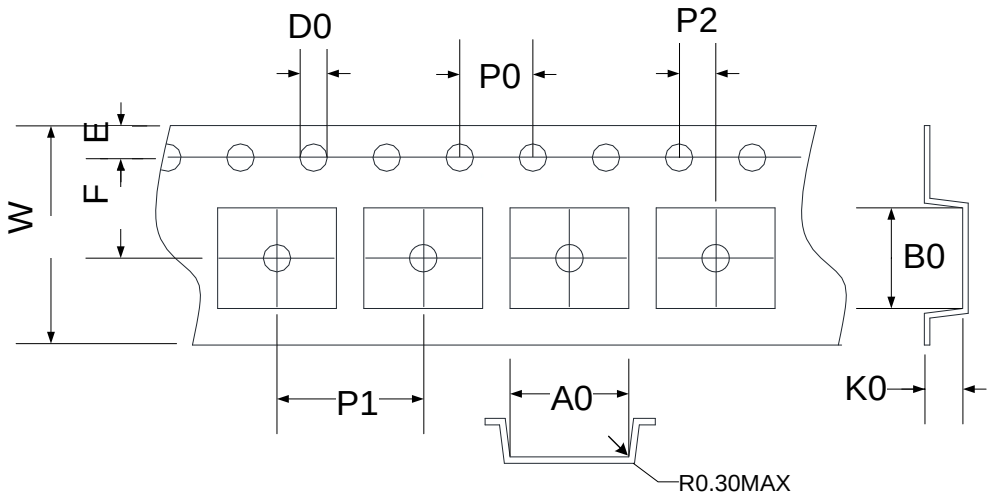
8.1.3. Tape & Reel Information

8.1.3.1. Reel Dimensions –Type1

Unit : mm



8.1.3.2. Carrier Tape Dimensions

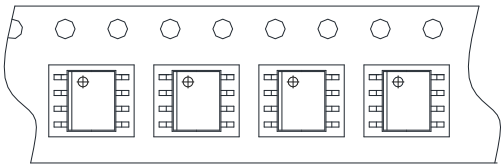


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.90	5.40	2.00	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

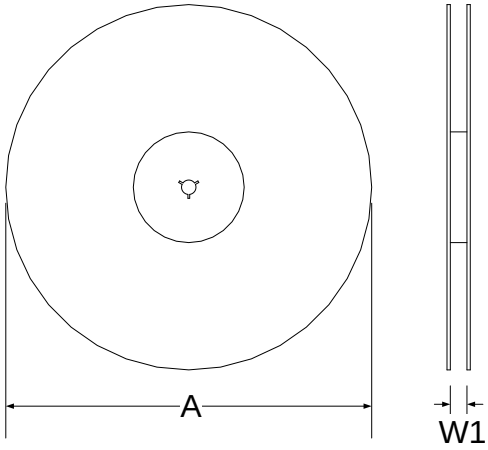
Unit : mm

8.1.3.3. Pin1 direction

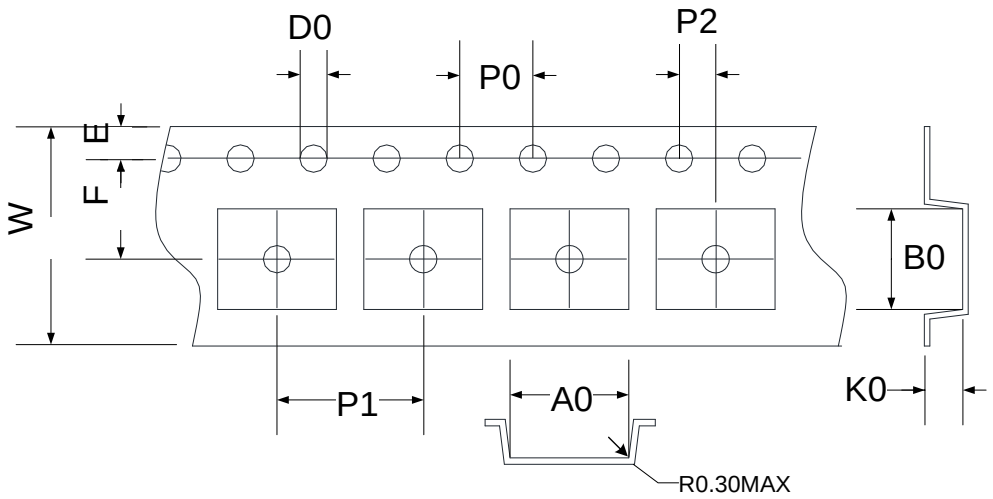


8.1.3.4. Reel Dimensions –Type2

Unit : mm



8.1.3.5. Carrier Tape Dimensions

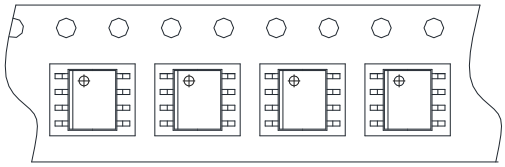


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.50	5.20	2.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

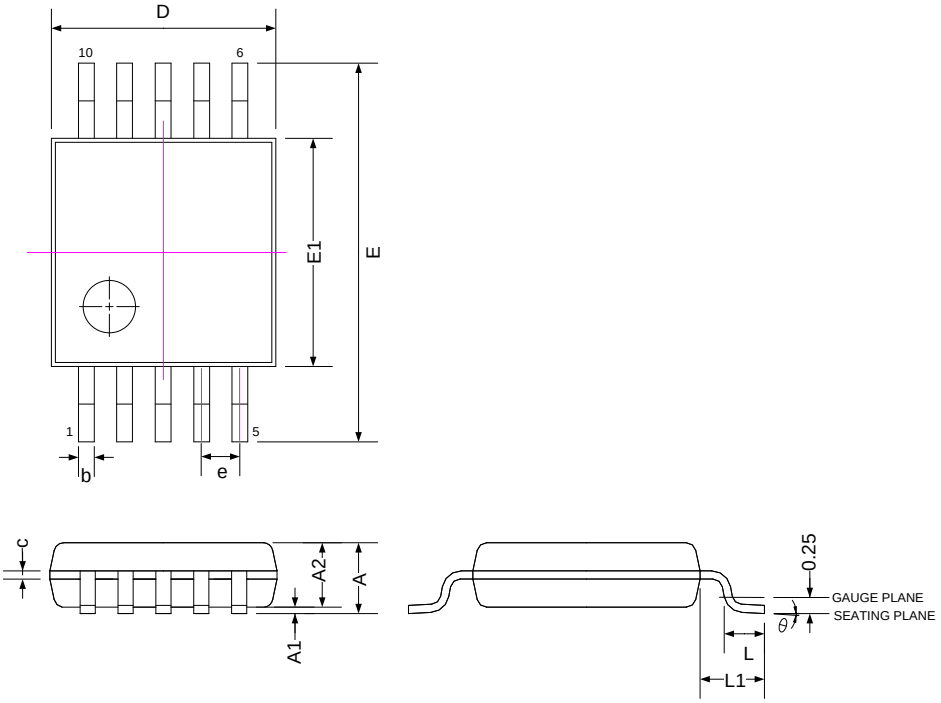
Unit : mm

8.1.3.6. Pin1 direction



8.2. MSOP10(M010)

8.2.1. Package Dimensions

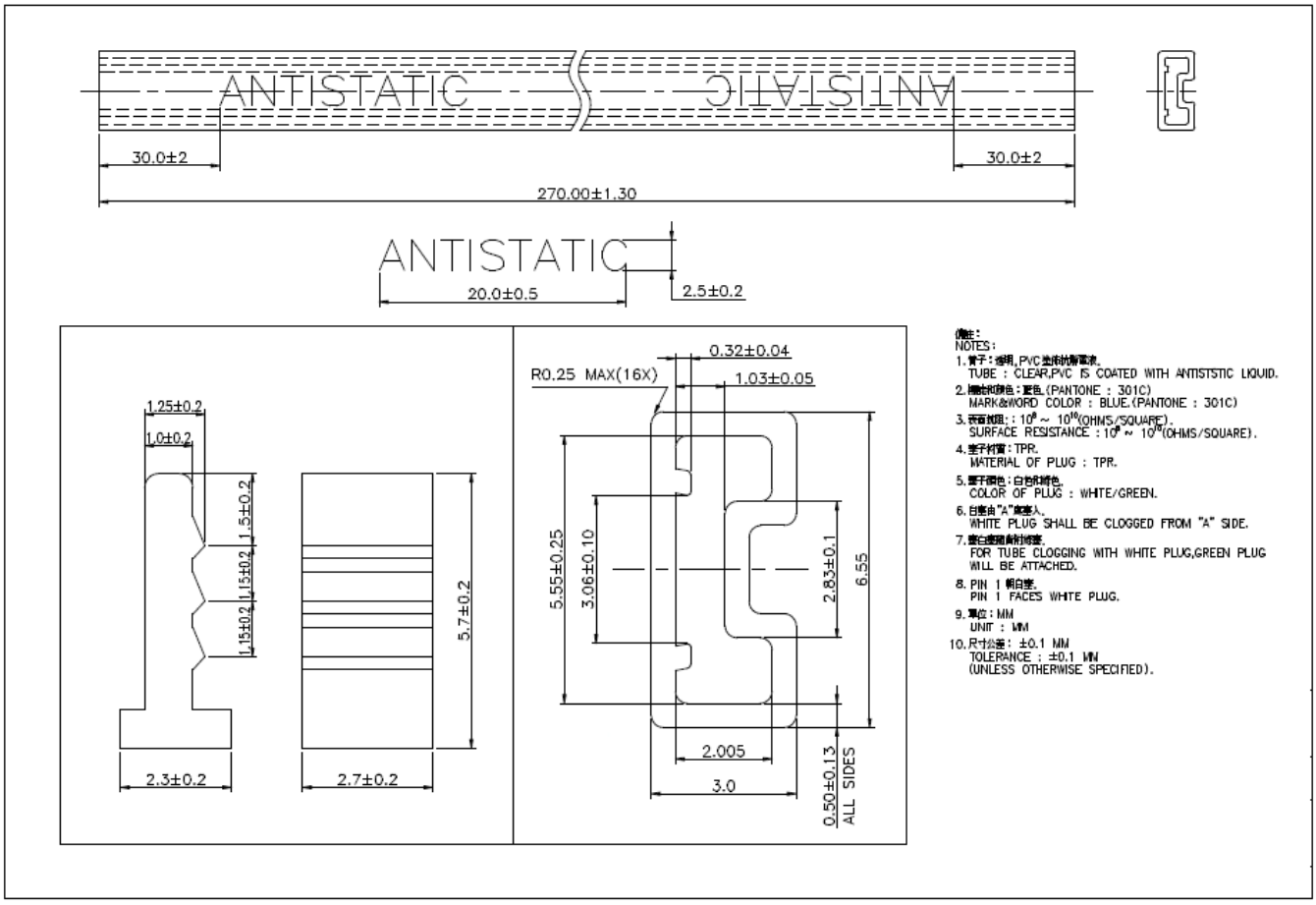


SYMBOLS	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	0.10	0.15
A2	0.75	0.85	0.95
b	0.17	0.20	0.27
c	0.08	0.15	0.23
D	3.00 BASIC		
E1	3.00 BASIC		
E	4.90 BASIC		
L	0.40	0.60	0.80
L1	0.95 REF		
e	0.50 BASIC		
θ°	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MO -187.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

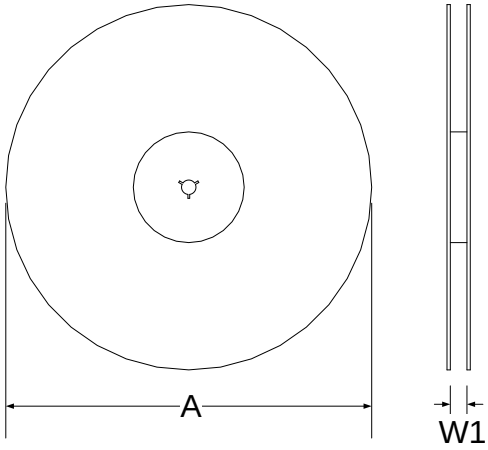
8.2.2. Tube Dimensions



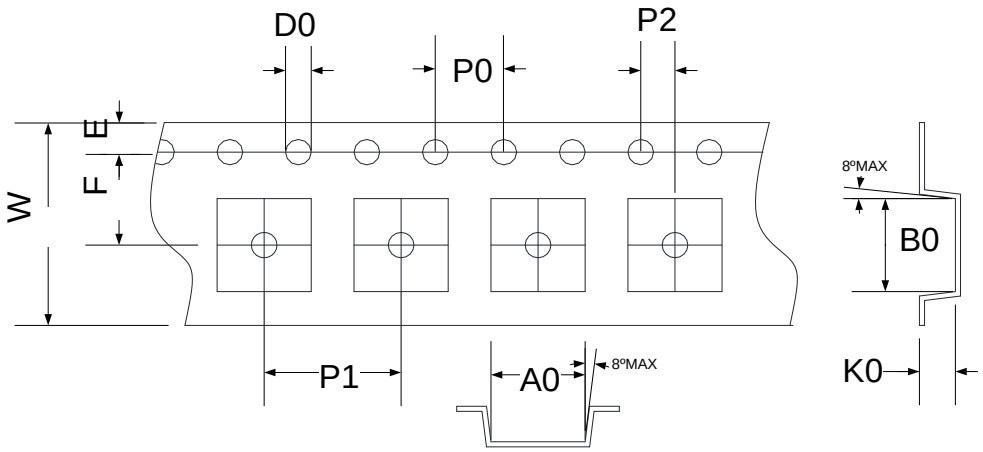
8.2.3. Tape & Reel Information

8.2.3.1. Reel Dimensions –Type1

Unit : mm



8.2.3.2. Carrier Tape Dimensions

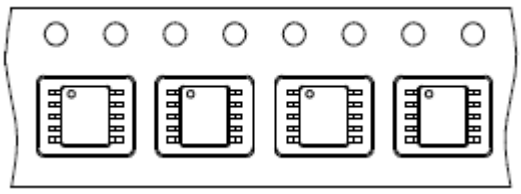


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	5.30	3.40	1.40	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	±2.00	±1.50	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.20

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

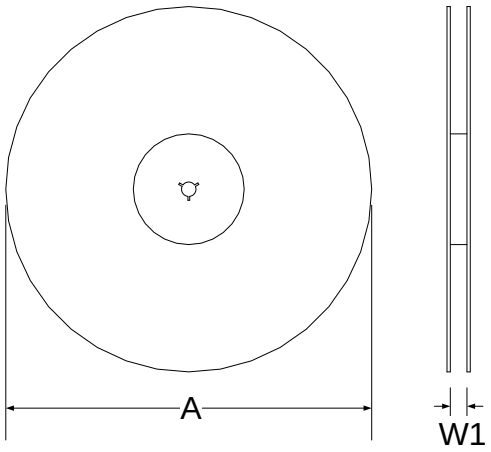
Unit : mm

8.2.3.3. Pin1 direction

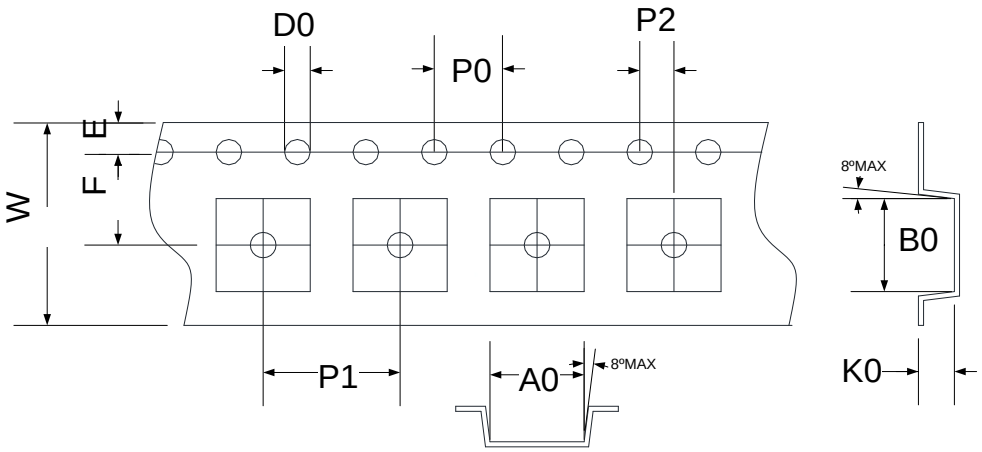


8.2.3.4. Reel Dimensions –Type2

Unit : mm



8.2.3.5. Carrier Tape Dimensions

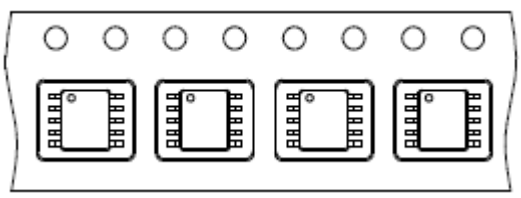


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	5.20	3.30	1.20	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	±2.00	±1.50	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

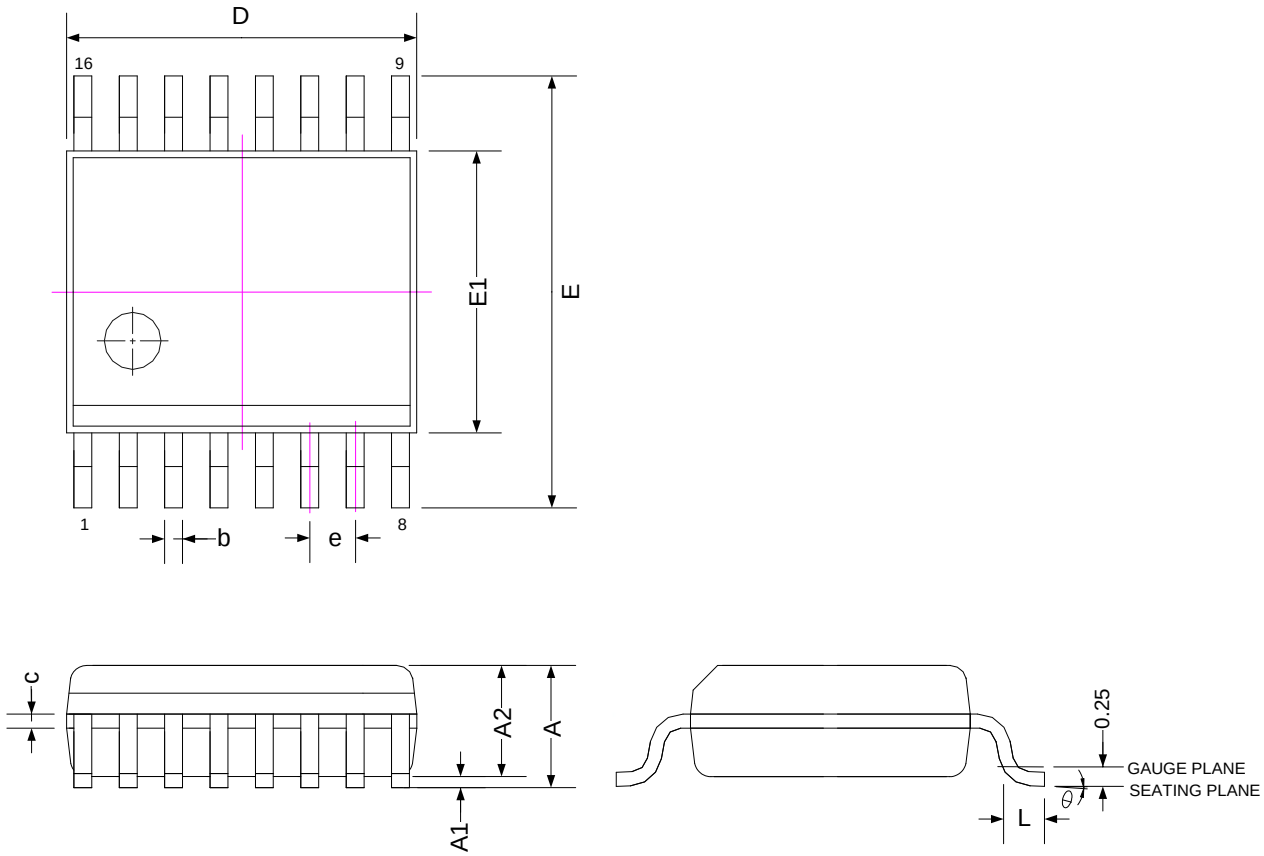
Unit : mm

8.2.3.6. Pin1 direction



8.3. SSOP16(E016)

8.3.1. Package Dimensions

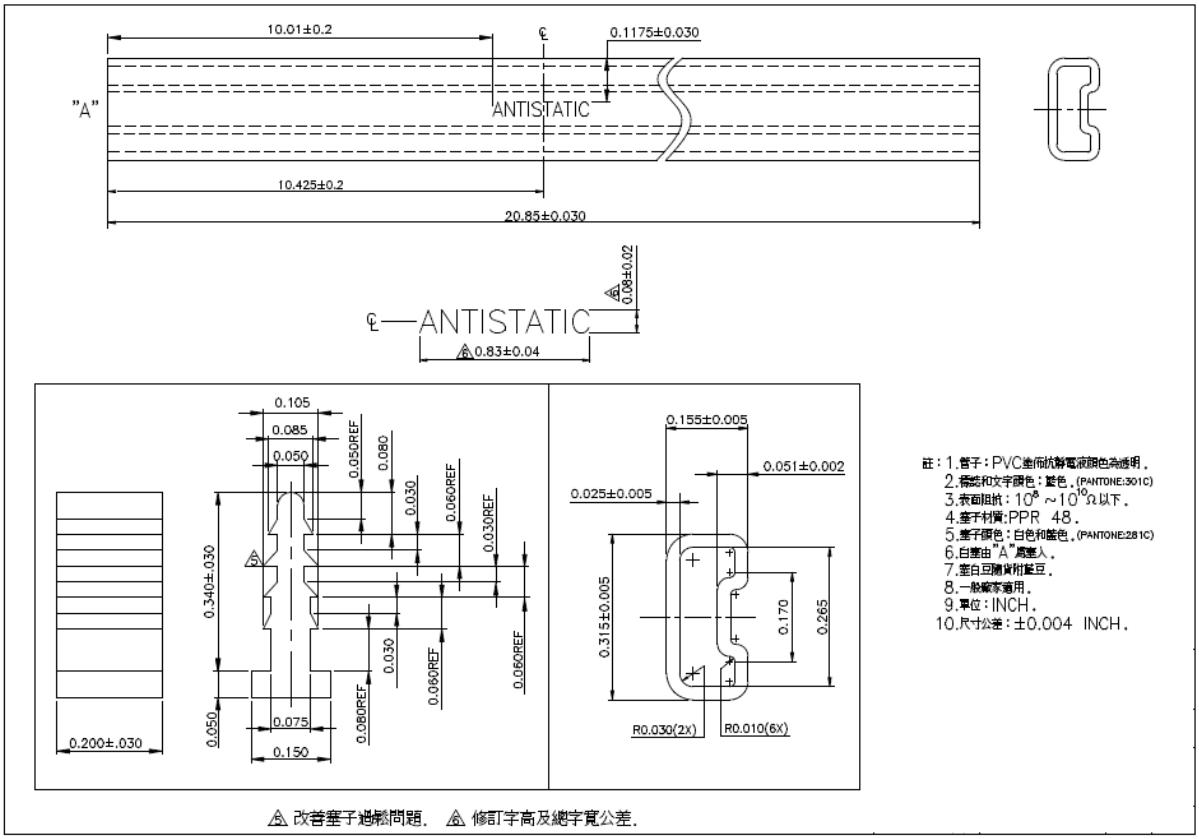


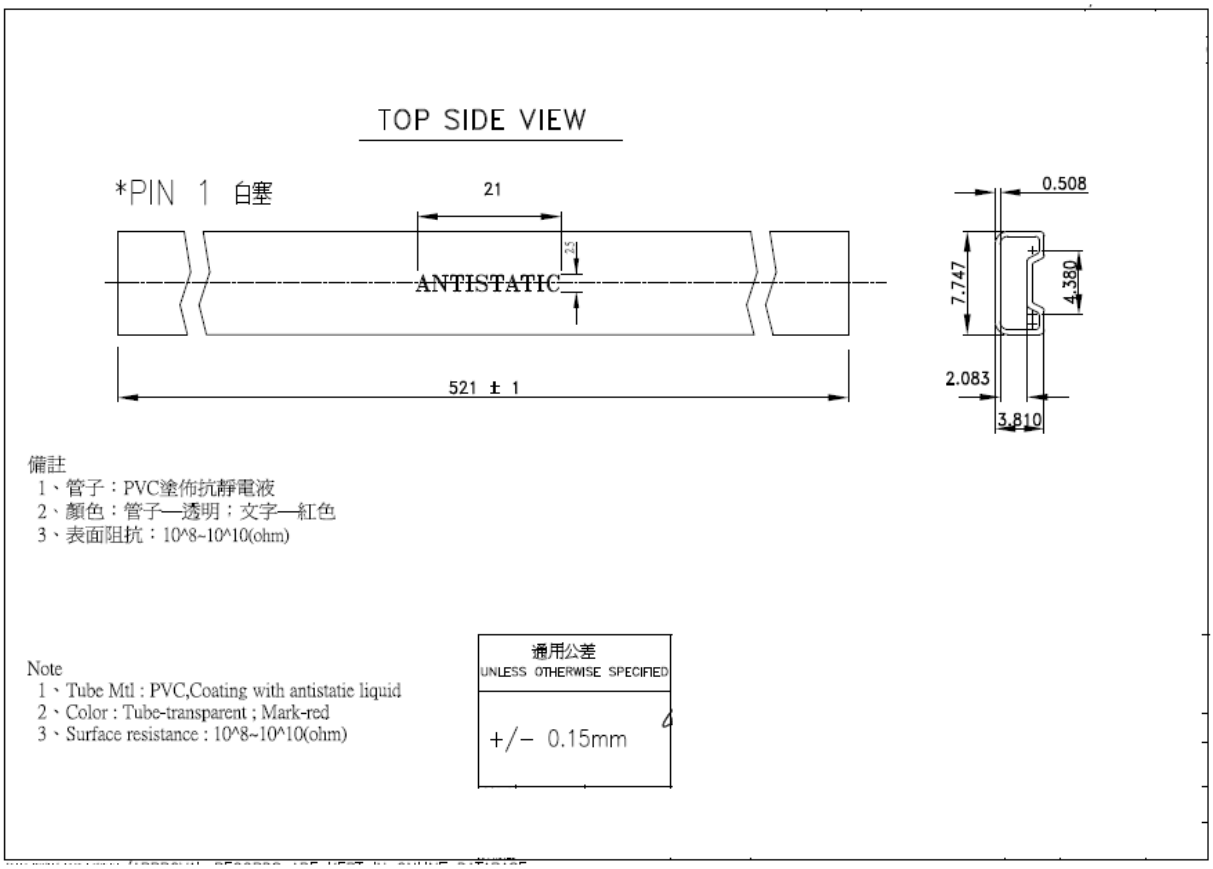
SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.25
A2	-	-	1.50
b	0.20	-	0.30
c	0.18	-	0.25
D	4.80	4.90	5.00
E1	3.81	3.91	3.99
E	5.79	5.99	6.20
L	0.41	-	1.27
e	0.635 BASIC		
θ°	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MO-137.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

8.3.2. Tube Dimensions

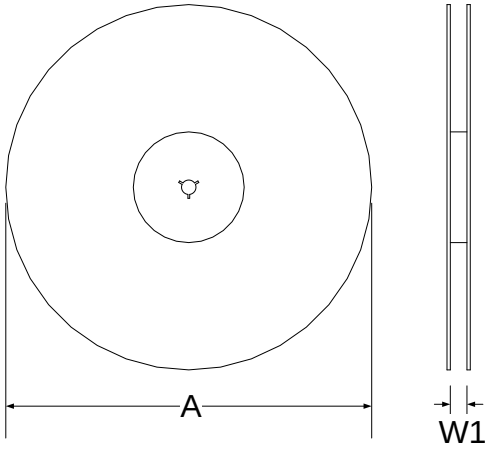




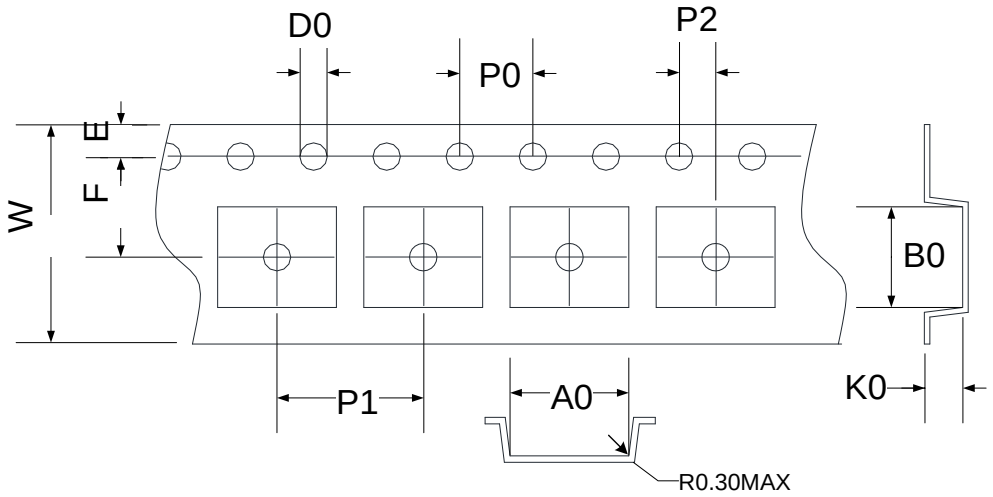
8.3.3. Tape & Reel Information

8.3.3.1. Reel Dimensions –Type1

Unit : mm



8.3.3.2. Carrier Tape Dimensions

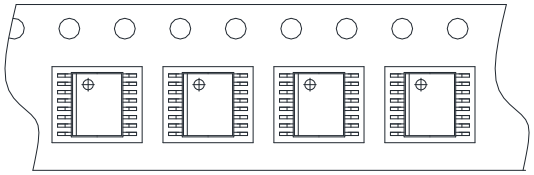


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.90	5.40	2.00	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

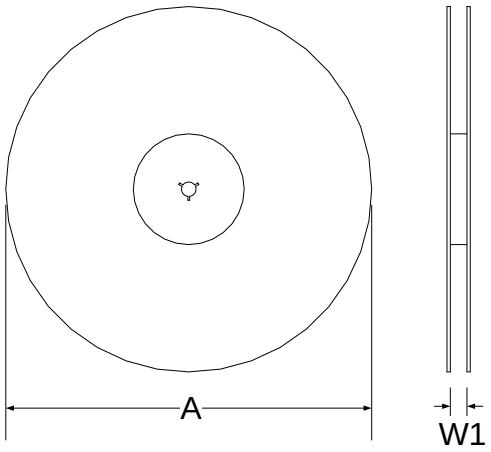
Unit : mm

8.3.3.3. Pin1 direction

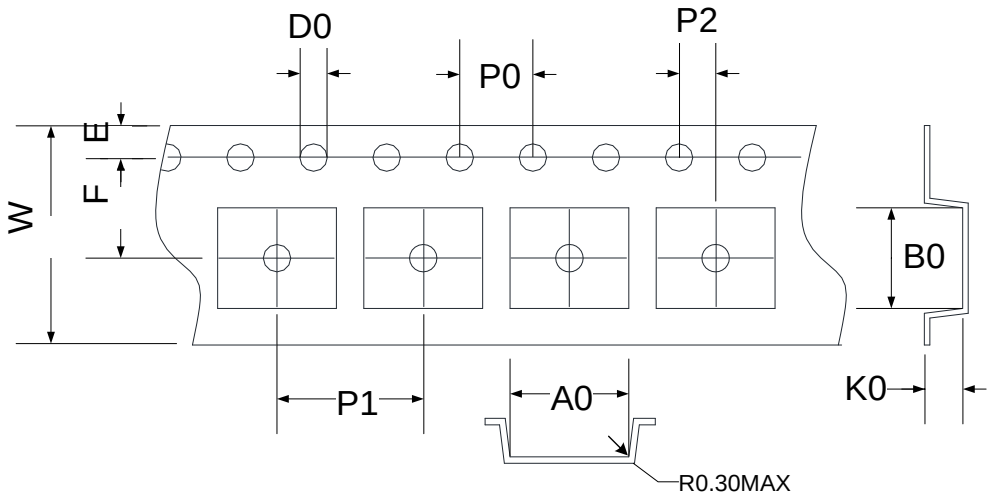


8.3.3.4. Reel Dimensions –Type2

Unit : mm



8.3.3.5. Carrier Tape Dimensions

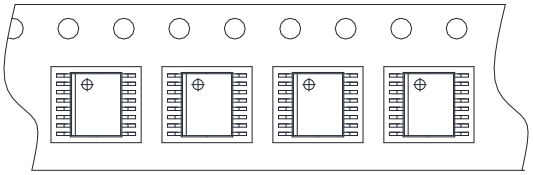


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	6.50	5.20	2.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.

Unit : mm

8.3.3.6. Pin1 direction



9. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
V01	All	First Edition
V03	All	Specification upgrade
V05	5	Reset function：delete RESET PIN
	6	Revise package pin name： VPP/RST/PT1.0/INT0 revised to VPP/PT1.0/INT1.0 PT2.0/AI6/PWMA0 revised to PT2.0/AI6/PWMA0/INT2.0 PT2.1/AI7/PWMA1 revised to PT2.1/AI7/PWMA1/INT2.1
	7	Add INT2.0 and INT2.1：Falling Edge Trigger Interrupt
	8	Delete RST
	9~10	Delete Reset circuit Revise package pin name： VPP/RST/PT1.0/INT0 revised to VPP/PT1.0/INT1.0 PT2.0/AI6/PWMA0 revised to PT2.0/AI6/PWMA0/INT2.0 PT2.1/AI7/PWMA1 revised to PT2.1/AI7/PWMA1/INT2.1
	13	0x23h、0x26h：Add E20IE、E21IE and E20IF、E21IF 0x23h、0x26h：E0IE and E0IF renamed as E10IE and E10IF 0x2Ch：Delete RST 0x41h：Delete EN_RST_PIN
	20	Remove External RST Pin related info.
	24	Revised SD18 ENOB Table and SD18 RMS Noise Table
V06	6	Remove HY10P40H SSOP16 pin map
	10	Remove 3.3. Charger Application Circuit
	25	Remove HY10P40H SSOP16 ordering Information
V07	9~10	Update Package marker information
	27	Update Green (RoHS & no Cl/Br)
	29	Update Tube Dimensions
	30~31	Update Tape & Reel Information
	33	Update Tube Dimensions
	34~35	Update Tape & Reel Information
	37	Update Tube Dimensions
	38~39	Update Tape & Reel Information