HYCON TECHNOLOGY

HY11P24
Datasheet

8-Bit RISC-Like Mixed Signal Microcontroller
Embedded Low Noise Amplifier
18-Bit ΣΔADC

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1. Features

- 8-bit RISC, 66 instructions included.
- Operating voltage range: 2.0V to 3.6V, operation temperature range: -40℃~85℃.
- External Crystal Oscillator and Internal High Precision RC Oscillator, 6 CPU clock rates enable users to have the most power-saving plan.
  - Active Mode 300uA@2MHz
  - Standby Mode 3uA@32KHz
  - Sleep Mode 1uA
- 8K Word OTP (One Time Programmable) Type program memory, 512 Byte Data Memory.
- Brownout detector and Watch dog Timer, prevents CPU from Crash.
- 18-bit fully differential input Sigma-Delta Analog-to-Digital Converter (A/D)
  - Build-in PGA (Programmable Gain Amplifier) 1/4x、1/2x、1x. …128x, 10 input signal gain selection.
  - Build-in Input zero point adjustment can increase measurement range according to different application.
  - Built-in high impedance input buffer (Not suitable for 4x or upwards input gain)
  - Build-in absolute temperature sensor
- Ultra-Low input noise (<1uVpp) OPAMP provides high output impedance small signal amplification and low current voltage transformation.
- 1.0V and 1.2V low temperatures drift parameter internal analog circuit common ground that equips with Push-Pull drive ability to provide sensor driving voltage.
- LVD low voltage detection function has 14 steps of voltage detect configuration and external input voltage detectable function.
- VDDA can select 4 different output voltage that equips with 10mA low dropout regulator function.
- Enhanced comparator
  - Two sets power voltage generator
  - Equipped with 0.25x or 0.5x operating voltage comparison and auto-transformation function and 15 steps comparison voltage configuration
  - Build-in temperature sensor
- 8-bit Timer A
- 16-bit Timer B Module has Capture/ Compare function
- 8-bit Timer C Module generates PWM/ PFD waveform
- Serial Communication SPI and EUART Module
- Support 8 stack level

2. Pin Definition

2.1 LQFP44 Pin Diagram

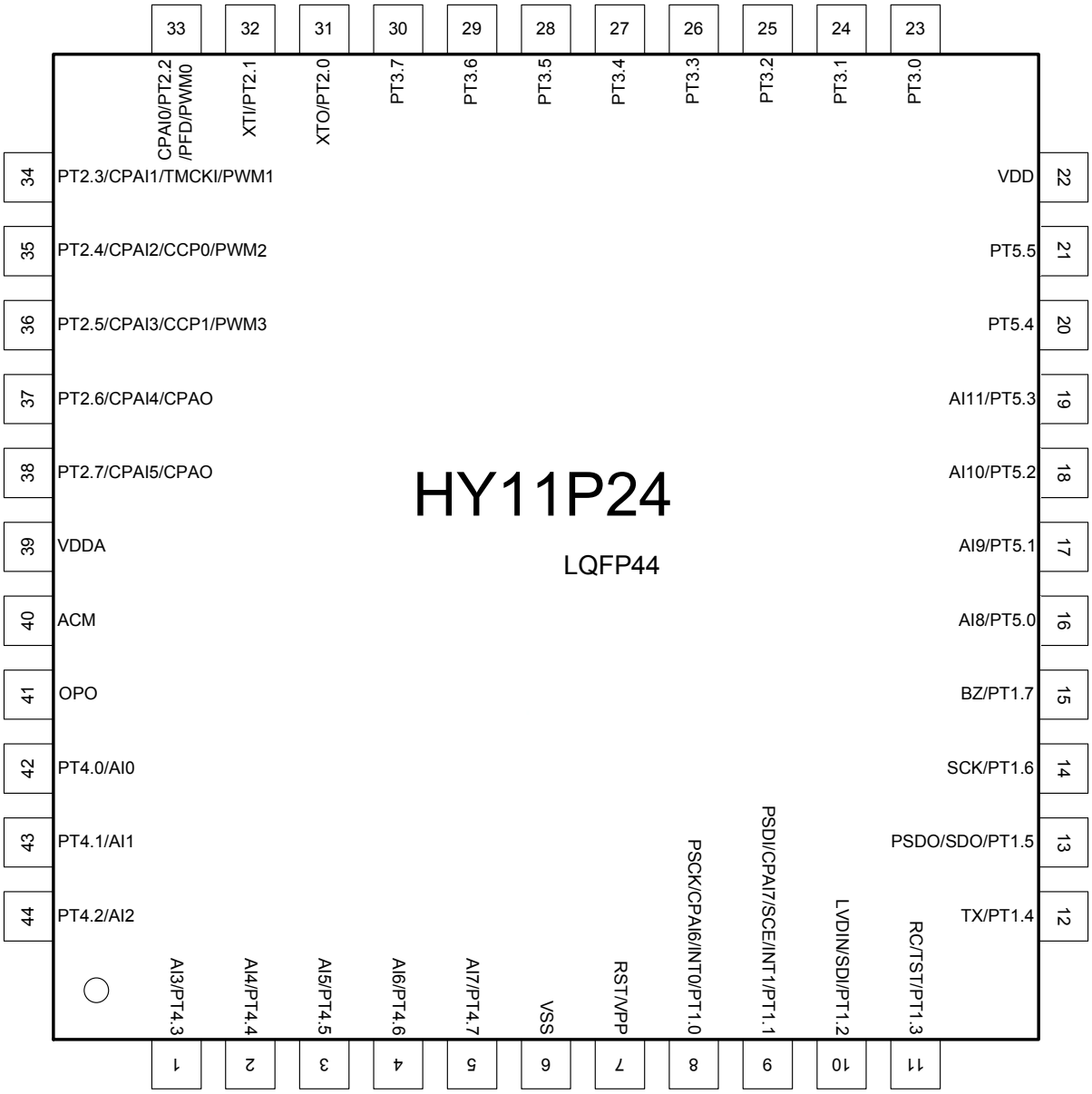

Figure 2-1 HY11P24 LQFP44 Pin Diagram

Note 1：VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2：TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3：If PT1.3 has not been configured as external button pin, the anti-interference ability will be enhanced.

2.2 LQFP48 Pin Diagram

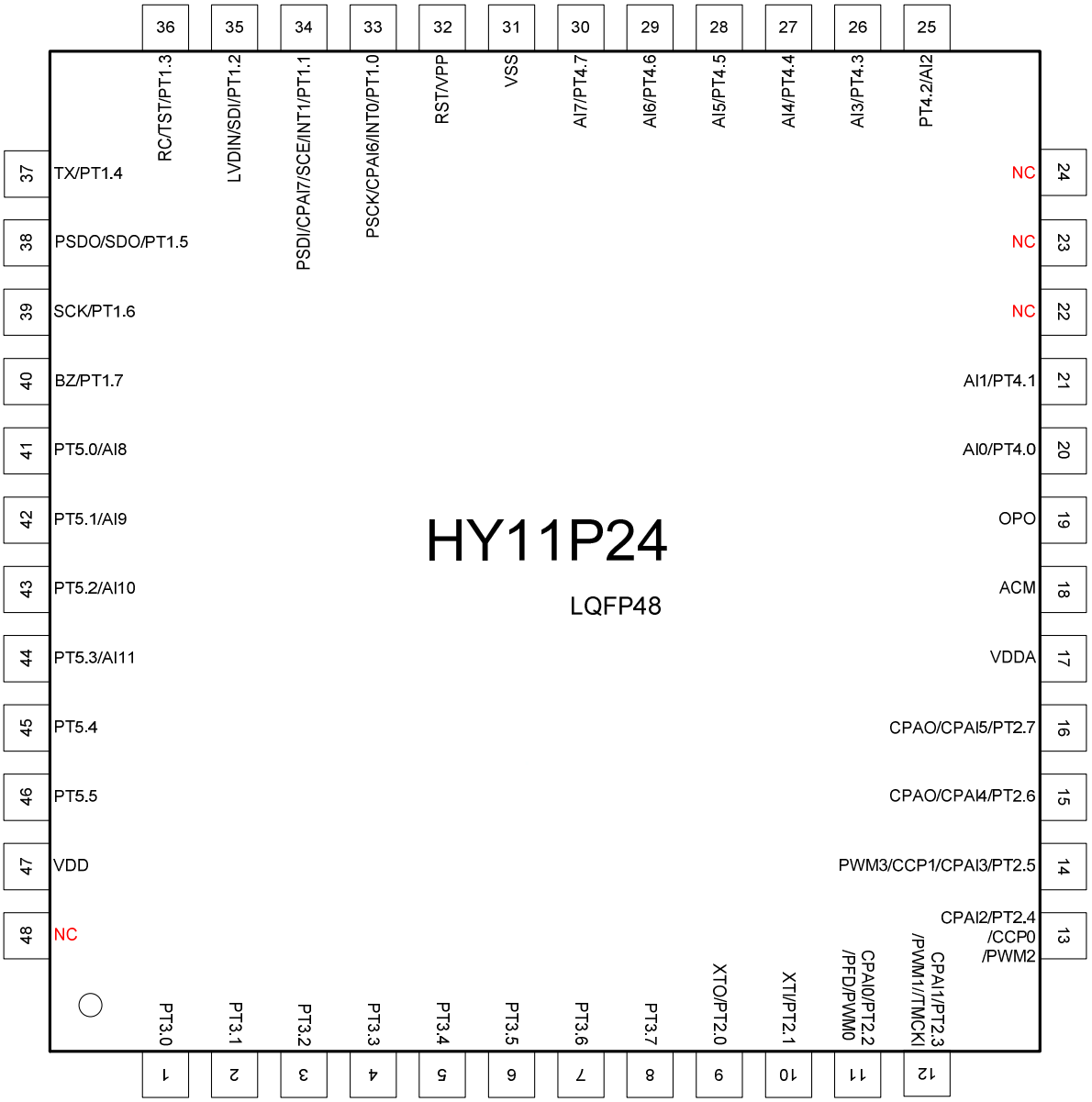

Figure 2-2 HY11P24 LQFP48 Pin Diagram

Note 1：VPP and RST use the same pin. Input voltage cannot exceed 5.8V when not programming EPROM.

Note 2：TST and PT1.3 use the same pin. Input voltage cannot exceed Vdd+0.3V while operating.

Note 3：If PT1.3 has not been configured as external button pin, the anti-interference ability will be enhanced.

2.3 LQFP44 Pinout I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

NO.	Pin Name	Pin Characteristic		Description
		Pin Type	Buffer Type	
1	PT4.3/AI3			
	PT4.3	I	C	Digital input
	AI3	A	A	Analog input channel
2	PT4.4/AI4			
	PT4.4	I	C	Digital input
	AI4	A	A	Analog input channel
3	PT4.5/AI5			
	PT4.5	I	C	Digital input
	AI5	A	A	Analog input channel
4	PT4.6/AI6			
	PT4.6	I	C	Digital input
	AI6	A	A	Analog input channel
5	PT4.7/AI7			
	PT4.7	I	C	Digital input
	AI7	A	A	Analog input channel
6	VSS	P	P	Grounding pin for IC operation power source
7	RST/VPP			
	RST	I	S	Reset IC
	VPP	P	P	EPROM programming voltage source
8	PT1.0/INT0/PSCK/CPAI6			
	PT1.0	I	S	Digital input
	INT0	I	S	Interrupt source INT0
	PSCK	I	S	OTP programming interface SCK
	CPAI6	I	A	ECPA analog input channel
9	PT1.1/INT1/PSDI/SCE/CPAI7			
	PT1.1	I	S	Digital input
	INT1	I	S	Interrupt source INT1
	PSDI	I	S	OTP programming interface SDI
	SCE	I/O	S	SPI communication interface SCE
	CPAI7	I	A	ECPA analog input channel
10	PT1.2/SDI/LVDIN			

	PT1.2	I	S	Digital input
	SDI	I/O	S	SPI communication interface SDI
	LVDIN	A	A	LVD external signal input
11	PT1.3/TST/RC			
	PT1.3	I	S	Digital input
	RC	I	S	EUART communication interface RC
	TST	I	S	Test Mode input pin (invalid)
12	PT1.4/TX			
	PT1.4	I/O	S	Digital I/O
	TX	I/O	S	EUART communication interface TX
13	PT1.5/PSDO/SDO			
	PT1.5	I/O	S	Digital I/O
	PSDO	O	C	OTP programming interface SDO
	SDO	I/O	S	SPI communication interface SDO
14	PT1.6/SCK			
	PT1.6	I/O	S	Digital I/O
	SCK	I/O	S	SPI communication interface SCK
15	PT1.7/BZ			
	PT1.7	I/O	S	Digital I/O
	BZ	O	C	Buzzer output
16	PT5.0/AI8			
	PT5.0	I	C	Digital input
	AI8	A	A	Analog input channel
17	PT5.1/AI9			
	PT5.1	I	C	Digital input
	AI9	A	A	Analog input channel
18	PT5.2/AI10			
	PT5.2	I	C	Digital input
	AI10	A	A	Analog input channel
19	PT5.3/AI11			
	PT5.3	I	C	Digital input
	AI11	A	A	Analog input channel
20	PT5.4	I	C	Digital input
21	PT5.5	I	C	Digital input
22	VDD	P	P	Voltage source for IC operation
23	PT3.0	I/O	C	Digital I/O
24	PT3.1	I/O	C	Digital I/O
25	PT3.2	I/O	C	Digital I/O

26	PT3.3	I/O	C	Digital I/O
27	PT3.4	I/O	C	Digital I/O
28	PT3.5	I/O	C	Digital I/O
29	PT3.6	I/O	C	Digital I/O
30	PT3.7	I/O	C	Digital I/O
31	PT2.0/XTO			
	PT2.0	I/O	S	Digital I/O
	XTO	A	A	External oscillator output
32	PT2.1/XTI			
	PT2.1	I/O	S	Digital I/O
	XTI	A	A	External oscillator input
33	PT2.2/PFD/CPAI0/PWM0			
	PT2.2	I/O	C	Digital I/O
	PFD	O	C	PFD output
	CPAI0	I	A	ECPA analog input channel
	PWM0	O	C	PWM output
34	PT2.3/TMCKI/CPAI1/PWM1			
	PT2.3	I/O	S	Digital I/O
	TMCKI	I	S	TIMERC clock source input
	CPAI1	I	A	ECPA analog input channel
	PWM1	O	C	PWM output
35	PT2.4/CCP0/CPAI2/PWM2			
	PT2.4	I/O	S	Digital I/O
	CCP0	I	S	Capture/compare mode signal port
	CPAI2	I	A	ECPA analog input channel
	PWM2	O	C	PWM output
36	PT2.5/CCP1/CPAI3/PWM3			
	PT2.5	I/O	S	Digital I/O
	CCP1	I	S	Capture/compare mode signal port
	CPAI3	I	A	ECPA analog input channel
	PWM3	O	C	PWM output
37	PT2.6/CPAI4/CPAO			
	PT2.6	I/O	C	Digital I/O
	CPAI4	I	A	ECPA analog input channel
	CPAO	I	A	ECPA comparator output
38	PT2.7/CPAI5/CPAO			
	PT2.7	I/O	C	Digital I/O
	CPAI5	I	A	ECPA analog input channel

	CPAO	I	A	ECPA comparator output
39	VDDA	P	P	Regulator output, analog circuit power source
40	ACM	P	P	Internal analog circuit command ground pin
41	OPO	A	A	OP output
42	PT4.0/AI0 PT4.0 AI0	 I A	 C A	 Digital input Analog input channel
43	PT4.1/AI1 PT4.1 AI1	 I A	 C A	 Digital input Analog input channel
44	PT4.2/AI2 PT4.2 AI2	 I A	 C A	 Digital input Analog input channel

Table 2-1 Pin Definition and Function Description

2.4 LQFP48 Pinout I/O Description

"I/O" input/output, "I" input, "O" output, "S" Smith Trigger, "C" CMOS features compatible input/output, "P" power supply, "A" analog channel

NO.	Pin Name	Pin Characteristic		Description
		Pin Type	Buffer Type	
1	PT3.0	I/O	C	Digital I/O
2	PT3.1	I/O	C	Digital I/O
3	PT3.2	I/O	C	Digital I/O
4	PT3.3	I/O	C	Digital I/O
5	PT3.4	I/O	C	Digital I/O
6	PT3.5	I/O	C	Digital I/O
7	PT3.6	I/O	C	Digital I/O
8	PT3.7	I/O	C	Digital I/O
9	PT2.0/XTO			
	PT2.0	I/O	S	Digital I/O
	XTO	A	A	External oscillator output
10	PT2.1/XTI			
	PT2.1	I/O	S	Digital I/O
	XTI	A	A	External oscillator input
11	PT2.2/PFD/CPAI0/PWM0			
	PT2.2	I/O	C	Digital I/O
	PFD	O	C	PFD output
	CPAI0	I	A	ECPA analog input channel
	PWM0	O	C	PWM output
12	PT2.3/TMCKI/CPAI1/PWM1			
	PT2.3	I/O	S	Digital I/O
	TMCKI	I	S	TIMERC clock source input
	CPAI1	I	A	ECPA analog input channel
	PWM1	O	C	PWM output
13	PT2.4/CCP0/CPAI2/PWM2			
	PT2.4	I/O	S	Digital I/O
	CCP0	I	S	Capture/compare mode signal port
	CPAI2	I	A	ECPA analog input channel
	PWM2	O	C	PWM output
14	PT2.5/CCP1/CPAI3/PWM3			
	PT2.5	I/O	S	Digital I/O
	CCP1	I	S	Capture/compare mode signal port
	CPAI3	I	A	ECPA analog input channel

	PWM3	O	C	PWM output
15	PT2.6/CPAI4/CPAO			
	PT2.6	I/O	C	Digital I/O
	CPAI4	I	A	ECPA analog input channel
	CPAO	I	A	ECPA comparator output
16	PT2.7/CPAI5/CPAO			
	PT2.7	I/O	C	Digital I/O
	CPAI5	I	A	ECPA analog input channel
	CPAO	I	A	ECPA comparator output
17	VDDA	P	P	Regulator output, analog circuit power source
18	ACM	P	P	Internal analog circuit command ground pin
19	OPO	A	A	OP output
20	PT4.0/AI0			
	PT4.0	I	C	Digital input
	AI0	A	A	Analog input channel
21	PT4.1/AI1			
	PT4.1	I	C	Digital input
	AI1	A	A	Analog input channel
22	NC	-	-	unused
23	NC	-	-	unused
24	NC	-	-	unused
25	PT4.2/AI2			
	PT4.2	I	C	Digital input
	AI2	A	A	Analog input channel
26	PT4.3/AI3			
	PT4.3	I	C	Digital input
	AI3	A	A	Analog input channel
27	PT4.4/AI4			
	PT4.4	I	C	Digital input
	AI4	A	A	Analog input channel
28	PT4.5/AI5			
	PT4.5	I	C	Digital input
	AI5	A	A	Analog input channel
29	PT4.6/AI6			
	PT4.6	I	C	Digital input
	AI6	A	A	Analog input channel

30	PT4.7/AI7 PT4.7 AI7	 I A	 C A	 Digital input Analog input channel
31	VSS	P	P	Grounding pin for IC operation power source
32	RST/VPP RST VPP	 I P	 S P	 Reset IC EPROM programming voltage source
33	PT1.0/INT0/PSCK/CPAI6 PT1.0 INT0 PSCK CPAI6	 I I I I	 S S S A	 Digital input Interrupt source INT0 OTP programming interface SCK ECPA analog input channel
34	PT1.1/INT1/PSDI/SCE/CPAI7 PT1.1 INT1 PSDI SCE CPAI7	 I I I I/O I	 S S S S A	 Digital input Interrupt source INT1 OTP programming interface SDI SPI communication interface SCE ECPA analog input channel
35	PT1.2/SDI/LVDIN PT1.2 SDI LVDIN	 I I/O A	 S S A	 Digital input SPI communication interface SDI LVD external signal input
36	PT1.3/TST/RC PT1.3 RC TST	 I I I	 S S S	 Digital input EUART communication interface RC Test Mode input pin (invalid)
37	PT1.4/TX PT1.4 TX	 I/O I/O	 S S	 Digital I/O EUART communication interface TX
38	PT1.5/PSDO/SDO PT1.5 PSDO SDO	 I/O O I/O	 S C S	 Digital I/O OTP programming interface SDO SPI communication interface SDO
39	PT1.6/SCK PT1.6 SCK	 I/O I/O	 S S	 Digital I/O SPI communication interface SCK

40	PT1.7/BZ PT1.7 BZ	I/O O	S C	Digital I/O Buzzer output
41	PT5.0/AI8 PT5.0 AI8	I A	C A	Digital input Analog input channel
42	PT5.1/AI9 PT5.1 AI9	I A	C A	Digital input Analog input channel
43	PT5.2/AI10 PT5.2 AI10	I A	C A	Digital input Analog input channel
44	PT5.3/AI11 PT5.3 AI11	I A	C A	Digital input Analog input channel
45	PT5.4	I	C	Digital input
46	PT5.5	I	C	Digital input
47	VDD	P	P	Voltage source for IC operation
48	NC	-	-	unused

Table 2-2 Pin Definition and Function Description

3. Application Circuit

3.1 Four Sets Bridge Sensor I

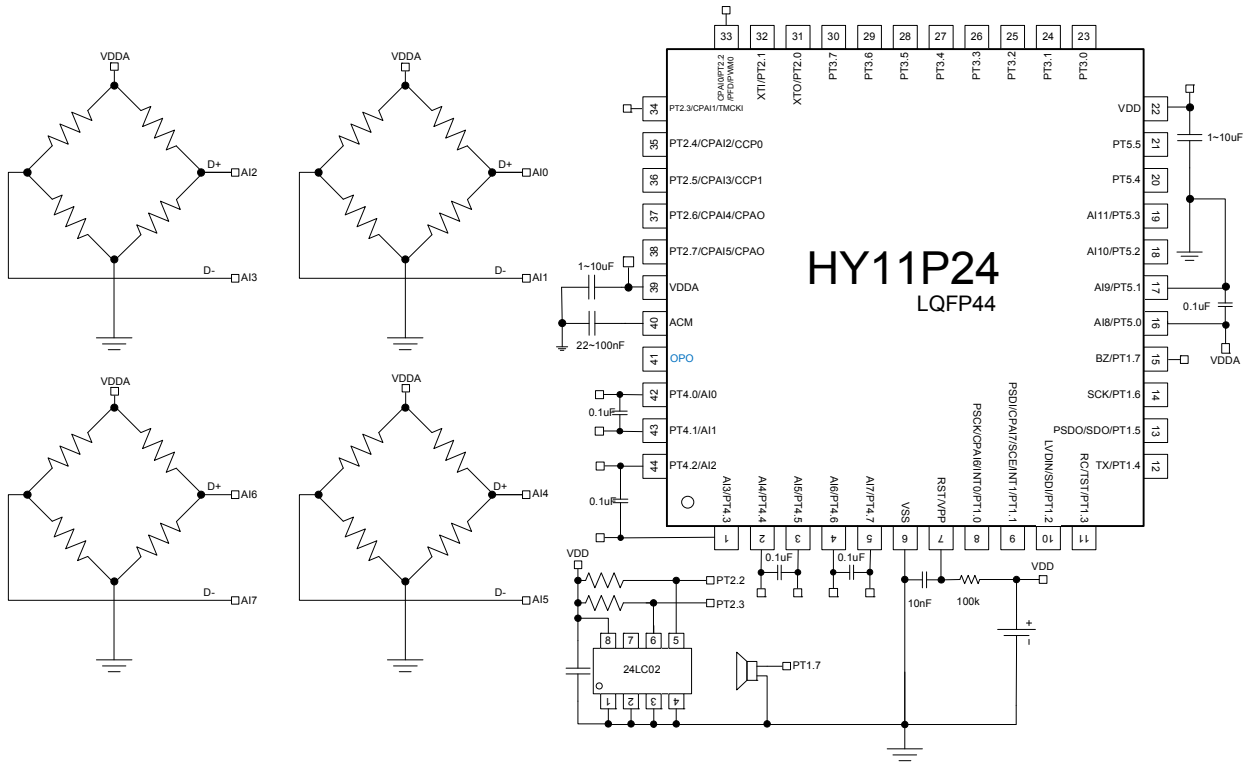

Figure 3-1 Applicaiton Circuit of Bridge Sensor

Note：DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address

3.2 Four Sets Bridge Sensor II

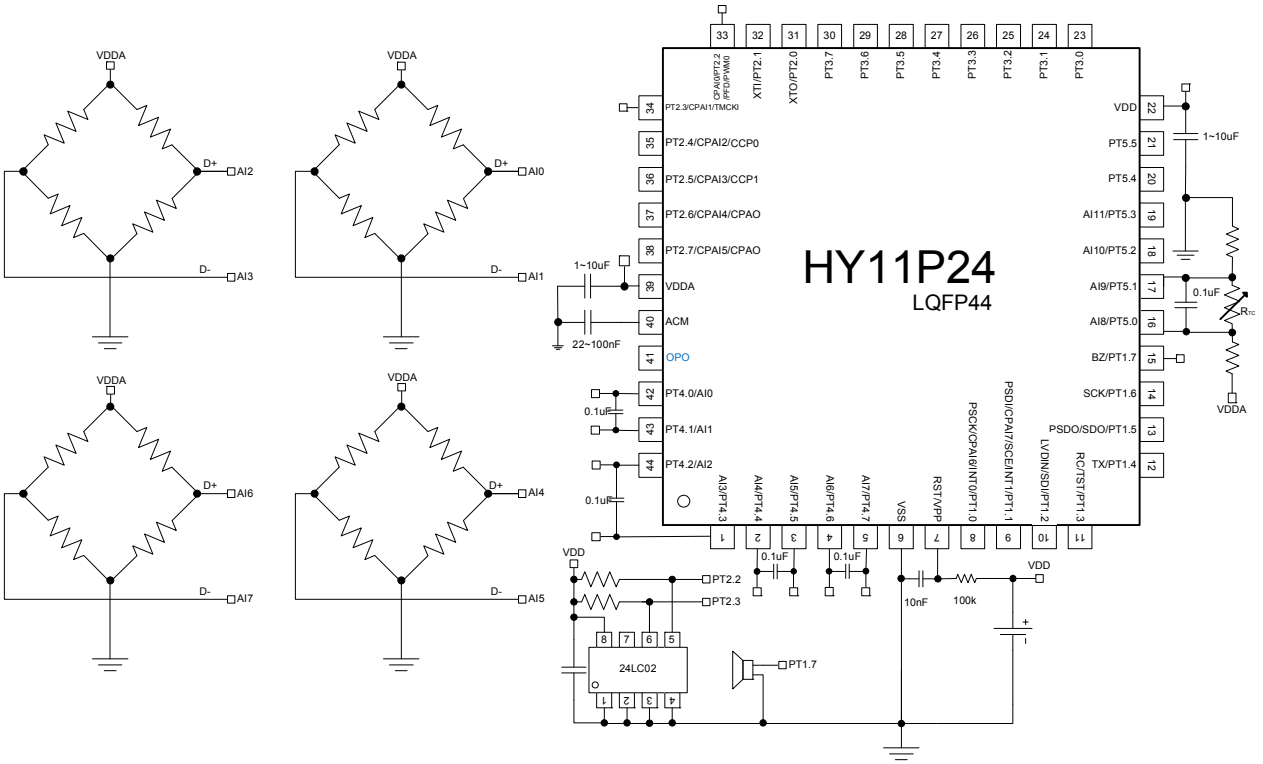

Figure 3-2 Application Circuit of Temperature Compensation Bridge Sensor

Note 1：Using temperature compensation resistor NTC basic circuit

Note 2：DCSET[2:0] can conduct bias adjustment of Load Cell zero point voltage address

4. Function Outline

4.1 Internal Block Diagram

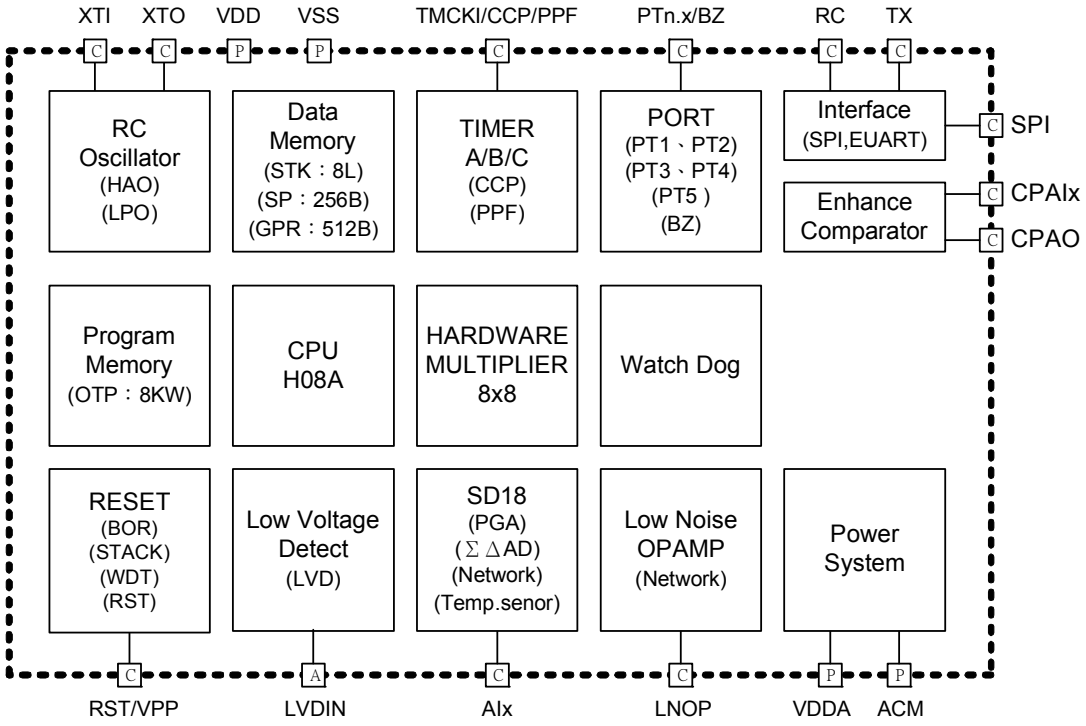

Figure 4-1 HY11P24 Internal Block Diagram

4.2 Related Description and Supporting Documents

IC Function Related Operating Instruction

DS-HY11P24-Vxx	HY11P24 Data Sheet
UG-HY11S14-Vxx	HY11Pxx Series Users' Manual
APD-CORE002-Vxx	H08A Instruction Description

Development Tool Related Operating Instruction

APD-HYIDE006-Vxx	HY11xxx Series Development Tool Software Instruction Manual
APD-HYIDE005-Vxx	HY11xxx Series Development Tool Hardware Instruction Manual
APD-OTP001-Vxx	OTP Products Programming Pin Manual

Product Production Related Operating Instruction

APD-HYIDE004-Vxx	HY1xxxx Series Production Line Specialized Programmer Manual
BDI-HY11P24-Vxx	HY11P24 Individual Product Die Bonding Information

4.3 SD18 Network

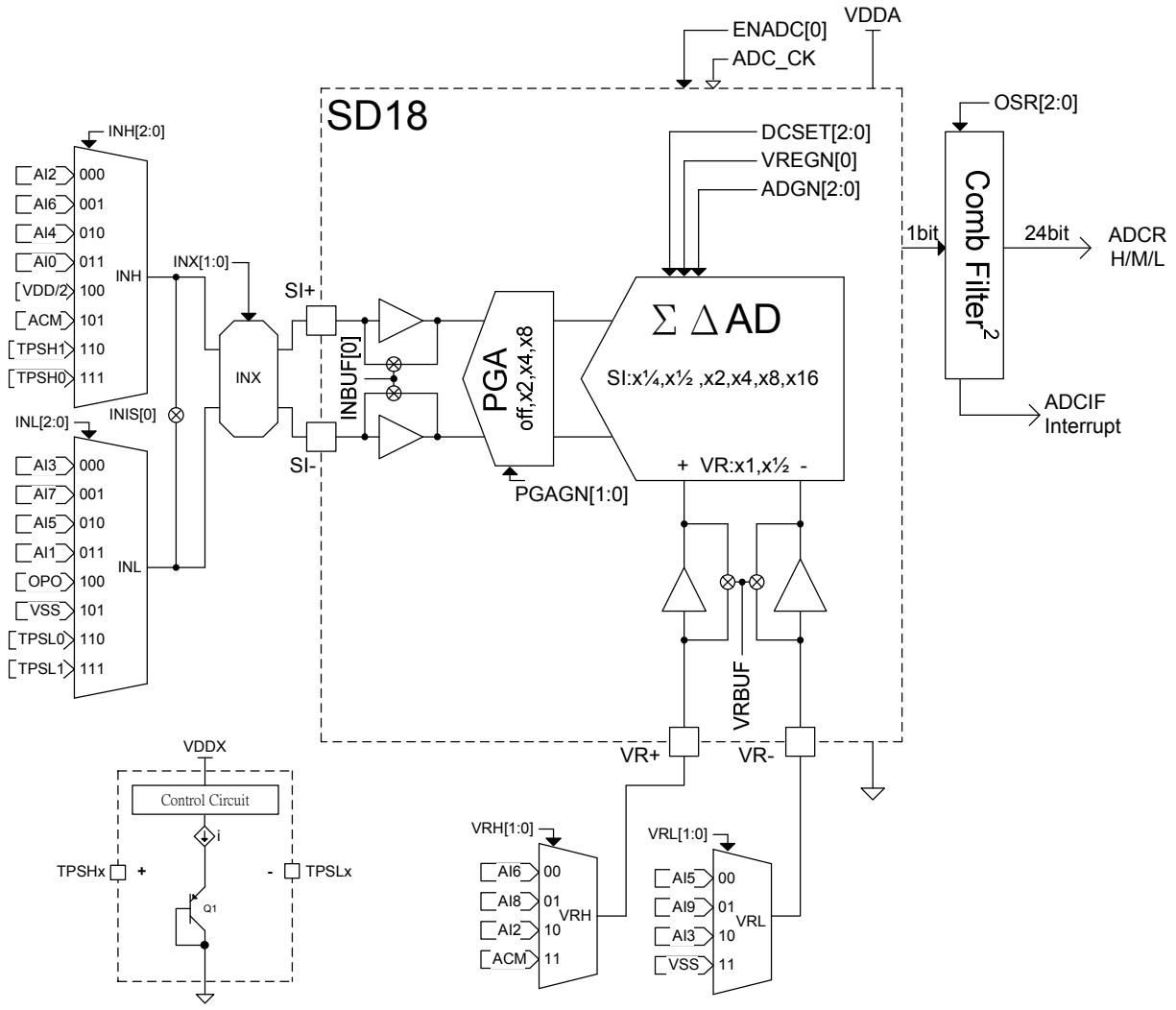

Figure 4-2 SD18 Network

4.4 Low Noise OPAMP Network

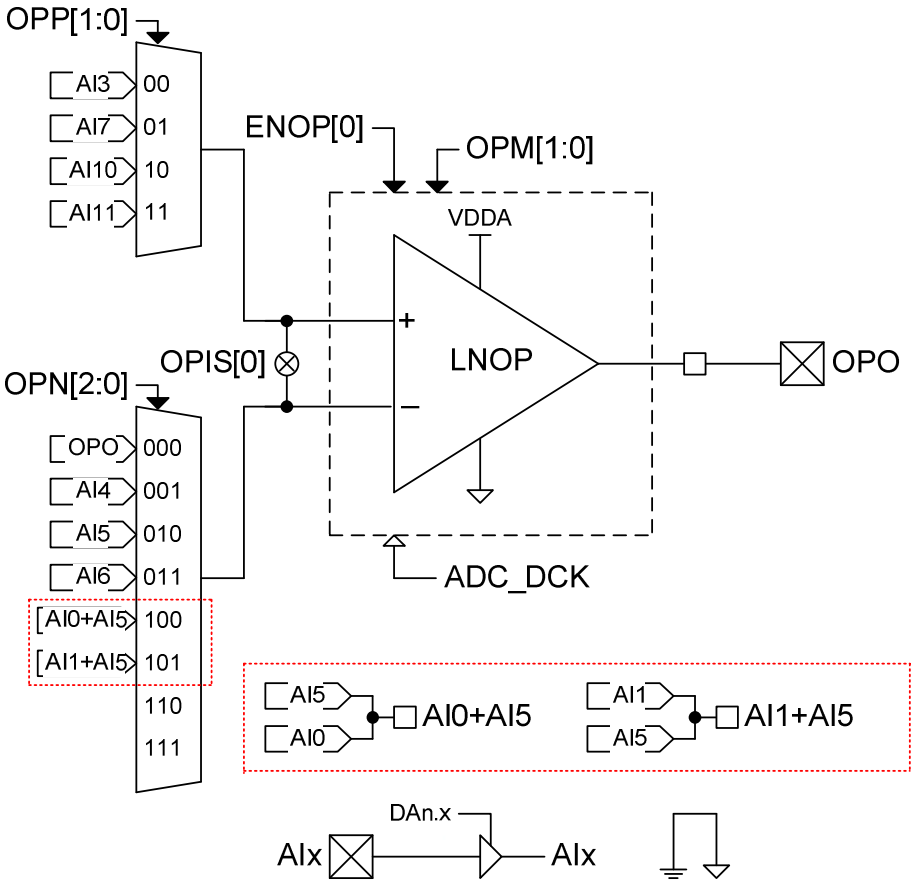

Figure 4-3 Low Noise OPAMP Network

4.5 Enhance Comparator Network

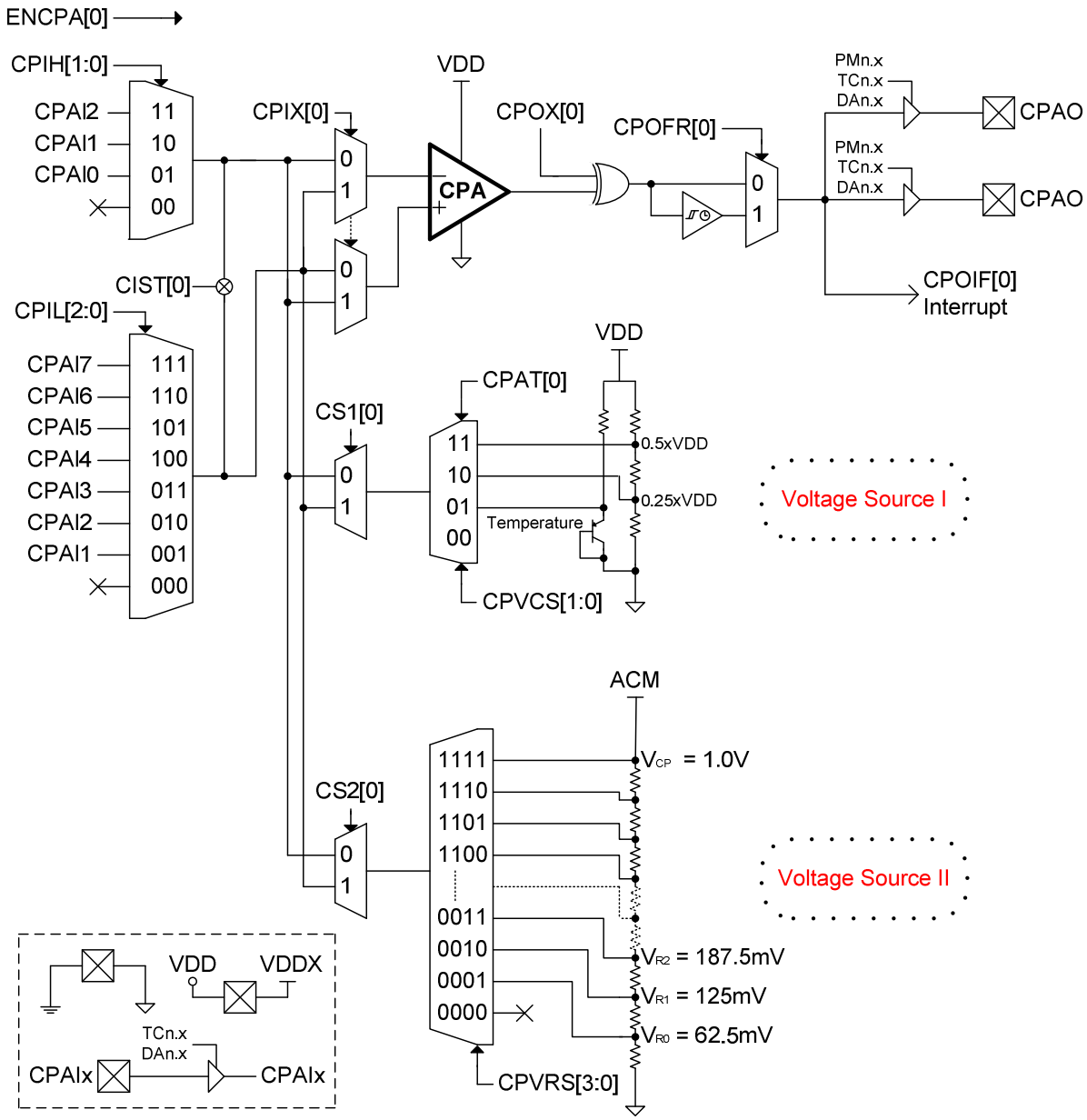

Figure 4-4 Enhance Comparator Network

5. Register List

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W
00H	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								N/A	N/A	* * * * * * * *
01H	POINC0	Contents of FSR0 to address data memory value of FSR0 post-incremented								N/A	N/A	* * * * * * * *
02H	PODEC0	Contents of FSR0 to address data memory value of FSR0 post-decremented								N/A	N/A	* * * * * * * *
03H	PRINC0	Contents of FSR0 to address data memory value of FSR0 pre-incremented								N/A	N/A	* * * * * * * *
04H	PLUSW0	Contents of FSR0 to address data memory value of FSR0 offset by W								N/A	N/A	* * * * * * * *
05H	INDF1	Contents of FSR1 to address data memory value of FSR0 not changed								N/A	N/A	* * * * * * * *
06H	POINC1	Contents of FSR1 to address data memory value of FSR0 post-incremented								N/A	N/A	* * * * * * * *
07H	PODEC1	Contents of FSR1 to address data memory value of FSR0 post-decremented								N/A	N/A	* * * * * * * *
08H	PRINC1	Contents of FSR1 to address data memory value of FSR0 pre-incremented								N/A	N/A	* * * * * * * *
09H	PLUSW1	Contents of FSR1 to address data memory value of FSR0 offset by W								N/A	N/A	* * * * * * * *
0FH	FSR0H							FSR0[9]	FSR0[8]	xx	.... ..uu	-,-,-,- -,-,*,*
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	* * * * * * * *
11H	FSR1H							FSR1[9]	FSR1[8]	xx	.... ..uu	-,-,-,- -,-,*,*
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	* * * * * * * *
16H	TOSH				TOS[12]	TOS[11]	TOS[10]	TOS[9]	TOS[8]	...0 0000	...0 0000	-,-,-,* * * * *
17H	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								0000 0000	0000 0000	* * * * * * * *
18H	STKPTR	STKFL	STKUN	STKOV		STKPRT[3:0]				000. 0000	000. 0000	r,rw0,rw0,- r,r,r,r
1AH	PCLATH				PC[12]	PC[11]	PC[10]	PC[9]	PC[8]	...0 0000	...0 0000	-,-,-,* * * * *
1BH	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	* * * * * * * *
1DH	TBLPTRH				TBLPTR[12]	TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]	...0 0000	...0 0000	-,-,-,* * * * *
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								0000 0000	0000 0000	* * * * * * * *
1FH	TBLDH	Program Memory Table Latch High Byte								0000 0000	0000 0000	* * * * * * * *
20H	TBLDL	Program Memory Table Latch Low Byte								0000 0000	0000 0000	* * * * * * * *
21H	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
22H	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
23H	INTE1	GIE	ADCIE	TMCIE	TMBIE	TMAIE	WDTIE	E1IE	E0IE	0000 0000	0000 0000	* * * * * * * *
24H	INTE2	TXIE	RCIE			CPOIE	SSPIE	CCP1IE	CCP0IE	00.. 0000	00.. 0000	* *,-,- * * * *
26H	INTF1		ADCIF	TMCIF	TMBIF	TMAIF	WDTIF	E1IF	E0IF	.000 0000	.000 0000	-,* * * * * * *
27H	INTF2	TXIF	RCIF			CPOIF	SSPIF	CCP1IF	CCP0IF	00.. 0000	00.. 0000	* *,-,- * * * *
29H	WREG	Working Register								xxxx xxxx	uuuu uuuu	* * * * * * * *
2AH	BSRCN							BSR[1]	BSR[0]	00	00	-,-,-,- -,-,*,*
2BH	STATUS				C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,-,* * * * *
2CH	Pstaus	PD	TO	IDL	BOR		SKERR			000d .0..	uduu .d..	rw0,rw0,rw0,rw0 -,rw0,-,-
2DH	LVDCN		LVDFG	LVD	LVDON	VLDX[3:0]				.000 0000	.000 uuuu	-,*,r,r * * * *
30H	PWRCN	ENVDDA	VDDAX[1:0]		ENACM					0000	0000	*,*,*,* -,-,-,-
31H	MCKCN1	ADCS[2:0]			ADCCK	XTHSP	XTSP	ENXT	ENHAO	0000 0001	0000 0001	* * * * * * * *
32H	MCKCN2			LSCK	HSCK	HSS[1:0]		CPUCK[1:0]		..00 0000	..00 0000	-,-,* * * * * *
33H	MCKCN3					PERCK	BZS[2:0]			 0000	 0000	-,-,-,- *,*,*,*
34H	CPACN1	ENCPA	CPIST	CPIX	CPIH[1:0]		CPIL[2:0]			0000 0000	0000 0000	* * * * * * * *
35H	CPACN2		CPOX	CPOFR	CS1	CPAT	CPVCS[1:0]			.000 000.	.000 000.	-,* * * r,* * *
36H	CPACN3				CS2	CPVRX[3:0]				...0 0000	...0 0000	-,-,-,* * *,*,*
37H	OPCN1	ENOP	OPM[1:0]		OPP[1:0]		OPN[2:0]			0000 0000	0000 0000	* * * * * * * *
39H	ADCRH	ADC conversion memory HighByte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3AH	ADCRM	ADC conversion memory Middle Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3BH	ADCRL	ADC conversion memory Low Byte								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
3CH	ADCCN1	ENADC	ENHIGN	ENCHP	PGAGN[1:0]		ADGN[2:0]			0000 0000	0000 0000	* * * * * * * *
3DH	ADCCN2			INBUF	VRBUF	VREGN	DCSET[2:0]			..00 0000	..00 0000	-,-,* * * * * *
3EH	ADCCN3	OSR[2:0]								000.	000.	* * *,- -,-,-,-
3FH	AINET1	INH[2:0]			INL[2:0]			INIS	OPIS	0000 0000	0000 0000	* * * * * * * *
40H	AINET2		VRH[1:0]		INX[1:0]		VRL[1:0]			.000 000.	.000 000.	-,* * * * * *,-
41H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDTS[2:0]			0000 0000	0000 0000	*,*,*,* w1,*,* *
42H	TMAR	TimerA data register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
43H	TMBCN	ENTMB	TMBCK	TMBS[1:0]		TMBSYC	TMBR2R			0000 00..	0000 00..	* * * * * *,-,-
44H	TMBRH	TimerB High Byte data register								xxxx xxxx	uuuu uuuu	* * * * * * * *
45H	TMBRL	TimerB Low Byte data register								xxxx xxxx	uuuu uuuu	* * * * * * * *
46H	TMCCN	ENTMC	TMCCK[1:0]		TMCS1[2:0]			TMCS0[1:0]		0000 0000	0000 0000	* * * * * * * *
47H	PRC	TimerC programmable register								1111 1111	1111 1111	* * * * * * * *
48H	TMCR	TimerC register								0000 0000	0000 0000	r,r,r,r r,r,r,r
49H	CCPCN	CCP1M[3:0]				CCP0M[3:0]				0000 0000	0000 0000	* * * * * * * *
4AH	CCP0RH	CCP0 High Byte data register								xxxx xxxx	uuuu uuuu	* * * * * * * *
4BH	CCP0RL	CCP0 Low Byte data register								xxxx xxxx	uuuu uuuu	* * * * * * * *
4CH	CCP1RH	CCP1 High Byte data register								xxxx xxxx	uuuu uuuu	* * * * * * * *
4DH	CCP1RL	CCP1 Low Byte data register								xxxx xxxx	uuuu uuuu	* * * * * * * *
4EH	PASC	PASF		PASCF[1:0]						0.00	0.00	*,-,* * -,-,-,-
4FH	PWMCN	ENPWM	ENPFD	PWMRL[1:0]						0000	0000	*,*,*,* -,-,-,-
50H	PDBD	ENPRS	DBDC[6:0]							0000 0000	0000 0000	* * * * * * * *
51H	PWMR	PWM MSB Byte register								xxxx xxxx	uuuu uuuu	* * * * * * * *

Table 5-1(a) HY11P24 Register List

"-"no use,"*"read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"omly write 1												
"."unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition												
Address	**File Name**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**A-RESET**	**i-RESET**	**R/W**
5EH	SSPCON1	SSPEN	CKP	CKE	SMP	—	—	SSPM<1:0>		0000 ..00	uuuu ..uu	*,*,*,*-,-,*,*
60H	SSPSTA	SSPBUY	SSPOV	Reserve for IIC					BF	00.. ...0	00.. ...0	r,r,-,- -,-,-,r
61H	SSPBUF	SSP Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
63H	URCON	ENSP	ENTX	TX9	TX9D	PARITY			WUE	0000 0..0	0000 0..0	*,*,*,*,-,-,*
64H	URSTA		RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	.000 0110	.000 0110	-,r,r,r r,r,r,rw0
65H	BAUDCON					ENCR	RC9	ENADD	ENABD	 0000	 0000	-,-,-,- *,*,*,*
66H	BRGRH	Baud Rate Generator Register High Byte								...x xxxx	...u uuuu	-,-,-,*,*,*,*,*
67H	BRGRL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
68H	TXREG	UART Transmit Register								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
69H	RCREG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
6AH	PT4	PT4.7	PT4.6	PT4.5	PT4.4	PT4.3	PT4.2	PT4.1	PT4.0	xxxx xxxx	uuuu uuuu	r,r,r,r r,r,r,r
6BH	PT4DA	DA4.7	DA4.6	DA4.5	DA4.4	DA4.3	DA4.2	DA4.1	DA4.0	1111 1111	1111 1111	*,*,*,*,*,*,*,*
6CH	PT4PU	PU4.7	PU4.6	PU4.5	PU4.4	PU4.3	PU4.2	PU4.1	PU4.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
6DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	*,*,*,* r,r,r,r
6EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4					0000	0000	*,*,*,* -,-,-,-
6FH	PT1DA						DA1.2	DA1.1	DA1.0	.... .000	.... .000	-,-,-,- -,*,*,*
70H	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
71H	PT1M1					INTEG1[1:0]		INTEG0[1:0]		 0000	 0000	-,-,-,- *,*,*,*
72H	PT1M2		PM1.7[0]		PM1.6[0]		PM1.5[0]		PM1.4[0]	.0.0 .0.0	.0.0 .0.0	-,*,-,* -,*,-,*
74H	PT2	PT2.7	PT2.6	PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
75H	TRISC2	TC2.7	TC2.6	TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
76H	PT2DA	DA2.7	DA2.6	DA2.5	DA2.4	DA2.3	DA2.2			0000 00..	0000 00..	*,*,*,*,*,-,-
77H	PT2PU	PU2.7	PU2.6	PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
78H	PT2M1		PM2.3[0]	PM2.2[1]	PM2.2[0]					.000	.000	-,*,*,* -,-,-,-
79H	PT2M2	PWMTR[1:0]			PM2.6[0]	PM2.5[1]	PM2.5[0]	PM2.4[1]	PM2.4[0]	00.0 0000	00.0 0000	*,*,-,*,*,*,*,*
7AH	PT3	PT3.7	PT3.6	PT3.5	PT3.4	PT3.3	PT3.2	PT3.1	PT3.0	xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
7BH	TRISC3	TC3.7	TC3.6	TC3.5	TC3.4	TC3.3	TC3.2	TC3.1	TC3.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
7DH	PT3PU	PU3.7	PU3.6	PU3.5	PU3.4	PU3.3	PU3.2	PU3.1	PU3.0	0000 0000	0000 0000	*,*,*,*,*,*,*,*
80H ~ FFH		GENERAL PURPOSE REGISTER @ 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
100H~17FH		GENERAL PURPOSE REGISTER @ 128Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*
192H	PT5			PT5.5	PT5.4	PT5.3	PT5.2	PT5.1	PT5.0	..xx xxxx	..xx uuuu	-,-,r,r r,r,r,r
193H	PT5DA					DA5.3	DA5.2	DA5.1	DA5.0	 1111	 1111	-,-,*,*,*,*,*,*
194H	PT5PU			PU5.5	PU5.4	PU5.3	PU5.2	PU5.1	PU5.0	..00 0000	..00 0000	-,-,*,*,*,*,*,*
200H ~ 2FFH		GENERAL PURPOSE REGISTER @ 256Byte								xxxx xxxx	uuuu uuuu	*,*,*,*,*,*,*,*

Table 5-1(b) HY11P24 Register List (continued)

6. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . −0.2 V to 4.0 V

Voltage applied to any pin . . . . −0.2 V to V_{DD} + 0.3 V

Voltage applied to RST/VPP pin . . . . −0.2 V to 6.9 V

Voltage applied to TST/PT1.3 pin . . . . −0.2 V to V_{DD} + 1 V

Diode current at any device terminal . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . −55℃ to 150℃

(programmed device) . . . . −40℃ to 85℃

Total power dissipation. 0.5w

Maximum output current sink by any PORT1 to PORT3 I/O pin. 25mA

6.1 Recommended Operating Conditions

T_A = -40℃ ~ 85℃,unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage		All digital peripherals and CPU		2.2		3.6	V
			Analog peripherals		2.4		3.6	
V_{SS}	Supply Voltage				0		0	
XT	External Oscillator Frequency	Watch crystal	V_{DD} = 2.2V, ENXT[0]=1	XTSP[0]=0, XTHSP[0]=0		32.768K		Hz
		Ceramic resonator		XTSP[0]=1, XTHSP[0]=0	450K		8M	
		Crystal		XTSP[0]=1, XTHSP[0]=0	1M		8M	

6.2 Internal RC Oscillator

T_A = 25°C,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1	1.8	2.0	2.2	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	22	28	35	KHz

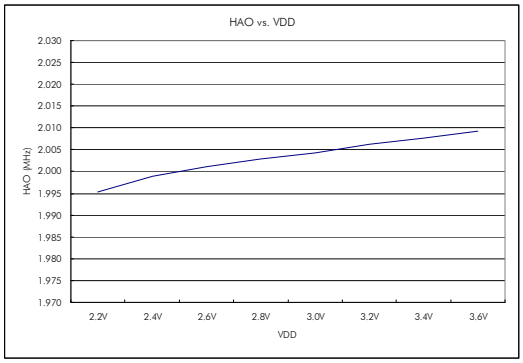

Figure 6.2-1 HAO vs. VDD

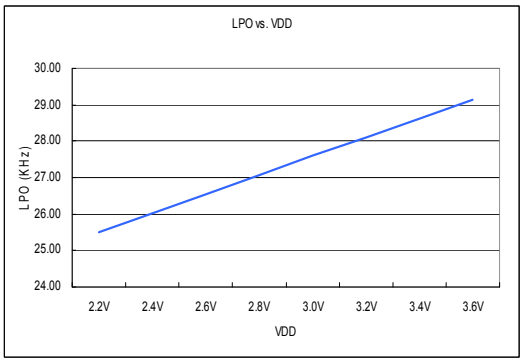

Figure 6.2-2 LPO vs. VDD

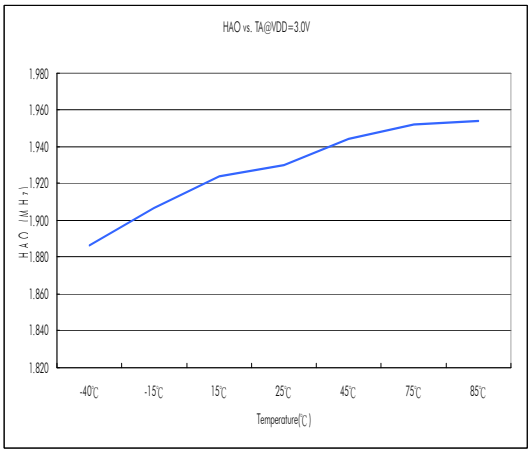

Figure 6.2-3 HAO vs. Temperature

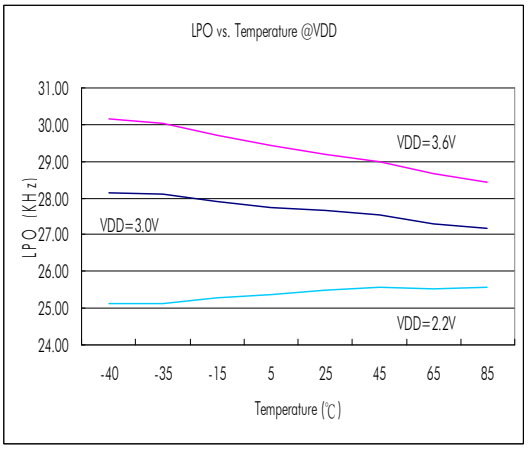

Figure 6.2-4 LPO vs. Temperature

6.3 Supply Current into VDD Excluding Peripherals Current

T_A = 25°C,V_{DD} = 3.0V,OSC_LPO = 28KHz, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = 8MHz, OSC_HAO = off, CPU_CK = 8MHz		1.34	2	mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		0.36	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		0.2	0.3	mA
I_{LP1}	Low Power 1	OSC_CY = 32768Hz, OSC_HAO = off, CPU_CK = 16384Hz		7	12	uA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.65	3	uA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_CY：External Oscillator frequency.

OSC_HAO：Internal High Accuracy Oscillator frequency.

CPU_CK：CPU core work frequency.

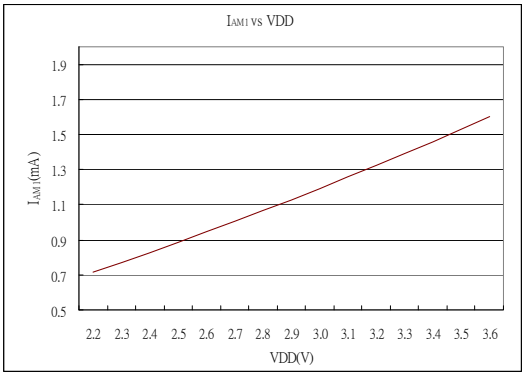

Figure 6.3-1 I_{AM1} vs. VDD

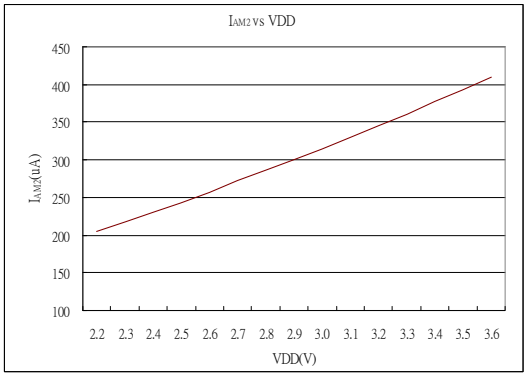

Figure 6.3-2 I_{AM2} vs. VDD

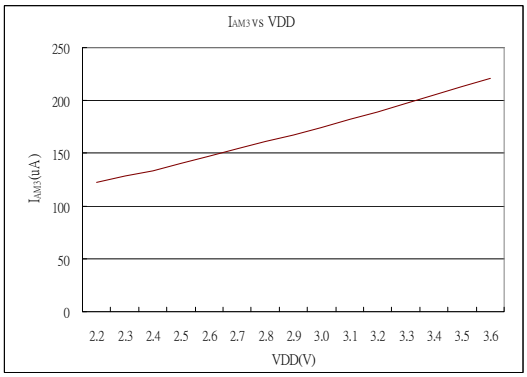

Figure 6.3-3 I_{AM3} vs. VDD

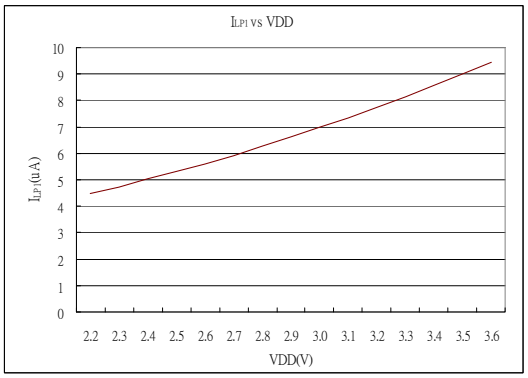

Figure 6.3-4 I_{LP1} vs. VDD

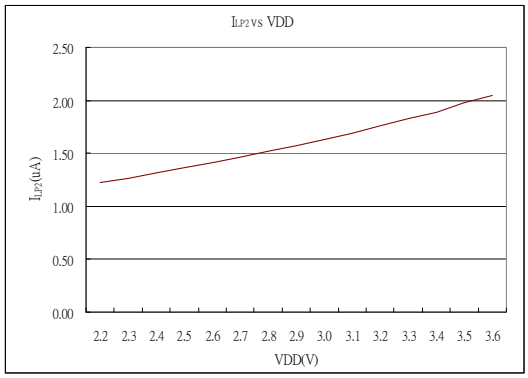

Figure 6.3-5 I_{LP2} vs. VDD

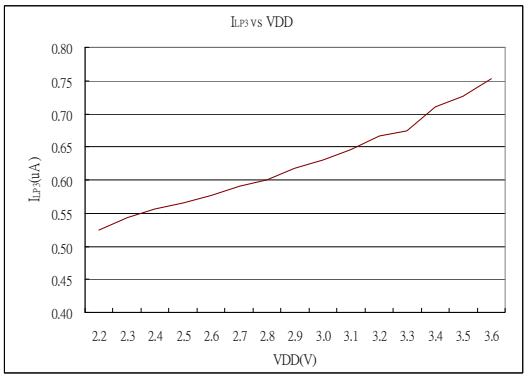

Figure 6.3-6 I_{LP3} vs. VDD

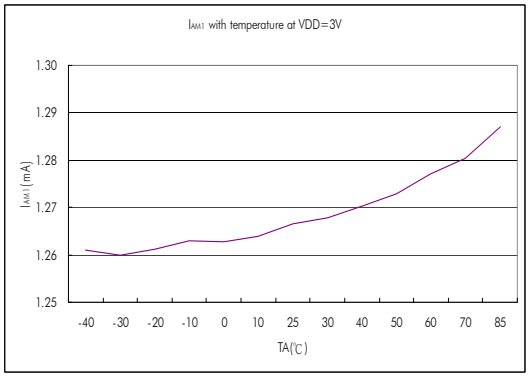

Figure 6.3-7 I_{AM1} vs. Temperature

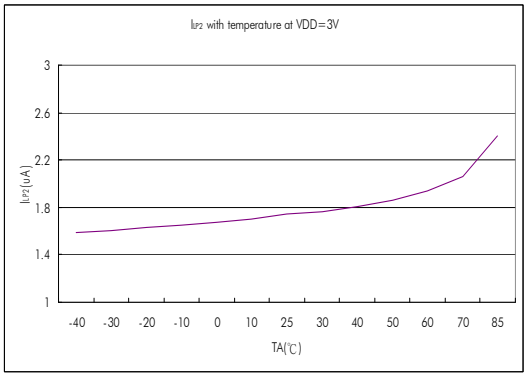

Figure 6.3-8 I_{LP2} vs. Temperature

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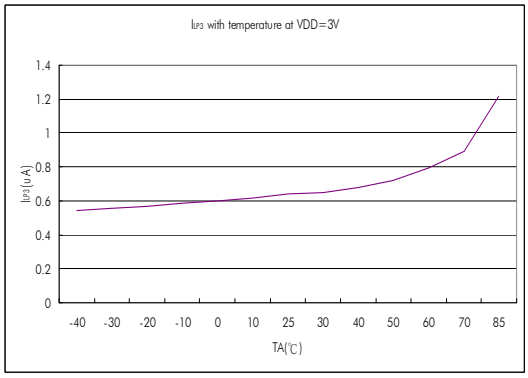


Figure 6.3-9 I_{LP3} vs. Temperature

6.4 Port 1~5

T_A = 25℃,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis(VIH - VIL)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		kΩ
Output voltage and current and frequency						
V_{OH}	High-level output voltage	I_{OH}=10mA	V_{DD} -0.3			V
V_{OL}	Low-level output voltage	I_{OL}=-10mA			VSS +0.3	

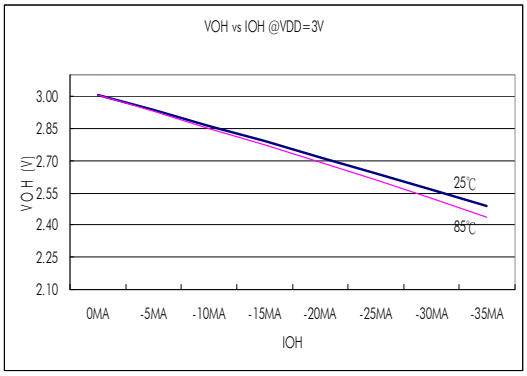


Figure 6.4-1 V_{OH} vs. I_{OH} @VDD=3.0V

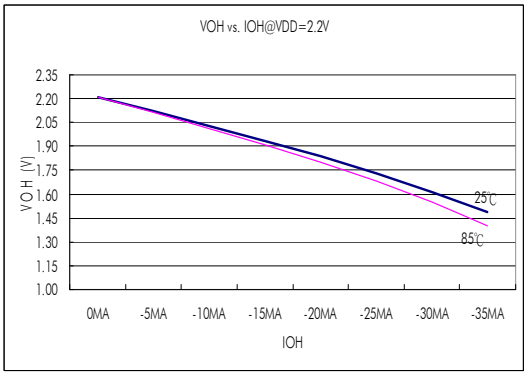


Figure 6.4-2 V_{OH} vs. I_{OH} @VDD=2.2V

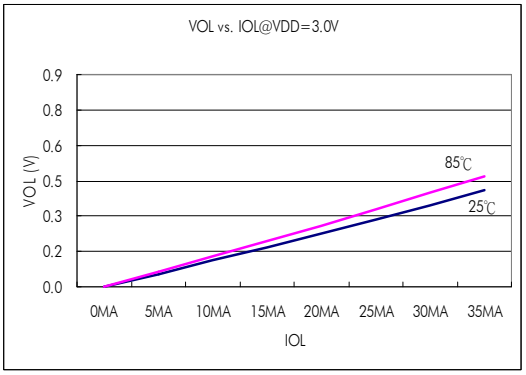


Figure 6.4-3 V_{OL} vs. I_{OL}@VDD=3.0V

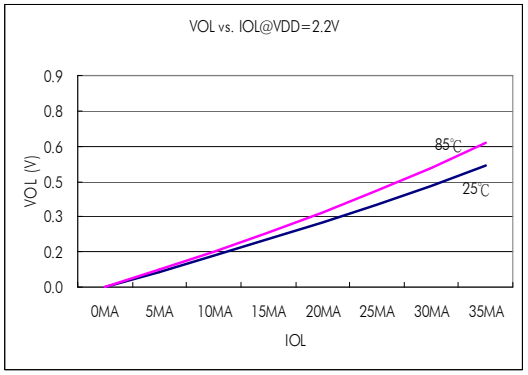


Figure 6.4-4 V_{OL} vs. I_{OL}@VDD=2.2V

6.5 Reset (Brownout, External RST Pin, Low Voltage Detect)

T_A = 25°C,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L➔H),V_{LVR}		1.6	1.85	2.1	V
	Hysteresis, $V_{HYS-LVR}$			70		mV
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us
	Input Voltage to accepted reset internally		0.9			V
	Hysteresis, $V_{HYS-RST}$			0.8		V
LVD	Operation current, I_{LVD}			10	15	uA
	External input voltage to compare reference voltage			1.2		V
	Compare reference voltage temperature drift	T_A = -40°C ~ 85 °C		100		ppm/°C
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=1110b			3.3		V
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=1101b			3.2		
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=1100b			3.1		
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=1011b			3.0		
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=1010b			2.9		
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=1001b			2.8		
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=1000b			2.7		
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=0111b			2.6		
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=0110b			2.5		
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=0101b			2.4		
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=0100b			2.3		
	Detect V_{DD} voltage rang by user option, V_{LVD} VLDx[3:0]=0011b			2.2		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0010b			2.1		
	Detect V_{DD} voltage rang by user option, V_{SVS} VLDx[3:0]=0001b			2.0		

BOR：Brownout Reset

LVR：Low Voltage Reset of BOR

LVD：Low Voltage Detect

RST：External Reset pin

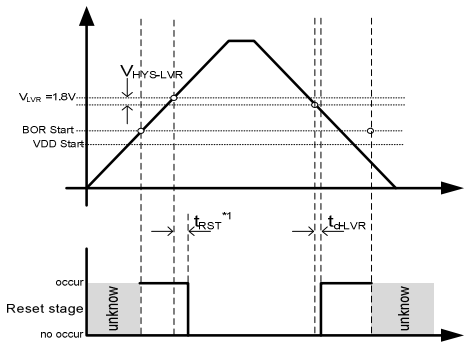


Figure 6.5-1 BOR Reset Diagram

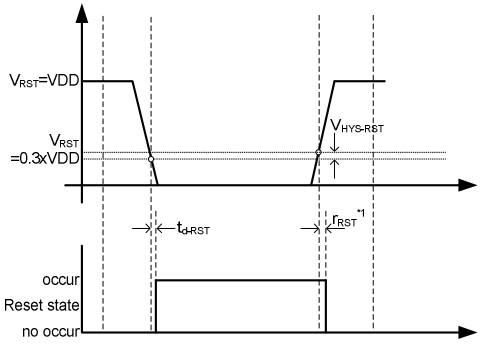


Figure 6.5-2 RST Reset Diagram

*1 r_{RST}：Please see BOR Introduce of HY11Pxx series User's Guide (UG-HY11S14-Vxx).

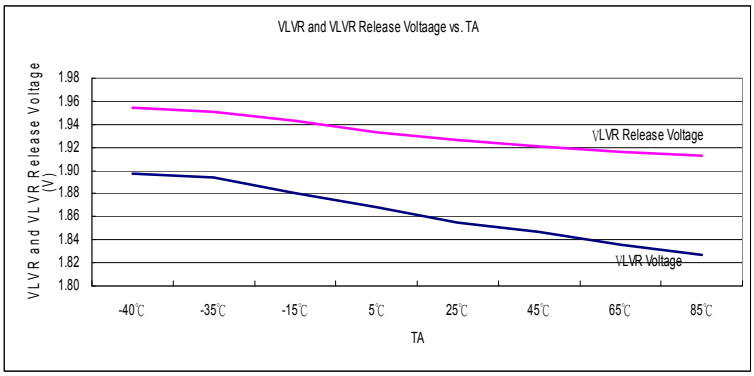


Figure 6.5-3 LVR vs. Temperature

6.6 Power System

T_A = 25°C,V_{DD} = 3.0V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	I_L = 0mA	VDDAX[1:0]=00b		22		uA
	Select VDDA output voltage	I_L = 0.1mA, VDD≧VDDA+0.2V	VDDAX[1:0]=00b		3.3		V
			VDDAX[1:0]=01b		2.9		V
			VDDAX[1:0]=10b		2.6		V
			VDDAX[1:0]=11b		2.4		V
	Dropout voltage	I_L = 10mA	VDDAX[1:0]=00b		135		mV
			VDDAX[1:0]=01b		150		mV
			VDDAX[1:0]=10b		165		mV
			VDDAX[1:0]=11b		180		mV
	Temperature drift	VDDAX[1:0]=11b	T_A=-40°C~85°C		50		ppm/°C
	V_{DD} Voltage drift	I_L = 0.1mA	V_{DD}=2.5V~3.6V		±0.2		%/V
ACM	ACM operation current, I_{ACM}	I_L = 0mA			20		uA
	Output voltage ,V_{ACM}	ENACM[0]=1, *1	I_L = 0uA		1.0		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Output voltage ,V_{ACM}	ENACM[0]=1, *2	I_L = 0uA		1.2		V
	Output voltage with Load		I_L = ±200uA	0.98		1.02	V_{ACM}
	Temperature drift	ENACM[0]=1,	T_A=-40°C~85°C		50		ppm/°C
	VDDA Voltage drift	I_L = 10uA			100		uV/V

VDDA：Adjust Voltage Regulator

ACM：Analog Common Mode Voltage

*1: V_{ACM} = 1.0V is just for VDDAX[1:0]=1xb mode. (at A/D differential voltage reference < 1.4V)

*2: V_{ACM} = 1.2V is just for VDDAX[1:0]=0xb mode. (at A/D differential voltage reference > 1.4V)

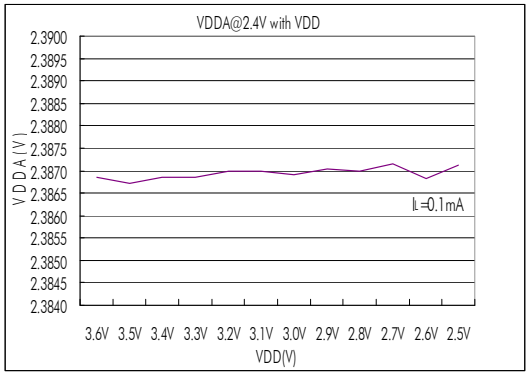


Figure 6.6-1 VDDA I_L=0.1mA vs. VDD

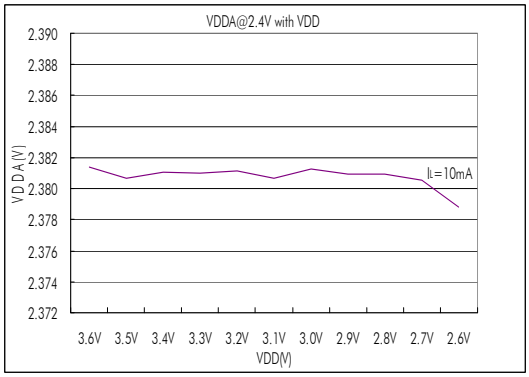


Figure 6.6-2 VDDA I_L=10mA vs. VDD

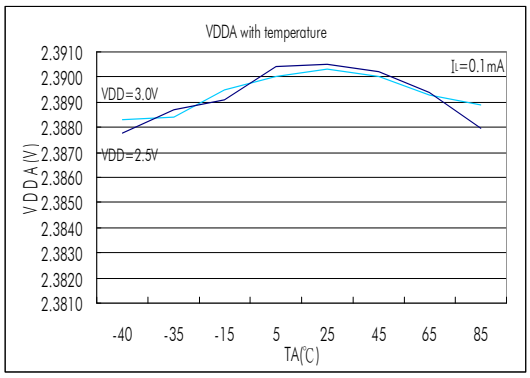


Figure 6.6-3 VDDA IL=0.1mA vs. Temperature

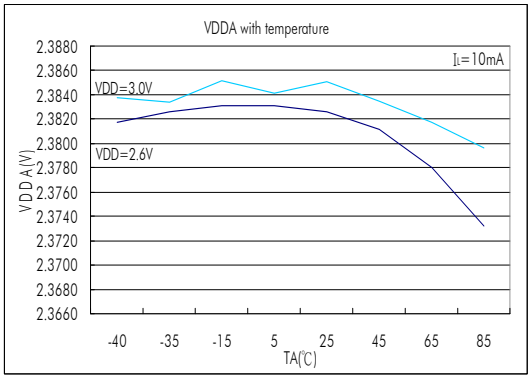


Figure 6.6-4 VDDA IL=10mA vs. Temperature

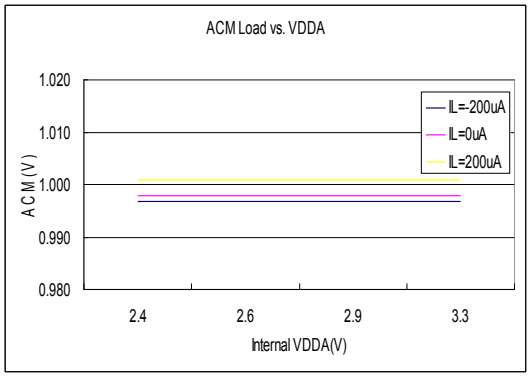


Figure 6.6-5 ACM Load vs. VDDA (a)

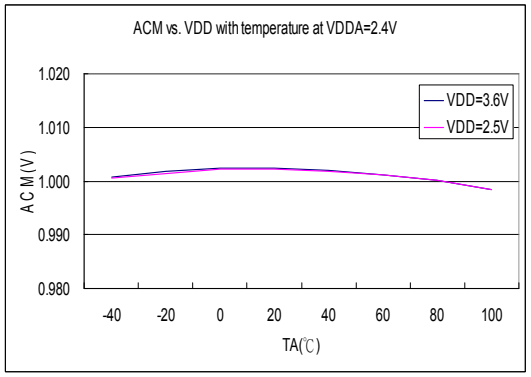


Figure 6.6-6 ACM vs. Temperature (a)

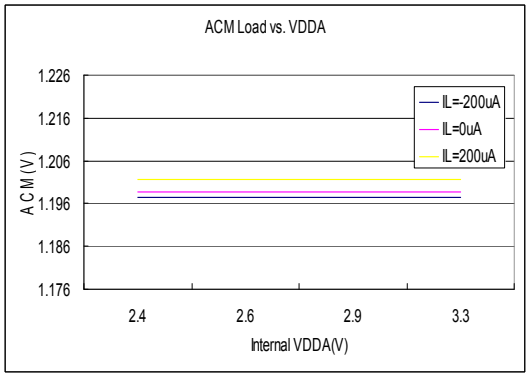


Figure 6.6-5 ACM Load vs. VDDA (b)

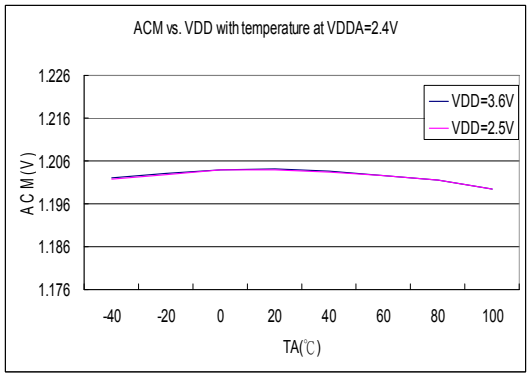


Figure 6.6-6 ACM vs. Temperature (b)

6.7 Low Noise OPAMP

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{LNOP}	Supply voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{LNOP}	Operation supply current		OPM[1:0]=xxb		200		uA
V_{OS-OP}	Input offset voltage without chopper.		OPM[1:0]=1xb	-2		2	mV
	Input offset voltage with chopper		OPM[1:0]=0xb		20		uV
	Input offset voltage temperature drift.	OPM[1:0]=00b	T_A=-40℃~85℃		0.1		uV/℃
		OPM[1:0]=10			2		
V_{OLR}	Unit gain load regulation	V_O=1.2V, VDDA=2.4V	I_L=+1mA		0.1		%V_O
			I_L=-1mA				
CMVR	Common-mode voltage input range		OPM[1:0]=xxb	0.1		VDDA-1.1	V
CMRR	Common-mode rejection ratio		OPM[1:0]=xxb		90		dB

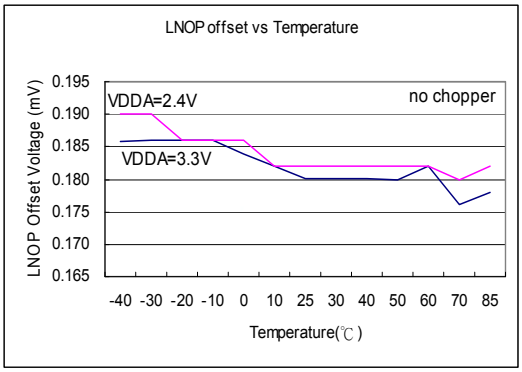


Figure 6.7-1 LNOP Offset Temperature

6.8 SD18, Power Supply and Recommended Operating Conditions

T_A = 25°C,V_{DD} = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
f_{SD18}	Modulator sample frequency, ADC_CK			25	250	300	KHz
	Over Sample Ratio, OSR			256		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1 INBUF[0]=1,VRBUF[0]=0	GAIN =4, ADC_CK=250KHz		168		uA
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=1			150		
		ENADC[0]=1 INBUF[0]=0,VRBUF[0]=0			120		

6.8.1 PGA, Power Supply and Recommended Operating Conditions

T_A = 25°C,V_{DD} = 3.0V, VDDA=2.4V, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{PGA}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		3.6	V
I_{PGA}	Operation supply current	PGAGN[1:0]=<01>or<1x>			320		uA
G_{PGA}	Gain temperature drift	T_A = -40°C~ 85°C	GAIN=128		5		ppm/°C

6.8.2 SD18, Performance II (fSD18=250KHz)

T_A = 25°C,V_{DD} = 3.0V, VDDA=2.9V,V_{VR}=1.0V,GAIN=1 without PGA, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	VDDA=2.4V,V_{VR}=1.0V,ΔSI=±200mV			±0.003	±0.01	%FSR
		VDDA=2.4V,V_{VR}=1.0V,ΔSI=±450mV					
	No Missing Codes[3]	ADC_CK=250KHz,OSR[2:0]=010b		23			Bits
G_{SD18}	Temperature drift Gain 1~x16 (INBUF[0]=0b) Gain 1~x4 (INBUF[0]=1b)	INBUF[0]=0b,VRBUF[0]=0b	T_A = -40°C~ 85°C		2		ppm/°C
		INBUF[0]=1b,VRBUF[0]=0b					
		INBUF[0]=0b,VRBUF[0]=1b					
		INBUF[0]=1b,VRBUF[0]=1b					
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper and Buffer(INBUF,VRBUF) without PGA	ΔAI=0V ΔVR=0.9V DCSET[2:0]=<000> * ΔAI is external short	Gain=2			1	%FSR
	Offset error of Full Scale Rang input voltage range with Chopper without PGA and Buffer(INBUF,VRBUF)		Gain=2			1	

	Offset temperature drift with chopper without PGA and Buffer (INBUF,VRBUF).		GAIN=1	2	uV/℃
			GAIN=2	1	
			GAIN=4	0.5	
			GAIN=16	0.15	
	Offset temperature drift with chopper and Buffer (INBUF,VRBUF) without PGA.		GAIN=1	2	
			GAIN=2	1	
			GAIN=4	0.5	
	Offset temperature drift with chopper without Buffer (INBUF,VRBUF).		GAIN=128	0.02	
CM_{SD18}	Common-mode rejection	V_{CM}=0.7V to 1.7V, V_{VR}=1.0V,without PGA	V_{SI}=0V, GAIN=1	90	dB
		V_{CM}=0.7V to 1.7V, V_{VR}=1.0V, without PGA	V_{SI}=0V, GAIN=16	75	
PSRR	DC power supply rejection	VDDA=3.0V, Δ VDDA=± 100mV,V_{VR}=1.0V, V_{SI}=1.2V,V_{SI-}=1.2V,	GAIN=1 PGA=off	75	dB
			GAIN=16 PGA=8		

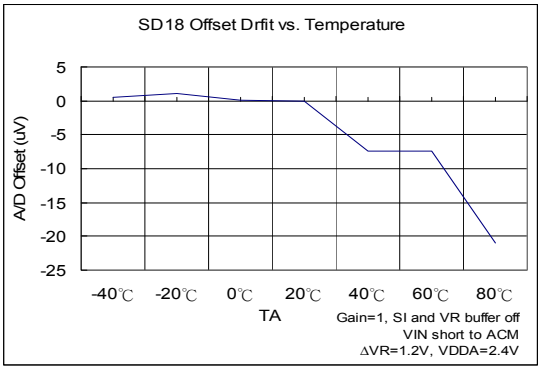


Figure 6.8-1(a) SD18 Offset Temperature Drift

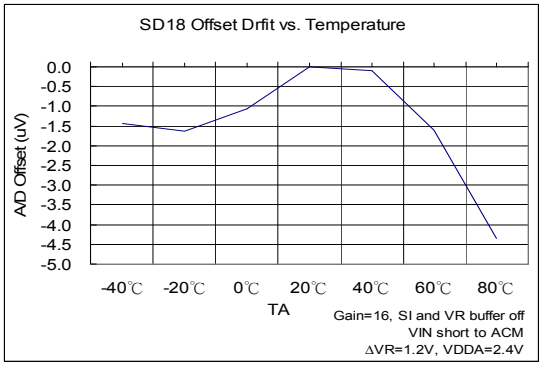


Figure 6.8-1(b) SD18 Offset Temperature Drift

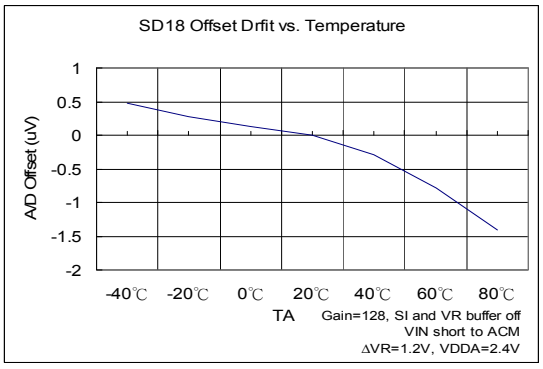


Figure 6.8-1(c) SD18 Offset Temperature Drift

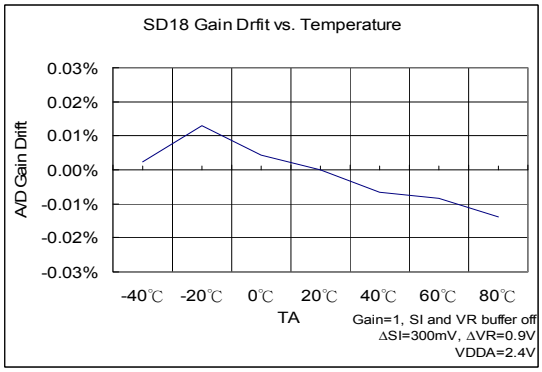


Figure 6.8-2(a) SD18 Gain Drift with Temperature

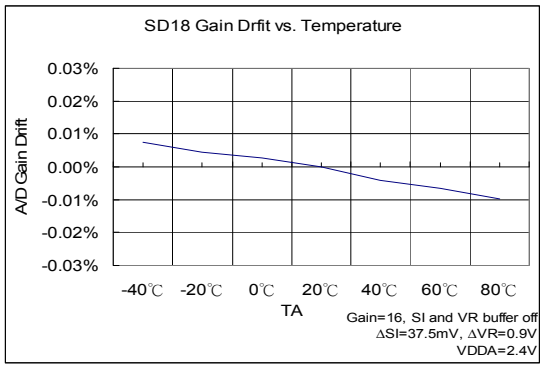


Figure 6.8-2(b) SD18 Gain Drift with Temperature

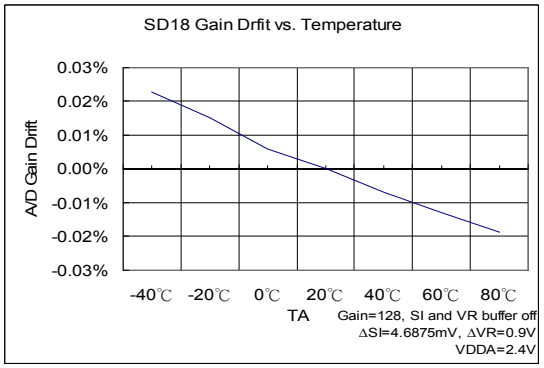


Figure 6.8-2(c) SD18 Gain Drift with Temperature

6.8.3 SD18, Temperature Sensor

T_A = 25℃,V_{DD} = 3.0V, VDDA=3.3V, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC_S	Sensor temperature drift			178		uV/℃
KT	Absolute Temperature Scale 0°K	INBUF[0]=1		-289		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

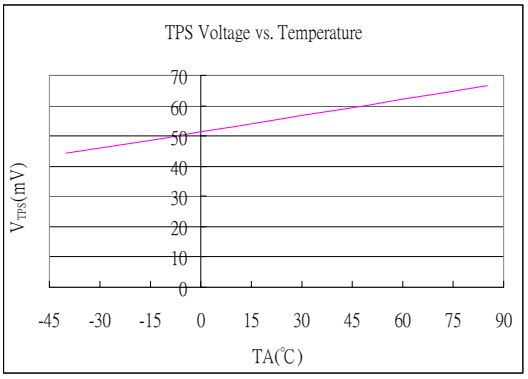


Figure 6.8-3 TPS Output Voltage vs. Temperature Drift

6.8.4 SD18 Noise Performance

T_A = 25℃,V_{DD} = 3.0V, VDDA=2.4V,unless otherwise noted

HY11P24 provides important input noise specification that aims at SD18. Table 6.8-4(a) and Table 6.8-4(b) lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF (1)	OSR					256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN								
±2400	0.25	=	1	×	0.25	16.3	17.4	17.9	18.5	19.0	19.5	20.0	20.4
±2160	0.5	=	1	×	0.5	16.3	17.3	17.9	18.4	18.9	19.4	19.8	20.2
±1080	1	=	1	×	1	16.2	17.2	17.8	18.3	18.8	19.3	19.7	20.1
±540	2	=	1	×	2	16.1	17.1	17.6	18.2	18.7	19.2	19.6	20.0
±270	4	=	1	×	4	16.0	16.9	17.5	18.0	18.5	18.9	19.4	19.8
±135	8	=	1	×	8	15.9	16.6	17.2	17.7	18.2	18.7	19.2	19.6
±68	16	=	1	×	16	15.6	16.3	16.8	17.3	17.7	18.3	18.8	19.3
±34	32	=	2	×	16	14.8	15.3	15.9	16.4	16.9	17.4	17.8	18.3
±17	64	=	4	×	16	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0
±8	128	=	8	×	16	14.0	14.6	15.1	15.6	16.0	16.6	17.0	17.5

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 6.8-4(a) SD18 ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=250Khz, VDDA=2.4V, VREF=1.2V													
Max. Vin(mV) =0.9*VREF	OSR					256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					977	488	244	122	61	31	15	8
	Gain	=	PGA	×	ADGN								
±2400	0.25	=	1	×	0.25	121.08	57.40	38.74	26.66	18.39	13.21	9.49	6.98
±2160	0.5	=	1	×	0.5	61.63	29.23	19.21	13.51	9.78	7.02	5.12	3.91
±1080	1	=	1	×	1	32.21	15.70	10.25	7.31	5.19	3.77	2.80	2.13
±540	2	=	1	×	2	16.59	8.54	5.91	4.06	2.86	2.06	1.48	1.12
±270	4	=	1	×	4	9.00	4.84	3.33	2.37	1.67	1.19	0.87	0.65
±135	8	=	1	×	8	5.04	2.97	2.02	1.44	1.01	0.73	0.51	0.39
±68	16	=	1	×	16	3.03	1.84	1.29	0.92	0.70	0.46	0.33	0.24
±34	32	=	2	×	16	2.61	1.81	1.27	0.89	0.62	0.45	0.32	0.23
±17	64	=	4	×	16	1.66	1.13	0.80	0.56	0.41	0.29	0.20	0.14
±8	128	=	8	×	16	1.13	0.77	0.55	0.38	0.28	0.19	0.14	0.10

Table 6.8-4(b) SD18 RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right) \Big/ \ln(2)$$

$$\text{RMS Noise} = \left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024}(\text{ADO}[k] - \text{Average})^2}\right) \Big/ 2^{23}$$

$$\text{Where FSR (Full - Scale Range)} = 2 \times \text{VREF/Gain.}$$

$$\text{Average} = \frac{\sum_{k=1}^{1024}(\text{ADO}[k])}{1024}$$

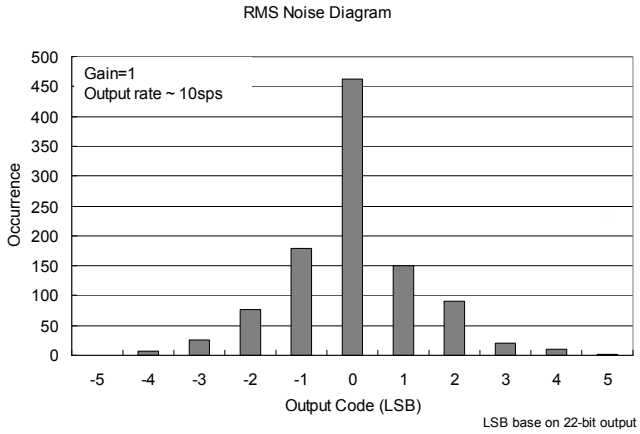


Figure 6.8-4(a) RMS Noise Diagram

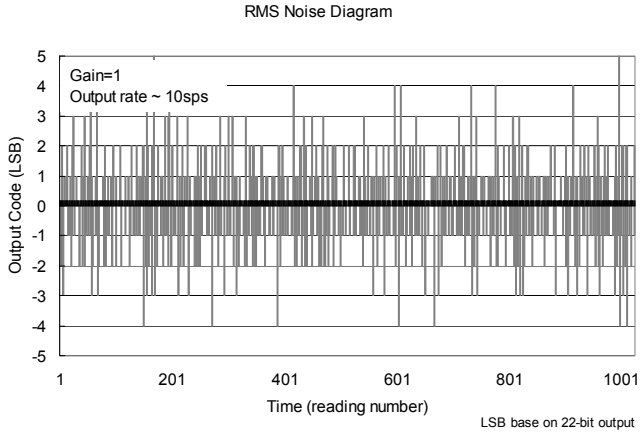


Figure 6.8-4(b) Output Code Diagram

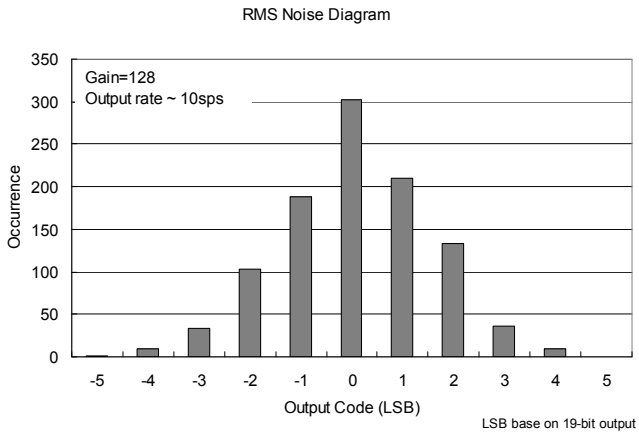


Figure 6.8-4(c) RMS Noise Diagram

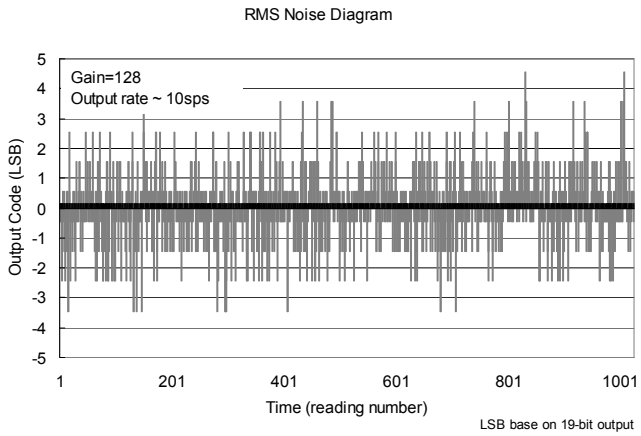


Figure 6.8-4(d) Output Code Diagram

7. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY11P24-D000	Die	-	D	000	000	-	140	Green[4]	-
HY11P24-L044	LQFP	44	L	044	000	Tray	160	Green[4]	MSL-3
HY11P24-L048	LQFP	48	L	048	000	Tray	250	Green[4]	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code** (Blank Code/ Standard/ Customized Programming Code)

Ex: Your customized programming code is 008 and you require die shipment.
The device No. will be HY11P24-D000-008

Ex: You request blank code in die package.
The device No. will be HY11P24-D000

Ex: You request blank code in LQFP 44 package.
The device No. will be HY11P24-L044
And please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 009 and you require products in LQFP48 package.
The device No. will be HY11P24-L048-009.
And please clearly indicate the shipment packing type when placing orders.

[2] **Code:**

"001"~ "999" is standard or customized programming code. Blank code does not have these numbers.

[3] **MSL:**

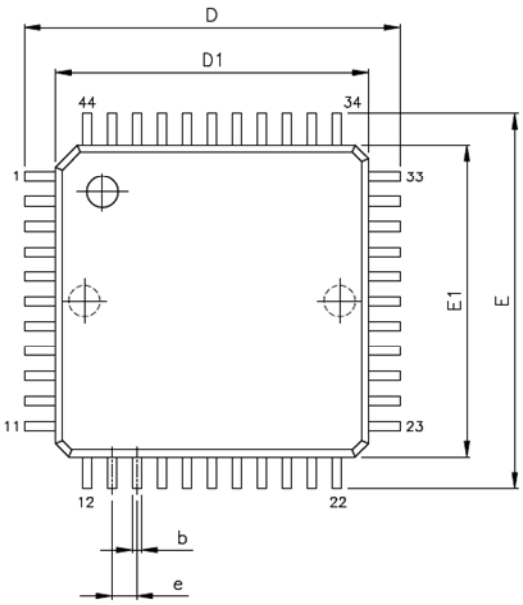
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[4] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%).

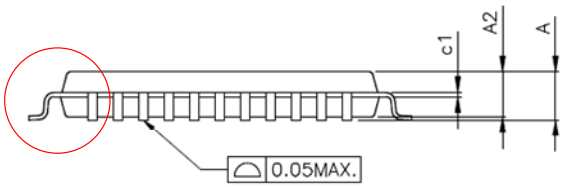
8. Package Information

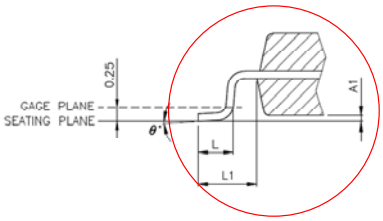
8.1 LQFP44(L044)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
c1	0.09	—	0.16
D		12.00 BSC	
D1		10.00 BSC	
E		12.00 BSC	
E1		10.00 BSC	
e		0.80 BSC	
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1		1.00 REF	
θ°	0°	3.5°	7°





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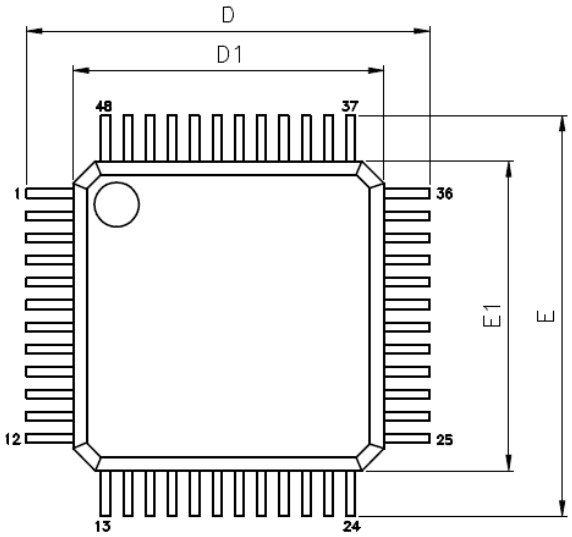
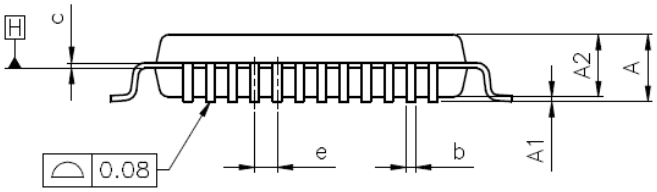
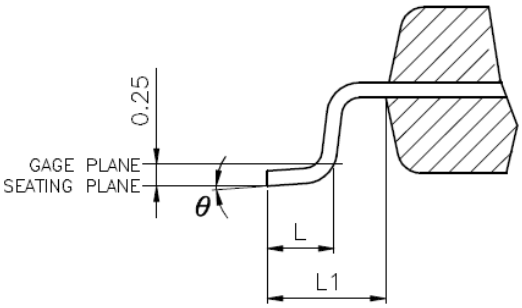
8.2 LQFP48(L048)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°





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9. Revision History

Major differences are stated thereinafter:

Version	Page	Revision Summary
V01	ALL	First edition
V02		With reference to documentation: DS-HY11P24-V02_TC
	4	Features revision
	6~8	Chapter 2.2 LQFP44 Pinout I/O Description revision
	10~11	Chapter 3 Application Circuit revision
	13~14	Chapter 5 Register List revision
	17~28	Chapter 6.3~6.8 revision
V03	4	Features revision
	7	Chapter 2.2 LQFP44 Pinout I/O Description revision
	22~23	Chapter 6.6 Power System revision
V04	4	Revised features content
	5	Add in Note 3 description
	10~11	Revised application circuit, added in RC circuit of RST
	12	Revised Internal Block Diagram
	20	Delete Detect V_{DD} voltage error description
V08	4	Revised features content
	6	Add in chapter 2.2 LQFP48 Pin Diagram
	13	Revised chapter 4.2 Development Tool Related Operating Instruction serial numbers
	14	Add in chapter 4.3 SD18 Network
	17	Chapter 6 Electrical Characteristics Revision
	24	Revise Power System Temperature Drift Spec
	25	The background color of Figure 6.6-5 and Figure 6.6-6 revision
	31~32	Add in chapter 6.8.4 SD18 Noise Performance
	33	Chapter 7 Ordering information revision
	35	Add in package information-Chapter 8.2 LQFP48(L048)
V09	5~6	Magnified the Pin Diagrams
	7	Added in the Pin Name, CPAI7
	11~14	Added in 4.4 LQFP48 Pinout I/O Description
	19	Added in Low Noise OPAMP Network
	20	Added in Enhance Comparator Network