



HY12P65/HY12P66

Datasheet

DMM Specialized IC
Embedded Digital T-RMS

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Attention :

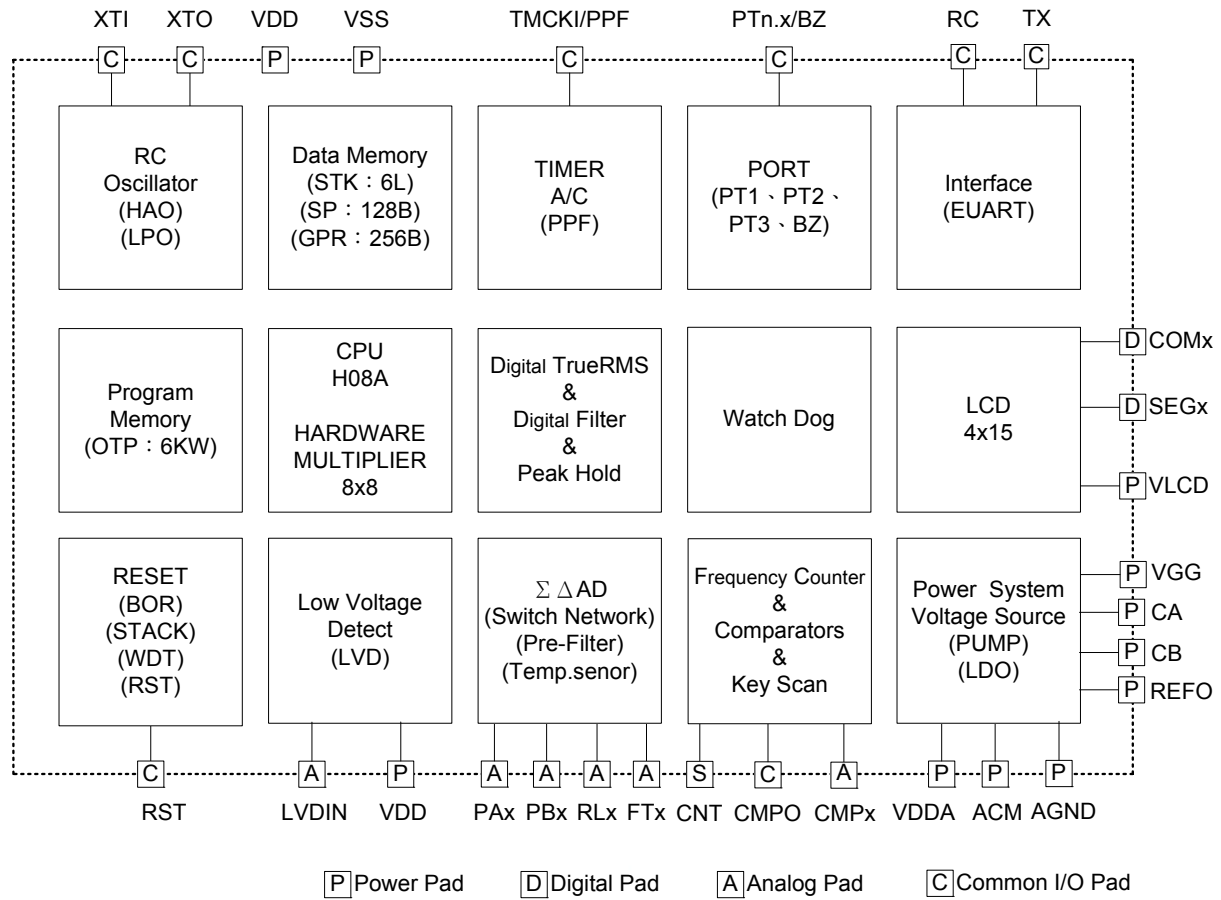
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1. Features

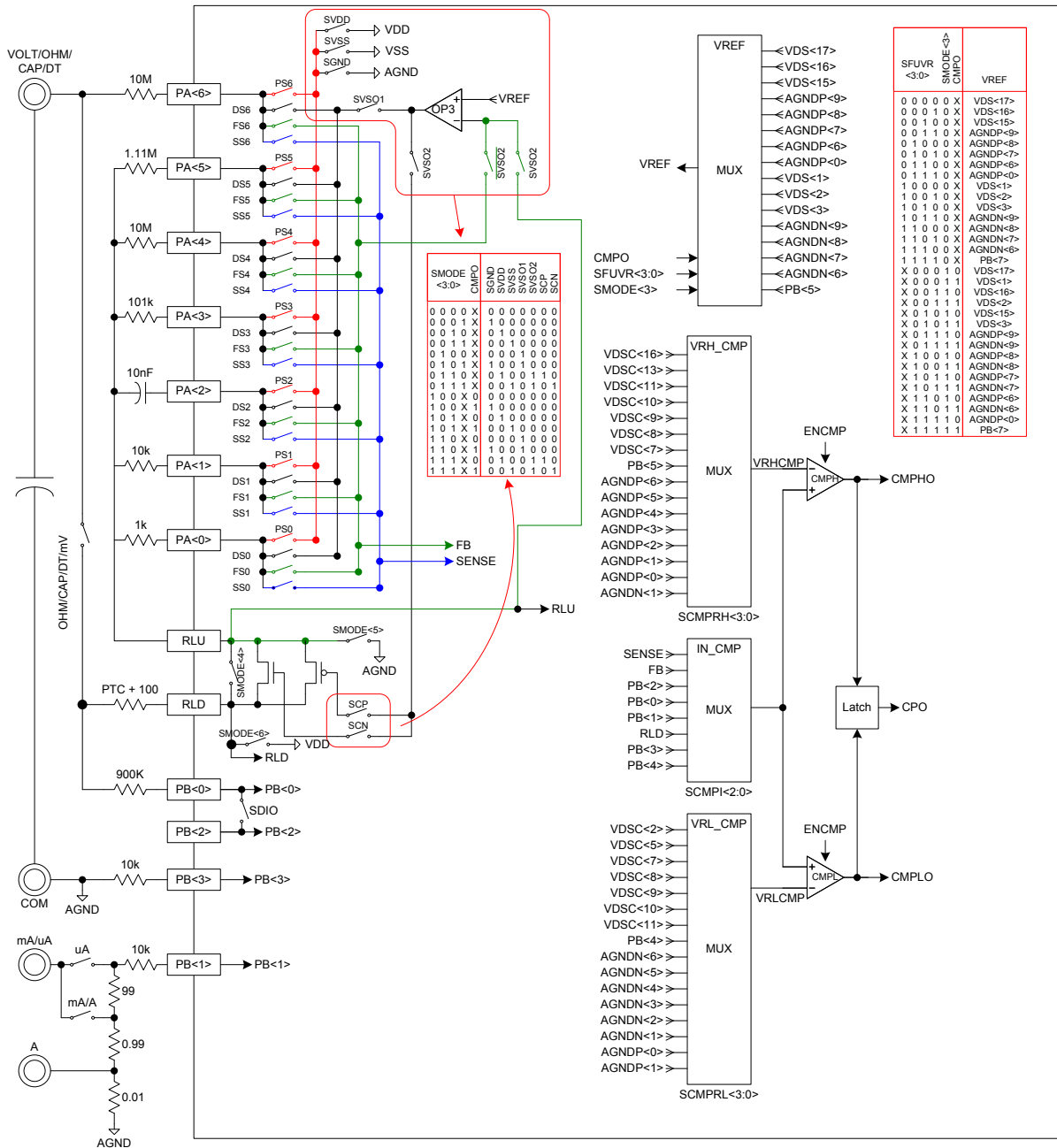
- Operation voltage: 2.4V~3.6V
- 6K Word OTP (One Time Programmable) program memory, 256Byte data memory
- Built-in Brownout and Watch dog timer, preventing CPU from crash
- Built-in high precision RC oscillator and support crystal oscillation circuit
 - Operation mode: 4MHz
 - Idle mode: 32KHz
- Programmable multi-functional network
 - Voltage/resistor/capacitor switch measurement
 - Constant voltage/current output
 - Self calibration components
 - Positive/negative electrode differential
- Multi-functional comparator
 - Equipped with delay and latch function, reducing glitch
 - Programmable comparison voltage configuration
 - Short circuit test, frequency measurement and capacitor charge/discharge frequency measurement
- High resolution $\Sigma\Delta$ ADC
- Zero input/output voltage
- High input impedance (built-in input buffer)
- Built-in absolute temperature sensor
- 1.2V internal analog circuit common-ground voltage source
- LVD low voltage detect function equips with 14-step voltage detect configuration and external input voltage detect function
- Analog voltage source, VDDA can set up 4 types of output voltage, equipping with 10mA regulated voltage source output ability
- 4x15 LCD driver
 - Built-in charge pump regulated circuit, providing 4 LCD bias voltage
 - Static, 1/2, 1/3, 1/4 Duty and 1/3 Bias software selection
- 8-bit Timer A
- 8-bit Timer C module can generate PWM/PFD waveform
- UART module
- Support 6 stack level

Model No.	PA Network	PB Channel	ADC	Program Memory	Data Memory	LCD	I/O	Cap.	T-RMS Bandwidth	Inrush Current	Peak Hold	Counts	Serial Port	Package
HY12P65	7	5+1	1	6Kx16	256x8	4x15	19	50mF	1.5KHz	Y	1ms	5000	UART	LQFP64
HY12P66	7	5+1	1	6Kx16	256x8	4x15	19	50mF	1.5KHz	-	-	5000	UART	LQFP64

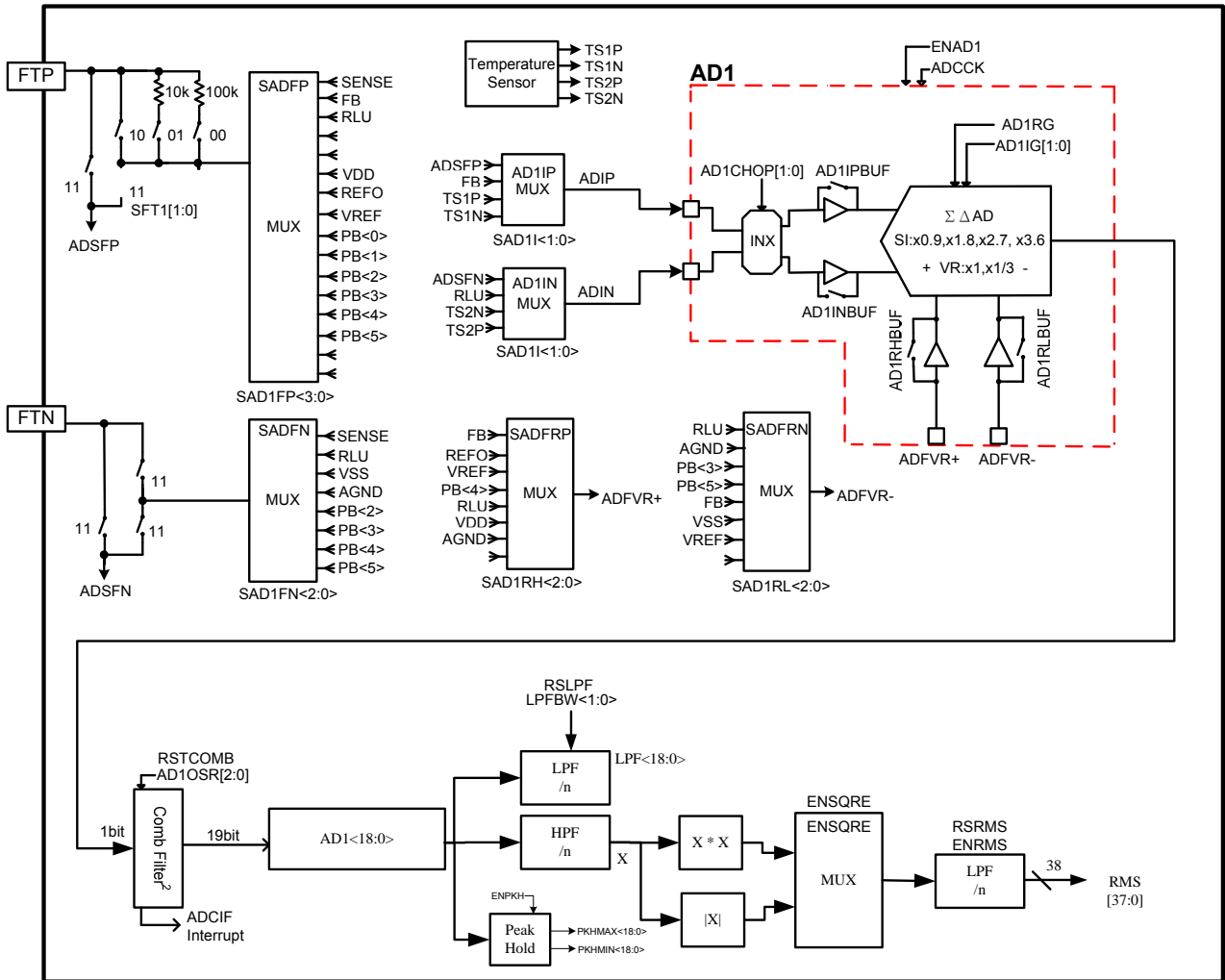
2. Block Diagram



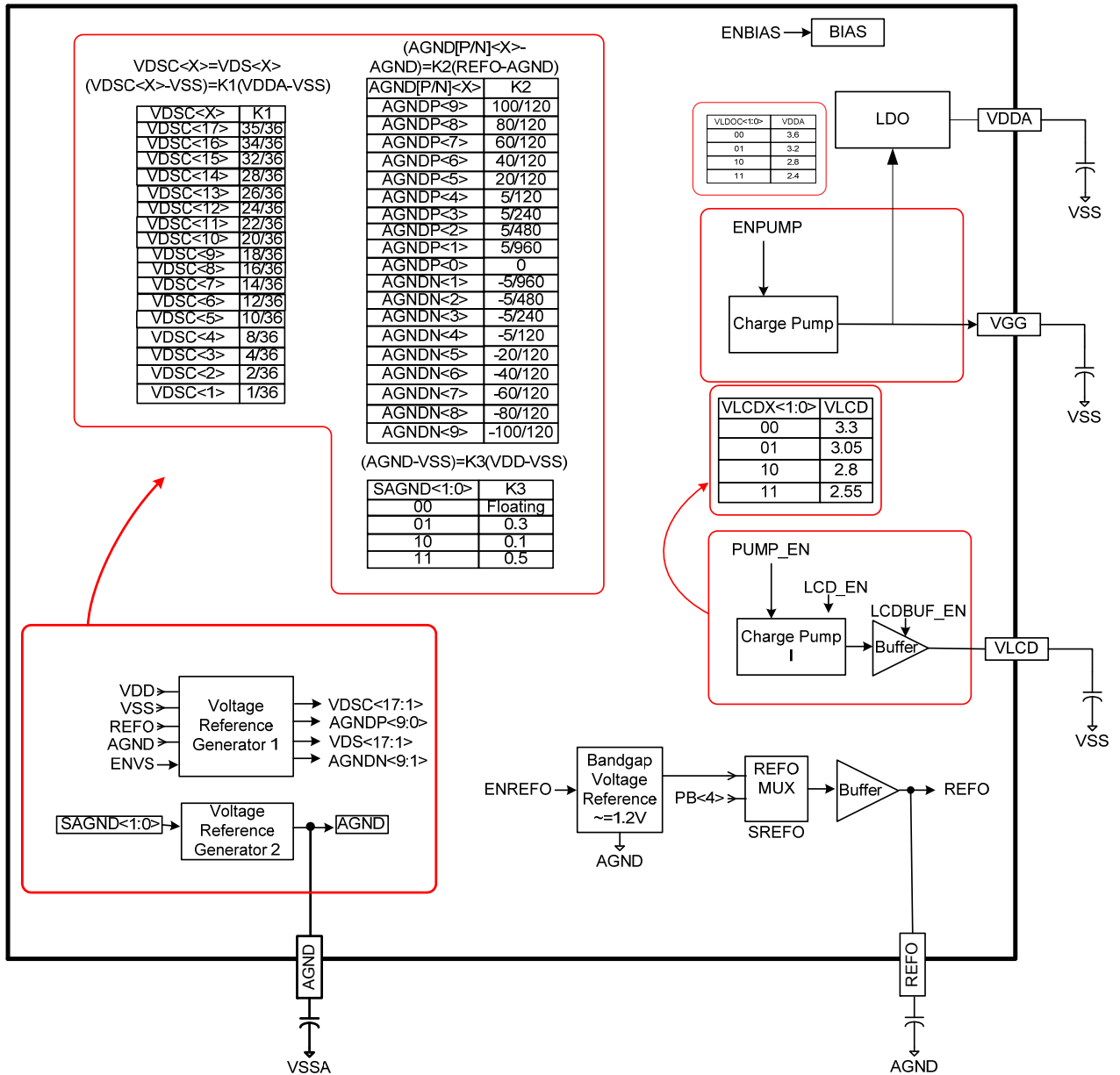
2.1 Multi-Function Block



2.2 ADC

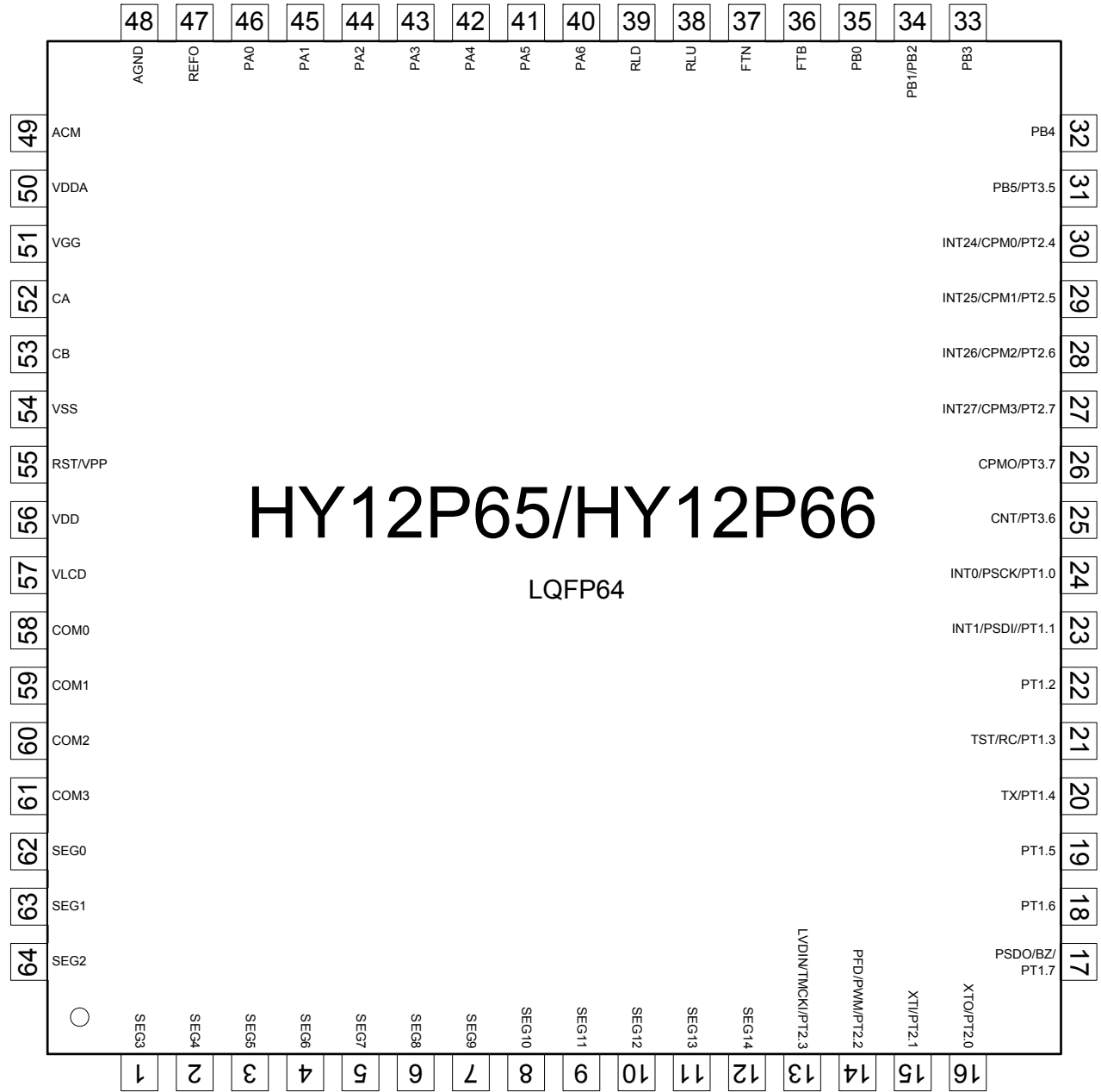


2.3 Power



3. Package And Pin

3.1 64PIN Diagram LQFP64



3.2 Pin Description

"I/O" Input/Output, "I" Input, "O" Output, "S" Schmitt Trigger, "C" CMOS, "P" Power, "A" Analog

Pin		Characteristic		Description
No.	Name	I/O	Type	
1	SEG3	O	A	Segment output of LCD
2	SEG4	O	A	Segment output of LCD
3	SEG5	O	A	Segment output of LCD
4	SEG6	O	A	Segment output of LCD
5	SEG7	O	A	Segment output of LCD
6	SEG8	O	A	Segment output of LCD
7	SEG9	O	A	Segment output of LCD
8	SEG10	O	A	Segment output of LCD
9	SEG11	O	A	Segment output of LCD
10	SEG12	O	A	Segment output of LCD
11	SEG13	O	A	Segment output of LCD
12	SEG14	O	A	Segment output of LCD
13	PT2.3/TMCKI/LVDIN			
	PT2.3	I/O	S	Digital input/output
	TMCKI	I	S	TIMERC clock source input port
	LVDIN	I	A	LVD external signal input port
14	PT2.2/PWM/PFD			
	PT2.2	I/O	C	Digital input/output
	PWM	O	C	PWM output port
	PFD	O	C	PFD output port
15	PT2.1/XTI			
	PT2.1	I/O	S	Digital input/output
	XTI	I	A	Input port of external oscillator
16	PT2.0/XTO			
	PT2.0	I/O	S	Digital input/output
	XTO	O	A	Output port of external oscillator
17	PT1.7/BZ/PSDO			
	PT1.7	I/O	S	Digital input/output
	BZ	O	C	Buzzer output port
	PSDO	O	C	PSDO port of OTP read/write interface
18	PT1.6			
	PT1.6	I/O	S	Digital input/output

19	PT1.5	PT1.5	I/O	S	Digital input/output
20	PT1.4/TX	PT1.4 TX	I/O O	S C	Digital input/output TX of EUART communication interface
21	PT1.3/RC/TST	PT1.3 RC TST	I I I	S S S	Digital input RC of EUART communication interface Enable input of test mode (invalid)
22	PT1.2	PT1.2	I/O	S	Digital input
23	PT1.1/PSDI/INT1	PT1.1 PSDI INT1	I/O I I	S S S	Digital input PSDI of OTP read/write interface Interrupt source, INT1
24	PT1.0/PSCK/INT0	PT1.0 PSCK INT0	I/O I I	S S S	Digital input PSCK of OTP read/write interface Interrupt source, INT0
25	PT3.6/CNT	PT3.6 CNT	I/O I	S S	Digital input/output Input port of frequency counter
26	PT3.7/CMPO	PT3.7 CMPO	I/O O	C C	Digital input/output Output port of comparator
27	PT2.7/CMP3/INT27	PT2.7 CMP3 INT27	I/O I I	C A C	Digital input/output Input port of comparator Interrupt source, E27IF
28	PT2.6/CMP2/INT26	PT2.6 CMP2 INT26	I/O I I	S A S	Digital input/output Input port of comparator Interrupt source, E26IF
29	PT2.5/CMP1/INT25	PT2.5 CMP1 INT25	I/O I I	S A S	Digital input/output Input port of comparator Interrupt source, E25IF
30	PT2.4/CMP0/INT24	PT2.4	I/O	S	Digital input/output

		CMP0	I	A	Input port of comparator
		INT24	I	S	Interrupt source, E24IF
31	PT3.5/PB5	PT3.5	I/O	C	Digital input/output
		PB5	I	A	Analog input channel
32	PB4		I	A	Analog input channel
33	PB3		I	A	Analog input channel
34	PB2 / PB1		I	A	Analog input channel
35	PB0		I	A	Analog input channel
36	FTP		I/O	A	Capacitor connect port of pre-filter
37	FTN		I/O	A	Capacitor connect port of pre-filter
38	RLU		I/O	A	Switch of analog network
39	RLD		I/O	A	Switch of analog network
40	PA6		I/O	A	Switch of analog network
41	PA5		I/O	A	Switch of analog network
42	PA4		I/O	A	Switch of analog network
43	PA3		I/O	A	Switch of analog network
44	PA2		I/O	A	Switch of analog network
45	PA1		I/O	A	Switch of analog network
46	PA0		I/O	A	Switch of analog network
47	REFO		I/O	P	Voltage reference port
48	AGND		I/O	P	Analog power ground end
49	ACM		I/O	P	Voltage reference port
50	VDDA		I/O	P	Analog circuit voltage source
51	VGG		O	P	Charge pump voltage source
52	CA		I/O	A	Charge pump capacitor port
53	CB		I/O	A	Charge pump capacitor port
54	VSS		P	P	Ground end of IC operation voltage source
55	RST/VPP	RST	I	S	Reset IC (Low active)
		VPP	P	P	EPROM read/write voltage source
56	VDD		P	P	Voltage source of IC operation
57	VLCD		I/O	P	Voltage source of LCD
58	COM0		O	A	COM output of LCD
59	COM1		O	A	COM output of LCD
60	COM2		O	A	COM output of LCD
61	COM3		O	A	COM output of LCD

62	SEG0	O	A	Segment output of LCD
63	SEG1	O	A	Segment output of LCD
64	SEG2	O	A	Segment output of LCD

4. Register list

"0" no use, "1" read/write, "w" write, "r" read, "r0" only read 0, "r1" only read 1, "w0" only write 0, "w1" only write 1																
": "unimplemented bit, "x" unknown, "u" unchanged, "d" depends on condition																
Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	I-RESET	R/W				
00H	INDF0	Contents of FSR0 to address data memory value of FSR0 not changed								N/A	N/A	*****				
01H	POINC0	Contents of FSR0 to address data memory value of FSR0 post-incremented								N/A	N/A	*****				
02H	PODEC0	Contents of FSR0 to address data memory value of FSR0 post-decremented								N/A	N/A	*****				
03H	PRINC0	Contents of FSR0 to address data memory value of FSR0 pre-incremented								N/A	N/A	*****				
04H	PLUSW0	Contents of FSR0 to address data memory value of FSR0 offset by W								N/A	N/A	*****				
05H	INDF1	Contents of FSR1 to address data memory value of FSR0 not changed								N/A	N/A	*****				
06H	POINC1	Contents of FSR1 to address data memory value of FSR0 post-incremented								N/A	N/A	*****				
07H	PODEC1	Contents of FSR1 to address data memory value of FSR0 post-decremented								N/A	N/A	*****				
08H	PRINC1	Contents of FSR1 to address data memory value of FSR0 pre-incremented								N/A	N/A	*****				
09H	PLUSW1	Contents of FSR1 to address data memory value of FSR0 offset by W								N/A	N/A	*****				
0FH	FSR0H									FSR0[8]xu	-----			
10H	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte, FSR0[7:0]								xxxx xxxx	uuuu uuuu	*****				
11H	FSR1H									FSR1[8]xu	-----			
12H	FSR1L	Indirect Data Memory Address Pointer 1 Low Byte, FSR1[7:0]								xxxx xxxx	uuuu uuuu	*****				
16H	TOSH			TOS[12]		TOS[11]		TOS[10]	TOS[9]	TOS[8]	...0 0000	...0 0000	-----			
17H	TOSL	Top-of-Stack Low Byte (TOS<7:0>)											0000 0000	0000 0000	*****	
18H	STKPTR	STKFL	STKUN	STKOV				STKPRT[2]	STKPRT[1]	STKPRT[0]	000. .000	000. .000	r,rw0,rw0,-,-r,r,f			
1AH	PCLATH				PC[12]		PC[11]	PC[10]	PC[9]	PC[8]	...0 0000	...0 0000	-----			
1BH	PCLATL	PC Low Byte for PC<7:0>											0000 0000	0000 0000	*****	
1DH	TBLPTRH				TBLPTR[12]		TBLPTR[11]	TBLPTR[10]	TBLPTR[9]	TBLPTR[8]	...0 0000	...0 0000	-----			
1EH	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)											0000 0000	0000 0000	*****	
1FH	TBLDH	Program Memory Table Latch High Byte											0000 0000	0000 0000	*****	
20H	TBLDL	Program Memory Table Latch Low Byte											0000 0000	0000 0000	*****	
21H	PRODH	Product Register of Multiply High Byte											xxxx xxxx	uuuu uuuu	r,r,f,r r,r,f,r	
22H	PRODL	Product Register of Multiply Low Byte											xxxx xxxx	uuuu uuuu	r,r,f,r r,r,f,r	
23H	INTE1	GIE		TMCIE		TMAIE	WDTIE	E1IE	E0IE	0.0. 0000	0.0. 0000	-----				
24H	INTE2	TXIE	RCIE	RMSIE	LPFIE	AD1IE	SSPIE	CTIE		0000 000.	0000 000.	*****				
25H	INTE3	E24IE	E25IE	E26IE	E27IE					0000	0000	-----				
26H	INTF1			TMCIF		TMAIF	WDTIF	E1IF	E0IF	...0 0000	...0 0000	-----				
27H	INTF2	TXIF	RCIF	RMSIF	LPFIF	AD1IF	SSPIF	CTIF		0000 000.	0000 000.	*****				
28H	INTF3	E24IF	E25IF	E26IF	E27IF					0000	0000	-----				
29H	WREG	Working Register											xxxx xxxx	uuuu uuuu	*****	
2AH	BSRCL										BSR[0] 0000 0000	-----		
2BH	STATUS				C	DC	N	OV	Z	...x xxxx	...u uuuu	-----				
2CH	PSTATUS	PD	TO	IDLEB	BOR	SKERR				000d .0.	uduu .d.	rw0,rw0,rw0,rw0,-,-				
2DH	LVDCN1	ENLVD	LVD	VJ1	VJ2	VLDX[3:0]										
2EH	LVDCN2	VSL	SVIN[2:0]			SVIP[3:0]										
2FH	SBMSET1	SKRST	HAOTR[5:0]											x.xx xxxx	u.uu uuuu	*****
30H	MCKCN1	HSSEL	CPUCK[1:0]		HSS[1:0]		HSCK	ENXT	ENHAO	0000 0001	0000 0001	*****				
31H	MCKCN2	LDCS[2:0]			ADCCK	PERCK	BZS[2:0]			0000 0000	0000 0000	*****				
32H	TMACN	ENTMA	TMACK	TMAS[1:0]		ENWDT	WDTSS[2:0]			0000 0000	0000 0000	***** w1,***				
33H	TMAR	TimerA data register											xxxx xxxx	uuuu uuuu	r,r,f,r r,r,f,r	
34H	TMCCN	ENTMC	TMCCK[1:0]		TMCS1[2:0]			TMCS0[1:0]			0000 0000	0000 0000	*****			
35H	PRC	TimerC programmable register											1111 1111	1111 1111	*****	
36H	TMCR	TimerC register											0000 0000	0000 0000	r,r,f,r r,r,f,r	
37H	PWMCN	ENPWM	ENPFD	PWMRL[1:0]						0000 0000	0000 0000	*****				
38H	PWMR	PWM MSB Byte register											xxxx xxxx	uuuu uuuu	*****	
39H	LCDCN1	ENLCD	LC DPR	VLC DX[1:0]			LCDBF	LCDBI[1:0]			0000 000.	0000 000.	*****			
3AH	LCDCN2	LCDBL	LC DMX[1:0]							000.	000.	-----				
3BH	LCD0	Segment SEG1@[7:4] and SEG0@[3:0] data register of LCD											xxxx xxxx	uuuu uuuu	*****	
3CH	LCD1	Segment SEG3@[7:4] and SEG2@[3:0] data register of LCD											xxxx xxxx	uuuu uuuu	*****	
3DH	LCD2	Segment SEG5@[7:4] and SEG4@[3:0] data register of LCD											xxxx xxxx	uuuu uuuu	*****	
3EH	LCD3	Segment SEG7@[7:4] and SEG6@[3:0] data register of LCD											xxxx xxxx	uuuu uuuu	*****	
3FH	LCD4	Segment SEG9@[7:4] and SEG8@[3:0] data register of LCD											xxxx xxxx	uuuu uuuu	*****	
40H	LCD5	Segment SEG11@[7:4] and SEG10@[3:0] data register of LCD											xxxx xxxx	uuuu uuuu	*****	
41H	LCD6	Segment SEG13@[7:4] and SEG12@[3:0] data register of LCD											xxxx xxxx	uuuu uuuu	*****	
42H	LCD7	Segment SEG14@[3:0] data register of LCD										 xxxx uuuu	-----	
46H	URCON	ENSP	ENTX	TX9	TX9D	PARITY	OERR	RCIDL	TRMT	ABDOVF	0000 0.0	0000 0.0	*****			
47H	URSTA				RC9D	PERR	FERR				...00 0110	...00 0110	-,-r,r,f r,r,f,rw0			
48H	BAUDCON				ENCR			RC9	ENADD	ENABD 0000 0000	*****			
49H	BRGRH	Baud Rate Generator Register High Byte											...x xxxx	...u uuuu	-----	
4AH	BRGRL	Baud Rate Generator Register Low Byte											xxxx xxxx	uuuu uuuu	*****	
4BH	TXREG	UART Transmit Register											xxxx xxxx	uuuu uuuu	*****	
4CH	RCREG	UART Receive Register											xxxx xxxx	uuuu uuuu	r,r,f,r r,r,f,r	

“-”no use, “*”read/write, “w”write, “r”read, “r0”only read 0, “r1”only read 1, “w0”only write 0, “w1”only write 1 “.”unimplemented bit, “x”unknown, “u”unchanged, “d”depends on condition														
Address	File Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	A-RESET	i-RESET	R/W		
4DH	PT1	PT1.7	PT1.6	PT1.5	PT1.4	PT1.3	PT1.2	PT1.1	PT1.0	xxxx xxxx	uuuu uuuu	r,r,r,r		
4EH	TRISC1	TC1.7	TC1.6	TC1.5	TC1.4	TC1.3	TC1.2	TC1.1	TC1.0	0000 0000	0000 0000	r,r,r,r,r,r		
4FH	PT1PU	PU1.7	PU1.6	PU1.5	PU1.4	PU1.3	PU1.2	PU1.1	PU1.0	0000 0000	0000 0000	r,r,r,r,r,r		
50H	PT1M1	PM1.7	PM1.6	PM1.5	PM1.4	INTEG1[1:0]		INTEG0[1:0]		0000 0000	0000 0000	r,r,r,r,r,r		
51H	PT2	PT2.7	PT2.6	PT2.5	PT2.4	PT2.3	PT2.2	PT2.1	PT2.0	xxxx xxxx	uuuu uuuu	r,r,r,r,r,r		
52H	TRISC2	TC2.7	TC2.6	TC2.5	TC2.4	TC2.3	TC2.2	TC2.1	TC2.0	0000 0000	0000 0000	r,r,r,r,r,r		
53H	PT2DA	DA2.7	DA2.6	DA2.5	DA2.4	DA2.3			PM2.2[1:0]	0000 0.00	0000 0.00	r,r,r,r,r,r		
54H	PT2PU	PU2.7	PU2.6	PU2.5	PU2.4	PU2.3	PU2.2	PU2.1	PU2.0	0000 0000	0000 0000	r,r,r,r,r,r		
55H	PT3	PT3.7	PT3.6	PT3.5			TC3.7	TC3.6	TC3.5	xxx. 000.	uuu. 000.	r,r,r,r,r,r		
56H	PT3PU	PU3.7	PU3.6	PU3.5			PM3.7	DA3.5		000. 0.0.	000. 0.0.	r,r,r,r,r,r		
57H	PAX6					PS6	DS6	FS6	SS6					
58H	PA54	PS5	DS5	FS5	SS5	PS4	DS4	FS4	SS4					
59H	PA32	PS3	DS3	FS3	SS3	PS2	DS2	FS2	SS2					
5AH	PA10	PS1	DS1	FS1	SS1	PS0	DS0	FS0	SS0					
5BH	PWRCN	DMMBIAS	SAGND[1:0]		ENVS	ENREFO	ENLDO	LDOC[1:0]						
5CH	PWRCN2	MCUBIAS	ENCPVGG	ENCOMP	ENCNTI	ENCTR	RSTCOMB	RSLPF	RSRMS					
5DH	ADCN1	SDIO	SREFO	SFT1<1:0>			SFUVR<3:0>							
5EH	ADCN2	SMODE<7:0>												
5FH	ADCN3	SCMPRH<3:0>				SCMPRL<3:0>								
60H	ADCN4	SCMPI<2:0>			AD1CHOP<1:0>		AD1OSR<2:0>							
61H	ADCN5	SAD1FP<3:0>			HSAD		SAD1FN<2:0>							
62H	ADCN6	SAD1RH<2:0>			SAD1RL<2:0>			SAD1I<1:0>						
63H	ADCN7	ENAD1	AD1IG<1:0>		AD1RG	AD1RHBUF	AD1RLBUF	AD1IPBUF	AD1INBUF					
64H	RMSCN	ENRMS	ENLPF	ENSQRE	LPFBW<1:0>		ENPKH							
65H	CTAU	CTA<23:16>												
66H	CTAH	CTA<15:8>												
67H	CTAL	CTA<7:0>												
68H	CTBU	CTB<23:16>												
69H	CTBH	CTB<15:8>												
6AH	CTBL	CTB<7:0>												
6BH	CTCU	CTC<23:16>												
6CH	CTCH	CTC<15:8>												
6DH	CTCL	CTC<7:0>												
6EH	CTSTA	CNTI	ACPO	CMPHO	CMPLO					CTBOV				
6FH	PKHMAXU	PKHMAX<18:11>												
70H	PKHMAXH	PKHMAX<10:3>												
71H	PKHMAXL	PKHMAX<2:0>												
72H	PKHMINU	PKHMIN<18:11>												
73H	PKHMINH	PKHMIN<10:3>												
74H	PKHMINL	PKHMIN<2:0>												
75H	RMSDATA4	RMS<37:30>												
76H	RMSDATA3	RMS<29:22>												
77H	RMSDATA2	RMS<21:14>												
78H	RMSDATA1	RMS<13:6>												
79H	RMSDATA0	RMS<5:0>												
7AH	LPFDATAU	LPF<18:11>												
7BH	LPFDATAH	LPF<10:3>												
7CH	LPFDATAL	LPF<2:0>												
7DH	AD1DATAU	AD1<18:11>												
7EH	AD1DATAH	AD1<10:3>												
7FH	AD1DATAL	AD1<2:0>												
80H ~ FFH	GPR0	General Purpose Register as 128Byte												
100H~17FH	GPR1	General Purpose Register as 128Byte												

*1 LPFBW<1> bit of HY12P66 is always “1”.

*2 ENPKH bit of HY12P66 is always “0”.

*3 HY12P66 does not have PKHMAXU, PKHMAXH, PKHMAXL, PKHMINU, PKHMINH, PKHMINL..registers.

5. Absolute Maximum Ratings

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

- Voltage applied at VDD (VDDA) to VSS (VSSA) -0.2 V to 4.0 V
- Voltage applied to any pin -0.2 V to V_{DD} + 0.3 V
- Diode current at any device terminal ±2 mA
- Storage temperature range, Tstg -55°C to 150°C
- Total power dissipation 0.5w
- Lead temperature (soldering, 10s) 300°C

5.1 Recommended Operating Conditions

T_A = -40°C ~ 85°C, unless otherwise noted

Sym.	Parameter		Test Conditions		Min.	Typ.	Max.	unit
V _{DD}	Supply Voltage		All digital peripherals and CPU		2.2		3.6	V
			Analog peripherals		2.4		3.6	
V _{SS}	Supply Voltage				0		0	
XT	External Oscillator	Ceramic resonator	V _{DD} = 2.2V, ENXT[0]=1b	HSSEL=0b,	450K		Hz	
	Frequency	Crystal		HSSEL=0b,	1M	8M		

5.2 Internal RC Oscillator

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO	High Speed Oscillator frequency	ENHAO[0]=1		4		MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO		32		KHz

5.3 Supply Current into VDD Excluding Peripherals Current

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}, \text{OSC_LPO} = 32\text{KHz}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = 8MHz, OSC_HAO = off, CPU_CK = 8MHz		1.34	2	mA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 4MHz, CPU_CK = 4MHz		0.36	0.55	mA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 4MHz, CPU_CK = 2MHz		0.2	0.3	mA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.65	1.2	uA

OSC_CY : External Oscillator frequency.

OSC_HAO : Internal High Accuracy Oscillator frequency.

CPU_CK : CPU core work frequency.

5.4 Port 1~3

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage				2.1	V
V_{IL}	Low-Level input voltage		0.9			
V_{hys}	Input Voltage hysteresis($V_{IH} - V_{IL}$)			0.8		V
I_{LKG}	Leakage Current				0.1	uA
R_{PU}	Port pull high resistance			180		k Ω
Output voltage and current and frequency						
V_{OH}	High-level output voltage	$I_{OH}=10\text{mA}$	$V_{DD} - 0.3$			V
V_{OL}	Low-level output voltage	$I_{OL}=-10\text{mA}$		$V_{SS} + 0.3$		

5.5 Reset(Brownout, External RST pin, Low Voltage Detect)

$T_A = 25^{\circ}\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit	
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us	
	V_{DD} Start Voltage to accepted reset internally (L→H), V_{LVR}		1.6	1.85	2.1	V	
	Hysteresis, $V_{HYS-LVR}$		70			mV	
RST	Pulse length needed as RST/VPP pin to accepted reset internally, t_{d-RST}		2			us	
	Input Voltage to accepted reset internally		0.9			V	
	Hysteresis, $V_{HYS-RST}$		0.8			V	
LVD Compare Mode	Operation current, I_{LVD}		10			15	uA
	External input voltage to compare reference voltage		1.2				V
	Compare reference voltage temperature drift		$T_A = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$		100		ppm/ $^{\circ}\text{C}$
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1110b$		3.3			V	
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1101b$		3.2				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1100b$		3.1				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1011b$		3.0				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1010b$		2.9				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1001b$		2.8				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=1000b$		2.7				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0111b$		2.6				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0110b$		2.5				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0101b$		2.4				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0100b$		2.3				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0011b$		2.2				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0010b$		2.1				
	Detect V_{DD} voltage rang by user option, $V_{SVS} VLDx[3:0]=0001b$		2.0				
VDD Ratio	Comparator Offset Error		-150		150		mV
Compare Mode	VDD Ratio Error		-5		5		%
BOR : Brownout Reset LVR : Low Voltage Reset of BOR LVD : Low Voltage Detect RST : External Reset pin							

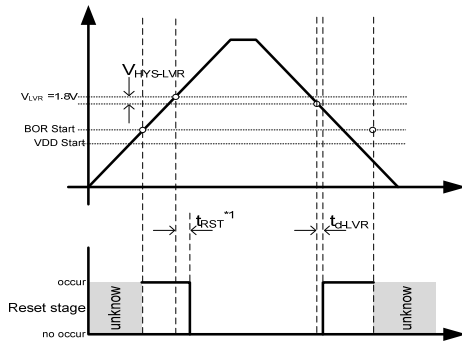


Figure 6.5-1 BOR reset diagram

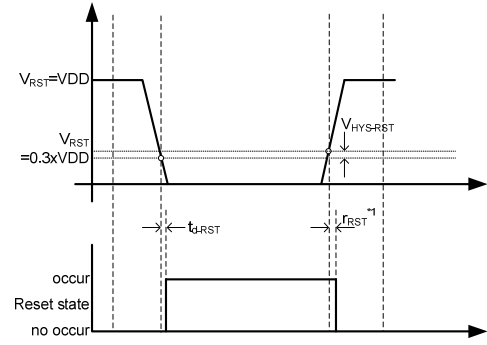


Figure 6.5-2 RST reset diagram

*1 t_{RST} : Please see BOR Introduce of HY12Pxx series User's Guide (UG-HY12S65-Vxx).

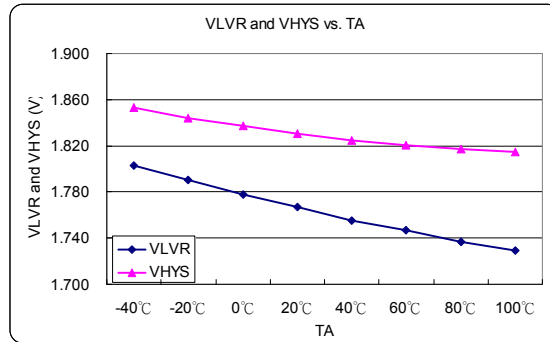


Figure 6.5-3 VLVR and VHYS vs. Temperature

5.6 Power System

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	$I_L = 0\text{mA}$	LDOC[1:0]=00b	22			μA
	Select VDDA output voltage	$I_L = 0.1\text{mA}$, $V_{DD}=3\text{V}$	LDOC[1:0]=00b	3.6			V
	Load Regulation	$V_{DD}=2.4\text{V}$ $I_L = 1\sim 5\text{mA}$	LDOC[1:0]=00b	10			mV
	Line Regulation	$V_{DD}=2.4\text{V}\sim 3.6\text{V}$ $I_L = 1\text{mA}$	LDOC[1:0]=00b	40			mV
	Temperature drift	LDOC[1:0]=11b	$T_A=-40^\circ\text{C}\sim 85^\circ\text{C}$	100			ppm/ $^\circ\text{C}$
	V_{DD} Voltage drift	$I_L = 0.1\text{mA}$	$V_{DD}=2.5\text{V}\sim 3.6\text{V}$	± 0.2			%/V
AGND	AGND operation current, I_{Agnd}	SAGND#00b	$I_L = 0\text{mA}$	20			μA
	Output voltage, V_{Agnd}		$I_L = 0\mu\text{A}$	1.0			V
	Output voltage with Load		$I_L = \pm 200\mu\text{A}$	0.98	1.02		V_{AGND}
REFO	V(REFO,AGND)	ENLDO=1b,	$I_L = 0\mu\text{A}$	1.2			V
	Temperature drift	SAGND#00b	$T_A=-40^\circ\text{C}\sim 85^\circ\text{C}$	100			ppm/ $^\circ\text{C}$
	RMS Noise			60			μVrms

5.7 LCD

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, C_{VLCD} = 4.7\mu\text{F}$, unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
I_{LCD}	Operation supply current without output buffer.(all segment turn on)	LCDPR[0]=1	$V_{DD} = 2.2\text{V}$	20			μA
			$V_{DD} = 3.0\text{V}$				
VLCD	Supply Voltage at VLCD pin	LCDPR[0]=0		2.2	3.6		V
	Embedded Charge Pump output voltage at VLCD pin	$V_{DD} = 2.2\text{V}$, LCDPR[0]=1, $C_{VLCD} = 4.7\mu\text{F}$	VLCDX[1:0]=11b	2.295	2.55	2.805	V
			VLCDX[1:0]=10b	2.52	2.8	3.08	
			VLCDX[1:0]=01b	2.745	3.05	3.355	
VLCDX[1:0]=00b	2.97	3.3	3.63				
Z_{LCD}	Output impedance with LCD buffer	$f_{LCD} = 128\text{Hz}, VLCD=3.05\text{V}$		10			k Ω

5.8 ΣΔADC, Power Supply and Recommended Operating Conditions

T_A = 25°C, V_{DD} = 3.0V, V_{DDA}=3.6V, V_R=1.2V, AGND=0.5V_{DD}, ADC Clock=400kHz Input buffer on unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
f _{ΣADC}	Modulator sample frequency, ADC_CK			400			KHz
I _{ΣADC}	Operation supply current	Input gain =0.9, input buffer on ADC_CK=400KHz		550			uA
D _{ΣADC}	Maximum ADC Output Code (ADC Gain Factor)	OSR=2500~20000		17D79		d	
		OSR=64~256		3FFFF			
		OSR=32		3FD7C			
Eos	Input offset voltage	Chopper on OSR=20000	Input gain=0.9, reference gain=1	20	100	uV	
			Input gain=3.6, reference gain=0.33	5	10		
Rev	Roll-over error voltage	Chopper on OSR=20000	Input gain=0.9, reference gain=1	200	600	uV	
			Input gain=3.6, reference gain=0.33	10	30		
Vrms	Input RMS Noise	Chopper on, OSR=20000, input gain=0.9 reference gain=1		10		uV	
		Chopper on, OSR=20000, input gain=3.6 reference gain=0.33		2			
		Chopper off, OSR=32, input gain=0.9 reference gain=1		400			
		Chopper off, OSR=32, input gain=3.6 reference gain=0.33		80			
NM	Normal Rejection ratio	Chopper On OSR=20000 ADCLK=1	Input gain=0.9, reference gain=1. Vin=200mVrms 50/60Hz	60		dB	
			Input gain=3.6, reference gain=0.33. Vin=20mVrms 50/60Hz				
AC _{bw}	AC Measurement	OSR=32, LPFBW=1024	Sine wave, 0.5% error	20	1.5k	Hz	
	Bandwidth		Sine wave, 3dB	6k			
			Square wave, 0.5%	0.1k			

			error		
			Triangle wave, 0.5%		1.2k
			error		

5.9 ΣΔADC, Temperature Sensor

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC _S	Sensor temperature drift			178		uV/°C
KT	Absolute Temperature Scale 0°K	ADC Gain=0.9, OSR=20000, Input buffer Off, VR:REFO-AGND		-281		°C
TC _{ERR}	One point calibrate error temperature	Calibration at 25°C of -40°C~85°C		±2		°C

5.10 Analog Input and Switch Performance

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=3.6\text{V}$ AGND=0.5VDDA unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I _{AL}	Analog Input Leakage Current	AGND=0.5 VDDA		10	100	pA
		AGND=0.3VDDA		10	100	
		AGND=0.1VDDA		100	500	
R _{sw}	Switch Turn On Resistance	PS0,PS1		20		Ohm
		DS0,DS1		40		
		DS2~DS6, PS2~PS6		80		
		SS0~SS6,FS0~FS6		400		

5.11 DMM Comparator

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=3.6\text{V}$ AGND=0.5VDDA, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I _{CMP}	Comparator Supply Current					uA
V _I	Comparator Input Range	CMPL	0		VDDA-0.7	V
		CMPH	0.4		VDDA	
V _{os}	Comparator Input Offset Voltage	CMPL, VRLCMP=AGND		5		mV
		CMPH VRHCMP=AGND		5		
V _n	Comparator Input peak to peak noise	CMPL		5		mV
		CMPH		5		
		CMPH&CMPL		10		
CMP _{BW}	Comparator Bandwidth	VRHCMP=AGNDP<2>, VRLCMP=AGNDN<2> VIN=100mVrms		1		MHz

6. Ordering Information

Device No. ¹	Package Type	Pins	Package Drawing		Code ²	Shipment Packing Type	Unit Q'ty	Material Composition	MSL ³
HY12P65-D000	Die	-	D	000	000	-	100	Green ⁴	-
HY12P65-L064	LQFP	64	L	064	000	Tray	250	Green ⁴	MSL-3

¹ **Device No.:** Model No. – Package Type Description – Code (Blank Code/ Standard/ Customized Programming Code)

Ex: Your customized programming code is 008 and you require die shipment.

The device No. will be HY12P65-D000-008.

Ex: You request blank code in die package.

The device No. will be HY12P65-D000.

Ex: You request blank code in LQFP 64 package.

The device No. will be HY12P65-L064.

And please clearly indicate the shipment packing type when placing orders.

Ex: Your customized programming code is 008 and you require products in LQFP 64 package.

The device No. will be HY12P65-L064-008.

And please clearly indicate the shipment packing type when placing orders.

² **Code :**

“001”~ “999” is standard or customized programming code.

Blank code does not have these numbers.

³ **MSL:**

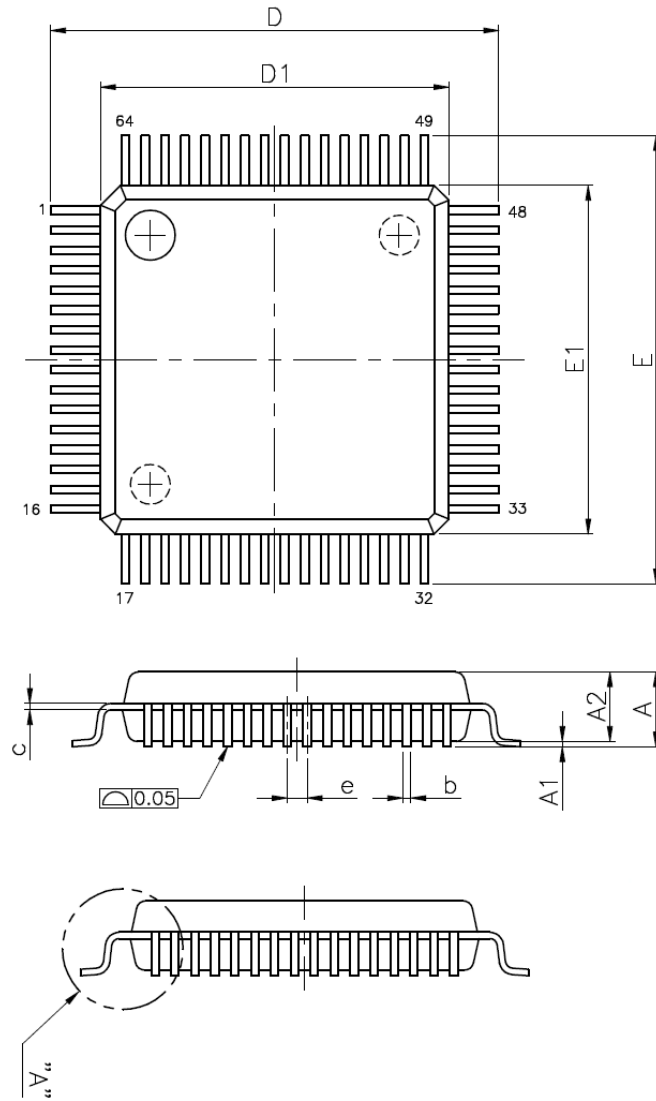
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization.

The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

⁴ **Green (RoHS & no Cl/Br):**

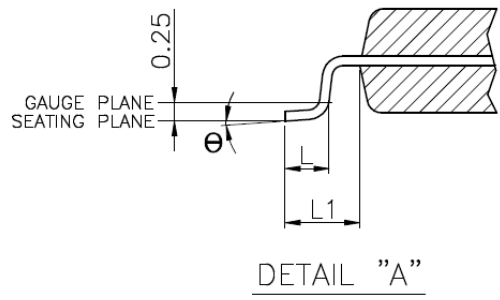
HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%)

7. Packaging Information



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°



JEDEC MS-026 Compliant

8. Revision Record

Major differences are stated thereafter:

Version	Page	Revision Summary
V02	All	First edition
V03	6~16	Updated the figures (removed SPI function)
	18	Revised chapter 5.3 Supply Current into VDD excluding Peripherals Current information.
	22	ADC max. Output code revision
V04	5	Add HY12P66 Difference
	11~12	Reviser Pin Description (Pin12~Pin34)
V05	8	Revise ADC diagram
	16	Revise register error
V06	22~23	Add-in AC Measurement Bandwidth specification.