



HY15P41

Datasheet

8-Bit RISC-like Mixed Signal Microcontroller

Embedded 18-Bit $\Sigma\Delta$ ADC

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- 8、本規格書中內容，未經本公司許可，嚴禁用於其他目的之轉載或複製。

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8-Bit RISC-like Mixed Signal Microcontroller

1. 特點

- 8-Bit RISC-like 微控制器，具有 66 條高性能指令集 H08C(同 H08A)
- 22-Bit $\Sigma\Delta$ ADC 類比數位轉換器
 - 梳狀濾波器採二階設計，轉換頻率達 7.8Ksps
 - 取樣頻率 500KHz
 - 超取樣頻率設置 64~32768
 - 全差動輸入信號
 - 測量範圍的零點調整
 - 信號放大
x1/4,x1/2,x1,x2,x4,x8,x16
 - 測量信號支援多通道輸入
 - 低溫飄係數
 - 內置絕對溫度感測器
- 內部電源系統
 - 內置 LDO 線性穩壓電源 VDDA
 - ◆ 內部類比電路或外部傳感器電壓源
 - ◆ 多段可輸出電壓設置，可外灌輸入電壓
 - ◆ 低操作功耗與低溫飄係數
- 計時器
 - Watch Dog
 - ◆ 復位事件與中斷事件
 - 8-bit Timer
 - ◆ 中斷事件
 - ◆ 比較事件
 - 16-bit Timer
 - ◆ 16-Bit PWM 輸出
 - ◆ 兩個 8-Bit PWM 輸出
 - ◆ 中斷事件
- 工作電壓與操作溫度範圍
 - V_{DD} : 2.2V ~ 5.5V
 - V_{DDA} : 2.4V ~ 4.5V
 - - 40°C ~ 85°C
- 工作頻率
 - 內建高精度 HAO 震盪器
2MHz/4MHz/8MHz
 - 內建低功耗 LPO 震盪器 14.5KHz
- 記憶體型式
 - 2KW OTP 程式記憶體
 - 128B 資料記憶體
 - 6 層堆棧
 - Build-In EPROEM
 - ◆ VPP 外部燒錄電壓 8.5V
 - ◆ 64W EPROM 記憶體
- 引腳特色
 - 具 10mA 驅動能力
- 復位機制
 - Power On Reset
 - Brown Out Reset
 - Watch Dog Reset
 - Stack Over Reset
- 串列通訊 EUART 模組
- I²C通信(Master/Slave mode)模組

功能列表

Model No.	VDD	System Clock (Hz)	Program Memory (word)	SRAM (byte)	BIE (word)	ADC ENOB (bit x ch)	Sample Rate (sps)	TPS	I/O	Timer (bit x ch)	PWM (bit x ch)	Serial Interface (I/F x ch)	Package
HY15P41	2.2V~5.5V	14.5K~8M	2K	128	64	18-bit x 5	15~7.8K	yes	1xI + 5xIO	8-bit x 1 16-bit x 1	8-bit x 2 16-bit x 1	EUART x 1 I2C x 1	SOP8 SOP16 DFN12

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2. 引腳定義

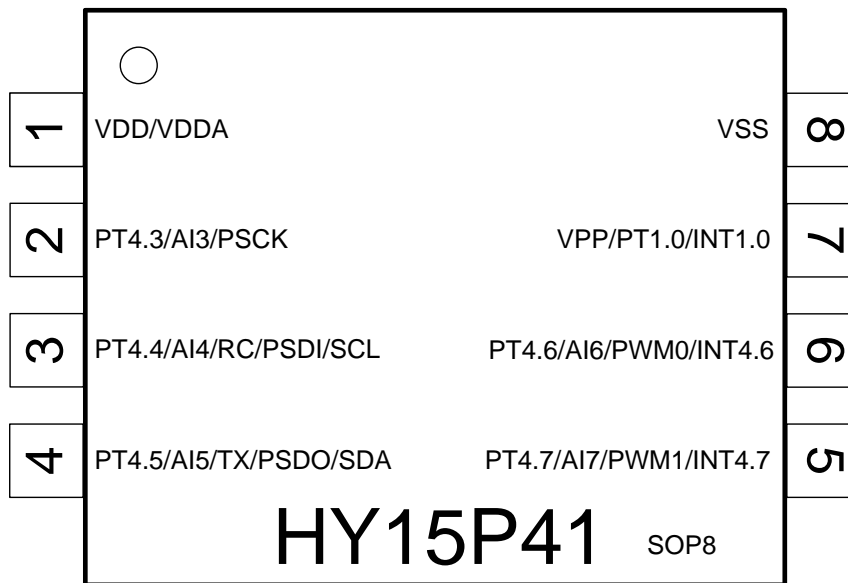


Figure 2-1 HY15P41 SOP8 引腳圖

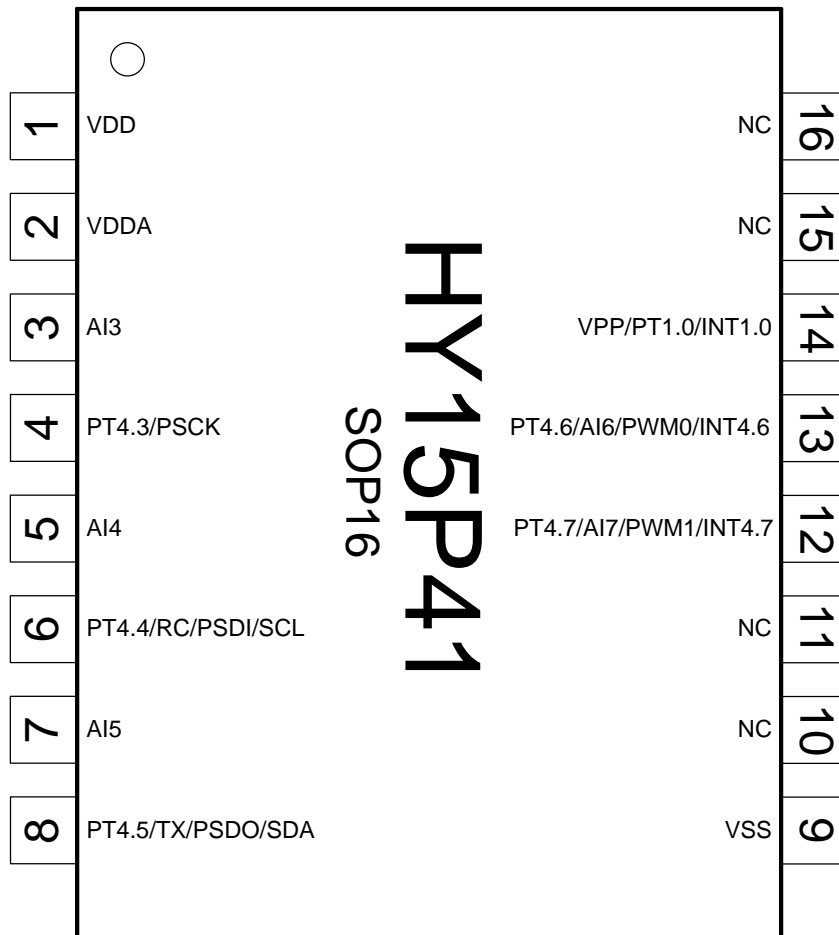


Figure 2-2 HY15P41 SOP16 引腳圖

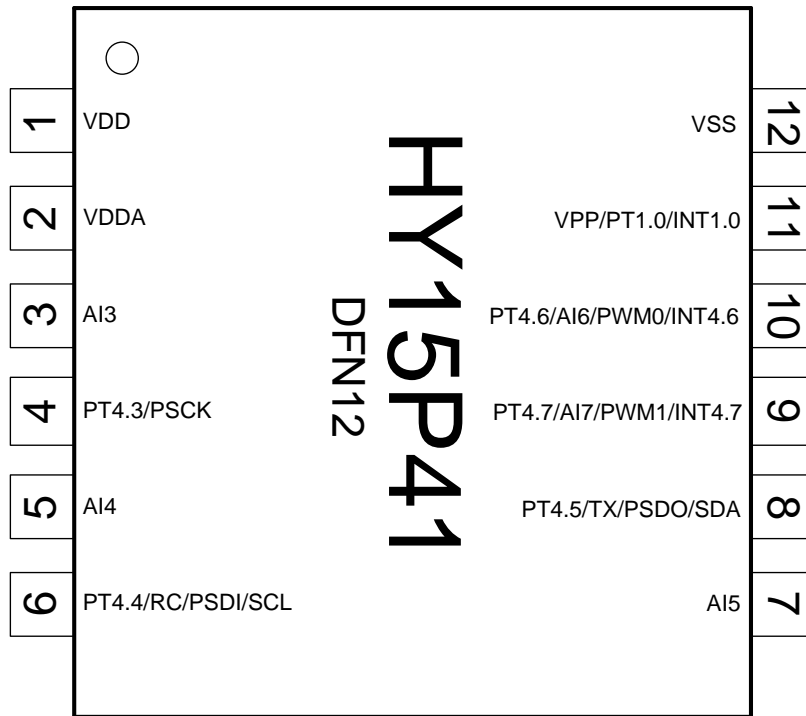


Figure 2-3 HY15P41 DFN12 引腳圖

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2.1. 引腳定義及標記信息說明

2.1.1. SOP8 引腳定義

“I”：輸入,“O”：輸出,“A”：類比,“S”：史密斯觸發,“C”：CMOS I/O,“P”：電壓源,“/”：或,“X”：可忽略					
封裝	引腳名稱	設計		描述	
		型式	緩衝		
SOP8					
1	VDD	P	P	晶片工作電壓源輸入引腳	
1	VDDA	P	P	LDO 線性穩壓電源輸出引腳	
2	PT4.3/AI3/PSCK	PT4.3	I/O	S/C	數位輸入 / 輸出引腳
		AI3	A	A	類比輸入通道
		PSCK	I	S	OTP 讀/寫介面 PSCK 接口
3	PT4.4/AI4/RC/PSDI/SCL	PT4.4	I/O	C	數位輸入 / 輸出引腳
		AI4	A	A	類比輸入通道
		RC	I	S	EUART 訊介面 RC 接口
		PSDI	I	S	OTP 讀/寫介面 PSDI 接口
		SCL	I/O	S	I2C 通訊介面時鐘接口
4	PT4.5/AI5/TX/PSDO/SDA	PT4.5	I/O	C	數位輸入 / 輸出引腳
		AI5	A	A	類比輸入通道
		TX	O	S	EUART 訊介面 TX 接口
		PSDO	I/O	S	OTP 讀/寫介面 PSDO 接口
		SDA	I/O	S	I2C 通訊介面數據接口
5	PT4.7/AI7/PWM1/INT4.7	PT4.7	I/O	C	數位輸入 / 輸出引腳
		AI7	A	A	類比輸入通道
		PWM1	O	C	TMB 的 PWM1 輸出引腳
		INT4.7	I	S	外部中斷源
6	PT4.6/AI6/PWM0/INT4.6	PT4.6	I/O	C	數位輸入 / 輸出引腳
		AI6	A	A	類比輸入通道
		PWM0	O	C	TMB 的 PWM0 輸出引腳
		INT4.6	I	S	外部中斷源
7	PT1.0/VPP/INT1.0	PT1.0	I	S	數位輸入
		VPP	P	P	晶片燒錄電壓源輸入引腳
		INT1.0	I	S	外部中斷源

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8	VSS	P	P	晶片工作電壓源接地端引腳
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表 2-1 引腳定義與功能說明

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2.1.2. SOP16 引腳定義

“I”：輸入,“O”：輸出,“A”：類比,“S”：史密斯觸發,“C”：CMOS I/O,“P”：電壓源,“/”：或,“X”：可忽略				
封裝	引腳名稱	設計		描述
		型式	緩衝	
SOP16				
1	VDD	P	P	晶片工作電壓源輸入引腳
2	VDDA	P	P	LDO 線性穩壓電源輸出引腳
3	AI3	A	A	類比輸入通道
4	PT4.3/PSCK	PT4.3 I/O PSCK I	S/C S	數位輸入 / 輸出引腳 OTP 讀/寫介面 PSCK 接口
5	AI4	A	A	類比輸入通道
6	PT4.4/RC/PSDI/SCL	PT4.4 I/O RC I PSDI I SCL I/O	C S S S	數位輸入 / 輸出引腳 EUART 訊介面 RC 接口 OTP 讀/寫介面 PSDI 接口 I2C 通訊介面時鐘接口
7	AI5	A	A	類比輸入通道
8	PT4.5/TX/PSDO/SDA	PT4.5 I/O TX O PSDO I/O SDA I/O	C S S S	數位輸入 / 輸出引腳 EUART 訊介面 TX 接口 OTP 讀/寫介面 PSDO 接口 I2C 通訊介面數據接口
9	VSS	P	P	晶片工作電壓源接地端引腳
12	PT4.7/AI7/PWM1/INT4.7	PT4.7 I/O AI7 A PWM1 O INT4.7 I	C A C S	數位輸入 / 輸出引腳 類比輸入通道 TMB 的 PWM1 輸出引腳 外部中斷源
13	PT4.6/AI6/PWM0/INT4.6	PT4.6 I/O AI6 A PWM0 O INT4.6 I	C A C S	數位輸入 / 輸出引腳 類比輸入通道 TMB 的 PWM0 輸出引腳 外部中斷源
14	PT1.0/VPP/INT1.0			

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		PT1.0	I	S	數位輸入
		VPP	P	P	晶片燒錄電壓源輸入引腳
		INT1.0	I	S	外部中斷源
Others	NC		-	-	Not Connect

表 2-2 引腳定義與功能說明

2.1.3. DFN12 引腳定義

“I”：輸入，“O”：輸出，“A”：類比，“S”：史密斯觸發，“C”：CMOS I/O，“P”：電壓源，“/”：或，“X”：可忽略					
封裝	引腳名稱	設計		描述	
		型式	緩衝		
DFN12					
1	VDD	P	P	晶片工作電壓源輸入引腳	
2	VDDA	P	P	LDO 線性穩壓電源輸出引腳	
3	AI3	A	A	類比輸入通道	
4	PT4.3/PSCK	PT4.3 PSCK	I/O I	S/C S	數位輸入 / 輸出引腳 OTP 讀/寫介面 PSCK 接口
5	AI4	AI4	A	A	類比輸入通道
6	PT4.4/RC/PSDI/SCL	PT4.4 RC PSDI SCL	I/O I I I/O	C S S S	數位輸入 / 輸出引腳 EUART 訊介面 RC 接口 OTP 讀/寫介面 PSDI 接口 I2C 通訊介面時鐘接口
7	AI5	AI5	A	A	類比輸入通道
8	PT4.5/TX/PSDO/SDA	PT4.5 TX PSDO SDA	I/O O I/O I/O	C S S S	數位輸入 / 輸出引腳 EUART 訊介面 TX 接口 OTP 讀/寫介面 PSDO 接口 I2C 通訊介面數據接口
9	PT4.7/AI7/PWM1/INT4.7	PT4.7 AI7 PWM1 INT4.7	I/O A O I	C A C S	數位輸入 / 輸出引腳 類比輸入通道 TMB 的 PWM1 輸出引腳 外部中斷源
10	PT4.6/AI6/PWM0/INT4.6	PT4.6 AI6 PWM0 INT4.6	I/O A O I	C A C S	數位輸入 / 輸出引腳 類比輸入通道 TMB 的 PWM0 輸出引腳 外部中斷源
11	PT1.0/VPP/INT1.0	PT1.0	I	S	數位輸入

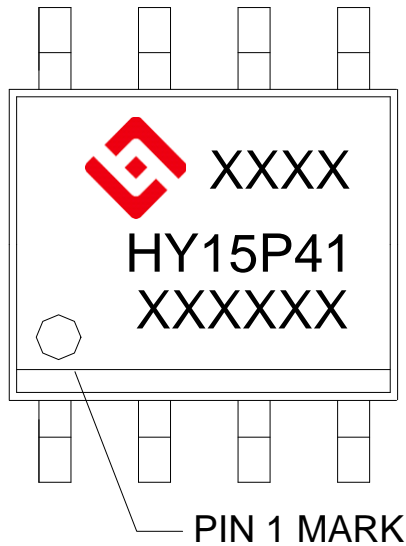
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		VPP	P	P	晶片燒錄電壓源輸入引腳
		INT1.0	I	S	外部中斷源
12	VSS		P	P	晶片工作電壓源接地端引腳

表 2-2 引腳定義與功能說明



- 紘康 Logo + 生產識別碼
- 產品名稱 : HY15P41
- 產品批號

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Embedded 18-Bit $\Sigma\Delta$ ADC
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3. 應用電路

3.1. 3*PIR application (Pyro-electric infrared detector)

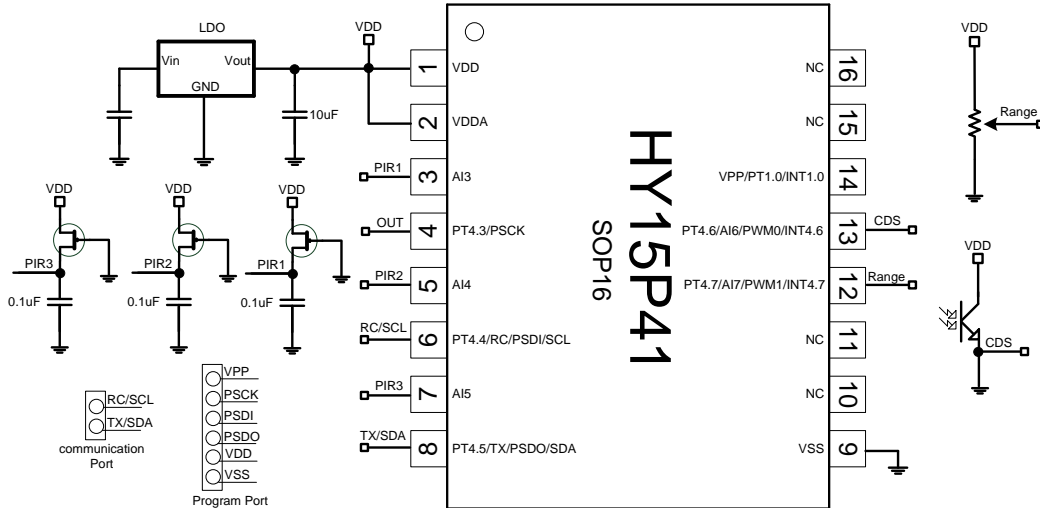


Figure 3-1 3*PIR 應用電路

3.2. Smart Pressure sensor application

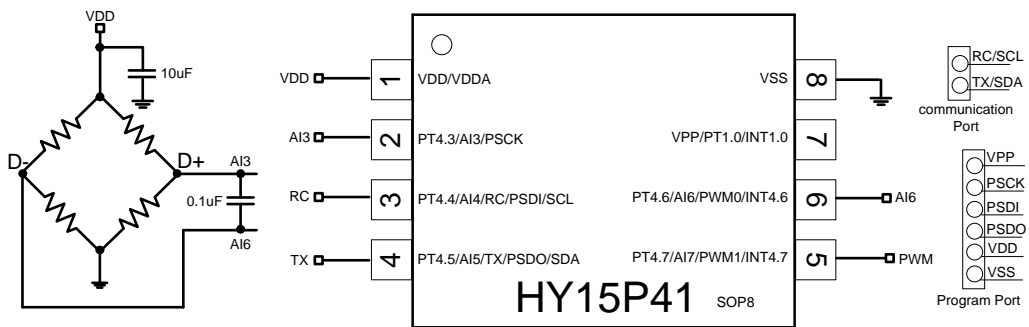


圖 3-2 Smart Pressure Sensor 應用電路

3.3. Battery voltage, current and temperature detection application

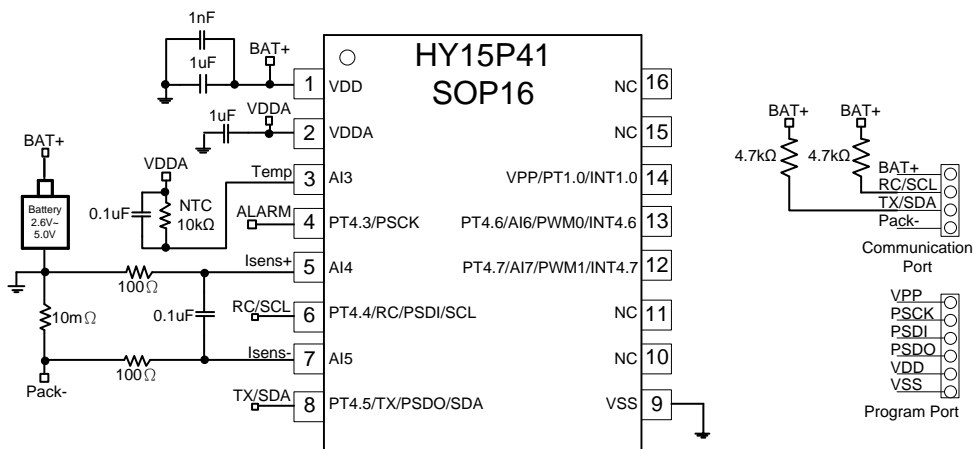


Figure 3-3 Battery voltage, current and temperature detection 應用電路

4. 功能概述

4.1. 内部方块图

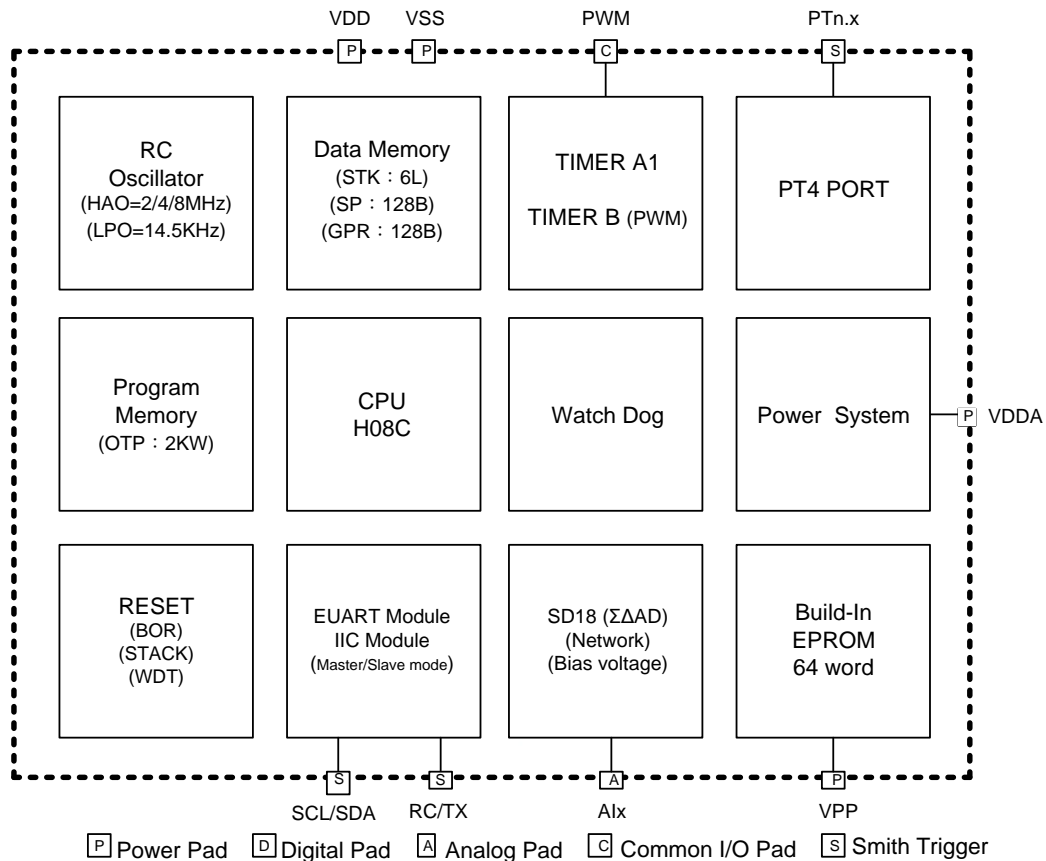


Figure 4-1 HY15P41 内部方块图

4.2. 相關說明與支援文件

晶片功能相關使用說明書

DS-HY15P41 HY15P41 說明書

UG-HY15S41 HY15P41 使用說明書

開發工具相關使用說明書

APD-HYIDE002 HY15P 系列開發工具軟體使用說明書

APD-HYIDE005 HY15S41 開發工具硬體使用說明書

APD-HYIDE003 HY15P 系列 HexLoader 說明書

APD-HYIDE013 HY10000-WK08C 整合型燒錄器使用說明書

BDI-HY15P41 HY15P41 個別產品的裸片打線資訊

4.3. Clock System

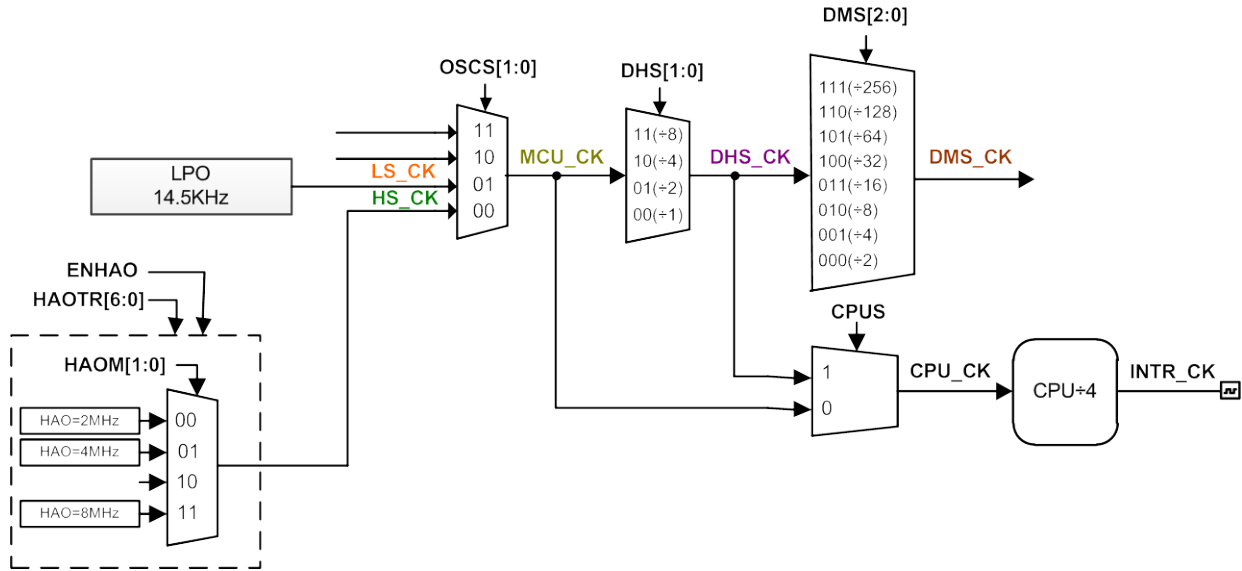


Figure 4-2 Clock System 方塊圖(一)

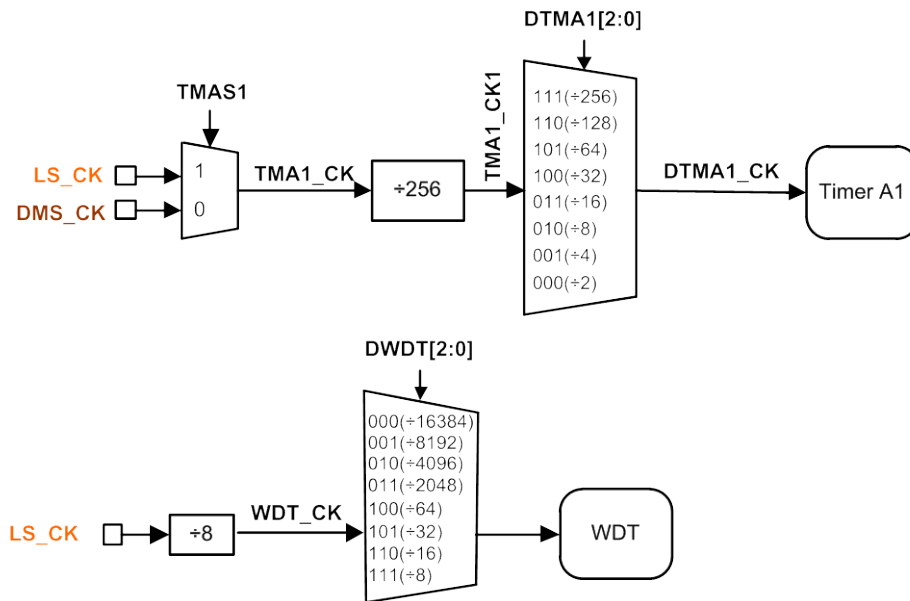


Figure 4-3 Clock System 方塊圖(二)

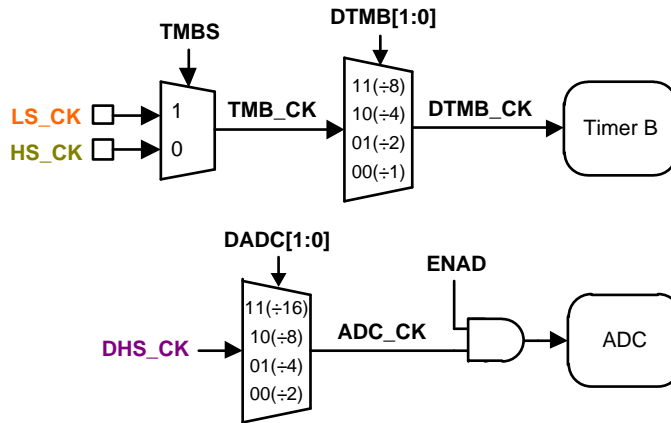


Figure 4-4 Clock System 方塊圖(三)

4.4. Reset

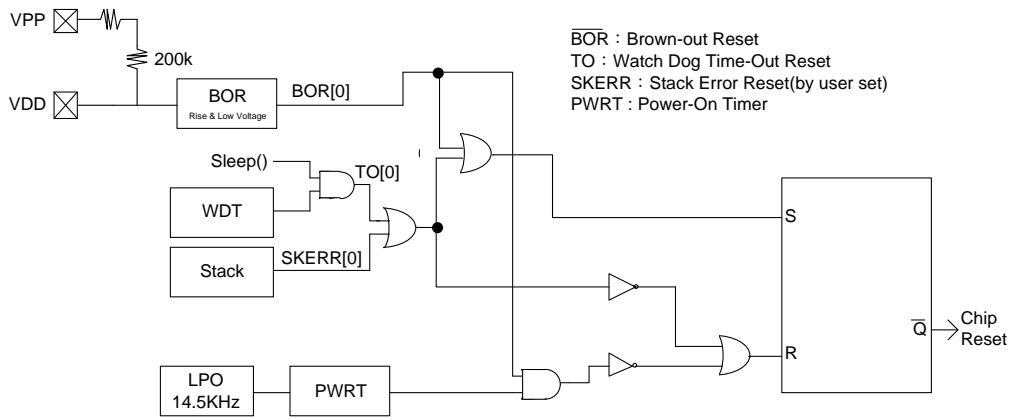


Figure 4-5 Reset 方塊圖

4.5. Power System

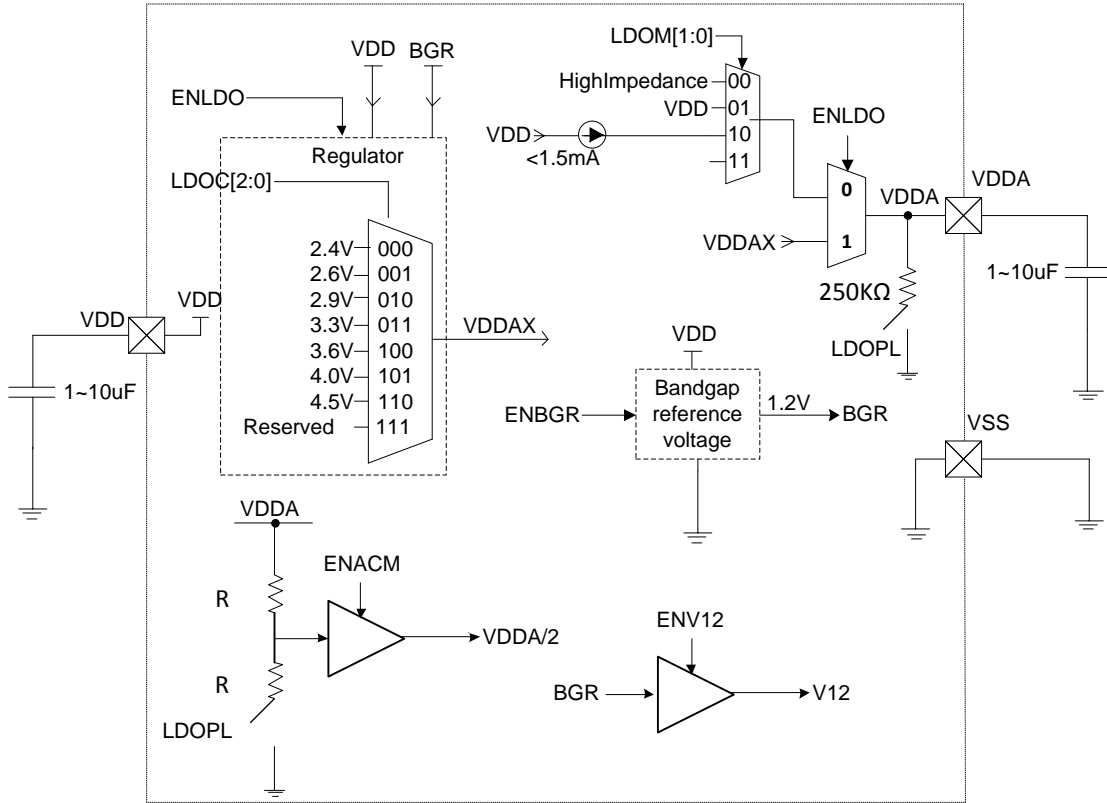


Figure 4-6 Power System 方塊圖

4.6. $\Sigma\Delta$ ADC Network

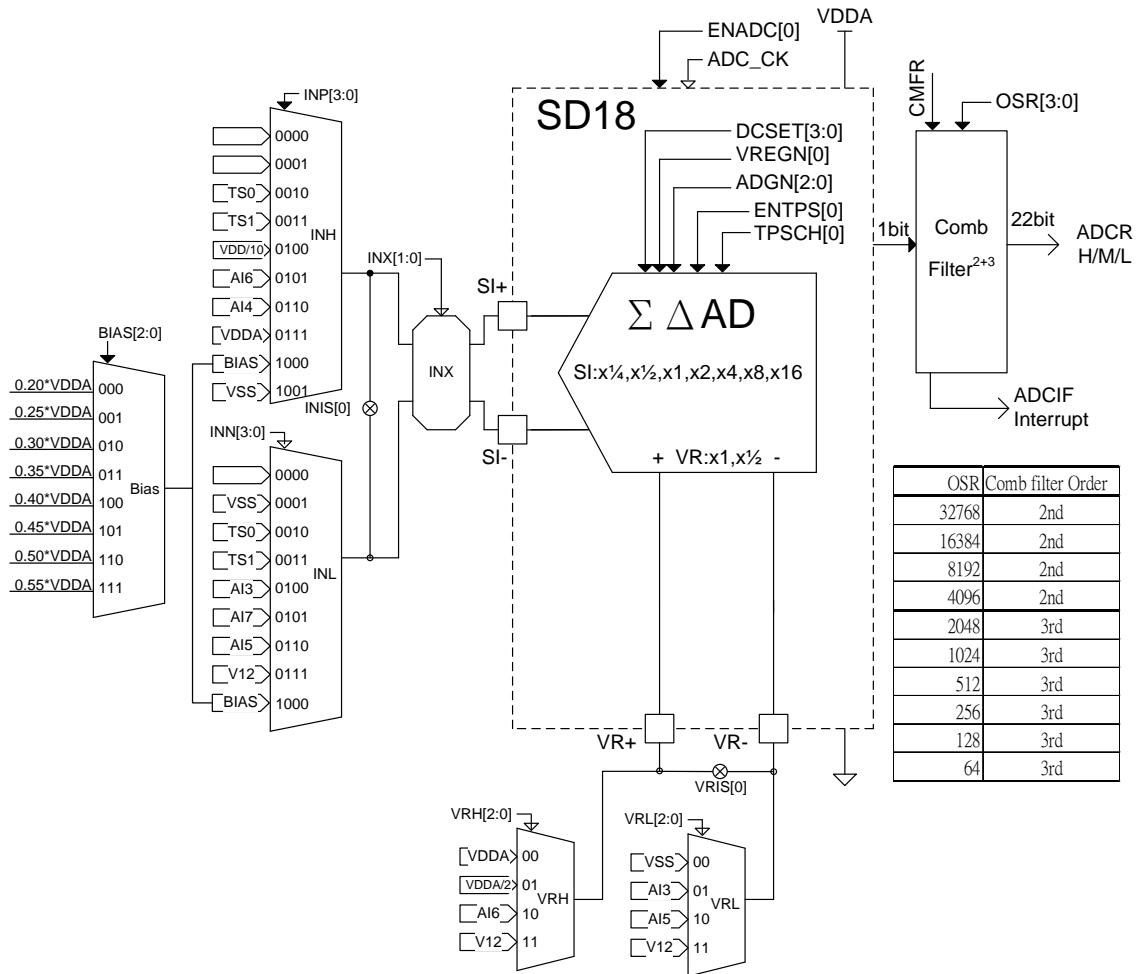


Figure 4-7 SD18 Network

4.7. GPIO System

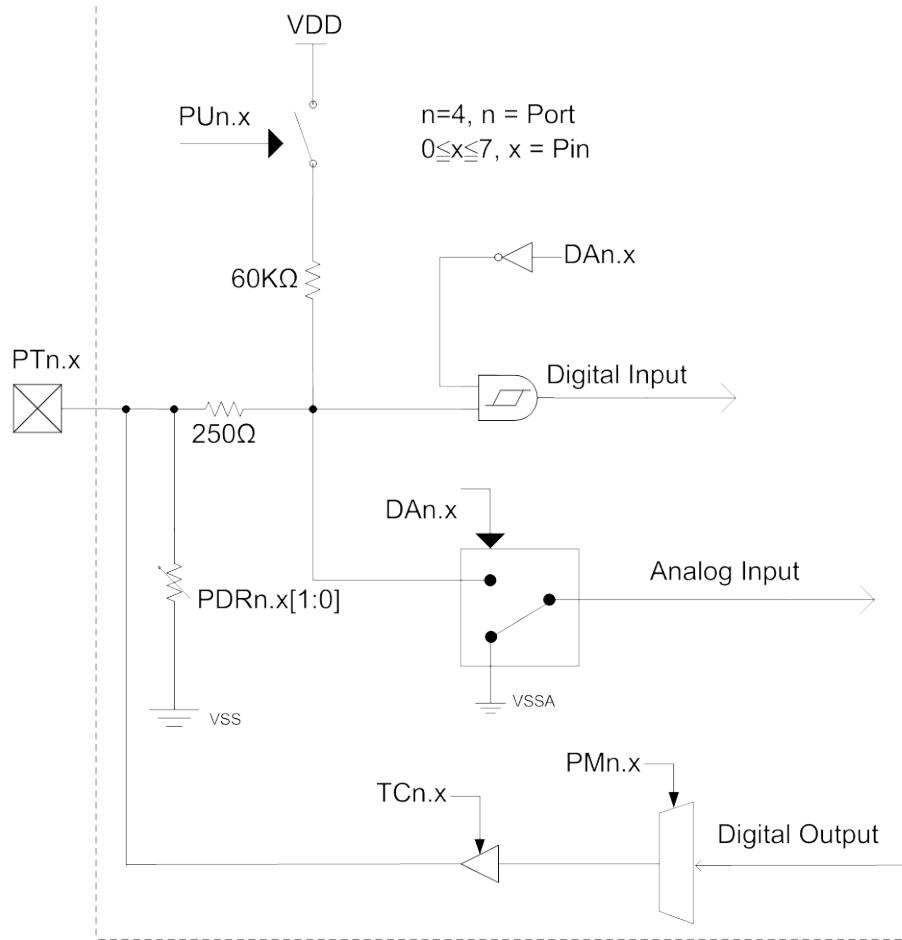


Figure 4-8 GPIO 方塊圖

4.8. Watch Dog System

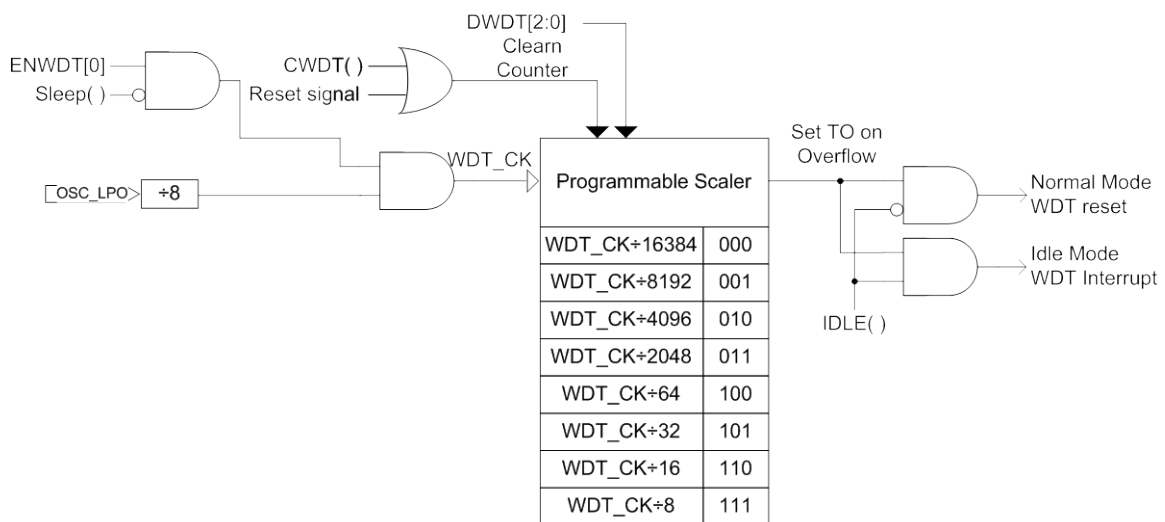


Figure 4-9 Watch Dog 方塊圖

4.11. EUART System

EUART TRANSMIT BLOCK DIAGRAM

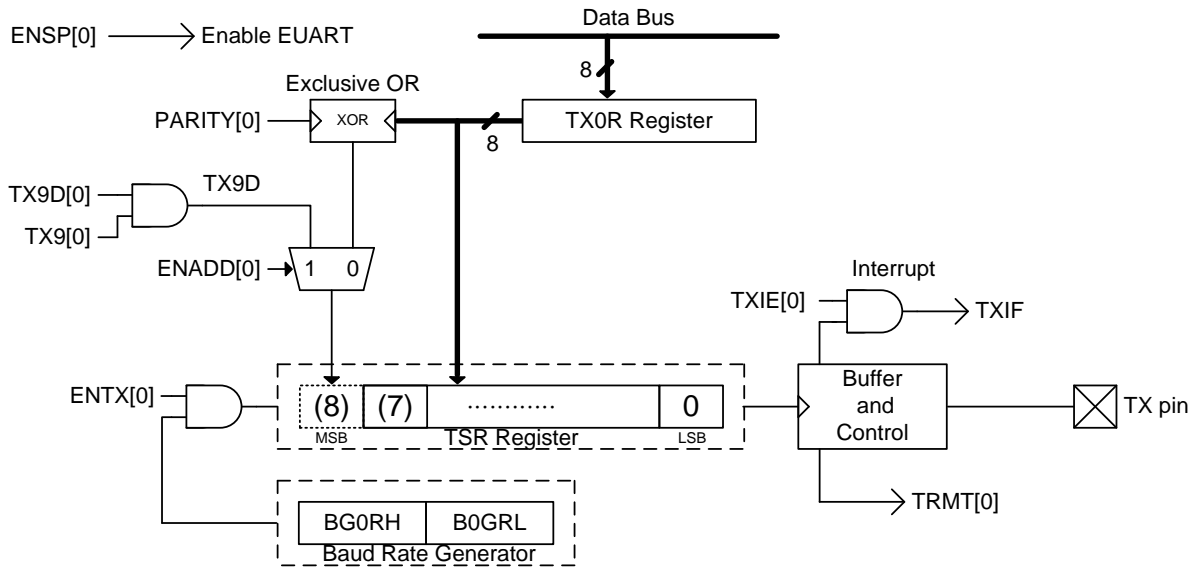
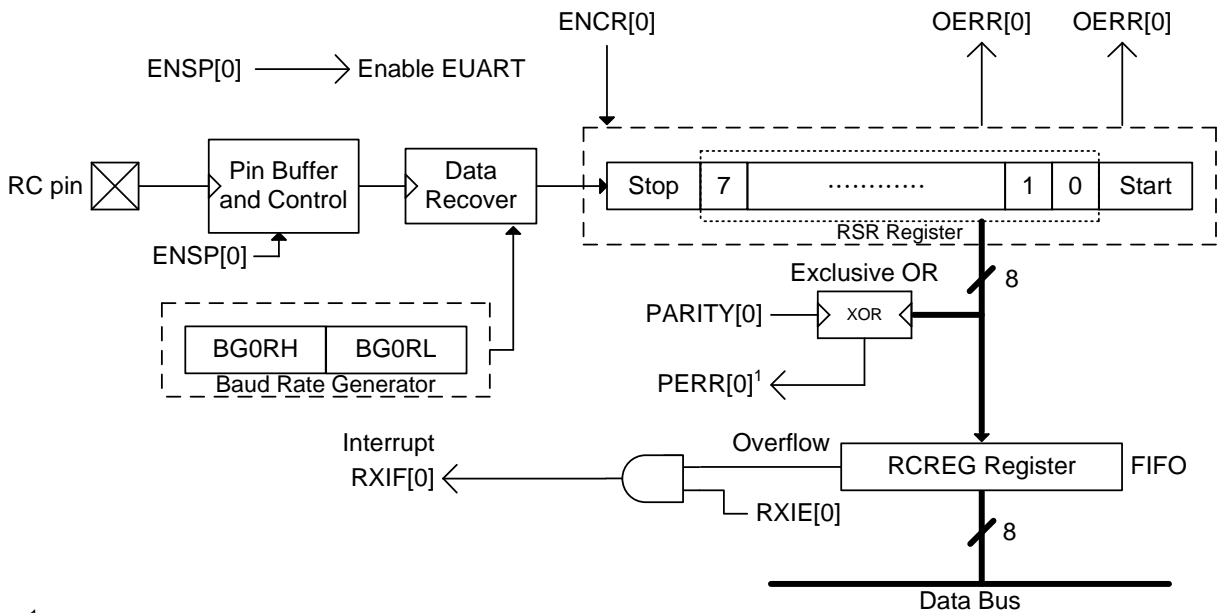


Figure 4-12 EUART 傳送方塊圖

EUART 8-BITS RECEIVE BLOCK DIAGRAM



¹Don't care PERR[0] state of 8-bits receive mode

Figure 4-13 EUART 8-bits 接收方塊圖

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5. 暫存器列表

"r" no use, "w" read/write, "w" write, "r" read, "r0" only read 0, "r1" only read 1, "w0" only write 0, "w1" only write 1
"\$" for event status, "-" unimplemented bit, "x" unknown, "u" unchanged, "d" depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W	
000h	INDF0	Contents of FSR0 to address data memoryvalue of FSR0 not changed								xxxx xxxx	uuuu uuuu	*****	
001h	POINC0	Contents of FSR0 to address data memoryvalue of FSR0 post-incremented								xxxx xxxx	uuuu uuuu	*****	
002h	PODEC0	Contents of FSR0 to address data memoryvalue of FSR0 post-decremented								xxxx xxxx	uuuu uuuu	*****	
003h	PRINC0	Contents of FSR0 to address data memoryvalue of FSR0 pre-incremented								xxxx xxxx	uuuu uuuu	*****	
004h	PLUSW0	Contents of FSR0 to address data memoryvalue of FSR0 offset by W								xxxx xxxx	uuuu uuuu	*****	
005h	INDF1	Contents of FSR1 to address data memoryvalue of FSR1 not changed								xxxx xxxx	uuuu uuuu	*****	
006h	POINC1	Contents of FSR1 to address data memoryvalue of FSR1 post-incremented								xxxx xxxx	uuuu uuuu	*****	
007h	PODEC1	Contents of FSR1 to address data memoryvalue of FSR1 post-decremented								xxxx xxxx	uuuu uuuu	*****	
008h	PRINC1	Contents of FSR1 to address data memoryvalue of FSR1 pre-incremented								xxxx xxxx	uuuu uuuu	*****	
009h	PLUSW1	Contents of FSR1 to address data memoryvalue of FSR1 offset by W								xxxx xxxx	uuuu uuuu	*****	
00Ah	INDF2	Contents of FSR2 to address data memoryvalue of FSR2 not changed								xxxx xxxx	uuuu uuuu	*****	
00Bh	POINC2	Contents of FSR2 to address data memoryvalue of FSR2 post-incremented								xxxx xxxx	uuuu uuuu	*****	
00Ch	PODEC2	Contents of FSR2 to address data memoryvalue of FSR2 post-decremented								xxxx xxxx	uuuu uuuu	*****	
00Dh	PRINC2	Contents of FSR2 to address data memoryvalue of FSR2 pre-incremented								xxxx xxxx	uuuu uuuu	*****	
00Eh	PLUSW2	Contents of FSR2 to address data memoryvalue of FSR2 offset by W								xxxx xxxx	uuuu uuuu	*****	
010h	FSR0L	Indirect Data Memory Address Pointer 0 Low Byte,FSR0[7:0]								xxxx xxxx	uuuu uuuu	*****	
012h	FSR1L	Indirect Data Memory Address Pointer 0 Low Byte,FSR1[7:0]								xxxx xxxx	uuuu uuuu	*****	
014h	FSR2L	Indirect Data Memory Address Pointer 0 Low Byte,FSR2[7:0]								xxxx xxxx	uuuu uuuu	*****	
016h	TOSH	-	-	-	-	TOS[11:8]			..xx xxxx	..uu uuuu	-,-,*****		
017h	TOSL	Top-of-Stack Low Byte (TOS<7:0>)								xxxx xxxx	uuuu uuuu	*****	
018h	SKCN	SKFL	SKUN	SKOV	-	-	SKPRT[2:0]		000. 0000	u\$. \$\$\$	rw 0,rw 0,rw 0,-,*,**		
01Ah	PCLATH	-	-	-	-	PC[11:8]			..00 0000	..00 0000	*****		
01Bh	PCLATL	PC Low Byte for PC<7:0>								0000 0000	0000 0000	*****	
01Dh	TBLPTRH	-	-	-	-	TBLPTR[11:8]			..xx xxxx	..uu uuuu	-,-,*****		
01Eh	TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)								xxxx xxxx	uuuu uuuu	*****	
01Fh	TBLDH	Program Memory Table Latch High Byte								xxxx xxxx	uuuu uuuu	*****	
020h	TBLDL	Program Memory Table Latch Low Byte								xxxx xxxx	uuuu uuuu	*****	
021h	PRODH	Product Register of Multiply High Byte								xxxx xxxx	uuuu uuuu	*****	
022h	PRODL	Product Register of Multiply Low Byte								xxxx xxxx	uuuu uuuu	*****	
023h	INTE0	GIE	TA1CIE	ADIE	WDTIE	TB1IE			E0IE	0000 0000	0uuu uuuu	*****	
024h	INTE1	TA1IE		TXIE	RCIE	I2CERIE	I2CIE			0000 0000	uuuu uuuu	*****	
026h	INTF0	-	TA1CIF	ADIF	WDTIF	TB1IF			E0IF	.000 0000	..uuu uuuu	*****	
027h	INTF1	TA1IF		TXIF	RCIF	I2CERIF	I2CIF			0000 0000	uuuu uuuu	***** r,r,*	
029h	WREG	Working Register								xxxx xxxx	uuuu uuuu	*****	
02Bh	MSTAT	-	-	-	C	DC	N	OV	Z	...x xxxx	...u uuuu	-,-,*****	
02Ch	PSTAT	POR	PD	TO	IDL	-	SKERR	-	-	\$000 \$00.	uu\$u u\$u.	rw0,rw0,rw0,rw0,rw0,rw0,-	
02Eh	BIECN	1	-	-	-	-	-	BIEWR	BIERD	1... \$000	1... \$uuu	r1,-,-, r1,*	
030h	BIEARL	-	-	BIE Address Register as BIEAL[5:0]						xxxx xxxx	uuuu uuuu	*****	
031h	BIERH	BIE High Byte Data Register								xxxx xxxx	uuuu uuuu	*****	
032h	BIERL	BIE Low Byte Data Register								xxxx xxxx	uuuu uuuu	*****	
033h	PWRCN	ENBGR	LDOC[2:0]		LDOM[0]	LDOM	ENLDO	CSFON		0000 0000	uuuu u00u	*****,w r0,w r0,*	
034h	OSCCN0	OSCS[1:0]		DHS[1:0]	DMS[2:0]			CUPS		0000 0000	uuuu uuuu	*****	
035h	OSCCN1	CCOPT	DADC[1:0]		DTMB[1:0]	TMBS		-		0000 0000	uuuu uuuu	*****,-	
036h	OSCCN2					HAOM[1:0]		ENHAO		0000 0001	uuuu uu01	*****	
037h	WDTCN					ENWDT	DWDWT[2:0]			0000 0000	uuuu \$000	-,* rw 1,*	
03Ah	AD1H	ADC1 conversion high byte data register								..00 0000	..uu uuuu	-,-,*****	
03Bh	AD1M	ADC1 conversion middle byte data register								0000 0000	uuuu uuuu	*****	
03Ch	AD1L	ADC1 conversion low byte data register								0000 0000	uuuu uuuu	*****	
03Dh	AD1CN0	ENAD1	-	-	OSR[3:0]			CMFR		000. 0000	uuu. uuuu	*****	
03Eh	AD1CN1	-	-	VREGN	ADGN[2:0]					xxxx xxxx	uuuu uuuu	*****	
03Fh	AD1CN2	-	BIAS[2:0]			DCSET[3:0]					xxxx xxxx	uuuu uuuu	*****
040h	AD1CN3	INF[3:0]			INN[3:0]					xxxx xxxx	uuuu uuuu	*****	
041h	AD1CN4	VRH[1:0]	VRL[1:0]		INX[1:0]	VRIS	INIS		0010 0000	uuuu uuuu	*****		
042h	AD1CN5	ENACM	ENV12	VCMIS	LDOPL	ENBS	-	ENTPS	TPSCH	0000 0000	uuuu uuuu	*****	
043h	CSFCN0	SKRST	HAOTR[6:0]								.1... ..	*****	
044h	TMA1CN	ENTMA1	TMACL1	TMAS1	DTMA1[2:0]		-	-	-	0000 00..	u0uu uu..	*,rw 1,*	
045h	TMA1R	TMA1 counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0,rw0,rw0,rw0	
046h	TMA1C	TMA1C counter Register								0000 0000	uuuu uuuu	rw0,rw0,rw0,rw0,rw0,rw0,rw0	

Table 5-1 資料記憶體列表

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Embedded 18-Bit ΣADC 8-Bit RISC-like Mixed Signal Microcontroller



"--no use,""read/write,"w"write,"r"read,"r0"only read 0,"r1"only read 1,"w0"only write 0,"w1"only write 1
"\$"for event status,"u"unimplemented bit,"x"unknown,"u"unchanged,"d"depends on condition

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ARST	IRST	R/W		
047h	AIXM1	APDR3[1:0]		-	-	-	-	-	-	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
048h	AIXM2	-	-	-	-	-	-	APDR4[1:0]		0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
04Eh	TB1Flag	-	-	PWM6A	PWM5A	PWM4A	PWM3A	PWM2A	PWM1A	..00 0000	..uu uuuu	-,-,r,r,r,r,r,r,f		
04Fh	TB1CN0	ENTB1	TB1M[1:0]		TB1RT[1:0]		TB1CL	-	-	0000 0000	uuuu u00u	*****,rw 1,* 1 1 1 1 1 1 1		
050h	TB1CN1	PA1IV	PWMA1[2:0]			PA0IV	PWMA0[2:0]			0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
051h	TB1RH	TimerB1 counter Register [15:8]								xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r		
052h	TB1RL	TimerB1 counter Register [7:0]								xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r		
053h	TB1COH	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1		
054h	TB1COL	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1		
055h	TB1C1H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1		
056h	TB1C1L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1		
057h	TB1C2H	TimerB1 counter Condition Register [15:8]								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1		
058h	TB1C2L	TimerB1 counter Condition Register [7:0]								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1		
059h	TCCN0	-	TC1S[1:0]		-	-	-	-	-	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
061h	CFG	-	-	-	-	-	GCRST	ENI2CT	ENI2C	0000 0000uuu	-,-,-,-,* 1 1 1 1 1 1 1		
062h	ACT	SLAVE	ADR10	SLAVE24	I2CER	START	STOP	I2CINT	ACK	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
063h	STA	MACTF	SACTF	RDBF	RWF	DF	ACKF	GCF	ARBF	0001 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
064h	CRG	CRG[7:0]								0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
065h	TOC	I2CTF	DI2C[2:0]			I2CTL[3:0]					0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1	
066h	RDB	RDB[7:1]							RDB[0]		xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1	
067h	TDB0	TDB0[7:1]							TDB0[0]		xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1	
068h	SID0	SID0[7:1],The corresponding address of the 7-bit mode								SID0V[0]	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1	
069h	UROCN	ENSP	ENTX	TX9	TX9D	PARITY	-	-	WUE	0000 0..0	uuuu u..u	***** 1 1 1 1 1 1 1		
06Ah	UR0STA	-	RC9D	PERR	FERR	OERR	RCIDL	TRMT	ABDOVF	..00 0010	..uuu uuuu	-,-,r,r,r,r,r,r,rw 0		
06Bh	BA0CN	-	-	-	-	ENCR	RC9	ENADD	ENABD 0000 uuuu	-,-,-,-,* 1 1 1 1 1 1 1		
06Ch	BG0RH	-	-	-	Baud Rate Generator Register High Byte						...x xxxx	...u uuuu	***** 1 1 1 1 1 1 1	
06Dh	BG0RL	Baud Rate Generator Register Low Byte								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1		
06Eh	TX0R	UART Transmit Register								xxxx xxxx	uuuu uuuu	***** 1 1 1 1 1 1 1		
06Fh	RCREG	UART Receive Register								xxxx xxxx	uuuu uuuu	r,r,r,r,r,r,r,r		
070h	PT1									PT1.0	xxxx xxxx	xxxx xxxx	***** 1 1 1 1 1 1 1	
074h	PT1M1	-	-	-	-	-	INTEG0[1:0]			0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
075h	PT4	PT4.7	PT4.6	PT4.5	PT4.4	PT4.3						xxxx xxxx	xxxx xxxx	***** 1 1 1 1 1 1 1
076h	TRISC4	TC4.7	TC4.6	TC4.5	TC4.4	TC4.3						0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
077h	PT4DA	DA4.7	DA4.6	DA4.5	DA4.4	DA4.3						0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
078h	PT4PU	PU4.7	PU4.6	PU4.5	PU4.4	PU4.3						0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1
079h	PT4PD1	PDR4.3[1:0]		-	-	-	-	-	-	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
07Ah	PT4PD2	PDR4.7[1:0]		PDR4.6[1:0]		PDR4.5[1:0]		PDR4.4[1:0]		0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
07Bh	PT4INT	INTG4.7	INTG4.6								0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1	
07Ch	PT4INTE	INTE4.7	INTE4.6								0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1	
07Dh	PT4INTF	INTF4.7	INTF4.6								0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1	
07Eh	PT4M2	-	PM4.7[0]	-	PM4.6[0]	-	-	-	-	0000 0000	uuuu uuuu	***** 1 1 1 1 1 1 1		
080h ~ 0FFh	SRAM as 128Byte									uuuu uuuu	uuuu uuuu	***** 1 1 1 1 1 1 1		

Table 5-2 資料記憶體列表(續)

HY15P41

Embedded 18-Bit Σ ADC
8-Bit RISC-like Mixed Signal Microcontroller



6. 電氣特性

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS}	-0.2 V to 6.0 V
Voltage applied to any pin	-0.2 V to $V_{DD} + 0.3$ V
Voltage applied to V_{PP} pin	-0.2 V to 8.75 V
Diode current at any device terminal	± 2 mA
Operating temperature range	-40°C to 85°C
Storage temperature, T_{stg} : (unprogrammed device)	-55°C to 150°C
(programmed device)	-40°C to 85°C
Total power dissipation.....	0.5w
Maximum output current sink by any port I/O pin.....	.25mA

6.1. Recommended operating conditions

$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{DD}	Digital Supply Voltage	All digital peripherals and CPU	2.2		5.5	V
V_{DDA}	Analog Supply Voltage	Analog peripherals	2.4		4.5	V
V_{SS}	Supply Voltage		0		0	

6.2. Internal RC Oscillator

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
HAO(2MHz)	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=00	-20%	2.0	+20%	MHz
HAO(4MHz)	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=01	-20%	4.0	+20%	MHz
HAO(8MHz)	High Speed Oscillator frequency	ENHAO[0]=1, HAOM[1:0]=11	-20%	8.0	+20%	MHz
LPO	Low Power Oscillator frequency	V_{DD} supply voltage be enable LPO	-20%	14.5	+20%	KHz

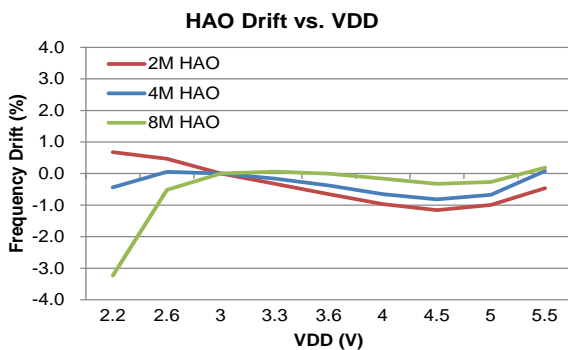


Figure 6.2-1 HAO vs. VDD

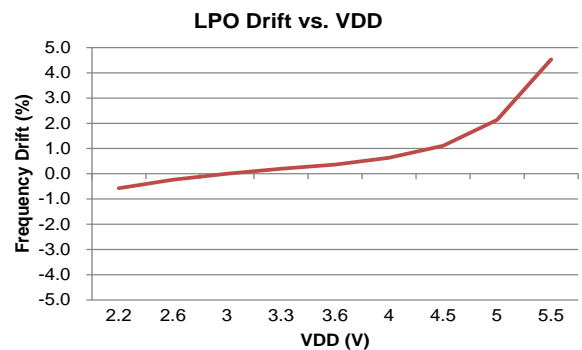


Figure 6.2-2 LPO vs. VDD

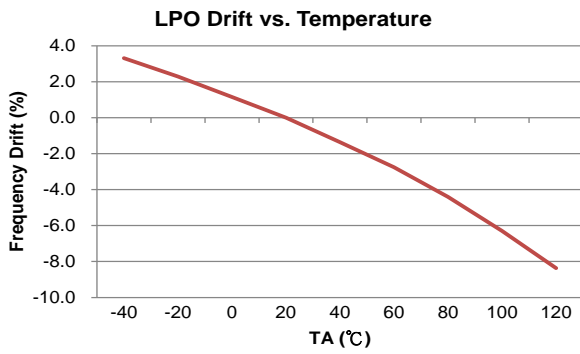


Figure 6.2-3 LPO vs. Temperature

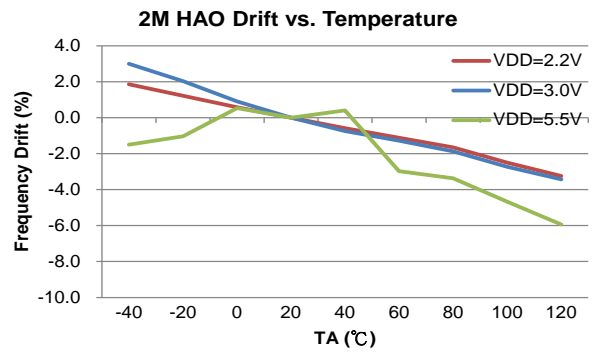


Figure 6.2-4 HAO(2.0MHz) vs. Temperature

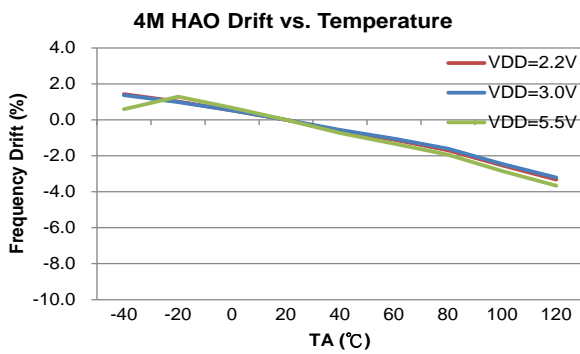


Figure 6.2-5 HAO(4.0MHz) vs. Temperature

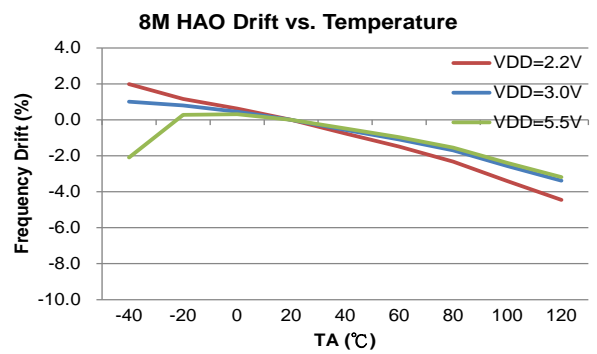


Figure 6.2-6 HAO(8.0MHz) vs. Temperature

6.3. Supply current into VDD excluding peripherals current

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, \text{OSC_LPO} = 14.5\text{KHz}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 8MHz, CPU_CK = 8MHz		600	1000	μA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 4MHz, CPU_CK = 4MHz		320	650	μA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		210	450	μA
I_{AM4}	Active mode 4	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		160	350	μA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO,		2	5	μA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		1.0	2.5	μA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.25	1.0	μA

$T_A = 25^\circ\text{C}, V_{DD} = 5.5\text{V}, \text{OSC_LPO} = 14.5\text{KHz}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_CY = off, OSC_HAO = 8MHz, CPU_CK = 8MHz		1200	1800	μA
I_{AM2}	Active mode 2	OSC_CY = off, OSC_HAO = 4MHz, CPU_CK = 4MHz		720	1200	μA
I_{AM3}	Active mode 3	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 2MHz		500	1000	μA
I_{AM4}	Active mode 4	OSC_CY = off, OSC_HAO = 2MHz, CPU_CK = 1MHz		400	800	μA
I_{LP1}	Low Power 1	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO,		4	10	μA
I_{LP2}	Low Power 2	OSC_CY = off, OSC_HAO = off, CPU_CK = LPO, Idle state		2.5	5	μA
I_{LP3}	Low Power 3	OSC_CY = off, OSC_HAO = off, CPU_CK = off, Sleep state		0.4	2	μA

OSC_HAO : Internal High Accuracy Oscillator frequency.

CPU_CK : CPU core work frequency.

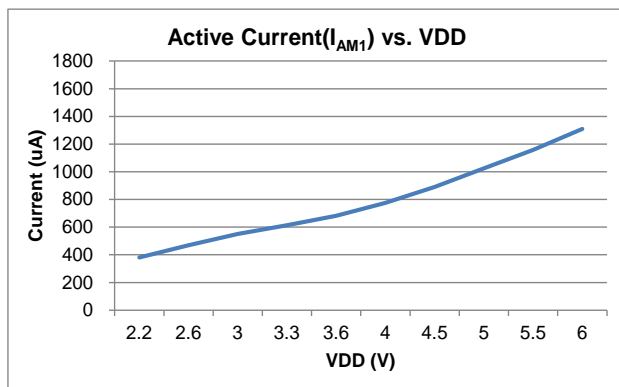


Figure 6.3-1 I_{AM1} vs. VDD

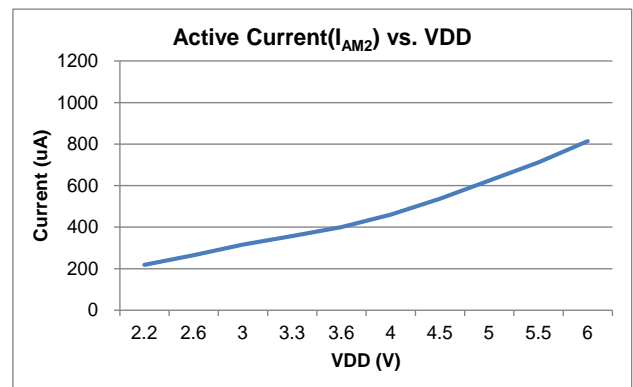


Figure 6.3-2 I_{AM2} vs. VDD

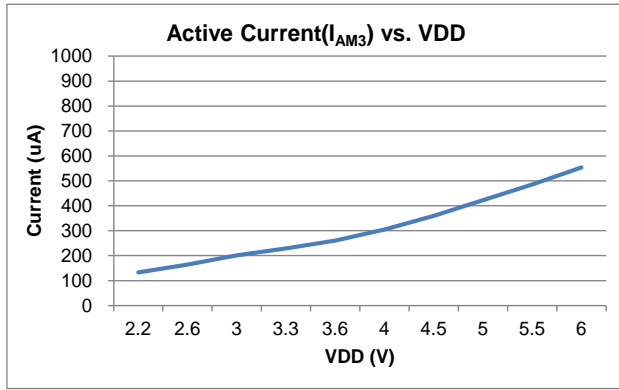


Figure 6.3-3 I_{AM3} vs. VDD

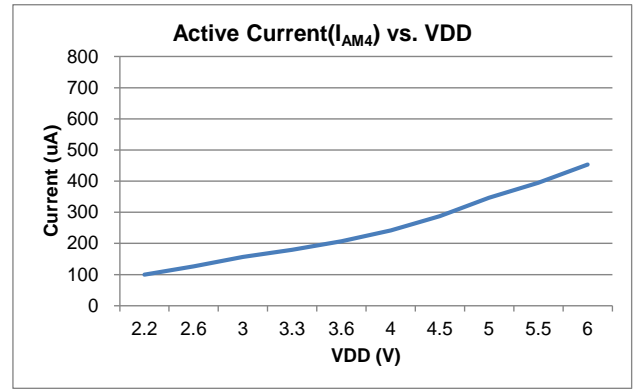


Figure 6.3-4 I_{AM4} vs. VDD

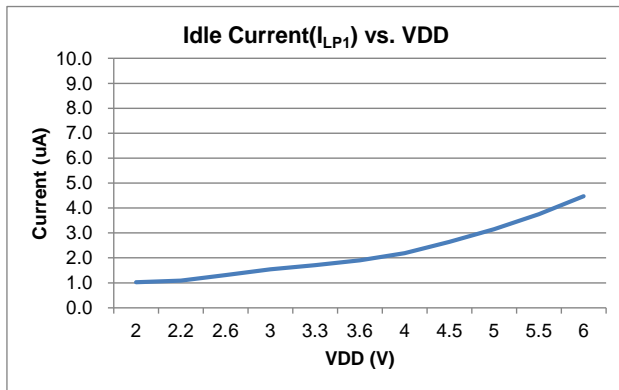


Figure 6.3-5 I_{LP1} vs. VDD

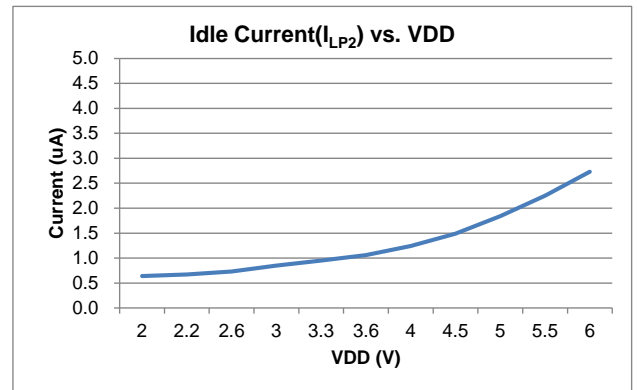


Figure 6.3-6 I_{LP2} vs. VDD

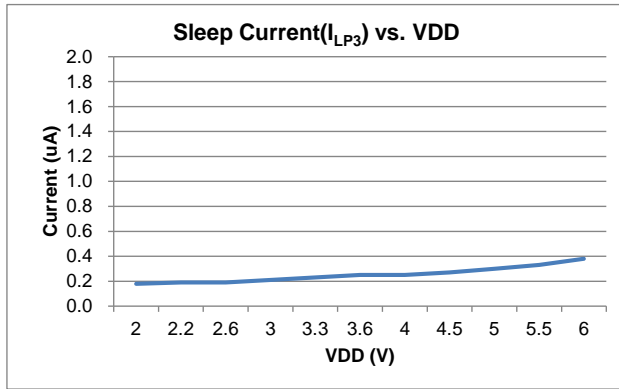


Figure 6.3-7 I_{LP3} vs. VDD

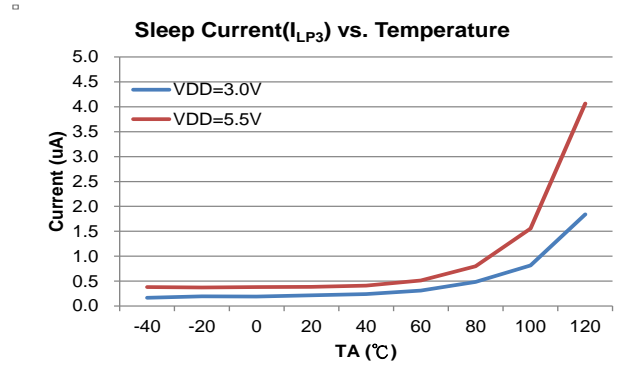


Figure 6.3-8 I_{LP3} vs. Temperature

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6.4. Port4

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
Input voltage and Schmitt trigger and leakage current and timing						
V_{IH}	High-Level input voltage		$0.7 \cdot V_{DD}$		V_{DD}	V
V_{IL}	Low-Level input voltage		V_{SS}		$0.3 \cdot V_{DD}$	
V_{hys}	Input Voltage hysteresis($V_{IH} - V_{IL}$)			0.8		V
I_{LKG}	Leakage Current				0.1	μA
R_{PU}	Port pull high resistance			60		$\text{k}\Omega$
R_{PD}	Port pull low resistance	PDR4.x/APDRX0 [1:0]=01		10		$\text{k}\Omega$
		PDR4.x/APDRX0 [1:0]=10		50		$\text{k}\Omega$
		PDR4.x/APDRX0 [1:0]=11		100		$\text{k}\Omega$
Output voltage and current						
V_{OH}	High-level output voltage	$V_{DD} \geq 3\text{V}, I_{OH} = 10\text{mA}$	$V_{DD} - 0.3$			V
		$V_{DD} < 3.0\text{V}, I_{OH} = 10\text{mA}$	$V_{DD} - 0.4$			
		$V_{DD} \geq 4\text{V}, I_{OH} = 15\text{mA}$	$V_{DD} - 0.4$			
V_{OL}	Low-level output voltage	$V_{DD} < 4\text{V}, I_{OL} = -10\text{mA}$			$V_{SS} + 0.3$	V
		$V_{DD} \geq 4\text{V}, I_{OL} = -15\text{mA}$			$V_{SS} + 0.4$	

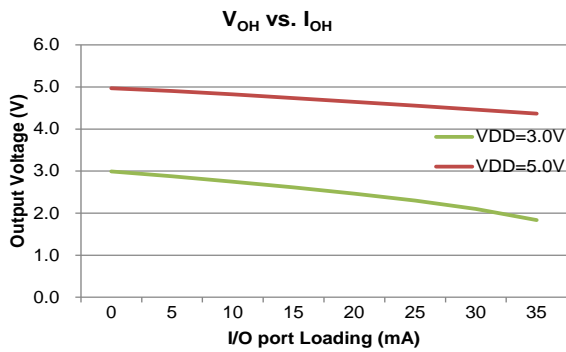


Figure 6.4-1 V_{OH} vs. I_{OH}

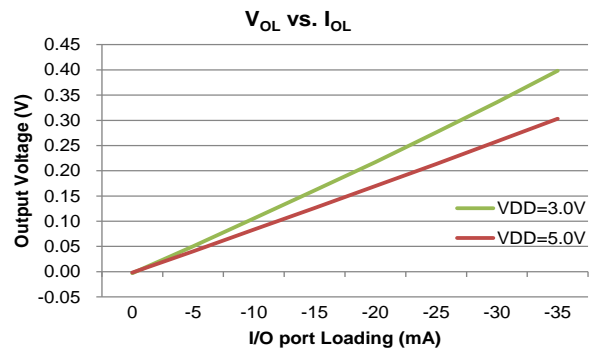


Figure 6.4-2 V_{OL} vs. I_{OL}

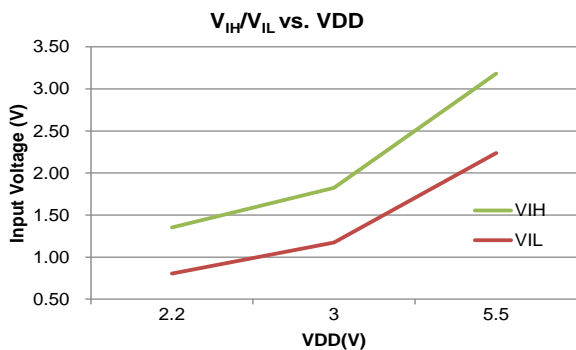


Figure 6.4-3 V_{IH}/V_{IL} vs. V_{DD}

6.5. Rest(Brownout)

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}		2			us
	V_{DD} Start Voltage to accepted reset internally (L→H), V_{HYS}		1.6	1.74	2.1	V
	V_{DD} Start Voltage to accepted reset internally (H→L), V_{LVR}		1.6	1.70	2.1	V
	Hysteresis, $V_{HYS-LVR}$		40			mV
BOR : Brownout Reset						

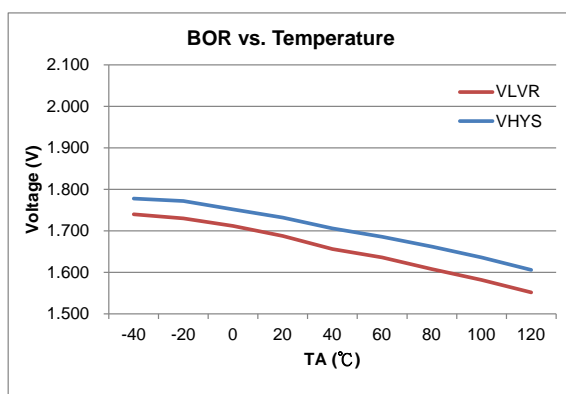


Figure 6.5-1 BOR vs. Temperature

6.6. Power System

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
VDDA	VDDA operation current, I_{VDDA}	$I_L = 0\text{mA}$	LDOC[2:0]=000b	20			μA
	Select VDDA output voltage	$I_L = 0.1\text{mA}$, $V_{DD} \geq V_{VDDA} + 0.25\text{V}$	LDOC [2:0]=000b	2.4		V	
			LDOC [2:0]=001b	2.6			
			LDOC [2:0]=010b	2.9			
			LDOC [2:0]=011b	3.3			
			LDOC [2:0]=100b	3.6			
			LDOC [2:0]=101b	4.0			
	LDOC [2:0]=110b	4.5					
Dropout voltage	$I_L = 10\text{mA}$	LDOC [2:0]=000b	250			mV	
Temperature drift	LDOC [2:0]=000b,	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$	50			ppm/ $^\circ\text{C}$	
V_{DD} Voltage drift	$I_L = 0.1\text{mA}$	$V_{DD} = 2.5\text{V} \sim 5.5\text{V}$	± 0.2			%/V	
ACM	ACM operation current, I_{ACM}	ENADC[0]=1b,	ENACM [0]=1b	50			μA
	Internal Analog Common Mode Voltage, $V_{ACM} = V_{VDDA}/2$		$I_L = 0\mu\text{A}$	$V_{VDDA}/2$			V
	Temperature drift	ENADC[0]=1b,	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$, ENACM [0]=1b	50			ppm/ $^\circ\text{C}$
V12	V12 operation current, I_{V12}	ENADC[0]=1b,	ENV12 [0]=1b	50			μA
	Internal Analog Common Mode Voltage, V_{12}		$I_L = 0\mu\text{A}$	1.2			V
	Temperature drift	ENADC[0]=1b,	$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$, ENV12 [0]=1b	50			ppm/ $^\circ\text{C}$

VDDA : Adjust Voltage Regulator
V12 : Internal Analog Common Mode Voltage (No output voltage)
ACM : Internal Analog Common Mode Voltage $V_{VDDA}/2$ (No voltage output)

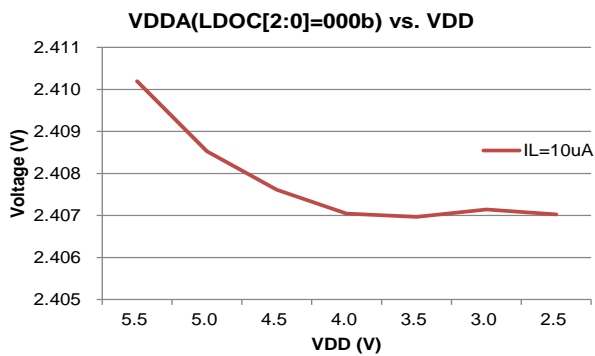


Figure 6.6-1 VDDA(000b) vs. VDD

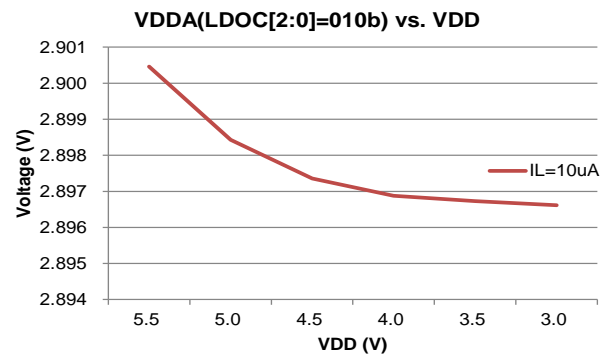


Figure 6.6-2 VDDA(010b) vs. VDD

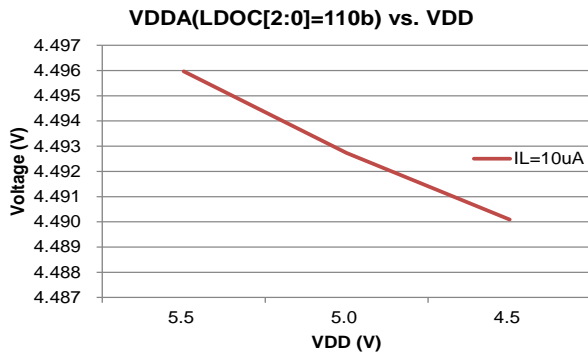


Figure 6.6-3 VDDA(110b) vs. VDD

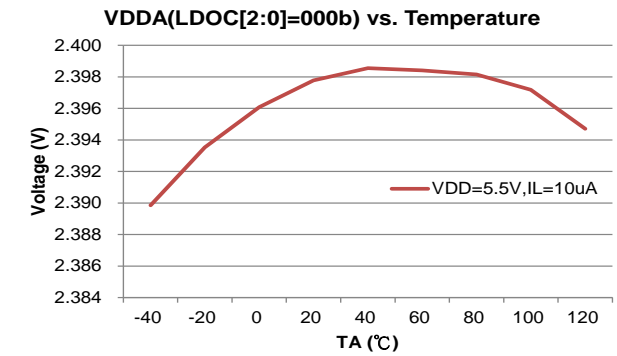


Figure 6.6-4 VDDA(000b) vs. Temperature

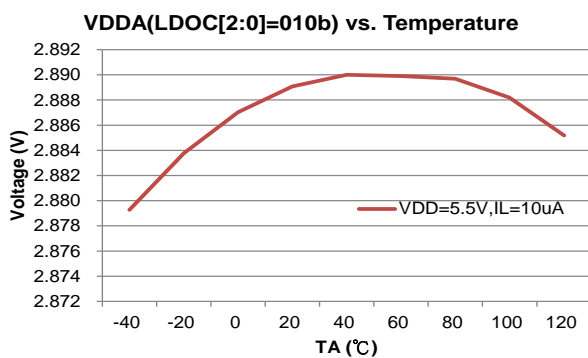


Figure 6.6-5 VDDA(010b) vs. Temperature

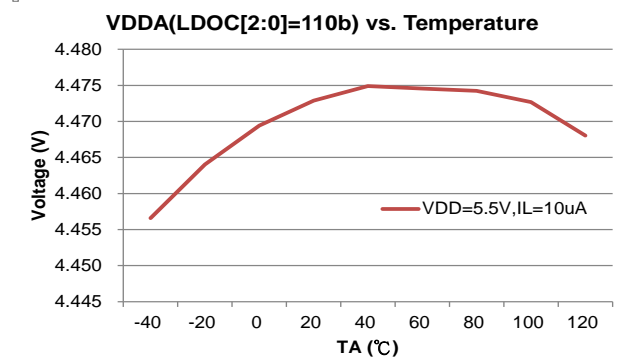


Figure 6.6-6 VDDA(110b) vs. Temperature

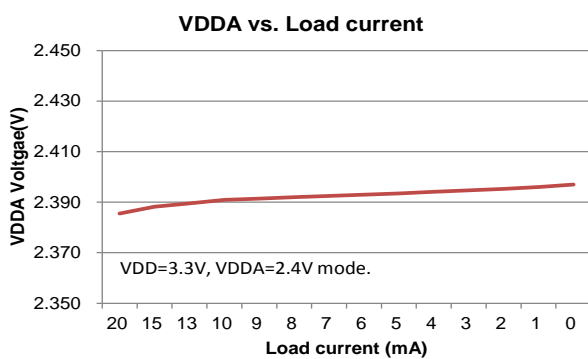


Figure 6.6-7 VDDA vs. Load current

6.7. $\Sigma\Delta$ ADC, Power Supply and recommended operating conditions

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{SD18}	Supply Voltage at VDDA	ENVDDA[0]=0		2.4		4.5	V
f_{SD18}	Modulator sample frequency, ADC_CK			125	500		KHz
	Over Sample Ratio, OSR			64		32768	
I_{SD18}	Operation supply current without PGA	ENADC[0]=1	GAIN =1, ADC_CK=500KHz		260		uA

6.7.1. $\Sigma\Delta$ ADC, performance

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA}=2.4\text{V}, V_{VR}=1.0\text{V}, \text{GAIN}=1, f_{SD18}=500\text{KHz}$, unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
INL	Integral Nonlinearity(INL)	$V_{DDA}=2.4\text{V}, V_{VR}=1.0\text{V}, \Delta\text{SI}=\pm 450\text{mV}$		± 0.01			%FSR
	No Missing Codes ³	ADC_CK=500KHz, OSR[3:0]=0001b		23			Bits
G_{SD18}	Temperature drift Gain 1~x16		$T_A = -40^\circ\text{C} \sim 85^\circ\text{C}$	10			ppm/ $^\circ\text{C}$
E_{OS}	Offset error of Full Scale Rang input voltage range with Chopper	$\Delta\text{AI}=0\text{V}$ $\Delta\text{VR}=0.9\text{V}$ DCSET[2:0]=<000> * ΔAI is external short	Gain=2	1			%FSR
	Offset temperature drift with chopper		GAIN=1	2			uV/ $^\circ\text{C}$
			GAIN=2	1			
			GAIN=4	0.5			
		GAIN=16	0.15				
CM_{SD18}	Common-mode rejection	$V_{CM}=0.7\text{V}$ to 1.7V, $V_{VR}=1.0\text{V}$	$V_{SI}=0\text{V},$ GAIN=1	90			dB
		$V_{CM}=0.7\text{V}$ to 1.7V, $V_{VR}=1.0\text{V},$	$V_{SI}=0\text{V},$ GAIN=16	75			
PSRR	DC power supply rejection	$V_{DDA}=3.0\text{V}, \Delta V_{DDA}=\pm 100\text{mV},$ $V_{VR}=1.0\text{V}, V_{SI}=V_{SI-}=1.2\text{V},$	GAIN=1	75			dB
			GAIN=16				

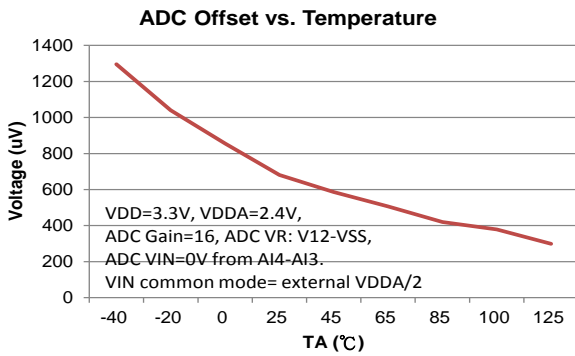


Figure 6.7-1 ADC Offset drift with Temperature

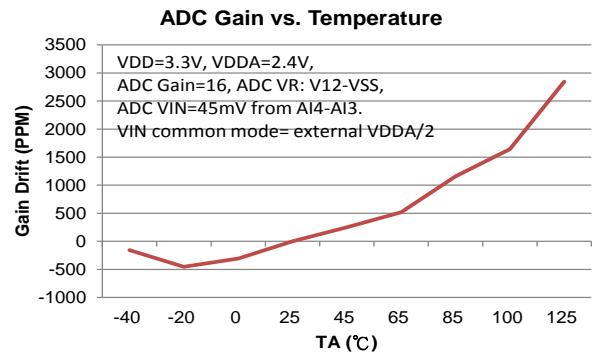


Figure 6.7-2 ADC Gain drift with Temperature

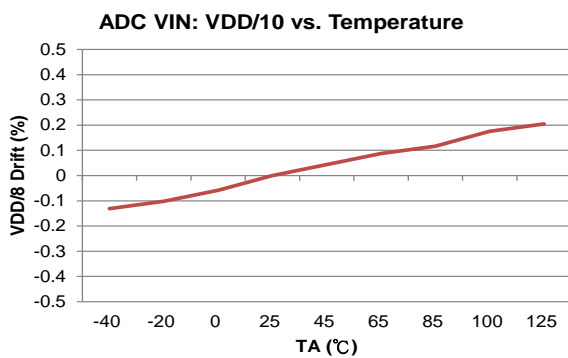


Figure 6.7-3 VDD/10 drift with Temperature

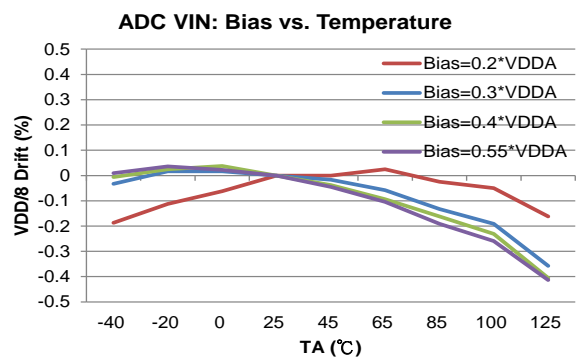


Figure 6.7-4 Bias drift with Temperature

6.7.2. $\Sigma\Delta$ ADC Noise Performance

$T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$, $V_{DDA}=2.4\text{V}$, unless otherwise noted

針對 $\Sigma\Delta$ ADC 提供了重要的輸入雜訊規格。Table6.7-2(a), Table6.7-2(b) 列出典型的雜訊規格表與 Gain, Output rate, 及單端最大輸入電壓等關係。測試條件設定在 AI3-AI4 外部輸入訊號短路，ADC 參考電壓源為使用內部 V12 及 VSS 當參考電壓源網路，等效參考電壓為 1.2V，取樣 1024 筆資料。

<i>ENOB(RMS) with OSR/GAIN at A/D Clock=500Khz, VDDA=2.4V, VREF=1.2V</i>												
Max. Vin(mV) =0.9*VREF ⁽¹⁾	OSR		64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)		7813	3906	1953	977	488	244	122	61	31	15
	Gain	ADGN										
±2160	0.25	= 0.25	13.6	15.8	16.2	16.6	17.1	17.6	17.9	18.4	18.7	18.2
±2160	0.5	= 0.5	13.4	15.7	16.3	16.7	17.1	17.6	18.0	18.5	18.6	18.2
±1080	1	= 1	13.7	15.7	16.2	16.7	17.2	17.5	17.9	18.3	18.7	18.5
±540	2	= 2	12.4	15.6	16.1	16.6	17.1	17.6	18.0	18.0	18.0	18.8
±270	4	= 4	12.6	15.5	16.0	16.5	17.0	17.5	17.6	17.7	18.3	18.7
±135	8	= 8	13.5	15.3	15.8	16.3	16.7	17.1	17.4	18.0	18.4	18.4
±68	16	= 16	11.7	15.0	15.5	16.0	16.4	16.8	17.2	17.9	18.4	18.7

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 6.7-2(a) ADC ENOB Table

<i>RMS Noise(uV) with OSR/GAIN at A/D Clock=500Khz, VDDA=2.4V, VREF=1.2V</i>												
Max. Vin(mV) =0.9*VREF ⁽¹⁾	OSR		64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)		7813	3906	1953	977	488	244	122	61	31	15
	Gain	ADGN										
±2160	0.25	= 0.25	764.77	173.20	130.68	95.36	69.10	47.20	40.37	28.33	22.78	32.07
±2160	0.5	= 0.5	443.87	92.50	61.54	44.77	34.33	24.33	17.85	13.45	12.48	15.83
±1080	1	= 1	181.43	45.93	31.25	23.10	16.54	12.83	9.56	7.24	5.62	6.47
±540	2	= 2	227.93	24.03	16.91	12.11	8.72	6.19	4.66	4.56	4.53	2.65
±270	4	= 4	99.24	13.10	9.27	6.65	4.73	3.35	2.93	2.85	1.86	1.43
±135	8	= 8	25.56	7.30	5.43	3.82	2.80	2.11	1.70	1.14	0.87	0.86
±68	16	= 16	44.04	4.52	3.15	2.33	1.76	1.32	1.03	0.64	0.44	0.36

Table 6.7-2(b) ADC RMS Noise Table

另外針對 $V_{DD}=V_{DDA}=5\text{V}$ 的高壓情況下， $\Sigma\Delta$ ADC 提供了重要的輸入雜訊規格。Table6.7-2(c), Table6.7-2(d) 列出典型的雜訊規格表與 Gain, Output rate, 及單端最大輸入電壓等關係。測試條件設定在 AI3-AI4 外部輸入訊號短路，ADC 參考電壓源為使用內部 $V_{DDA}/2$ 及 VSS 當參考電壓源網路，等效參考電壓為 2.5V，取樣 1024 筆資料。

<i>ENOB(RMS) with OSR/GAIN at VDD=VDDA=5.0V, A/D Clock=500Khz, VR=VDDA/2-VSS</i>											
Max. Vin(mV) =0.9*VREF ⁽¹⁾	OSR	64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)	7813	3906	1953	977	488	244	122	61	31	15
	GAIN										
±9000	1/4	14.4	15.6	16.1	16.7	17.0	17.6	18.0	18.6	19.1	19.5
±4500	1/2	14.1	15.8	16.3	16.9	17.4	17.8	18.2	18.7	19.3	19.7
±2250	1	13.8	15.7	16.2	16.7	17.1	17.7	18.1	18.5	19.0	19.5
±1125	2	14.4	15.6	16.4	16.8	17.3	17.9	18.2	18.7	19.2	19.6
±562.5	4	13.0	15.6	16.3	16.7	17.1	17.7	18.1	18.6	19.1	19.5
±281.25	8	14.5	15.5	16.1	16.6	17.1	17.5	17.9	18.4	18.8	19.3
±140.625	16	11.7	15.5	16.1	16.6	17.0	17.3	17.6	18.4	18.8	19.3

Table 6.7-2(c) ADC ENOB Table

<i>RMS Noise(μV) with OSR/GAIN at VDD=VDDA=5.0V, A/D Clock=500Khz, VR=VDDA/2-VSS</i>											
Max. Vin(mV) =0.9*VREF (1)	OSR	64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)	7813	3906	1953	977	488	244	122	61	31	15
	GAIN										
± 9000	1/4	960.2	407.4	278.9	192.6	148.2	99.9	76.4	51.9	36.4	27.5
± 4500	1/2	590.3	178.7	124.1	80.1	58.8	44.4	34.2	24.3	15.7	12.1
± 2250	1	344.9	93.0	64.5	48.0	35.0	24.1	17.5	13.8	9.8	6.8
± 1125	2	118.9	49.2	29.8	22.5	15.8	10.2	8.5	5.7	4.1	3.2
± 562.5	4	155.7	25.5	15.8	11.8	8.9	5.8	4.5	3.1	2.3	1.6
± 281.25	8	26.8	13.2	8.8	6.5	4.4	3.3	2.5	1.8	1.3	1.0
± 140.625	16	97.0	6.7	4.6	3.3	2.5	1.9	1.5	0.9	0.7	0.5

Table 6.7-2(d) ADC RMS Noise Table

The RMS noise are referred to the input. The Effective Number of Bits (ENOB(RMS Bit)) is defined as:

$$\text{ENOB(RMS)} = \frac{\ln\left(\frac{\text{FSR}}{\text{RMS Noise}}\right)}{\ln(2)}$$

$$\text{RMS Noise} = \frac{\left(2 \times \text{VREF} \times \sqrt{\sum_{k=1}^{1024} (\text{ADO}[k] - \text{Average})^2}\right)}{2^{23}}$$

Where FSR (Full - Scale Range) = $2 \times \text{VREF}/\text{Gain}$.

$$\text{Average} = \frac{\sum_{k=1}^{1024} (\text{ADO}[k])}{1024}$$

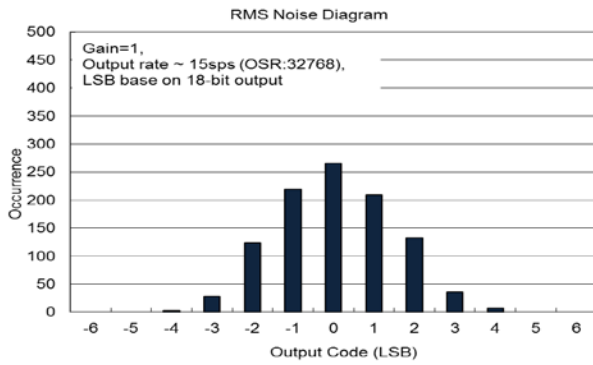


Figure 6.7-5 RMS Noise Diagram

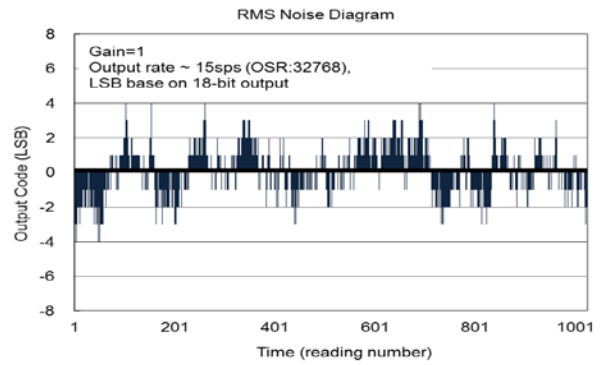


Figure 6.7-6 Output Code Diagram

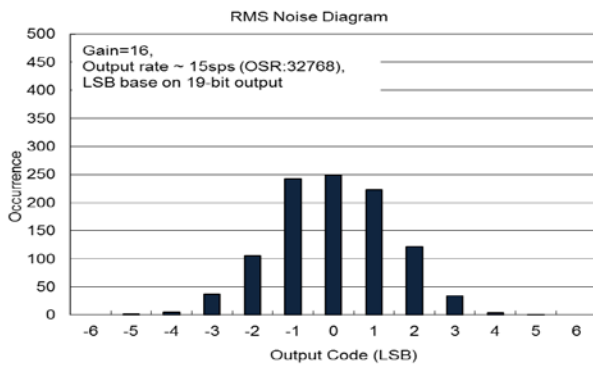


Figure 6.7-7 RMS Noise Diagram

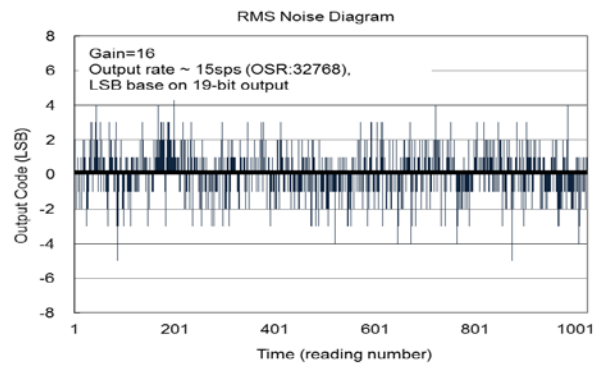


Figure 6.7-8 Output Code Diagram

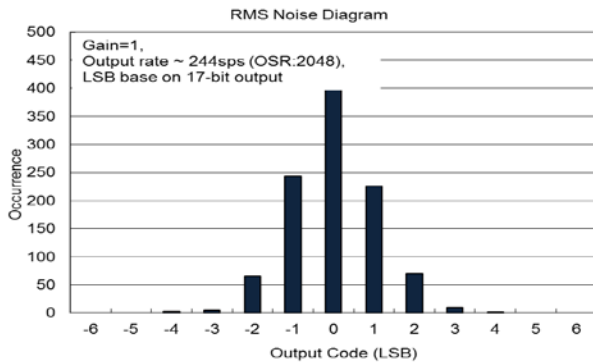


Figure 6.7-9 RMS Noise Diagram

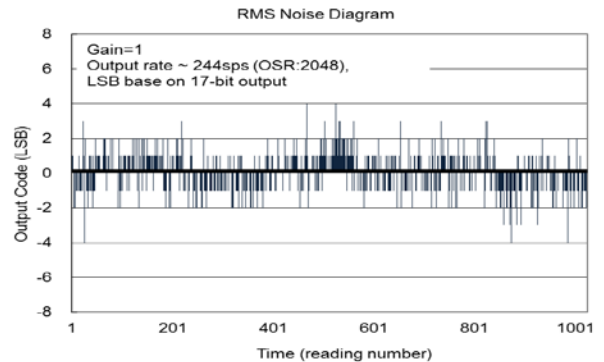


Figure 6.7-10 Output Code Diagram

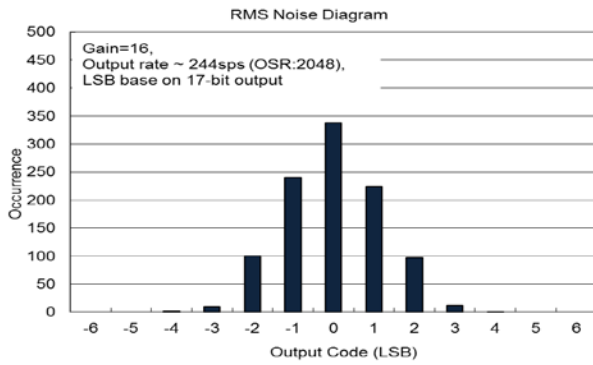


Figure 6.7-11 RMS Noise Diagram

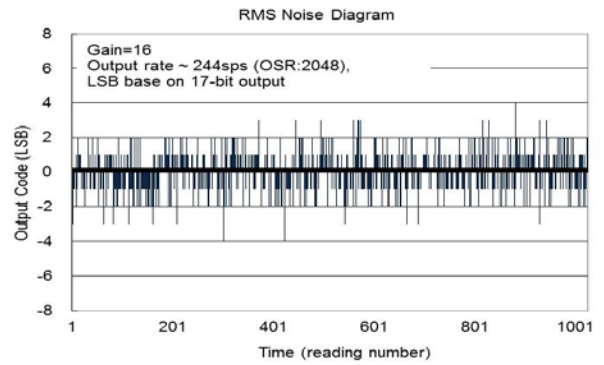


Figure 6.7-12 Output Code Diagram

6.7.3. $\Sigma \Delta$ ADC, Temperature Sensor

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}, V_{DDA} = 2.4\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
TC _S	Sensor temperature drift			173		uV/°C
KT	Absolute Temperature Scale 0°K			-284		°C
TC _{ERR}	One point calibrate error temperature	Calibration at 25°C of -40°C ~85°C		±2		°C

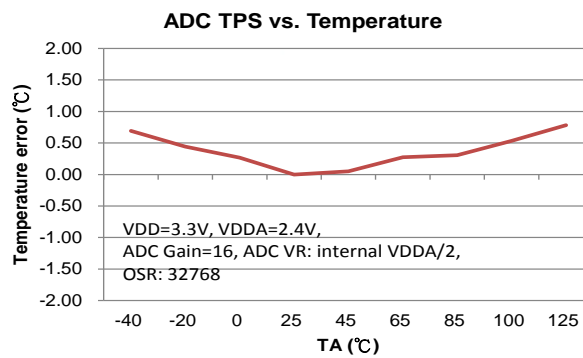


Figure 6.7-13 ADC Temperature Error

6.8. Build-In EPROM(BIE)

$T_A = 25^\circ\text{C}, V_{DD} = 3.0\text{V}$, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
T_O	Operation temperature range		0	25	40	$^\circ\text{C}$
V_{DD}	Operation supply Voltage		2.75		5.5	V
V_{BIE}	Supply Voltage			8.5	8.75	V
I_{BIE}	Operation supply current			5		mA
V_{SS}	Supply Voltage			0		V

When connecting to the external V_{BIE} power source to program the BIE block, users can use the instruction to program the words one by one into the BIE block.

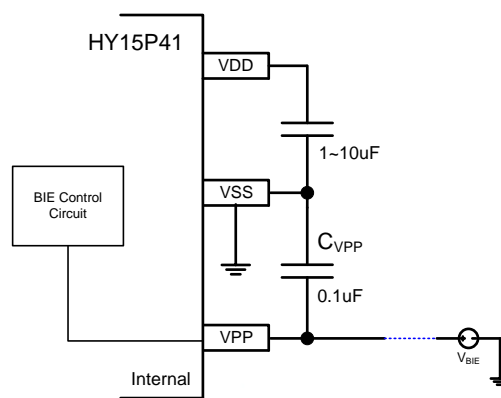


Figure 6-8 BIE typical application 方塊圖

7. 訂貨資訊

下單品名 ¹	封裝型式	引腳數	封裝型式		程式碼 編號 ²	出貨包裝形式	個裝數量	材料組成	MSL ³
			A	S					
HY15P41-AS12	DFN	12	A	S12	000	Tape & Reel	500	Green ⁴	MSL-3
HY15P41-S016	SOP	16	S	016	000	Tube	50	Green ⁴	MSL-3
HY15P41-S016	SOP	16	S	016	000	Tape & Reel	2500	Green ⁴	MSL-3
HY15P41-S008	SOP	8	S	008	000	Tube	100	Green ⁴	MSL-3
HY15P41-S008	SOP	8	S	008	000	Tape & Reel	2500	Green ⁴	MSL-3

¹ 產品名稱 – 封裝型式描述方式 – 程式碼編號 (空白片 / 標準品 / 代客燒錄碼)

例如：您的代客燒錄服務申請的程式碼編號為 007，且需要的產品是 SOP16 出貨。
則下單品名為 HY15P41-S016-007

例如：您的需求是不帶程式碼的空白片且需要的產品是 SOP16 出貨。則下單品名為 HY15P41-S016

例如：您的代客燒錄服務申請的程式碼編號為 008，而需求的產品是封裝片 SOP8 出貨，則下單品名為 HY15P41-S008-008，且需以 Tape & Reel 出貨，則除下單品名外，請特別註明出貨包裝形式為 Tape & Reel

² 程式碼編號

“001”~“999” 為標準品或代客燒錄申請的程式碼編號，而空白晶片不帶此碼。

³ MSL:

濕度敏感性等級係依據 IPC/JEDEC J-STD-020 的規範加以試驗分級，並參考 IPC/JEDEC J-STD-033 的標準處理、包裝、運輸與使用。

⁴ Green (RoHS & no Cl/Br):

HYCON 產品皆為 Green Product，符合 RoHS 指令以及無鹵素規定(Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)

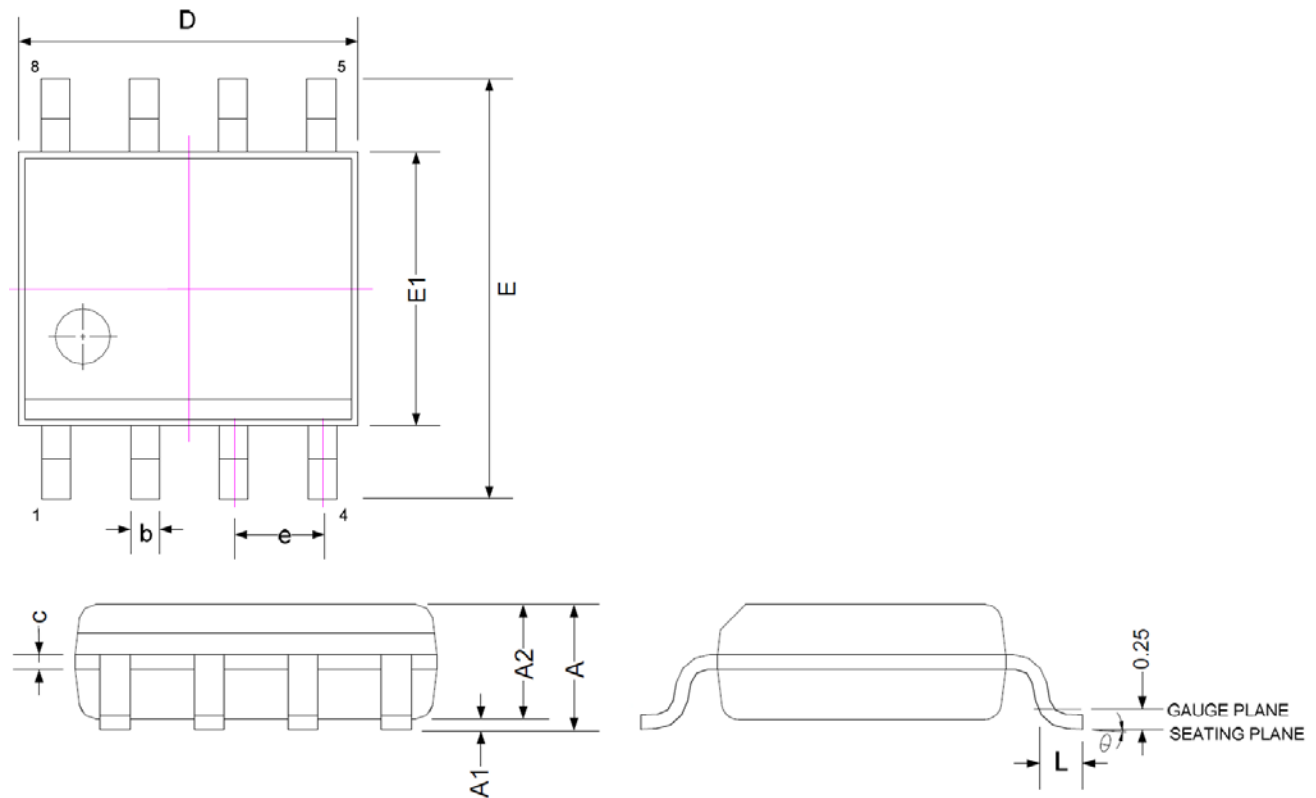
HY15P41

Embedded 18-Bit $\Sigma\Delta$ ADC
8-Bit RISC-like Mixed Signal Microcontroller

8. 封裝型式資訊

8.1. SOP8(S008)

8.1.1. Package Dimensions



SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.10	-	0.25
D	4.90 BSC		
E1	3.90 BSC		
E	6.00 BSC		
L	0.40	-	1.27
e	1.27 BSC		
θ°	0	-	8

Note:

1. All dimensions refer to JEDEC OUTLINE MS-012.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

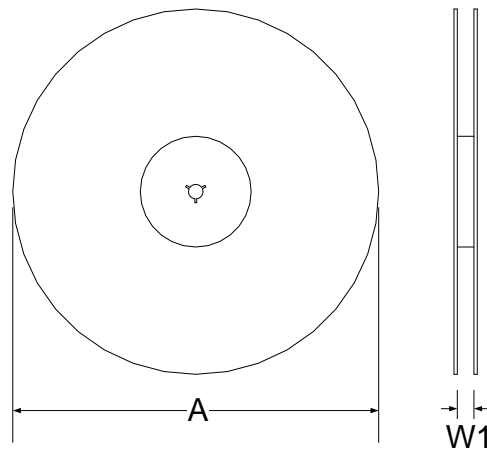
HY15P41

Embedded 18-Bit $\Sigma\Delta$ ADC
8-Bit RISC-like Mixed Signal Microcontroller

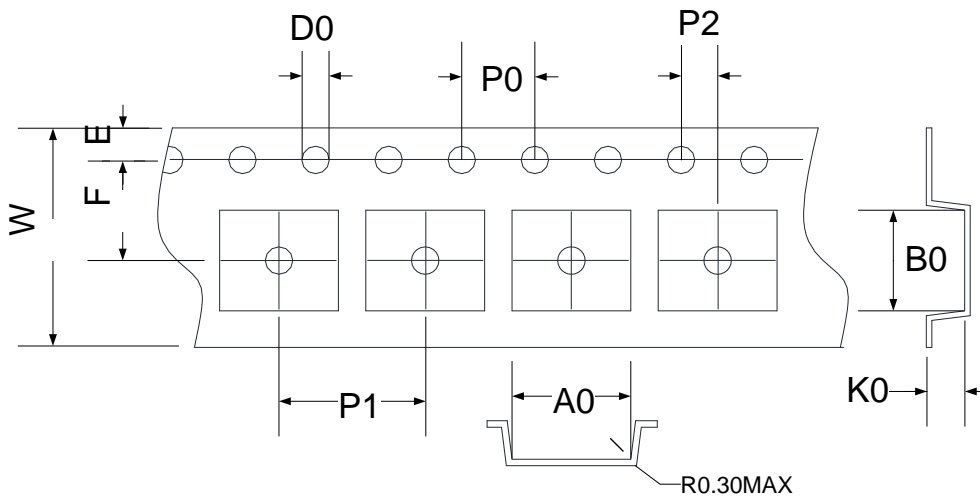
8.1.3. Tape & Reel Information

8.1.3.1. Reel Dimensions –Type1

Unit : mm



8.1.3.2. Carrier Tape Dimensions

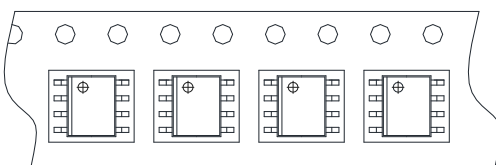


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions										
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W	
Spec.	330	12.5	6.90	5.40	2.00	4.00	8.00	2.00	1.75	5.50	1.50	12.00	
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ± 0.20 mm.

Unit : mm

8.1.3.3. Pin1 direction



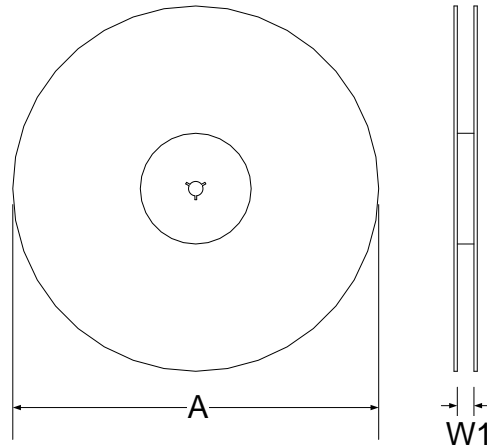
HY15P41

Embedded 18-Bit $\Sigma\Delta$ ADC
8-Bit RISC-like Mixed Signal Microcontroller

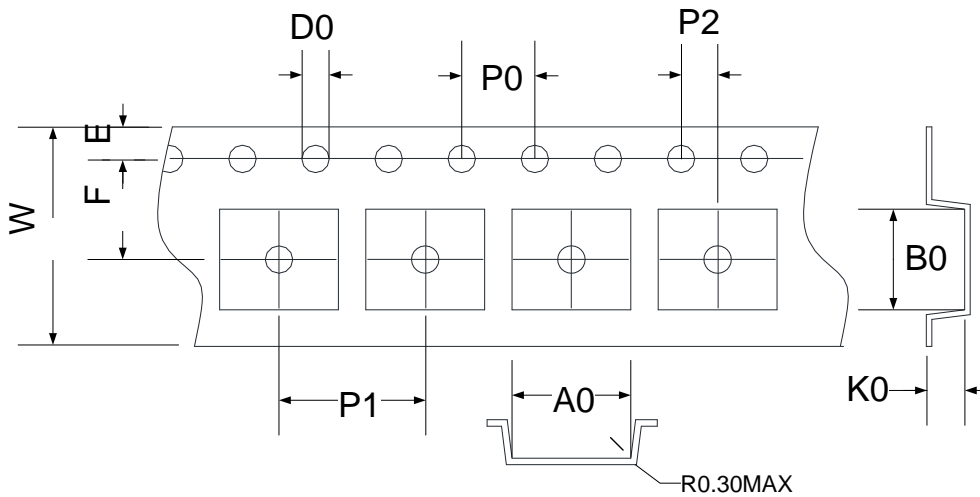


8.1.3.4. Reel Dimensions –Type2

Unit : mm



8.1.3.5. Carrier Tape Dimensions

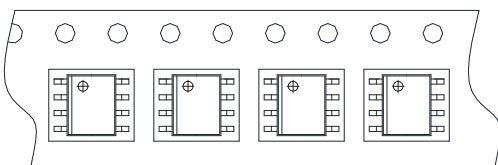


SYMBOLS	Reel Dimensions		Carrier Tape Dimensions										
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W	
Spec.	330	12.5	6.50	5.20	2.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00	
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0	±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ± 0.20 mm.

Unit : mm

8.1.3.6. Pin1 direction

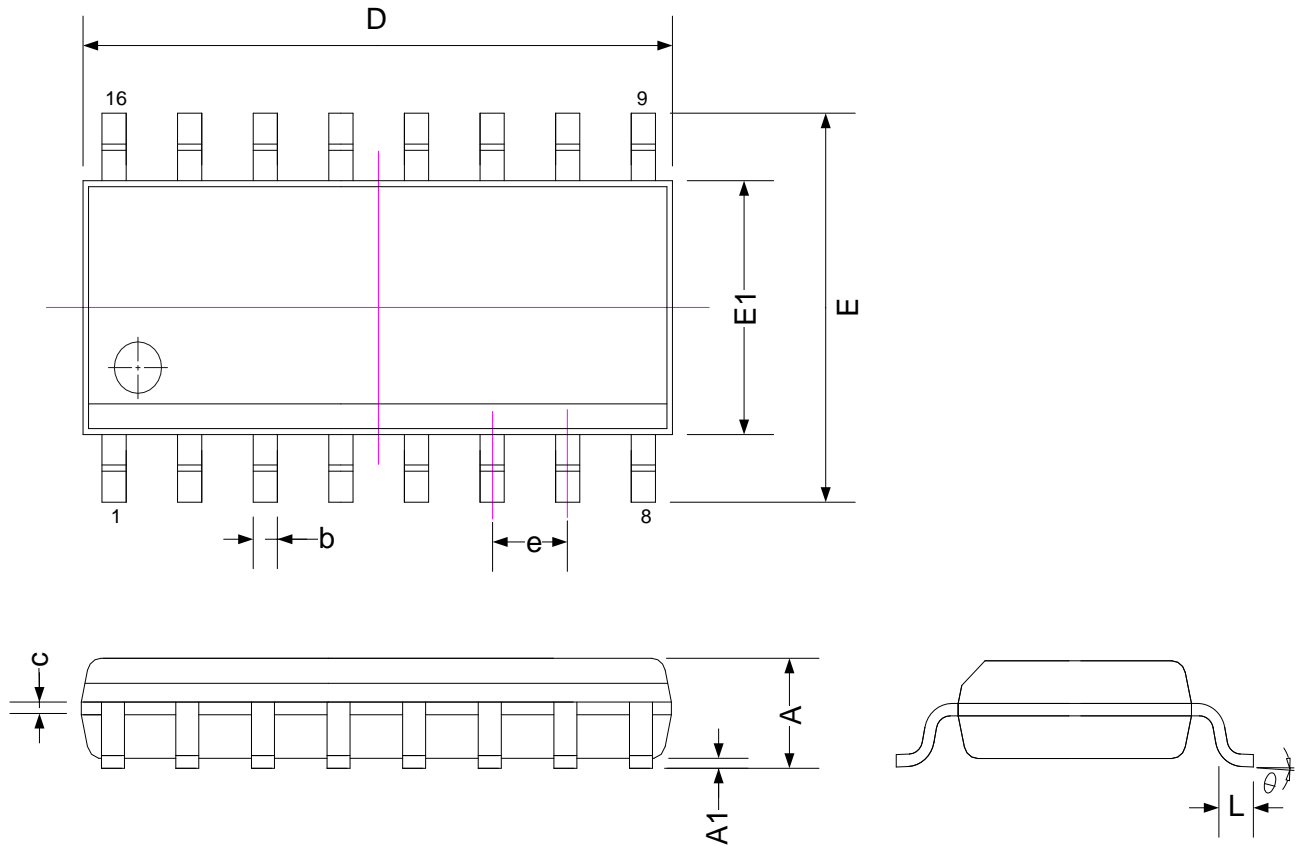


HY15P41

Embedded 18-Bit $\Sigma\Delta$ ADC
8-Bit RISC-like Mixed Signal Microcontroller

8.2. SOP16(S016)

8.2.1. Package Dimensions



SYMBOLS	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
b	0.31	-	0.51
c	0.10	-	0.25
D	9.90 BASIC		
E1	3.90 BASIC		
E	6.00 BASIC		
L	0.40	-	1.27
e	1.27 BASIC		
θ	0	-	8

Note :

1. All dimensions refer to JEDEC OUTLINE MS-012.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

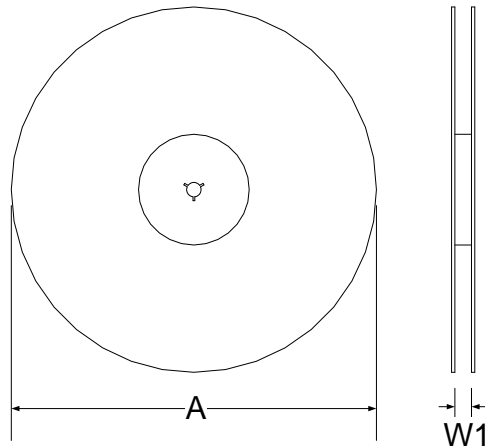
HY15P41

Embedded 18-Bit $\Sigma\Delta$ ADC
8-Bit RISC-like Mixed Signal Microcontroller

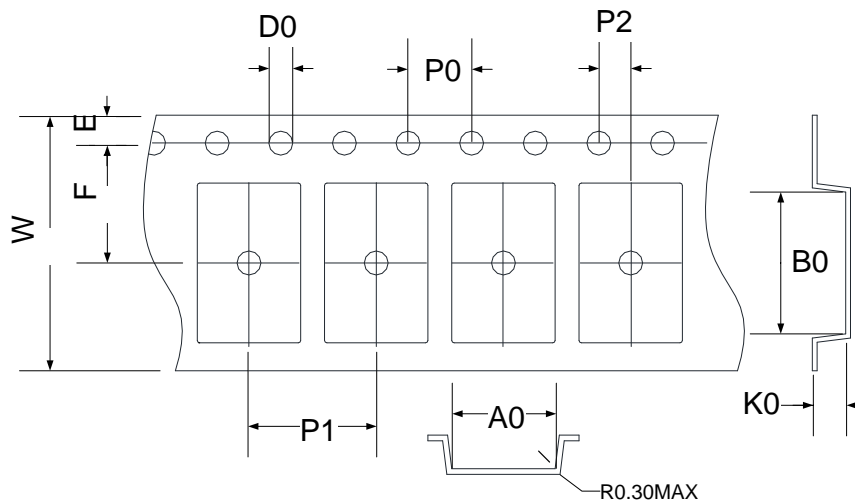
8.2.3. Tape & Reel Information

8.2.3.1. Reel Dimensions –Type1

Unit : mm

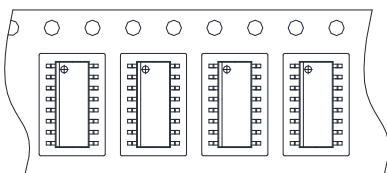


8.2.3.2. Carrier Tape Dimensions



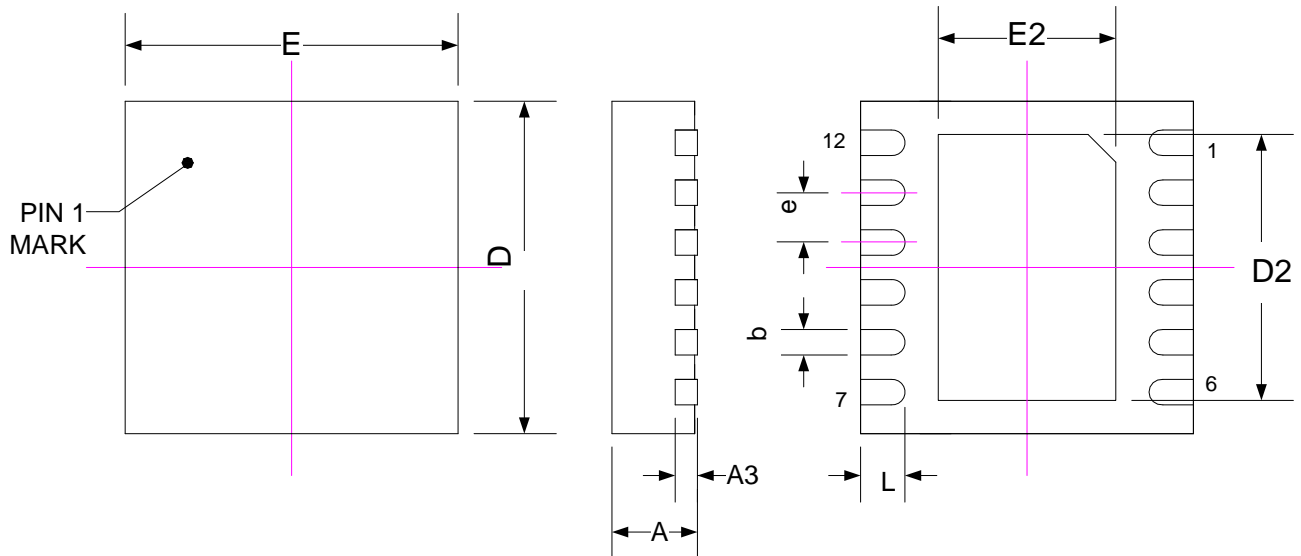
SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	16.5	6.50	10.30	2.10	4.00	8.00	2.00	1.75	7.50	1.50	16.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.10	+0.1/-0	±0.30

8.2.3.3. Pin1 direction



8.3. DFN12(AS12)

8.3.1. Package Dimensions



SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A3	0.20 REF.		
b	0.18	0.24	0.28
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	2.25	2.40	2.55
E2	1.50	1.65	1.75
L	0.30	0.40	0.50
e	0.45 BSC		

Note :

1. All dimensions refer to JEDEC OUTLINE MS-012.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm.

HY15P41

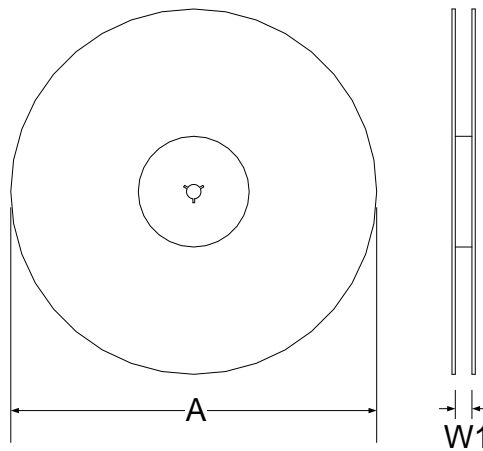
Embedded 18-Bit $\Sigma\Delta$ ADC
8-Bit RISC-like Mixed Signal Microcontroller



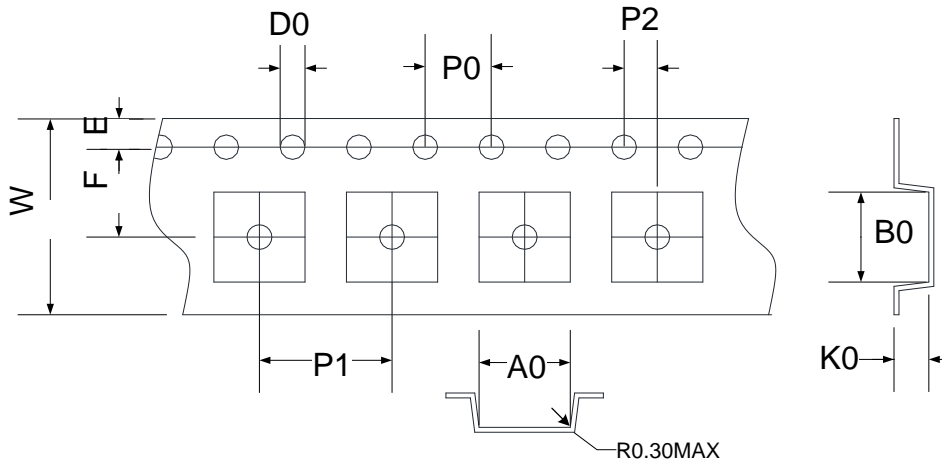
8.3.2. Tape & Reel Information

8.3.2.1. Reel Dimensions –Type1

Unit : mm



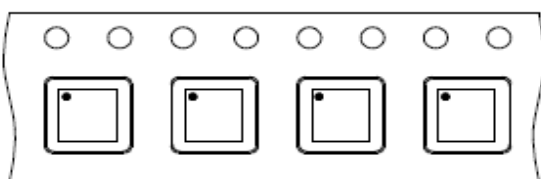
8.3.2.2. Carrier Tape Dimensions



SYMBOLS	Reel Dimensions		Carrier Tape Dimensions									
	A	W1	A0	B0	K0	P0	P1	P2	E	F	D0	W
Spec.	330	12.5	3.30	3.30	1.10	4.00	8.00	2.00	1.75	5.50	1.50	12.00
Tolerance	+6/-3	+1.5/-0	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.05	±0.10	±0.05	+0.1/-0 ±0.30

Note: 10 Sprocket hole pitch cumulative tolerance is ± 0.20 mm.

8.3.2.3. Pin1 direction



9. 修訂記錄

以下描述本文件差異較大的地方，而標點符號與字形的改變不在此描述範圍。

版本	頁次	變更摘要
V01	All	初版發行
V02	11	更新應用電路圖
	20~21	更新暫存器列表
V03	20~21	更新暫存器列表
	22~35	更新電氣規格與增加圖表說明
V04	15	更新 ADC 網路通道
	27	更新 BOR 規格與曲線
V05	5	新增功能列表
	All	更新 SOP8 引腳定義
	All	刪除 SSOP16 封裝訊息，新增 SOP16 封裝訊息
V06	13	更新 CLK 方塊圖
	34	新增 VDD=5V 情況下，ENOB Table
V07	12	新增 DFN12 引腳定義
	41~50	刪除 Die 販售訊息，新增 DFN12 封裝需訊息