



HY16F196B

HY16F197B

HY16F198B

Datasheet

High Precision Mixed-Signal Controller
4x36 ~ 6x34 LCD Driver
32-Bit Low Power MCU
21-bit ENOB $\Sigma\Delta$ ADC
64KB Flash

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1. Features

Digital Circuit

- 32-bit MCU 1T Andes Core N801
- C Compiler & User Friendly Development Tools
- 2.2V to 3.6V operational voltage.
- -40 to 85°C operational environment
- Low power operation:
 - Normal Mode:0.6mA@CPU_CK:2MHz/2
 - Idle Mode:5uA@LSRC=35KHz
 - Sleep Mode:Typ.2.5uA
- 64K Byte Flash ROM
- 8K Byte SRAM
- 16-bit Timer A, Timer B(x2), Timer C
- 16-bit PWM controller
- I²C/SPI/ UART(x2) communication Hardware IP
- RTC Hardware IP
- Low voltage detection/BOR circuit
- 32 programmable digital I/O ports
 - 16 general propose digital I/O ports
 - 16 programmable digital I/O ports multiplexed with LCD Segment
- 4x36 ~ 6x34 LCD Driver
 - Support 1/3, 1/4, 1/5, 1/6 duty @ 1/3 bias mode
 - R-type, External VLCD Application
 - 3.3V, 3.0V, 2.8V, or 2.6V internal charge pump VLCD

Analog Circuit

- An ultra low noise 24-bit SD ADC
 - Down to 65nVrms input refer noise
 - Conversion rate up to 350KSPS
 - Input amplification gain up to 128
 - Operation voltage 2.4V to 3.6V
- External High Speed Oscillator Max 16MHz
- External Low Speed Oscillator Mode 32768Hz
- Internal High Speed Oscillator Max 16MHz
- Internal Low Speed Oscillator 35KHz
- Power management
 - Charge Pump regulation
 - Build-in selectable VDDA voltage LDO
 - 1.2V Band gap reference output
- A resistor ladders can be used as 8-bit Resistance Ladder
 - Programmable potentiometer
 - Monotonic guarantee
- A rail-to-rail operation amplifier
 - CMOS input, 1MHz bandwidth
 - Unit Gain Buffer, Integrator
 - S/H circuit, software SAR ADC
 - Can use as comparator
- Multi-function Analog Comparator
 - support touch key
 - Low Voltage Detection

HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver



Part No.	Flash ROM (KB)	SRAM (KB)	ΣΔADC VIN Ch.	I/O	Touch Key (Ch.)	LCD		Charge pump	ISP Mode	Package	Others: (All the products have the same IP)
						COM	SEG				
HY16F196B-L064	16	2	8	18+22	6	4~6	24~22	Y	Y	LQFP64	Analog Parts: One hardware RTC and calendar. One 8-bit resistance ladders for DAC. One rail-to-rail OPAMP. One multi-function comparator. One built-in temperature sensor. Digital Parts: One 32-bit programmable SPI One I ² C(master and slave mode.) Two enhanced UART Four channels PWM function,
HY16F196B-N068	16	2	8	18+26	6	4~6	28~26	Y	Y	QFN68	
HY16F197B-L064	32	4	5	18+24	6	4~6	26~24	Y	Y	LQFP64	
HY16F197B-N068	32	4	5	18+28	6	4~6	30~28	Y	Y	QFN68	
HY16F198B-L100	64	8	8	22+34	8	4~6	36~34	Y	Y	LQFP100	
HY16F198B-N088	64	8	8	22+34	8	4~6	36~34	Y	Y	QFN88	
HY16F198B-L064	64	8	6	22+24	8	4~6	26~24	N	Y	LQFP64	

2. Pin Definition

2.1. HY16F198B series pin diagram

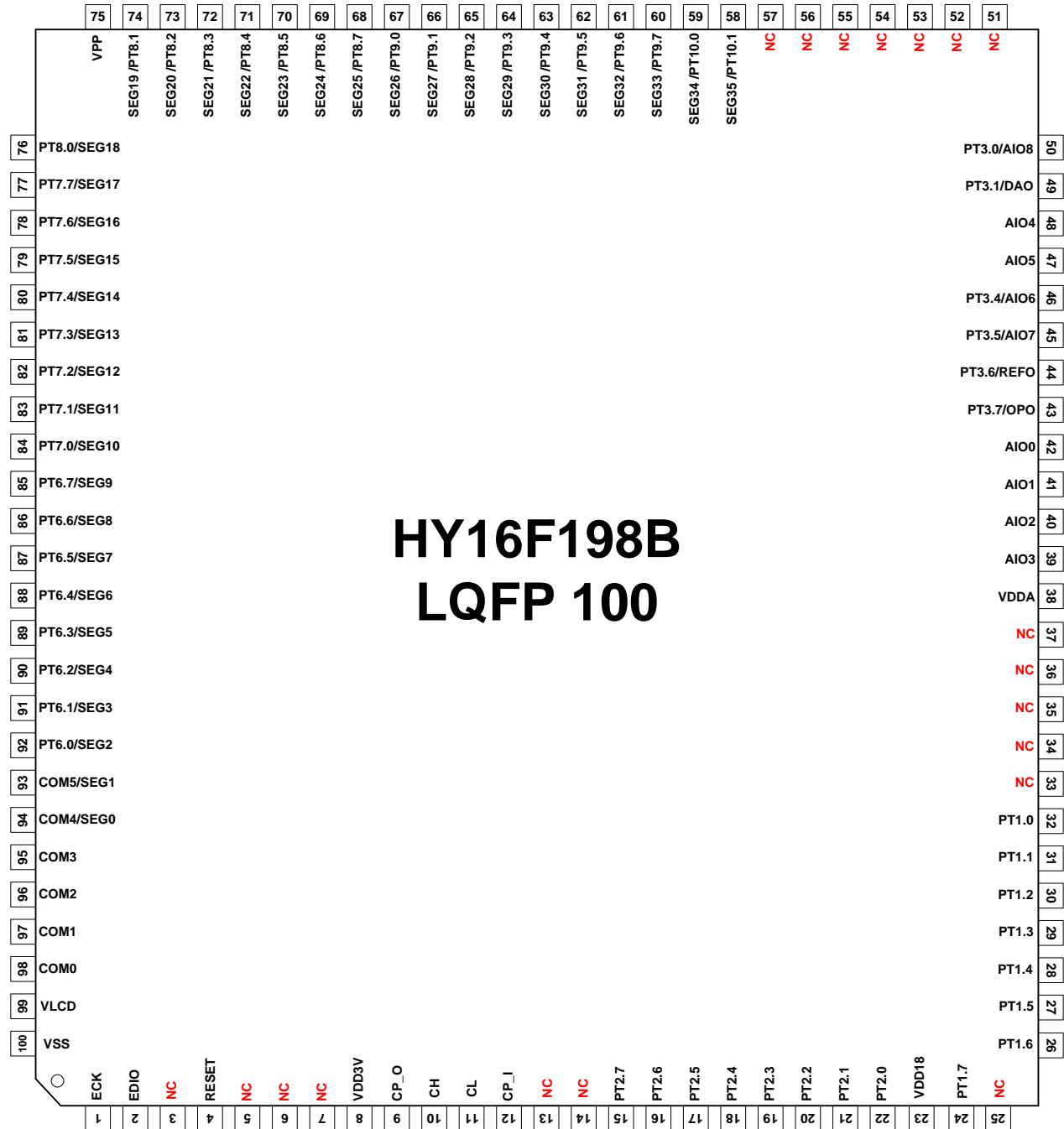


Figure 2-1-1 HY16F198B LQFP100 Pin Diagram

HY16F196B/HY16F197B/HY16F198B Datasheet

21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash

4X36~6X34 LCD Driver

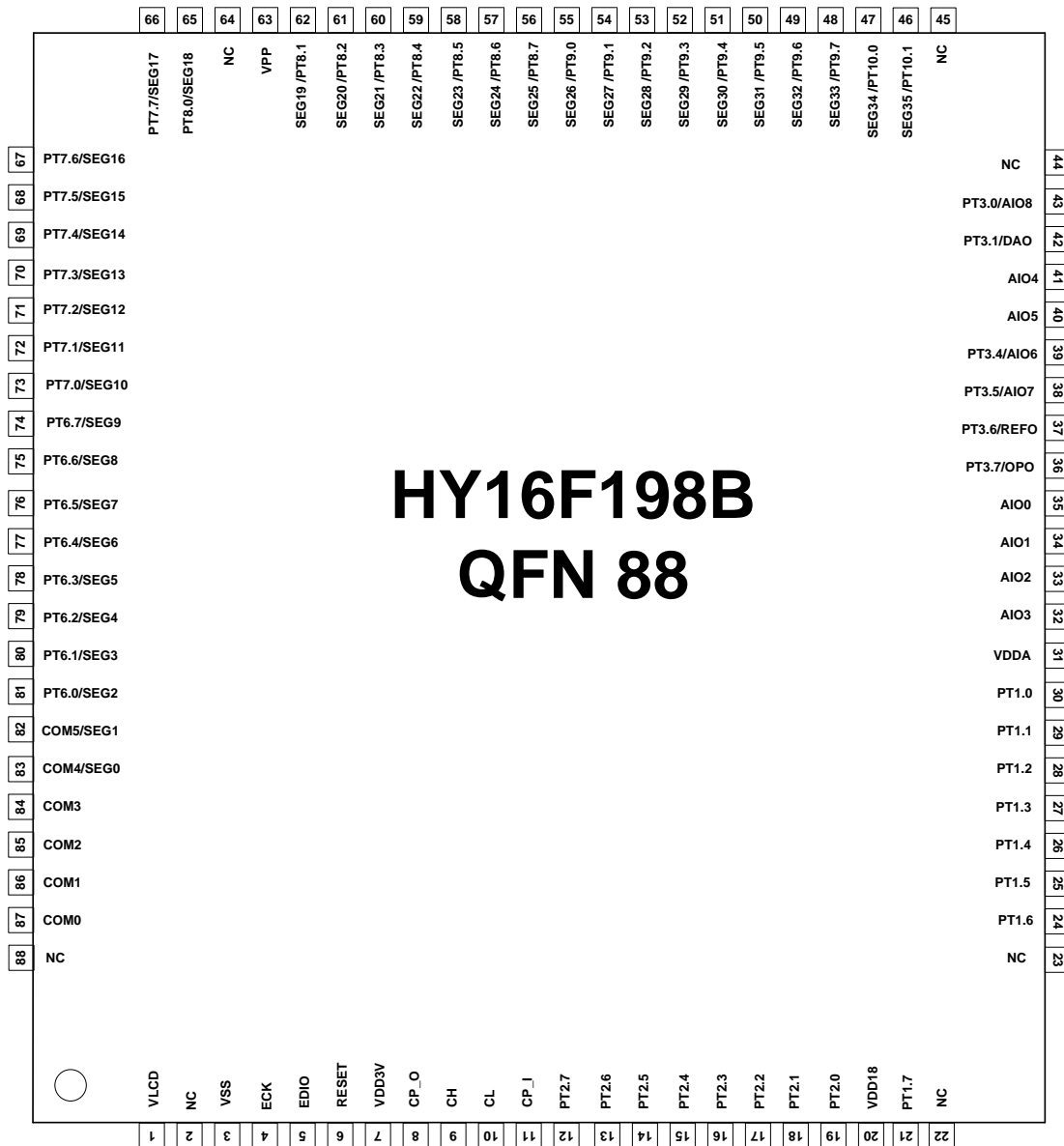


Figure 2-1-2 HY16F198B QFN88 Diagram

HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver

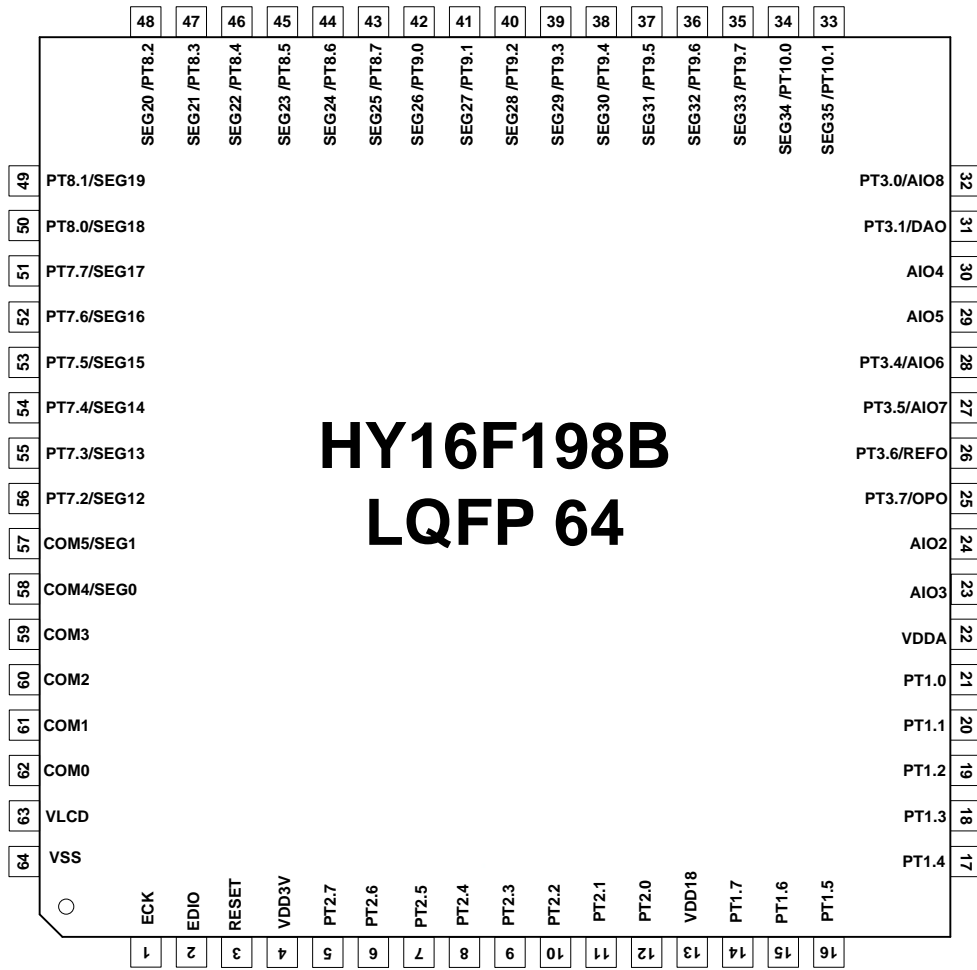


Figure 2-1-3 HY16F198B LQFP64 Diagram

2.2. HY16F197B Series Pin Diagram

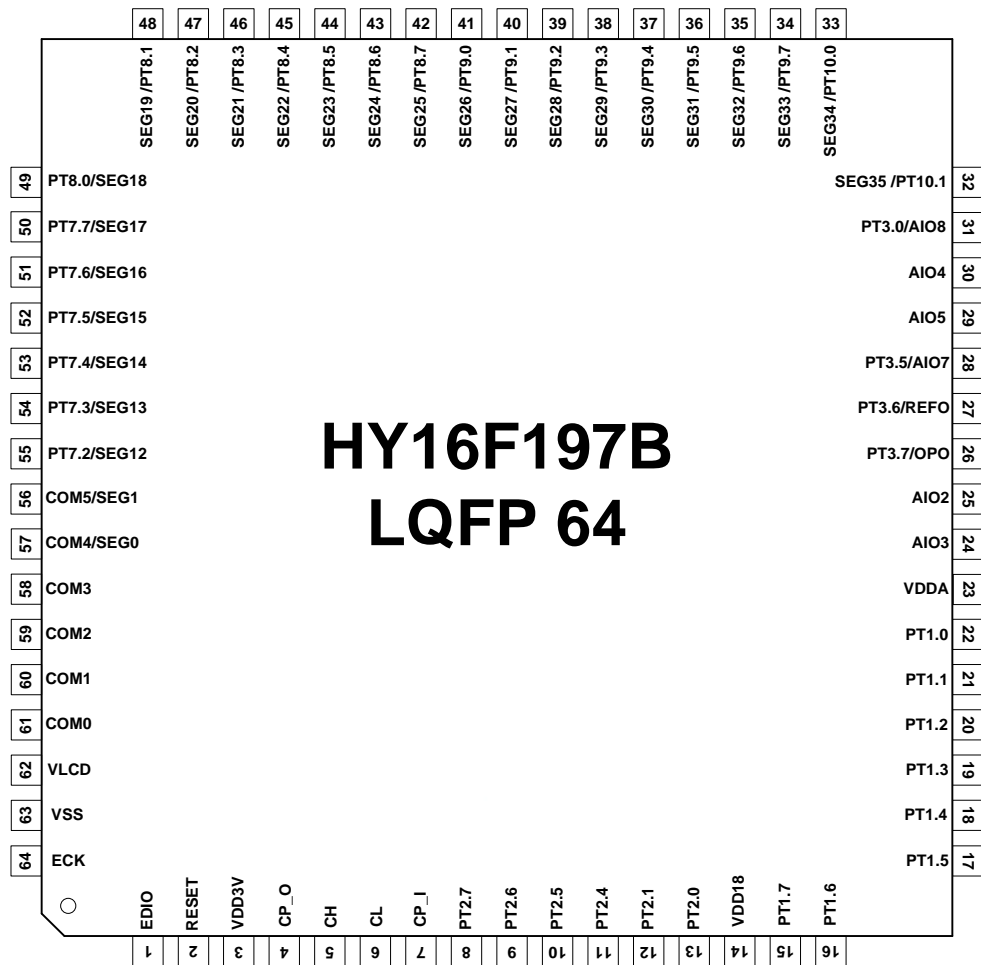


Figure 2-2-1 HY16F197B LQFP64 Pin Diagram

HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver

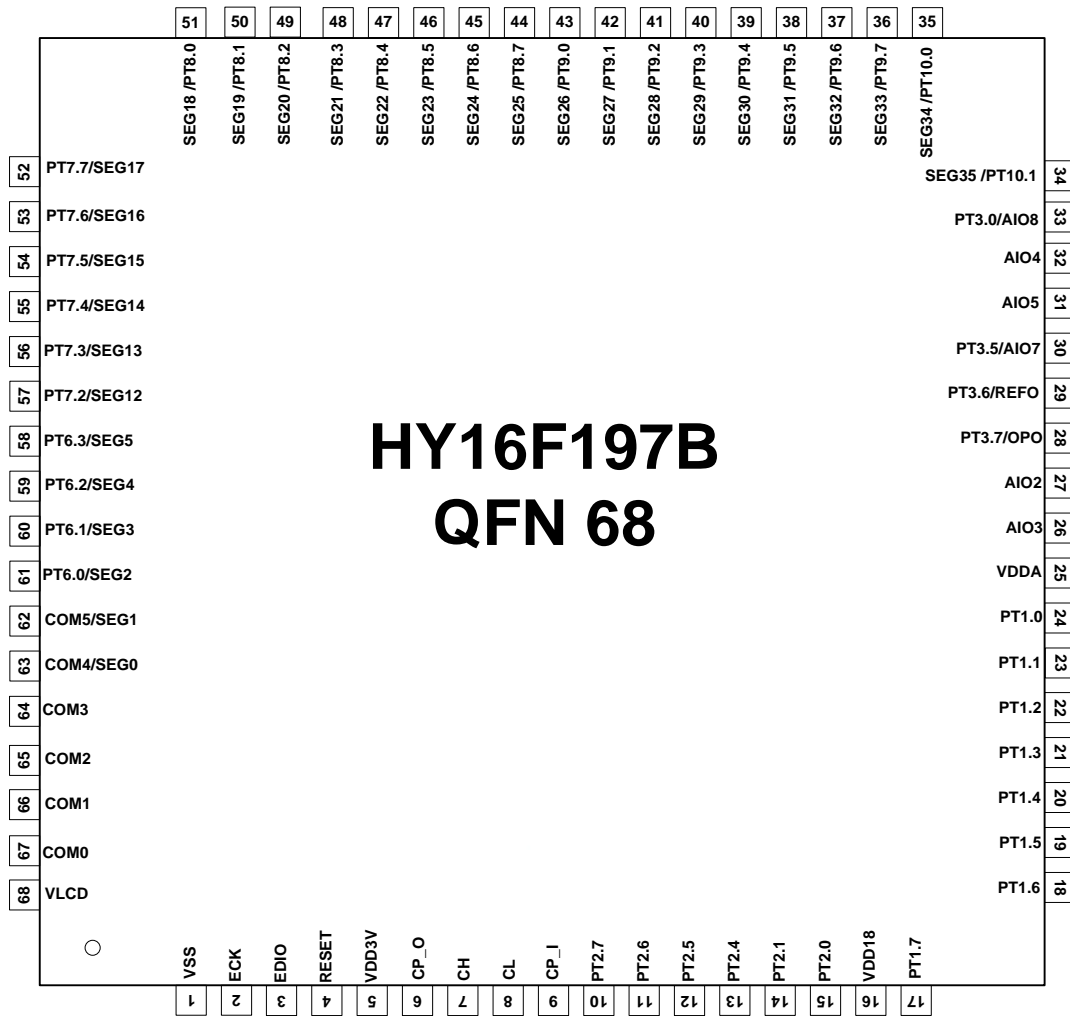


Figure 2-2-2 HY16F197B QFN 68 Pin Diagram

2.3. HY16F196B Series Pin Diagram

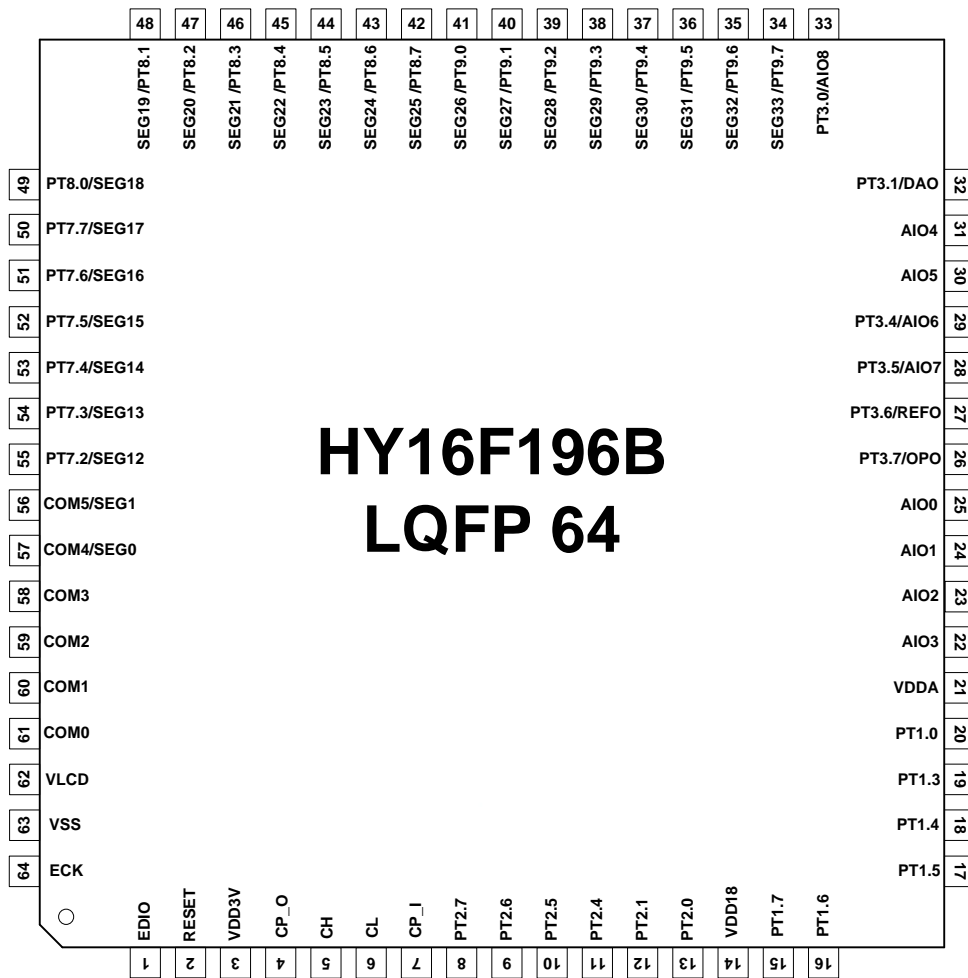


Figure 2-3-1 HY16F196B LQFP 64 Pin Diagram

HY16F196B/HY16F197B/HY16F198B Datasheet

21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash

4X36~6X34 LCD Driver

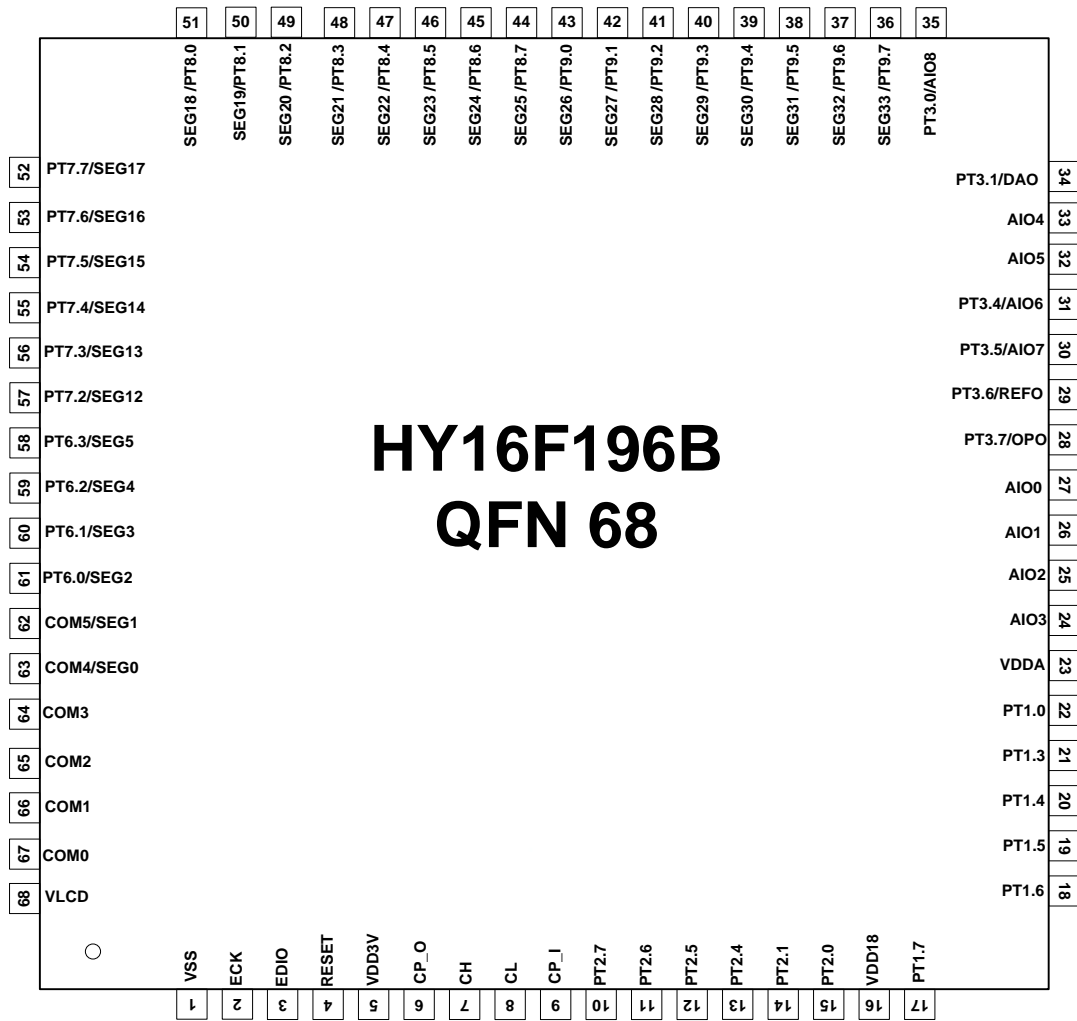


Figure 2-3-2 HY16F196B QFN 68 Pin Diagram

2.4. Pin Description

2.4.1. HY16F19xB Series

TYPE Definition : I = Digital Input. O = Digital Output. OD = Open-drain Output.

AI = Analog Input. AO = Analog Output. P = Power Connection.

Table 2-1 HY16F198B/197B/196B Pin definition and description

Name	HY16F198B			HY16F197B		HY16F196B		Type	Pin Name	Description
	Package	L100	N088	L064	N068	L064	N068			
ECK	1	4	1	2	64	2	64	DIO	ECK	Embedded Debug Module (EDM) Clock Input PIN. 100K Resistance to VSS.
EDIO	2	5	2	3	1	3	1	DIO	EDIO	Embedded Debug Module (EDM) Data Input/ Output PIN. 100K Resistance to VSS.
RESET	4	6	3	4	2	4	2	DI	RESET	Active Low Reset 100K Resistance to VDD3V, 100nF Cap to VSS.
VDD3V	8	7	4	5	3	5	3	PI	VDD3V	Power Input For System, 10uF Cap to VSS.
CP_O	9	8	-	6	4	6	4	PO	CP_O	Charge pump output 3.3V, 10uF Cap to VSS.
CH	10	9	-	7	5	7	5	PIO	CH	Charge Pump Capacitor High Voltage Plate, 1uF Cap to CL
CL	11	10	-	8	6	8	6	PIO	CL	Charge Pump Capacitor Low Voltage Plate, 1uF Cap to CH
CP_I	12	11	-	9	7	9	7	PI	CP_I	Charge Pump Power Input, 10uF Cap to VSS.
PT2.7	15	12	5	10	8	10	8	IO	PT2.7	Digital Input/ Output Pin
								XO	HS_XOUT	High Speed Crystal XOUT ,2~16MHZ
								I	INT2.7	Interrupt Source INT 2.7
								O	PWM3_4	TimerB2, PWM3_4 Output Pin
								O	MOSI_4	SPI Interface MOSI_4(Master output, Slave input)
								I	RX2_4	EUART2 Interface RX2_4
								I	TCI2_8	Capture Comparator Input Source Pin TCI2_8

HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver



Name	HY16F198B			HY16F197B		HY16F196B		Type	Pin Name	Description
	Package	L100	N088	L064	N068	L064	N068			
PT2.6	16	13	6	11	9	11	9	IO	SDA_8	I2C Interface SDA_8
								IO	PT2.6	Digital Input/ Output Pin
								XI	HS_XIN	High Speed Crystal XIN ,2~16MHZ
								I	INT2.6	Interrupt Source INT 2.6
								O	PWM2_4	TimerB2, PWM2_4 Output Pin
								I	MISO_4	SPI Interface MISO_4(Master input, Slave output)
								IO	TX2_4	EUART2 Interface TX2_4
								I	TCI1_8	Capture Comparator Input Source Pin TCI1_8
PT2.5	17	14	7	12	10	12	10	IO	PT2.5	Digital Input/ Output Pin
								XI	LS_XIN	Low Speed Crystal XIN 32768HZ
								I	INT2.5	Interrupt Source INT 2.5
								O	PWM1_4	TimerB, PWM1_4 Output Pin
								I	CK_4	SPI Interface CK_4
								I	RX_4	EUART Interface RX_4
								I	TCI2_7	Capture Comparator Input Source Pin TCI2_7
								IO	SDA_7	I2C Interface SDA_7
PT2.4	18	15	8	13	11	13	11	IO	PT2.4	Digital Input/ Output Pin
								XO	LS_XOUT	Low Speed Crystal XOUT 32768HZ
								I	INT2.4	Interrupt Source INT 2.4
								O	PWM0_4	TimerB, PWM0_4 Output Pin
								I	CS_4	SPI Interface CS_4
								IO	TX_4	EUART Interface TX_4
								I	TCI1_7	Capture Comparator Input Source Pin TCI1_7
								IO	SCL_7	I2C Interface SCL_7
PT2.3	19	16	9	-	-	-	-	IO	PT2.3	Digital Input/ Output Pin
								I	INT2.3	Interrupt Source INT 2.3
								O	PWM3_3	TimerB2, PWM3_3 Output Pin

HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver



Name	HY16F198B			HY16F197B		HY16F196B		Type	Pin Name	Description
	Package	L100	N088	L064	N068	L064	N068			
								O	MOSI_3	SPI Interface MOSI_3(Master output, Slave input)
								I	RX2_3	EUART2 Interface RX2_3
								I	TCI2_6	Capture Comparator Input Source Pin TCI2_6
								IO	SDA_6	I2C Interface SDA_6
								AI	CL8	Comparator Analog Input CL8
PT2.2	20	17	10	-	-	-	-	IO	PT2.2	Digital Input/ Output Pin
								I	INT2.2	Interrupt Source INT 2.2
								O	PWM2_3	TimerB2, PWM2_3 Output Pin
								I	MISO_3	SPI Interface MISO_3(Master input, Slave output)
								IO	TX2_3	EUART2 Interface TX2_3
								I	TCI1_6	Capture Comparator Input Source Pin TCI1_6
								IO	SCL_6	I2C Interface SCL_6
								AI	CL7	Comparator Analog Input CL7
PT2.1	21	18	11	14	12	14	12	IO	PT2.1	Digital Input/ Output Pin
								I	INT2.1	Interrupt Source INT 2.1
								O	PWM1_3	TimerB, PWM1_3 Output Pin
								I	CK_3	SPI Interface CK_3
								I	RX_3	EUART Interface RX_3
								I	TCI2_5	Capture Comparator Input Source Pin TCI2_5
								IO	SDA_5	I2C Interface SDA_5
								AI	CL6	Comparator Analog Input CL6
PT2.0	22	19	12	15	13	15	13	IO	PT2.0	Digital Input/ Output Pin
								I	INT2.0	Interrupt Source INT 2.0
								O	PWM0_3	TimerB, PWM0_3 Output Pin
								I	CS_3	SPI Interface CS_3
								IO	TX_3	EUART Interface TX_3
								I	TCI1_5	Capture Comparator Input Source Pin TCI1_5

HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver



Name	HY16F198B			HY16F197B		HY16F196B		Type	Pin Name	Description
	Package	L100	N088	L064	N068	L064	N068			
								IO	SCL_5	I2C Interface SCL_5
								AI	CL5	Comparator Analog Input CL5
VDD18	23	20	13	16	14	16	14	PI	VDD18	Digital Power Supply output 1.8V, 1uF Cap to VSS
PT1.7	24	21	14	17	15	17	15	IO	PT1.7	Digital Input/ Output Pin
								AO	CMPO	Comparator Output (Digital)
								I	INT1.7	Interrupt Source INT 1.7
								O	PWM3_2	TimerB2, PWM3_2 Output Pin
								O	MOSI_2	SPI Interface MOSI_2(Master output, Slave input)
								I	RX2_2	EUART2 Interface RX2_2
								I	TCI2_4	Capture Comparator Input Source Pin TCI2_4
								IO	SDA_4	I2C Interface SDA_4
PT1.6	26	24	15	18	16	18	16	IO	PT1.6	Digital Input/ Output Pin
								I	INT1.6	Interrupt Source INT 1.6
								O	PWM2_2	TimerB2, PWM2_2 Output Pin
								I	MISO_2	SPI Interface MISO_2(Master input, Slave output)
								IO	TX2_2	EUART2 Interface TX2_2
								I	TCI1_4	Capture Comparator Input Source Pin TCI1_4
								IO	SCL_4	I2C Interface SCL_4
								AI	CL4	Comparator Analog Input CL4
PT1.5	27	25	16	19	17	19	17	IO	PT1.5	Digital Input/ Output Pin
								I	INT1.5	Interrupt Source INT 1.5
								O	PWM1_2	TimerB, PWM1_2 Output Pin
								I	CK_2	SPI Interface CK_2
								I	RX_2	EUART Interface RX_2
								I	TCI2_3	Capture Comparator Input Source Pin TCI2_3
								IO	SDA_3	I2C Interface SDA_3
								AI	CL3	Comparator Analog Input CL3

HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver



Name	HY16F198B			HY16F197B		HY16F196B		Type	Pin Name	Description
	Package	L100	N088	L064	N068	L064	N068			
PT1.4	28	26	17	20	18	20	18	IO	PT1.4	Digital Input/ Output Pin
								I	INT1.4	Interrupt Source INT 1.4
								O	PWM0_2	TimerB, PWM0_2 Output Pin
								I	CS_2	SPI Interface CS_2
								IO	TX_2	EUART Interface TX_2
								I	TCI1_3	Capture Comparator Input Source Pin TCI1_3
								IO	SCL_3	I2C Interface SCL_3
								AI	CL2	Comparator Analog Input CL2
PT1.3	29	27	18	21	19	21	19	IO	PT1.3	Digital Input/ Output Pin
								I	INT1.3	Interrupt Source INT1.3
								O	PWM3_1	TimerB2, PWM3_1 Output Pin
								O	MOSI_1	SPI Interface MOSI_1(Master output, Slave input)
								I	RX2_1	EUART2 Interface RX2_1
								I	TCI2_2	Capture Comparator Input Source Pin TCI1_2
								IO	SDA_2	I2C Interface SDA_2
								AI	CL1	Comparator Analog Input CL1
PT1.2	30	28	19	22	20	-	-	IO	PT1.2	Digital Input/ Output Pin
								I	INT1.2	Interrupt Source INT 1.2
								O	PWM2_1	TimerB2, PWM2_1 Output Pin
								I	MISO_1	SPI Interface MISO_1(Master input, Slave output)
								IO	TX2_1	EUART2 Interface TX2_1
								I	TCI1_2	Capture Comparator Input Source Pin TCI1_2
								IO	SCL_2	I2C Interface SCL_2
								AI	CH3	Comparator Analog Input CH3
PT1.1	31	29	20	23	21	-	-	IO	PT1.1	Digital Input/ Output Pin
								I	INT1.1	Interrupt Source INT 1.1
								O	PWM1_1	TimerB, PWM1_1 Output Pin
								I	CK_1	SPI Interface CK_1

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4X36~6X34 LCD Driver



Name	HY16F198B			HY16F197B		HY16F196B		Type	Pin Name	Description
	Package	L100	N088	L064	N068	L064	N068			
								I	RX_1	EUART Interface RX_1
								I	TCI2_1	Capture Comparator Input Source Pin TCI2_1
								IO	SDA_1	I2C Interface SDA_1
								AI	CH2	Comparator Analog Input CH2
PT1.0	32	30	21	24	22	22	20	IO	PT1.0	Digital Input/ Output Pin
								I	INT1.0	Interrupt Source INT 1.0
								O	PWM0_1	TimerB, PWM0_1 Output Pin
								I	CS_1	SPI Interface CS_1
								IO	TX_1	EUART Interface TX_1
								I	TCI1_1	Capture Comparator Input Source Pin TCI1_1
								IO	SCL_1	I2C Interface SCL_1
								AI	CH1	Comparator Analog Input CH1
VDDA	38	31	22	25	23	23	21	PIO	VDDA	Analog voltage source input / output (connect 1 ~ 10 uF capacitor to VSS)
AIO3	39	32	23	26	24	24	22	AI	AIO3	ADC Analog Input Signal Port AIO3
AIO2	40	33	24	27	25	25	23	AI	AIO2	ADC Analog Input Signal Port AIO2
AIO1	41	34	-	-	-	26	24	AI	AIO1	ADC Analog Input Signal Port AIO1
AIO0	42	35	-	-	-	27	25	AI	AIO0	ADC Analog Input Signal Port AIO0
PT3.7	43	36	25	28	26	28	26	IO	PT3.7	Digital Input/ Output Pin
								AO	OPO	Rail-to-rail OPAMP Analog Output Pin
PT3.6	44	37	26	29	27	29	27	IO	PT3.6	Digital Input/ Output Pin
								PIO	REFO	Reference Voltage output 1.2V, 0.1uF Cap to VSS.
PT3.5	45	38	27	30	28	30	28	IO	PT3.5	Digital Input/ Output Pin
								AI	AIO7	ADC Analog Input Signal Port AIO7
PT3.4	46	39	28	-	-	31	29	IO	PT3.4	Digital Input/ Output Pin
								AI	AIO6	ADC Analog Input Signal Port AIO6
AIO5	47	40	29	31	29	32	30	AI	AIO5	ADC Analog Input Signal Port AIO5
AIO4	48	41	30	32	30	33	31	AI	AIO4	ADC Analog Input Signal Port AIO4

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4X36~6X34 LCD Driver



Name	HY16F198B			HY16F197B		HY16F196B		Type	Pin Name	Description
	Package	L100	N088	L064	N068	L064	N068			
PT3.1	49	42	31	-	-	34	32	IO	PT3.1	Digital Input/ Output Pin
								AO	OPO2	Rail-to-rail OPAMP Digital Output Pin
								AO	DAO	8-BIT Resistance Ladders Output Pin
PT3.0	50	43	32	33	31	35	33	IO	PT3.0	Digital Input/ Output Pin
								AO	OPO1	Rail-to-rail OPAMP Digital Output Pin
								AI	AIO8	ADC Analog Input Signal Port AIO8
SEG35	58	46	33	34	32	-	-	IO	PT10.1	Digital Input/ Output Pin
								AO	SEG35	LCD Segment Output
SEG34	59	47	34	35	33	-	-	IO	PT10.0	Digital Input/ Output Pin
								AO	SEG34	LCD Segment Output
SEG33	60	48	35	36	34	36	34	IO	PT9.7	Digital Input/ Output Pin
								AO	SEG33	LCD Segment Output
								O	PWM3_8	TimerB2, PWM3_8 Output Pin
								O	MOSI_8	SPI Interface MOSI_8(Master output, Slave input)
								I	RX2_8	EUART2 Interface RX2_8
SEG32	61	49	36	37	35	37	35	IO	PT9.6	Digital Input/ Output Pin
								AO	SEG32	LCD Segment Output
								O	PWM2_8	TimerB2, PWM2_8 Output Pin
								O	MISO_8	SPI Interface MISO_8(Master input, Slave output)
								I	TX2_8	EUART2 Interface TX2_8
SEG31	62	50	37	38	36	38	36	IO	PT9.5	Digital Input/ Output Pin
								AO	SEG31	LCD Segment Output
								O	PWM1_8	TimerB, PWM1_8 Output Pin
								O	CK_8	SPI Interface CK_8
								I	RX_8	EUART Interface RX_8
SEG30	63	51	38	39	37	39	37	IO	PT9.4	Digital Input/ Output Pin
								AO	SEG30	LCD Segment Output
								O	PWM0_8	TimerB, PWM0_8 Output Pin
								O	CS_8	SPI Interface CS_8
								I	TX_8	EUART Interface TX_8

HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver



Name	HY16F198B			HY16F197B		HY16F196B		Type	Pin Name	Description
	Package	L100	N088	L064	N068	L064	N068			
SEG29	64	52	39	40	38	40	38	IO	PT9.3	Digital Input/ Output Pin
								AO	SEG29	LCD Segment Output
								O	PWM3_7	TimerB2, PWM3_7 Output Pin
								O	MOSI_7	SPI Interface MOSI_7(Master output, Slave input)
								I	RX2_7	EUART2 Interface RX2_7
SEG28	65	53	40	41	39	41	39	IO	PT9.2	Digital Input/ Output Pin
								AO	SEG28	LCD Segment Output
								O	PWM2_7	TimerB2, PWM2_7 Output Pin
								O	MISO_7	SPI Interface MISO_7(Master input, Slave output)
								I	TX2_7	EUART2 Interface TX2_7
SEG27	66	54	41	42	40	42	40	IO	PT9.1	Digital Input/ Output Pin
								AO	SEG27	LCD Segment Output
								O	PWM1_7	TimerB, PWM1_7 Output Pin
								O	CK_7	SPI Interface CK_7
								I	RX_7	EUART Interface RX_7
SEG26	67	55	42	43	41	43	41	IO	PT9.0	Digital Input/ Output Pin
								AO	SEG26	LCD Segment Output
								O	PWM0_7	TimerB, PWM0_7 Output Pin
								O	CS_7	SPI Interface CS_7
								I	TX_7	EUART Interface TX_7
SEG25	68	56	43	44	42	44	42	IO	PT8.7	Digital Input/ Output Pin
								AO	SEG25	LCD Segment Output Pin
								O	PWM3_6	TimerB2, PWM3_6 Output
								O	MOSI_6	SPI Interface MOSI_6(Master output, Slave input)
								I	RX2_6	EUART2 Interface RX2_6
								I	TCI3_8	Timer B2 Clock Trigger PIN TCI3_8
SEG24	69	57	44	45	43	45	43	IO	PT8.6	Digital Input/ Output Pin
								AO	SEG24	LCD Segment Output
								O	PWM2_6	TimerB2, PWM2_6 Output Pin

HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver



Name	HY16F198B			HY16F197B		HY16F196B		Type	Pin Name	Description
	Package	L100	N088	L064	N068	L064	N068			
								O	MISO_6	SPI Interface MISO_6(Master input, Slave output)
								I	TX2_6	EUART2 Interface TX2_6
SEG23	70	58	45	46	44	46	44	IO	PT8.5	Digital Input/ Output Pin
								AO	SEG23	LCD Segment Output
								O	PWM1_6	TimerB, PWM1_6 Output Pin
								O	CK_6	SPI Interface CK_6
								I	RX_6	EUART Interface RX_6
								I	TCI3_7	Timer B2 Clock Trigger PIN TCI3_7
SEG22	71	59	46	47	45	47	45	IO	PT8.4	Digital Input/ Output Pin
								AO	SEG22	LCD Segment Output
								O	PWM0_6	TimerB, PWM0_6 Output Pin
								O	CS_6	SPI Interface CS_6
								I	TX_6	EUART Interface TX_6
SEG21	72	60	47	48	46	48	46	IO	PT8.3	Digital Input/ Output Pin
								AO	SEG21	LCD Segment Output
								O	PWM3_5	TimerB2, PWM3_5 Output Pin
								O	MOSI_5	SPI Interface MOSI_5(Master output, Slave input)
								I	RX2_5	EUART2 Interface RX2_5
								I	TCI3_6	Timer B2 Clock Trigger PIN TCI3_6
SEG20	73	61	48	49	47	49	47	IO	PT8.2	Digital Input/ Output Pin
								AO	SEG20	LCD Segment Output
								O	PWM2_5	TimerB2, PWM2_5 Output Pin
								O	MISO_5	SPI Interface MISO_5(Master input, Slave output)
								I	TX2_5	EUART2 Interface TX2_5
SEG19	74	62	49	50	48	50	48	IO	PT8.1	Digital Input/ Output Pin
								AO	SEG19	LCD Segment Output
								O	PWM1_5	TimerB, PWM1_5 Output Pin
								O	CK_5	SPI Interface CK_5
								I	RX_5	EUART Interface RX_5

HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver



Name	HY16F198B			HY16F197B		HY16F196B		Type	Pin Name	Description
	Package	L100	N088	L064	N068	L064	N068			
								I	TCI3_5	Timer B2 Clock Trigger PIN TCI3_5
VPP	75	63	-	-	-	-	-	PI	VPP	Reserve (keep floating status)
SEG18	76	65	50	51	49	51	49	IO	PT8.0	Digital Input/ Output Pin
								AO	SEG18	LCD Segment Output
								O	PWM0_5	TimerB, PWM0_5 Output
								O	CS_5	SPI Interface CS_5
								I	TX_5	EUART Interface TX_5
SEG17	77	66	51	52	50	52	50	IO	PT7.7	Digital Input/ Output Pin
								AO	SEG17	LCD Segment Output
								I	TCI3_4	Timer B2 Clock Trigger PIN TCI3_4
SEG16	78	67	52	53	51	53	51	IO	PT7.6	Digital Input/ Output Pin
								AO	SEG16	LCD Segment Output
SEG15	79	68	53	54	52	54	52	IO	PT7.5	Digital Input/ Output Pin
								AO	SEG15	LCD Segment Output
								I	TCI3_3	Timer B2 Clock Trigger PIN TCI3_3
SEG14	80	69	54	55	53	55	53	IO	PT7.4	Digital Input/ Output Pin
								AO	SEG14	LCD Segment Output
SEG13	81	70	55	56	54	56	54	IO	PT7.3	Digital Input/ Output Pin
								AO	SEG13	LCD Segment Output
								I	TCI3_2	Timer B2 Clock Trigger PIN TCI3_2
SEG12	82	71	56	57	55	57	55	IO	PT7.2	Digital Input/ Output Pin
								AO	SEG12	LCD Segment Output
SEG11	83	72	-	-	-	-	-	IO	PT7.1	Digital Input/ Output Pin
								AO	SEG11	LCD Segment Output
								I	TCI3_1	Timer B2 Clock Trigger PIN TCI3_1
SEG10	84	73	-	-	-	-	-	IO	PT7.0	Digital Input/ Output Pin
								AO	SEG10	LCD Segment Output
SEG9	85	74	-	-	-	-	-	IO	PT6.7	Digital Input/ Output Pin
								AO	SEG9	LCD Segment Output
SEG8	86	75	-	-	-	-	-	IO	PT6.6	Digital Input/ Output Pin
								AO	SEG8	LCD Segment Output

HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver



Name	HY16F198B			HY16F197B		HY16F196B		Type	Pin Name	Description
	Package	L100	N088	L064	N068	L064	N068			
SEG7	87	76	-	-	-	-	-	IO	PT6.5	Digital Input/ Output Pin
								AO	SEG7	LCD Segment Output
SEG6	88	77	-	-	-	-	-	IO	PT6.4	Digital Input/ Output Pin
								AO	SEG6	LCD Segment Output
SEG5	89	78	-	58	-	58	-	IO	PT6.3	Digital Input/ Output Pin
								AO	SEG5	LCD Segment Output
SEG4	90	79	-	59	-	59	-	IO	PT6.2	Digital Input/ Output Pin
								AO	SEG4	LCD Segment Output
SEG3	91	80	-	60	-	60	-	IO	PT6.1	Digital Input/ Output Pin
								AO	SEG3	LCD Segment Output
SEG2	92	81	-	61	-	61	-	IO	PT6.0	Digital Input/ Output Pin
								AO	SEG2	LCD Segment Output
SEG1	93	82	57	62	56	62	56	IO	PT10.3	Digital Input/ Output Pin
								AO	SEG1	LCD Segment Output
								AO	COM5	LCD Common Output
SEG0	94	83	58	63	57	63	57	IO	PT10.2	Digital Input/ Output Pin
								AO	SEG0	LCD Segment Output
								AO	COM4	LCD Common Output
COM3	95	84	59	64	58	64	58	AO	COM3	LCD Common Output
COM2	96	85	60	65	59	65	59	AO	COM2	LCD Common Output
COM1	97	86	61	66	60	66	60	AO	COM1	LCD Common Output
COM0	98	87	62	67	61	67	61	AO	COM0	LCD Common Output
VLCD	99	1	63	68	62	68	62	PIO	VLCD	LCD Power Supply Output, or Power Supply Input, 10uF Cap to VSS.
VSS	100	3	64	1	63	1	63	PI	VSS	System Power Ground
Others	-	-	-	-	-	-	-	-	NC	Not Connect

2.4.2. GPIO Port Function Configuration

Function	INT	Timer C Capture	Special Function	SPI	I ² C	UART	AIP	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	0	1	2	3	4	5	6
PT1.0	INT1.0	TCI1_1		CS_1	SCL_1	Tx_1		CH1	PWM0_1
PT1.1	INT1.1	TCI2_1		CK_1	SDA_1	Rx_1		CH2	PWM1_1
PT1.2	INT1.2	TCI1_2		MISO_1	SCL_2	Tx2_1		CH3	PWM2_1
PT1.3	INT1.3	TCI2_2		MOSI_1	SDA_2	Rx2_1		CL1	PWM3_1
PT1.4	INT1.4	TCI1_3		CS_2	SCL_3	Tx_2		CL2	PWM0_2
PT1.5	INT1.5	TCI2_3		CK_2	SDA_3	Rx_2		CL3	PWM1_2
PT1.6	INT1.6	TCI1_4		MISO_2	SCL_4	Tx2_2		CL4	PWM2_2
PT1.7	INT1.7	TCI2_4		MOSI_2	SDA_4	Rx2_2	CMPO		PWM3_2
PT2.0	INT2.0	TCI1_5		CS_3	SCL_5	Tx_3		CL5	PWM0_3
PT2.1	INT2.1	TCI2_5		CK_3	SDA_5	Rx_3		CL6	PWM1_3
PT2.2	INT2.2	TCI1_6		MISO_3	SCL_6	Tx2_3		CL7	PWM2_3
PT2.3	INT2.3	TCI2_6		MOSI_3	SDA_6	Rx2_3		CL8	PWM3_3
PT2.4	INT2.4	TCI1_7	LS_XOUT	CS_4	SCL_7	Tx_4			PWM0_4
PT2.5	INT2.5	TCI2_7	LS_XIN	CK_4	SDA_7	Rx_4			PWM1_4
PT2.6	INT2.6	TCI1_8	HS_XIN	MISO_4	SCL_8	Tx2_4			PWM2_4
PT2.7	INT2.7	TCI2_8	HS_XOUT	MOSI_4	SDA_8	Rx2_4			PWM3_4
PT3.0							OPO1	AIO8	
PT3.1							OPO2	DAO	
PT3.4								AIO6	
PT3.5								AIO7	
PT3.6								REFO	
PT3.7								OPO	
RESET	RESET								
AIO0								AIO0	
AIO1								AIO1	
AIO2								AIO2	
AIO3								AIO3	
AIO4								AIO4	
AIO5								AIO5	
COM0			COM 0						
COM1			COM 1						
COM2			COM 2						
COM3			COM 3						
PT10.2			COM 4/SEG 0						

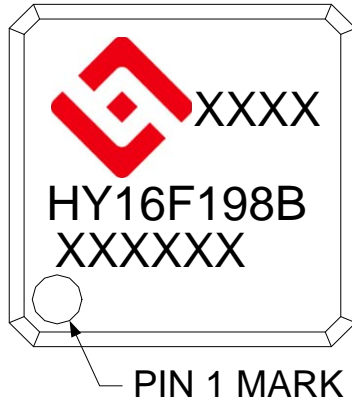
HY16F196B/HY16F197B/HY16F198B Datasheet
21-bit ENOB ΣΔADC, 32-bit MCU & 64KB Flash
4X36~6X34 LCD Driver



Function	INT	Timer C Capture	Special Function	SPI	I ² C	UART	AIP	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	0	1	2	3	4	5	6
PT10.3			COM 5/SEG 1						
PT6.0			SEG 2						
PT6.1			SEG 3						
PT6.2			SEG 4						
PT6.3			SEG 5						
PT6.4			SEG 6						
PT6.5			SEG 7						
PT6.6			SEG 8						
PT6.7			SEG 9						
PT7.0			SEG 10						
PT7.1		TCI3_1	SEG 11						
PT7.2			SEG 12						
PT7.3		TCI3_2	SEG 13						
PT7.4			SEG 14						
PT7.5		TCI3_3	SEG 15						
PT7.6			SEG 16						
PT7.7		TCI3_4	SEG 17						
PT8.0			SEG 18	CS_5		Tx_5			PWM0_5
PT8.1		TCI3_5	SEG 19	CK_5		Rx_5			PWM1_5
PT8.2			SEG 20	MISO_5		Tx2_5			PWM2_5
PT8.3		TCI3_6	SEG 21	MOSI_5		Rx2_5			PWM3_5
PT8.4			SEG 22	CS_6		Tx_6			PWM0_6
PT8.5		TCI3_7	SEG 23	CK_6		Rx_6			PWM1_6
PT8.6			SEG 24	MISO_6		Tx2_6			PWM2_6
PT8.7		TCI3_8	SEG 25	MOSI_6		Rx2_6			PWM3_6
PT9.0			SEG 26	CS_7		Tx_7			PWM0_7
PT9.1			SEG 27	CK_7		Rx_7			PWM1_7
PT9.2			SEG 28	MISO_7		Tx2_7			PWM2_7
PT9.3			SEG 29	MOSI_7		Rx2_7			PWM3_7
PT9.4			SEG 30	CS_8		Tx_8			PWM0_8
PT9.5			SEG 31	CK_8		Rx_8			PWM1_8
PT9.6			SEG 32	MISO_8		Tx2_8			PWM2_8
PT9.7			SEG 33	MOSI_8		Rx2_8			PWM3_8
PT10.0			SEG 34						
PT10.1			SEG 35						

2.5. Package marking information

2.5.1. HY16F198B LQFP Package marking information

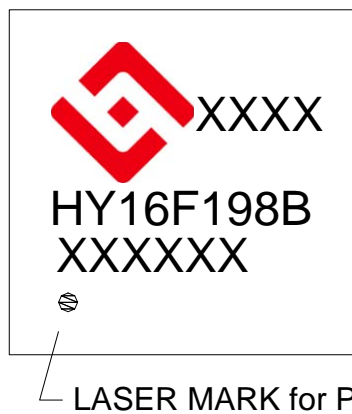


HYCON's Logo + Traceability code

Product Name:HY16F198B

Product Lot No.

2.5.2. HY16F198B QFN Package marking information



HYCON's Logo + Traceability code

Product Name:HY16F198B

Product Lot No.

3. Application Circuit

3.1. Bridge Sensor

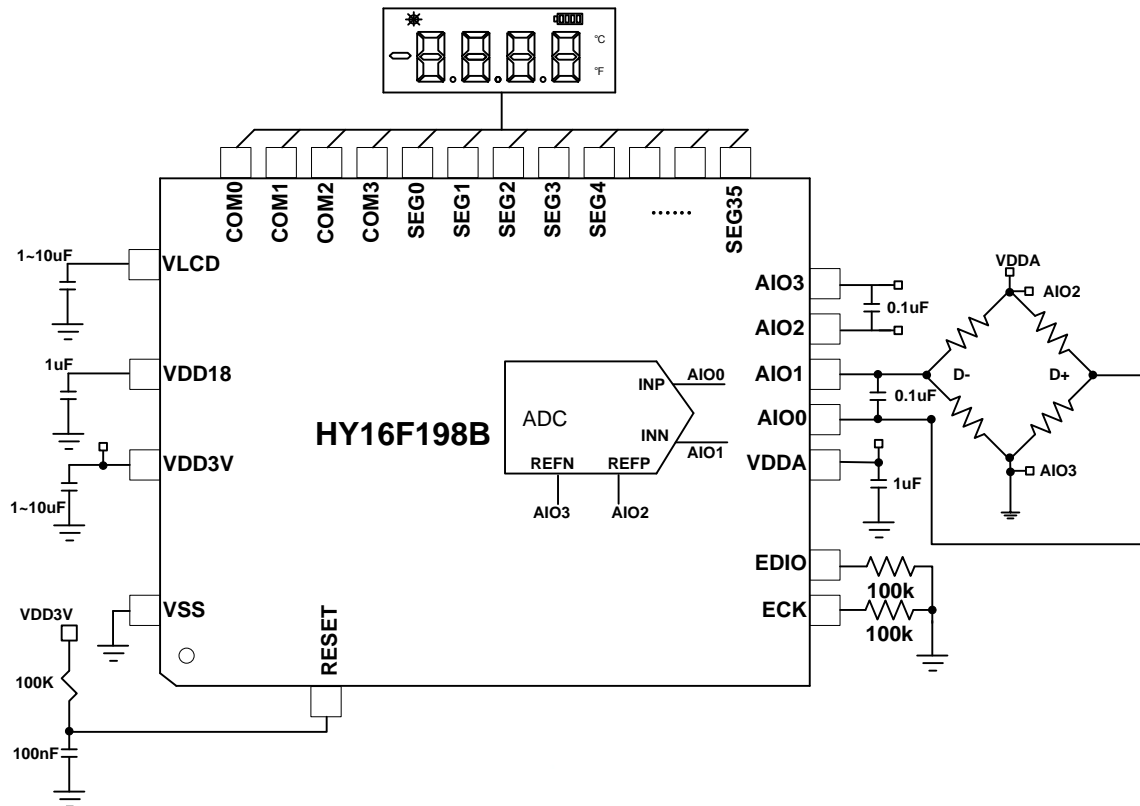


Figure 3-1 Bridge Sensor Circuit

3.2. Blood Pressure Sensor

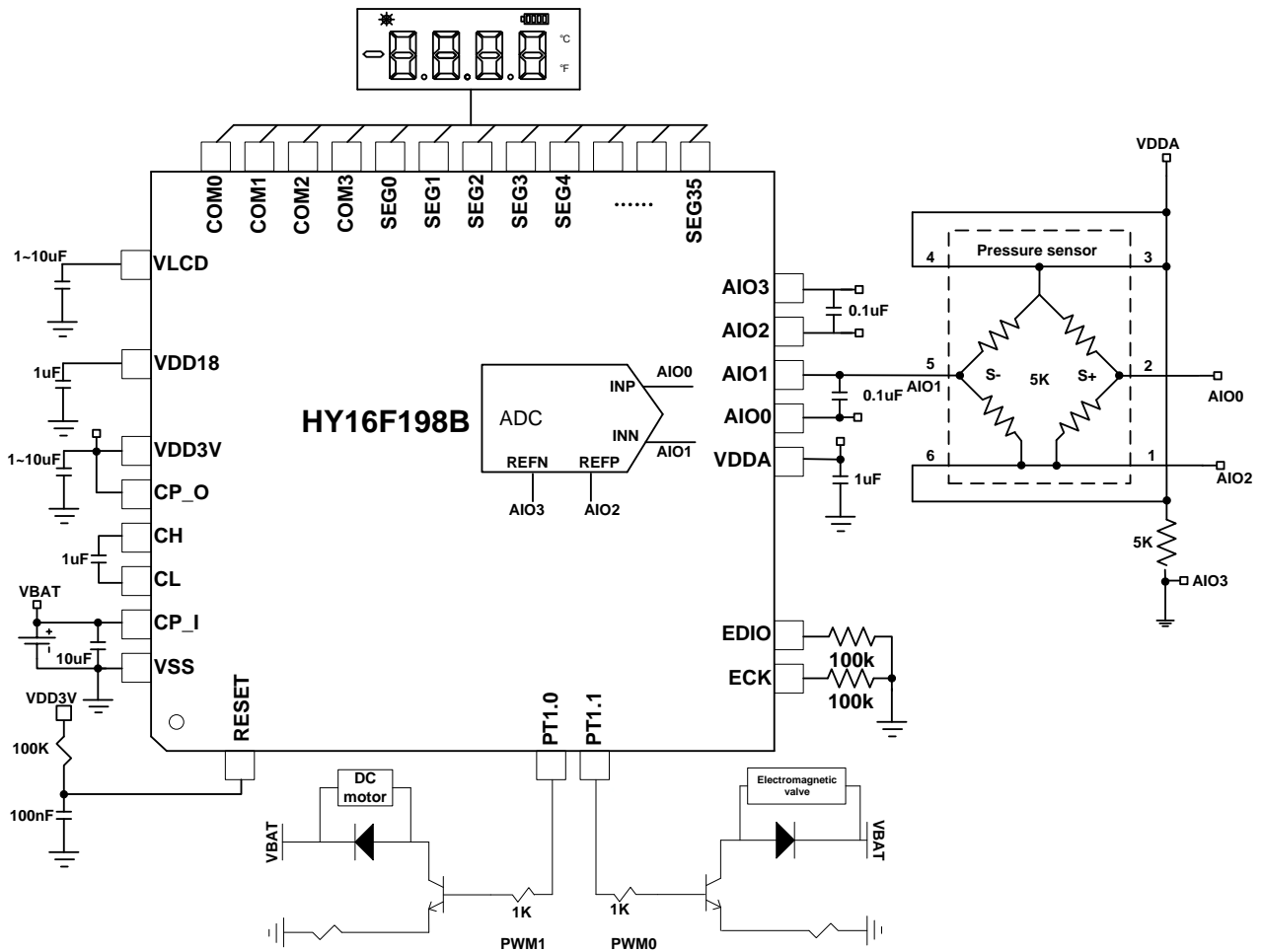


Figure 3-2 Blood Pressure Sensor Circuit

3.3. Electrochemical Sensor

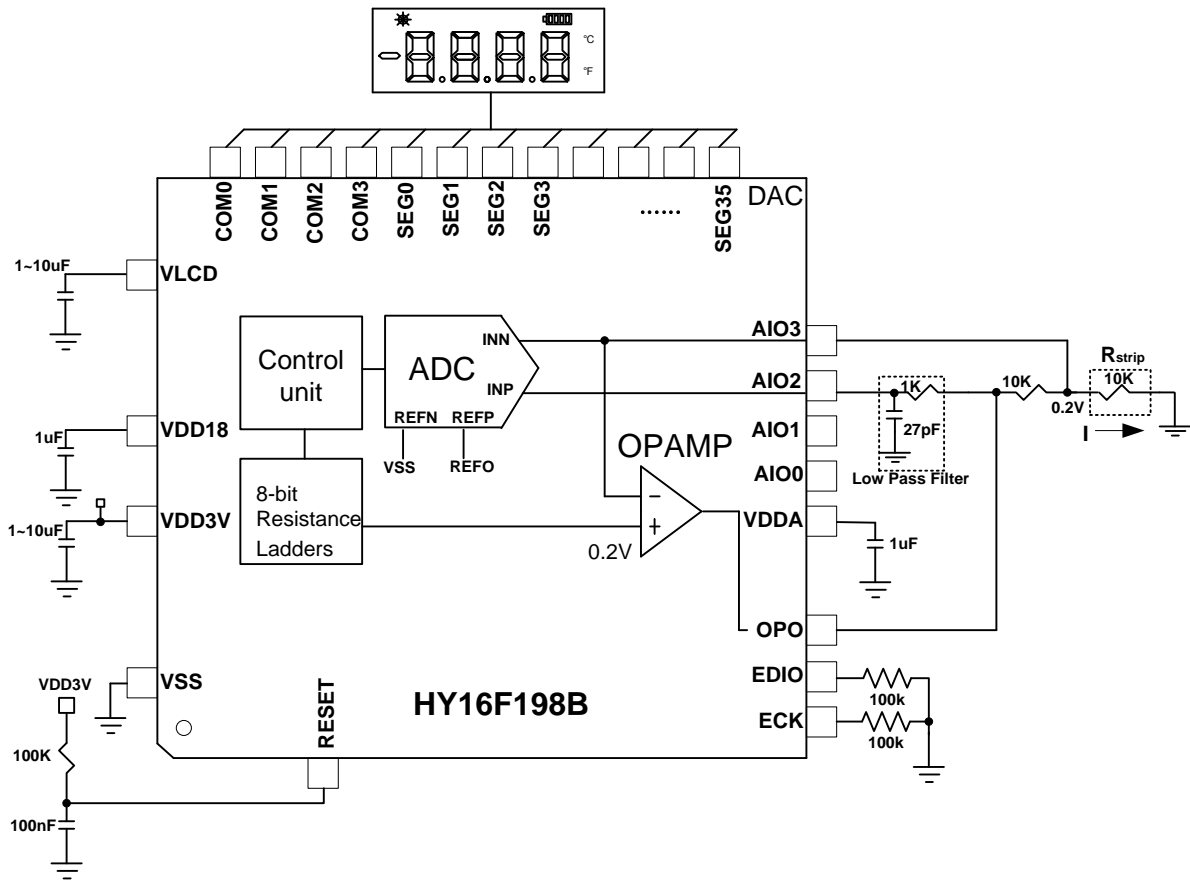


Figure 3-3 Electrochemical Sensor Circuit

3.4. Touch Key Sensor

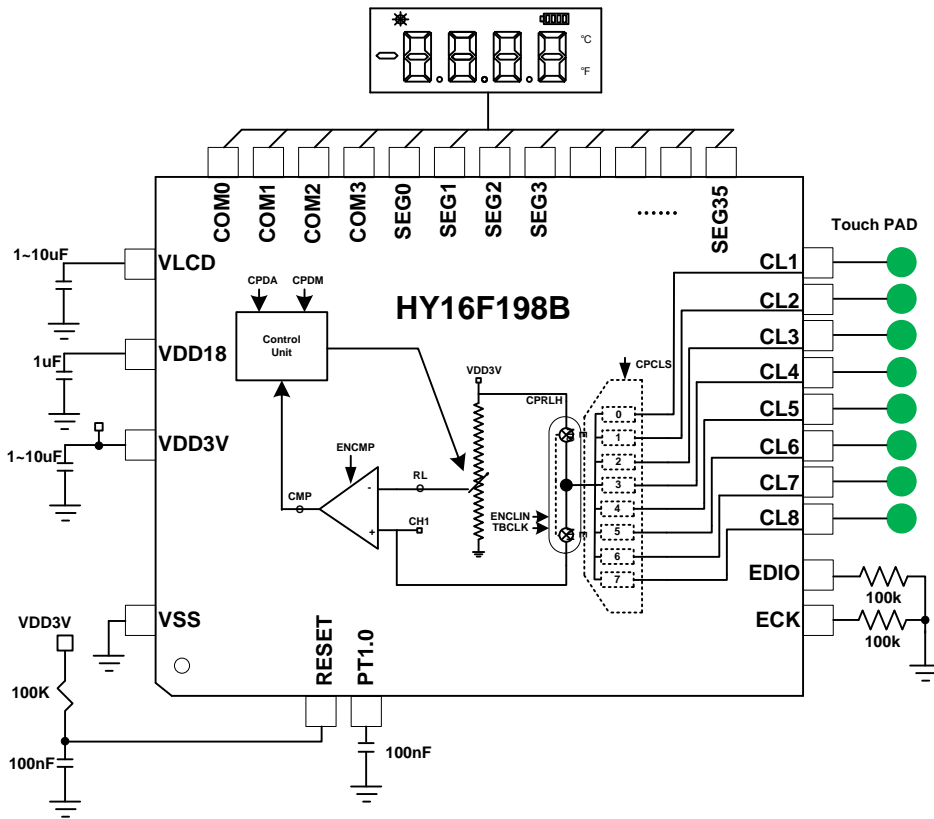


Figure 3-4 Touch Key Sensor Circuit

3.5. 3-in-1 Blood Glucose Meter

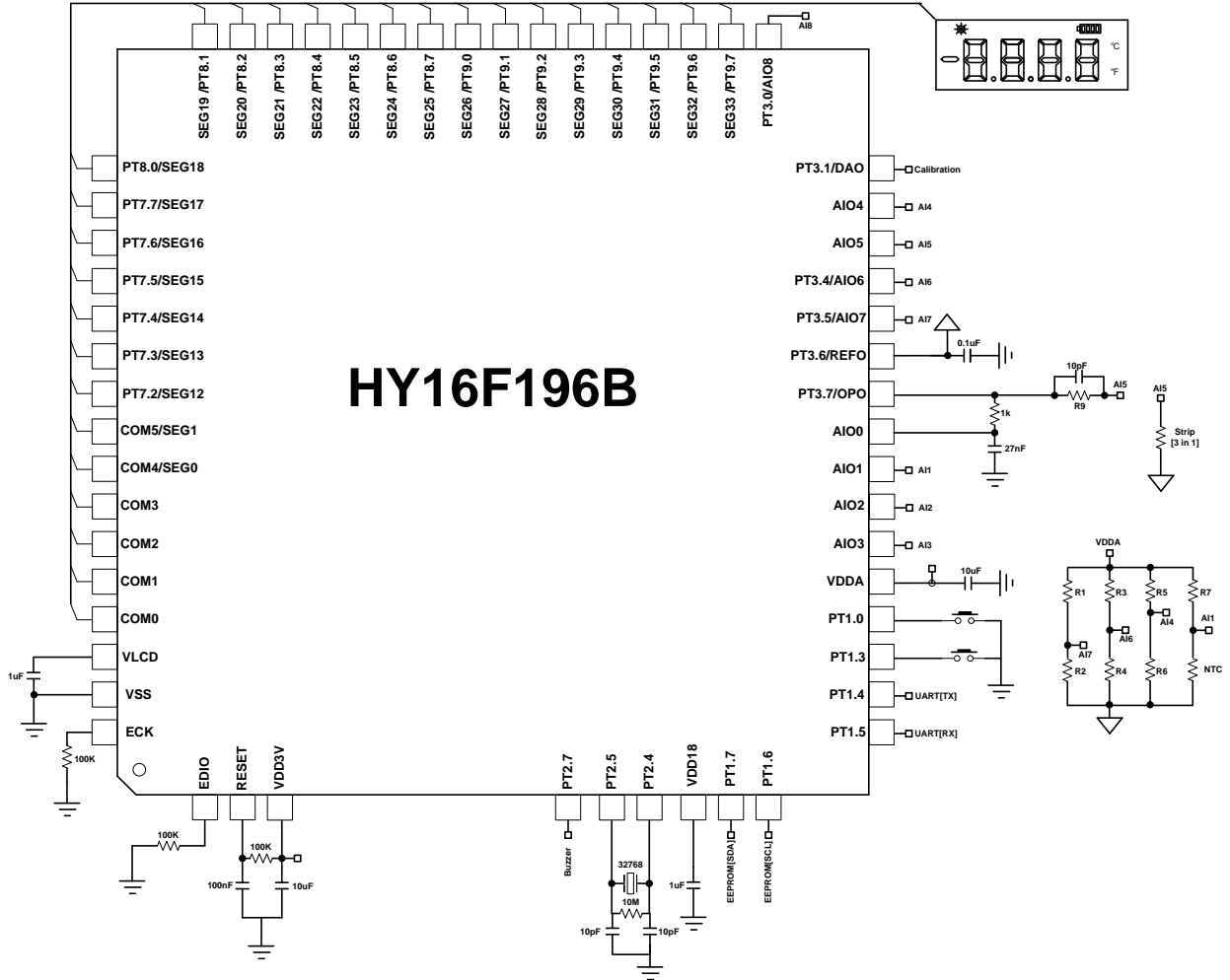


Figure 3-5 3-in-1 Blood Glucose Meter Circuit

4. Function Outline

4.1. Internal Block Diagram

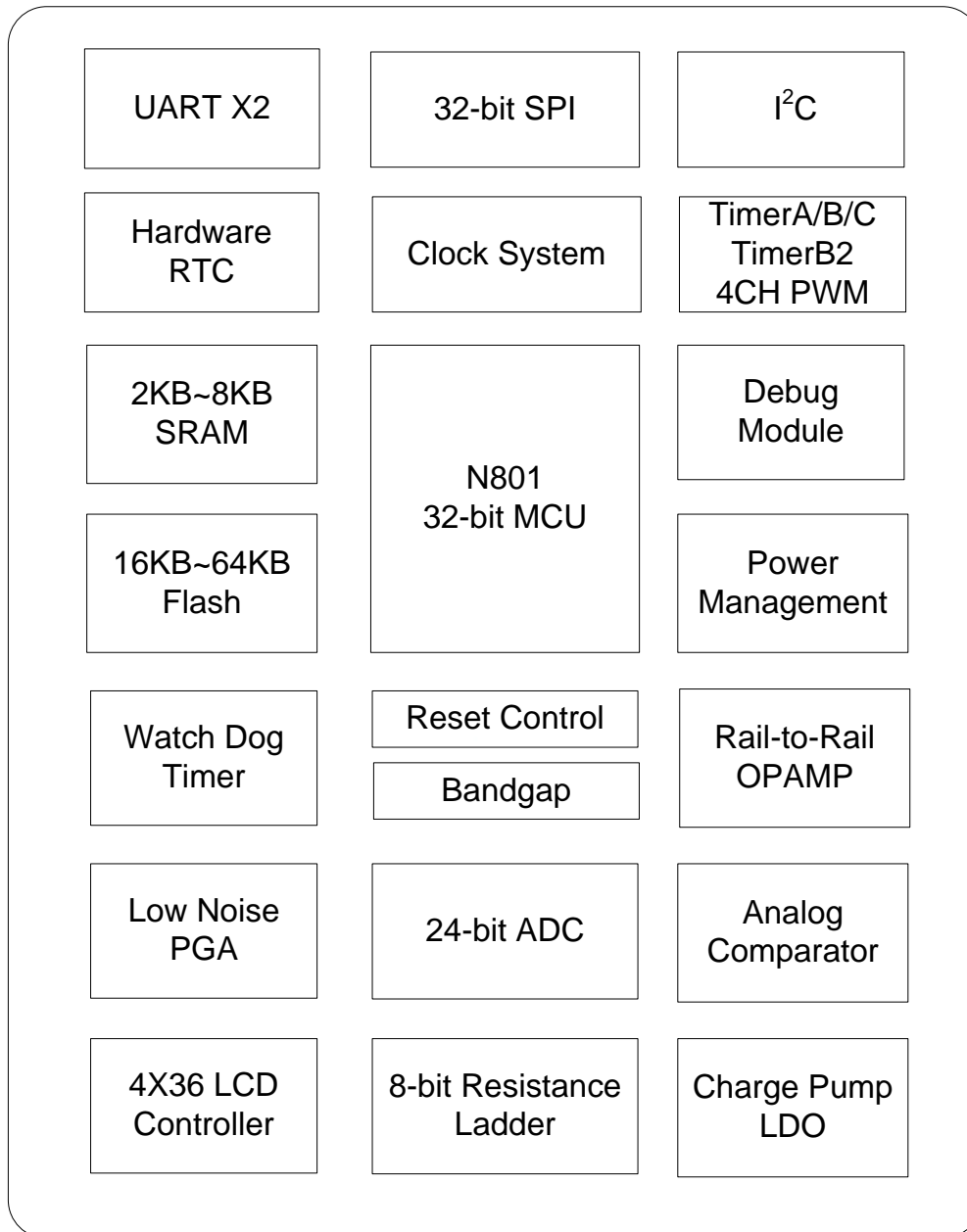


Figure 4-1 HY16F198B Internal Block Diagram

4.2. Building Block Diagram

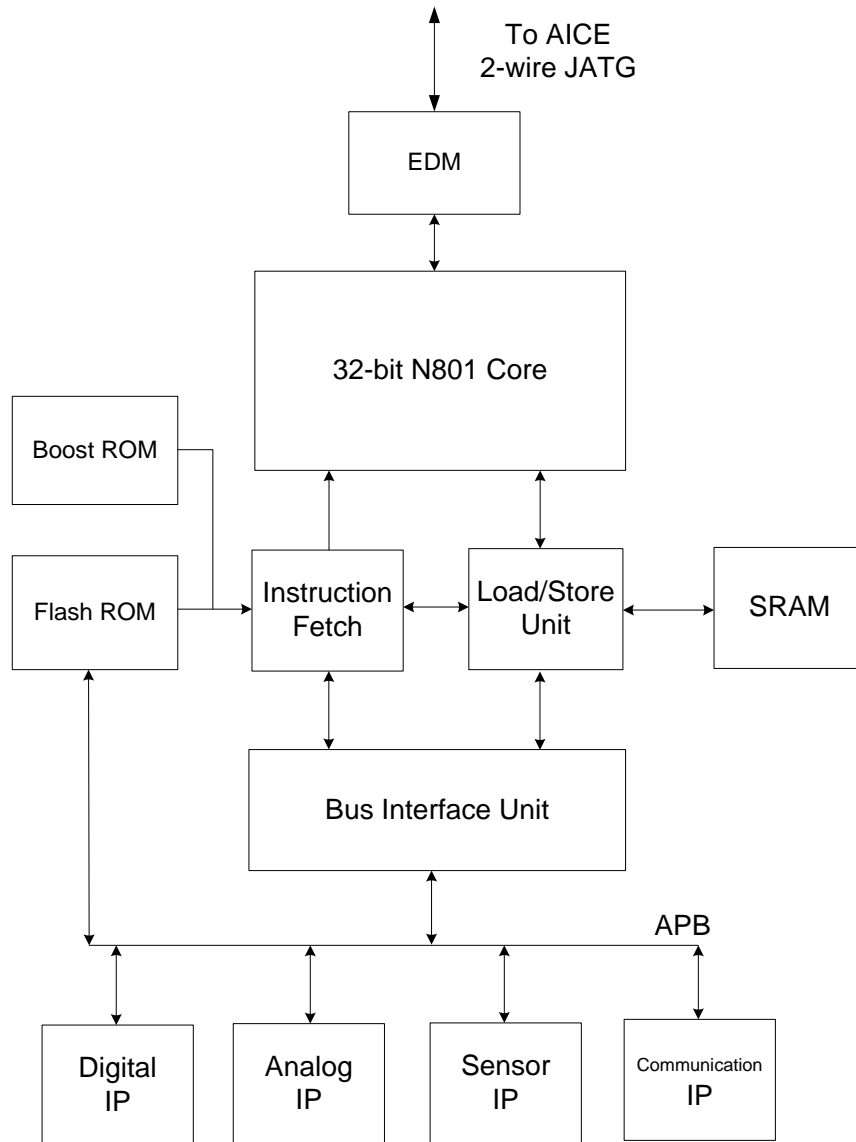
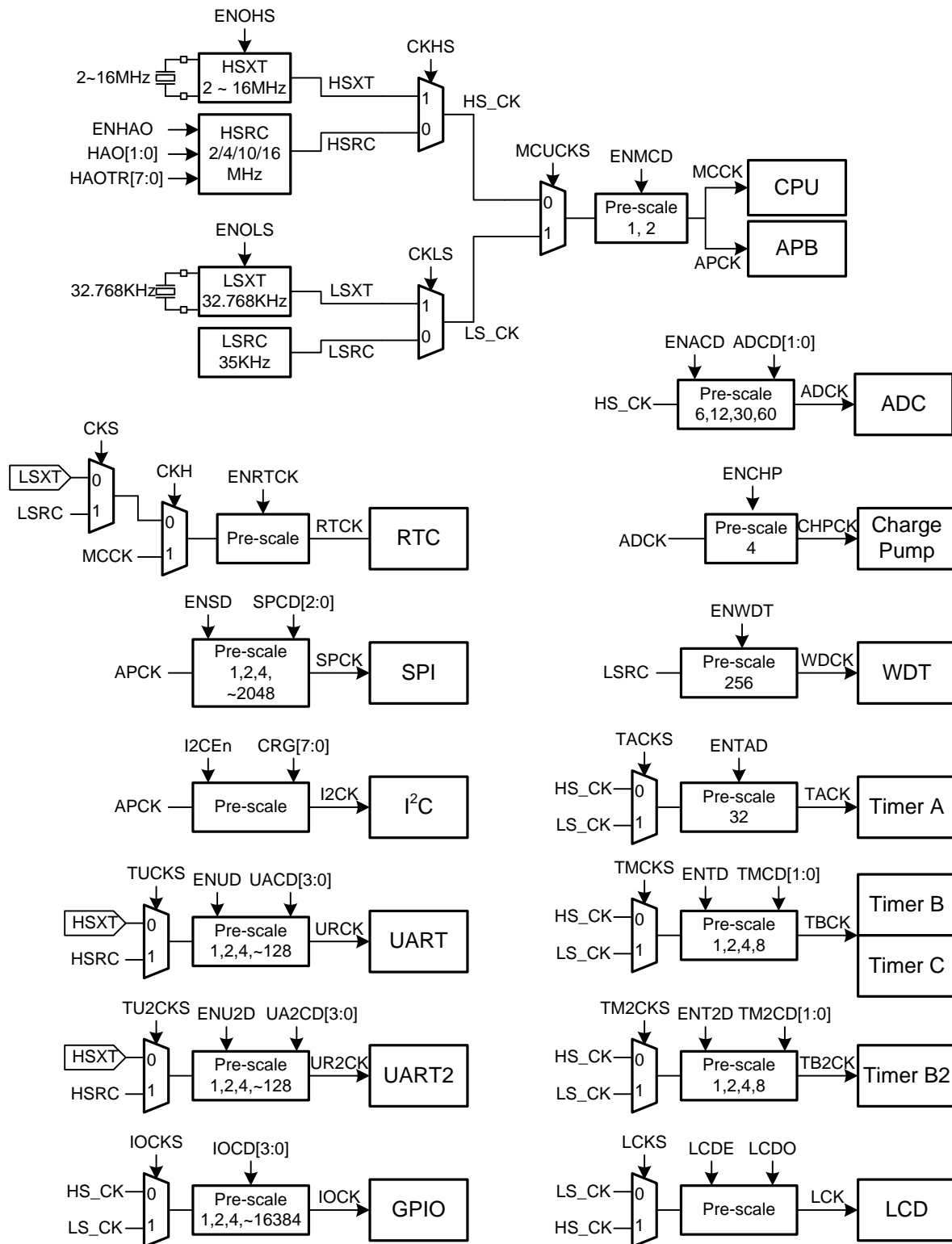


Figure 4-2 Building Block Diagram

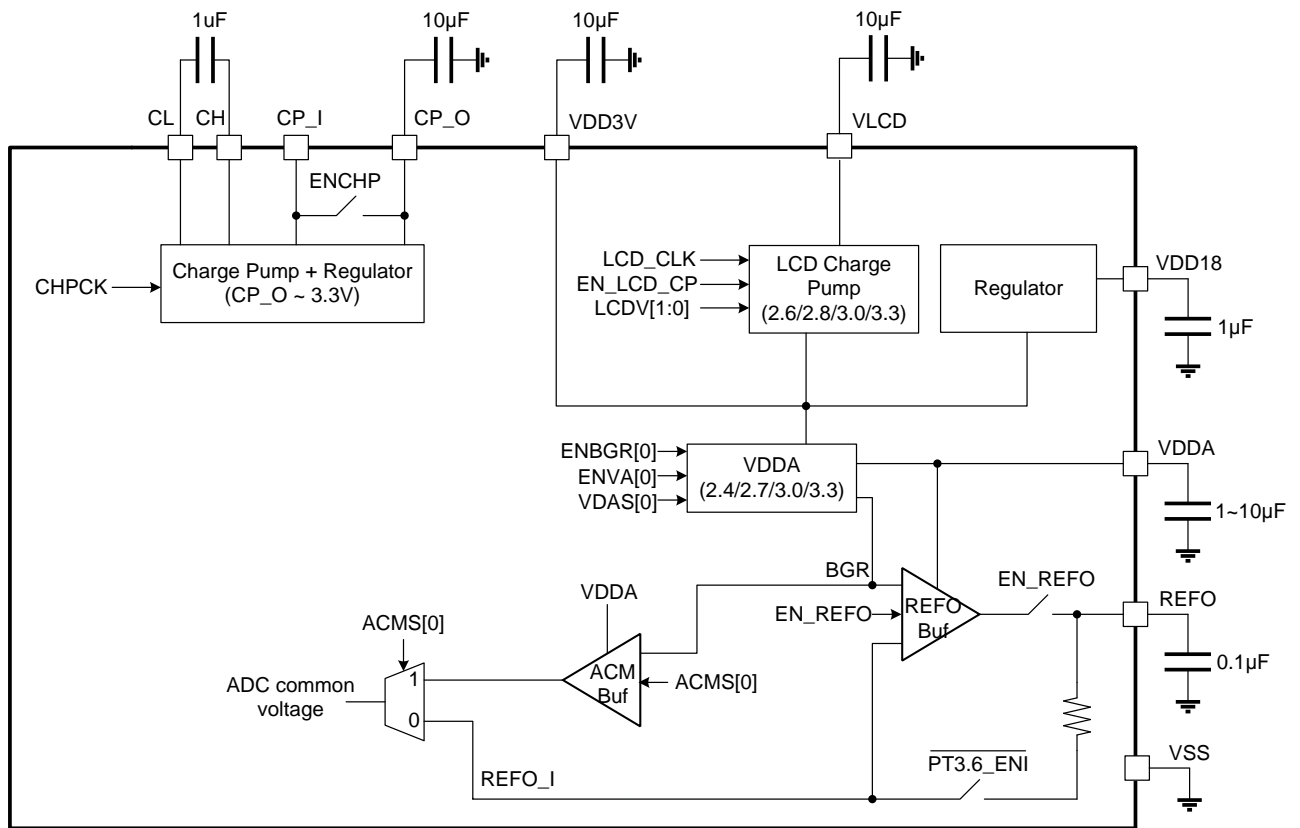
4.3. Related Description and Supporting Document

File Name	Description
UG-HY16F198B_EN	HY16F198B User Guide
APD-HY16IDE007	HY16F19X C Library Manual
APD-HY16IDE005	HY16F19X C Compile operation description
APD-HY16IDE008	HY16F19X IP User Manual
APD-HY16IDE001	HY16F Series IDE Software User Manual/ HY16F Series Device setup file
APD-HY16IDE009	HY16F Series IDE Hardware User Manual
APD-HY16IDE006	HY16F Series Writer kit User Manual

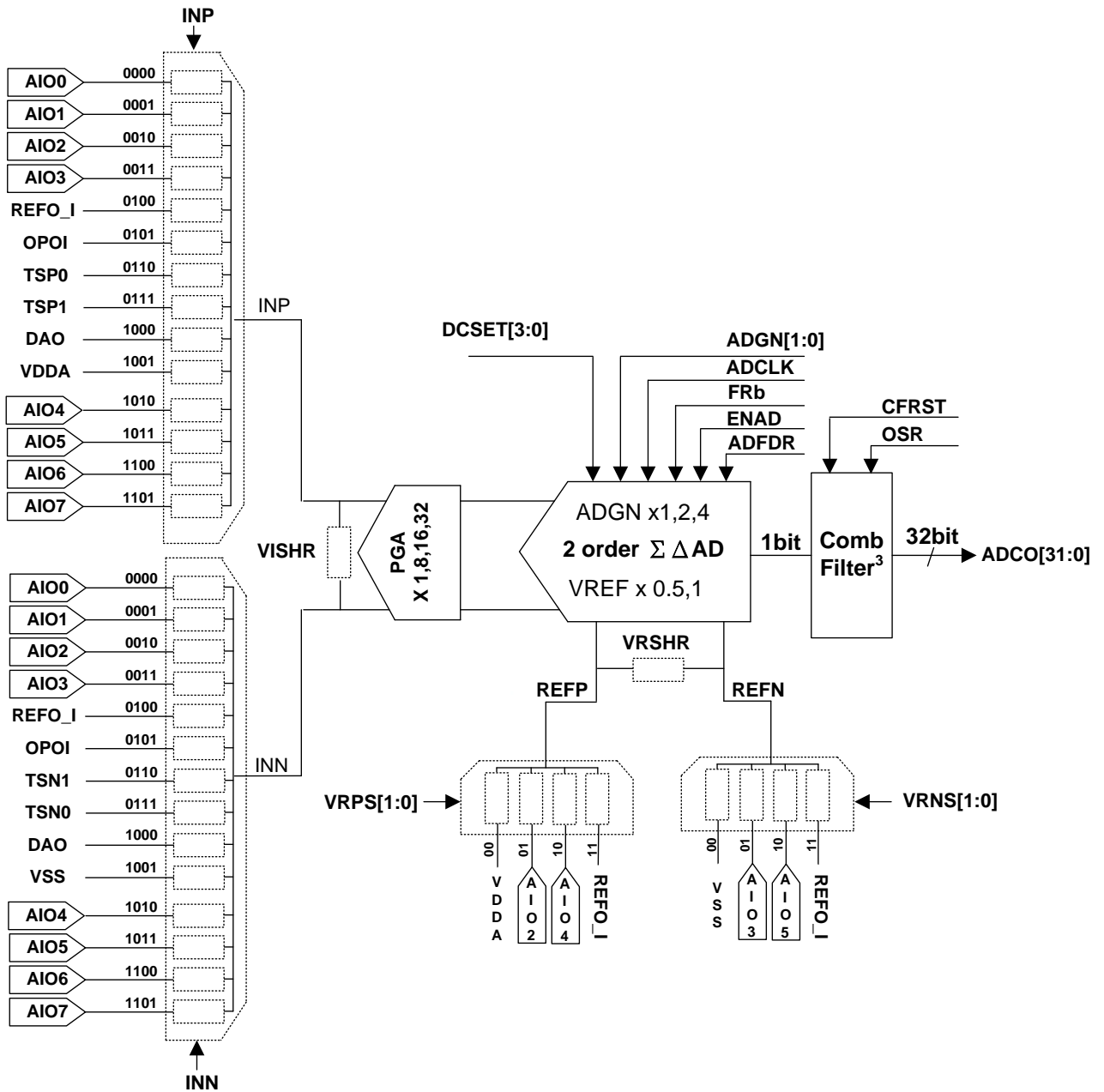
4.4. Clock System Network



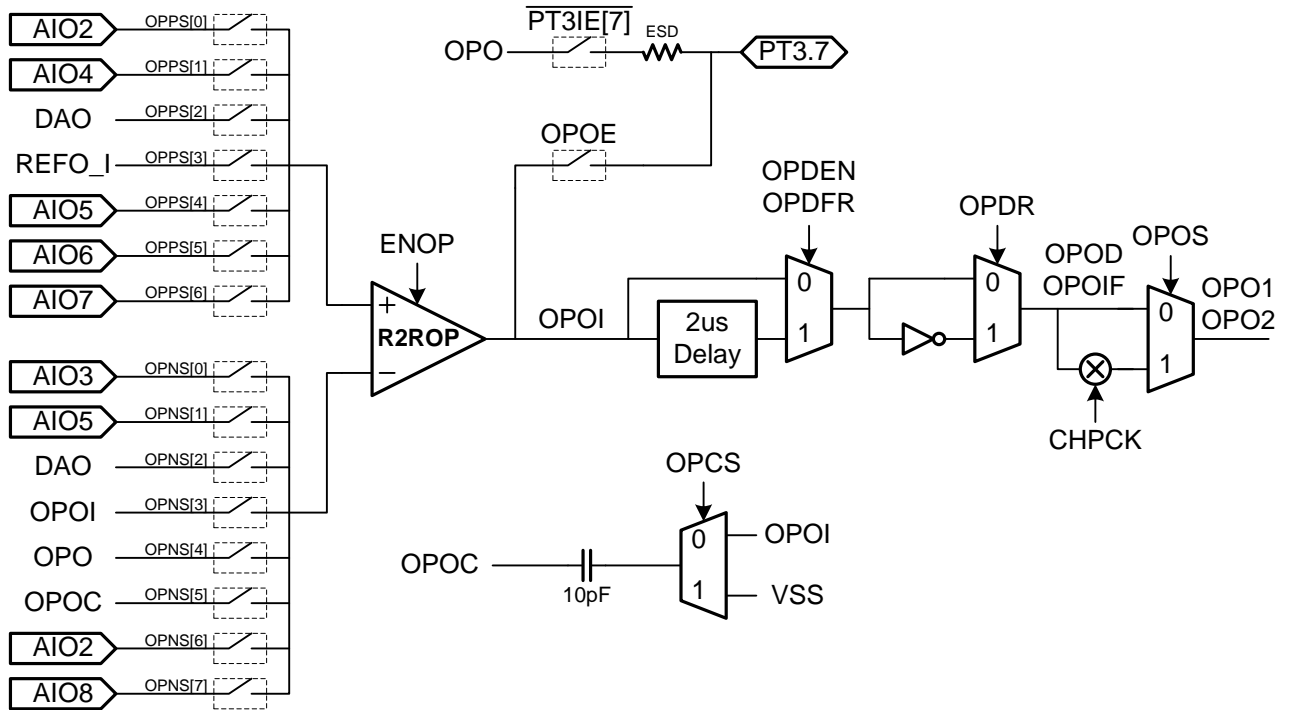
4.5. Power System Network



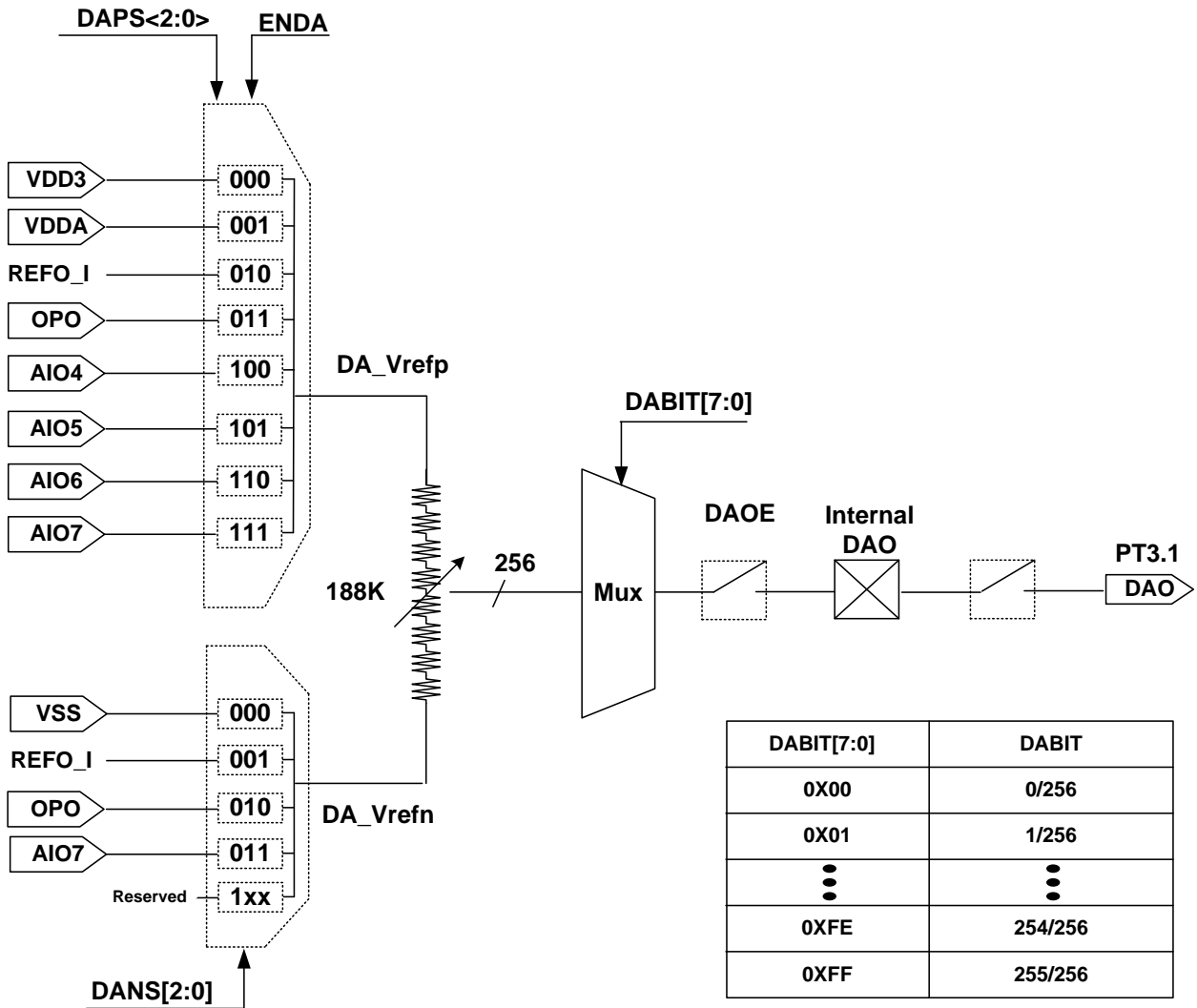
4.6. 24-bit $\Sigma\Delta$ ADC Network



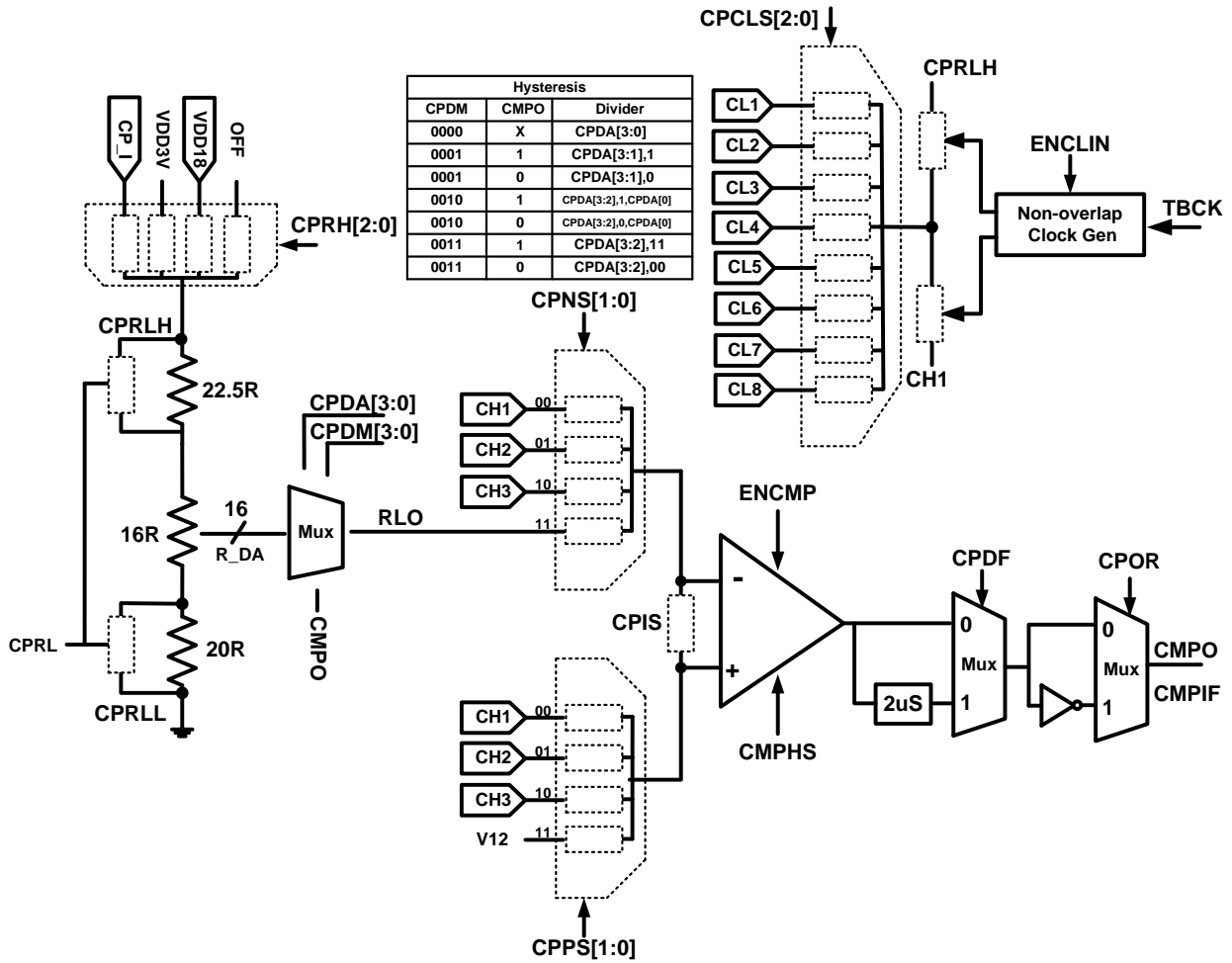
4.7. Rail to Rail OPAMP Network



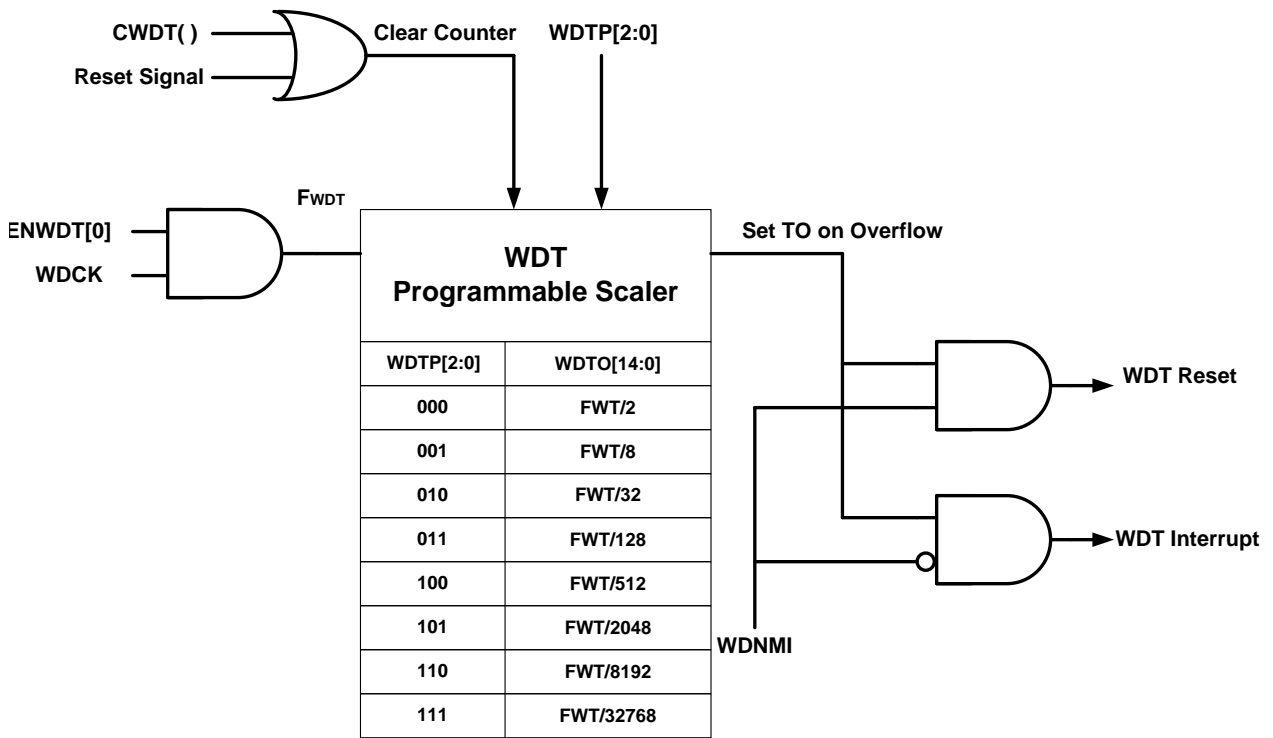
4.8. 8-bit Resistance Ladder Network



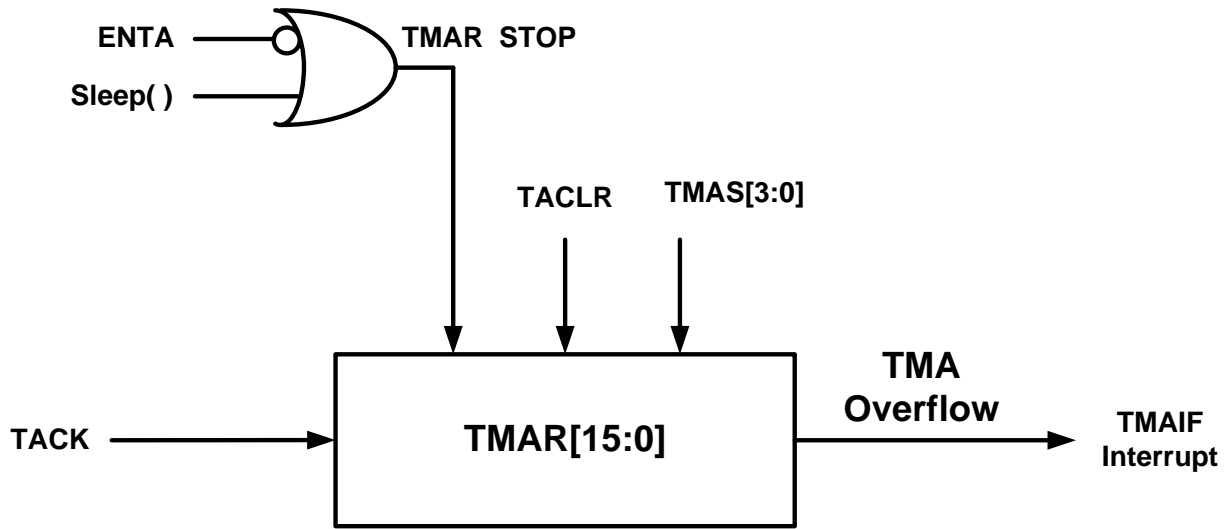
4.9. Analog Comparator Network



4.10. Watch Dog Timer Network

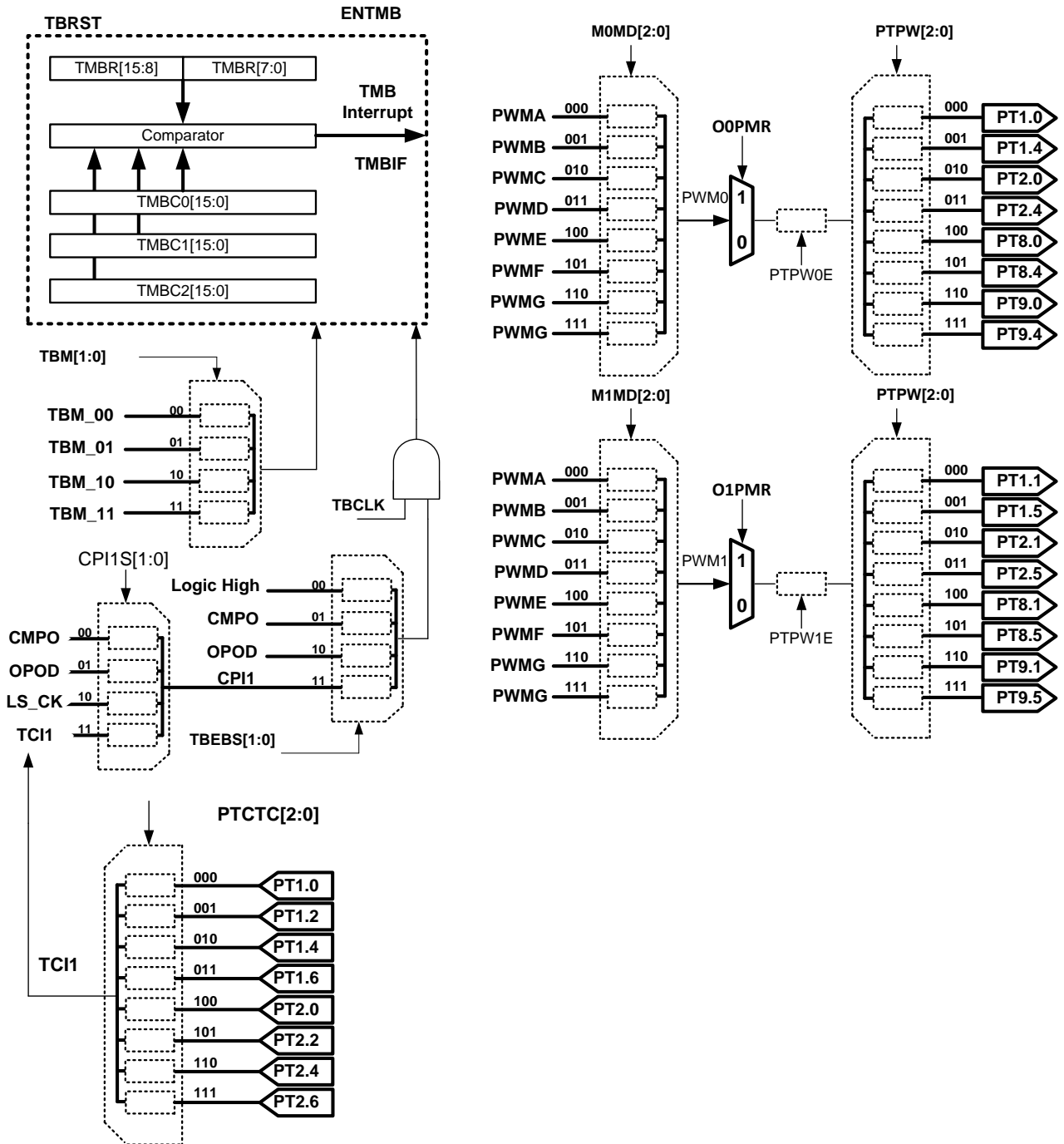


4.11. Timer A Network

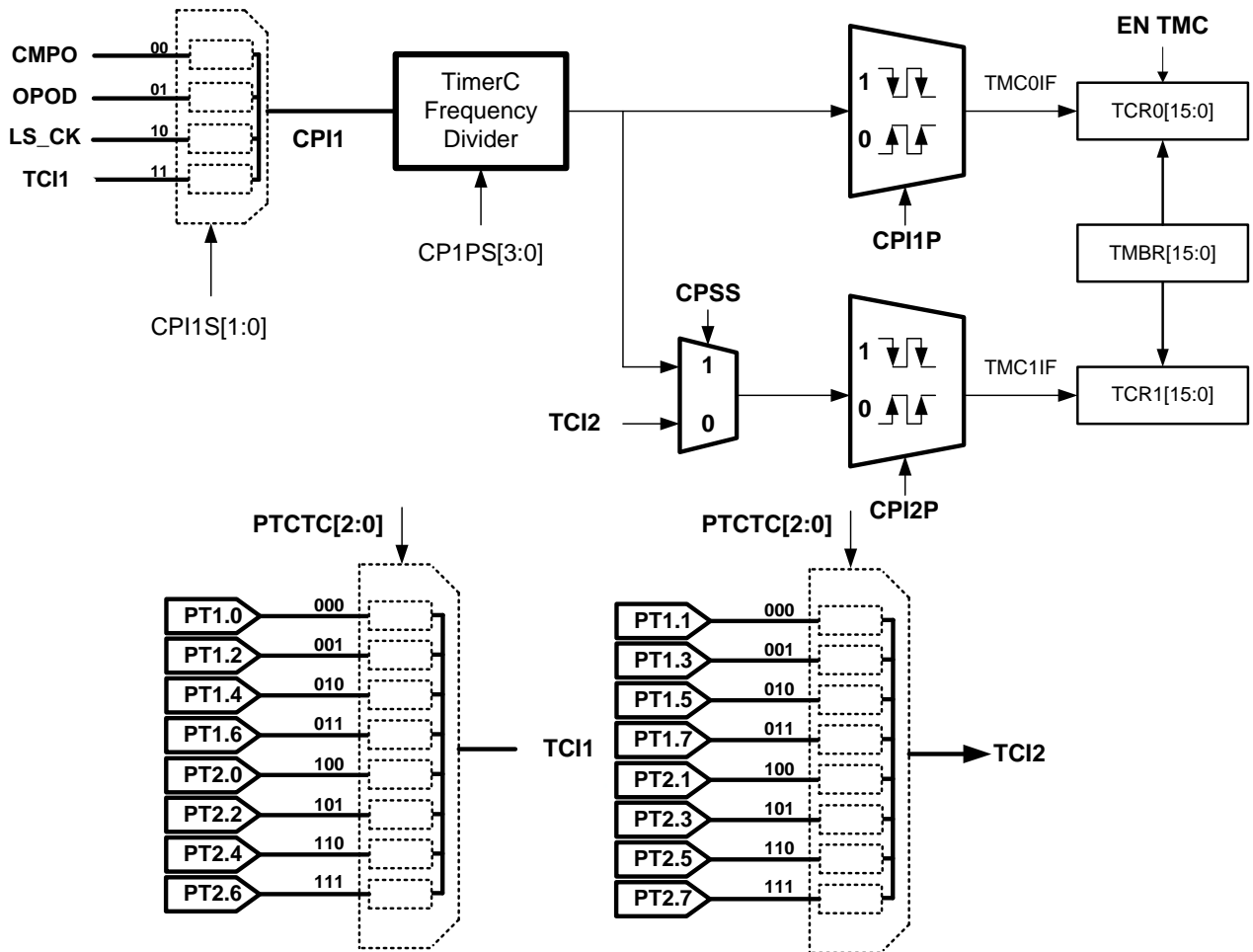


TMAS[3:0]	TMAR[15:0]	TMAS[3:0]	TMAR[15:0]
0000	TACK/2	1000	TACK/512
0001	TACK/4	1001	TACK/1024
0010	TACK/8	1010	TACK/2048
0011	TACK/16	1011	TACK/4096
0100	TACK/32	1100	TACK/8192
0101	TACK/64	1101	TACK/16384
0110	TACK/128	1110	TACK/32768
0111	TACK/256	1111	TACK/65536

4.12. Timer B Network

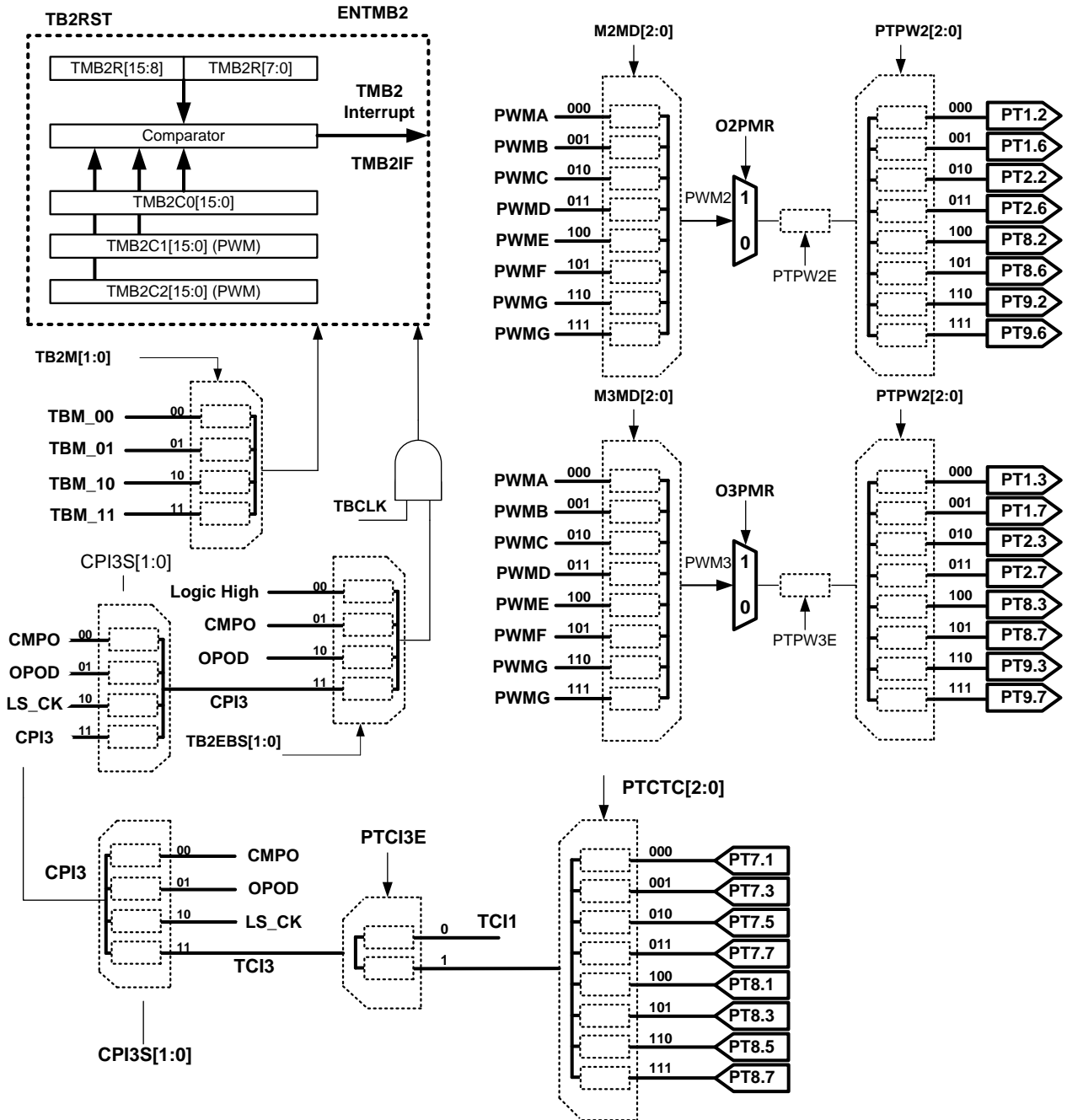


4.13. Timer C Network

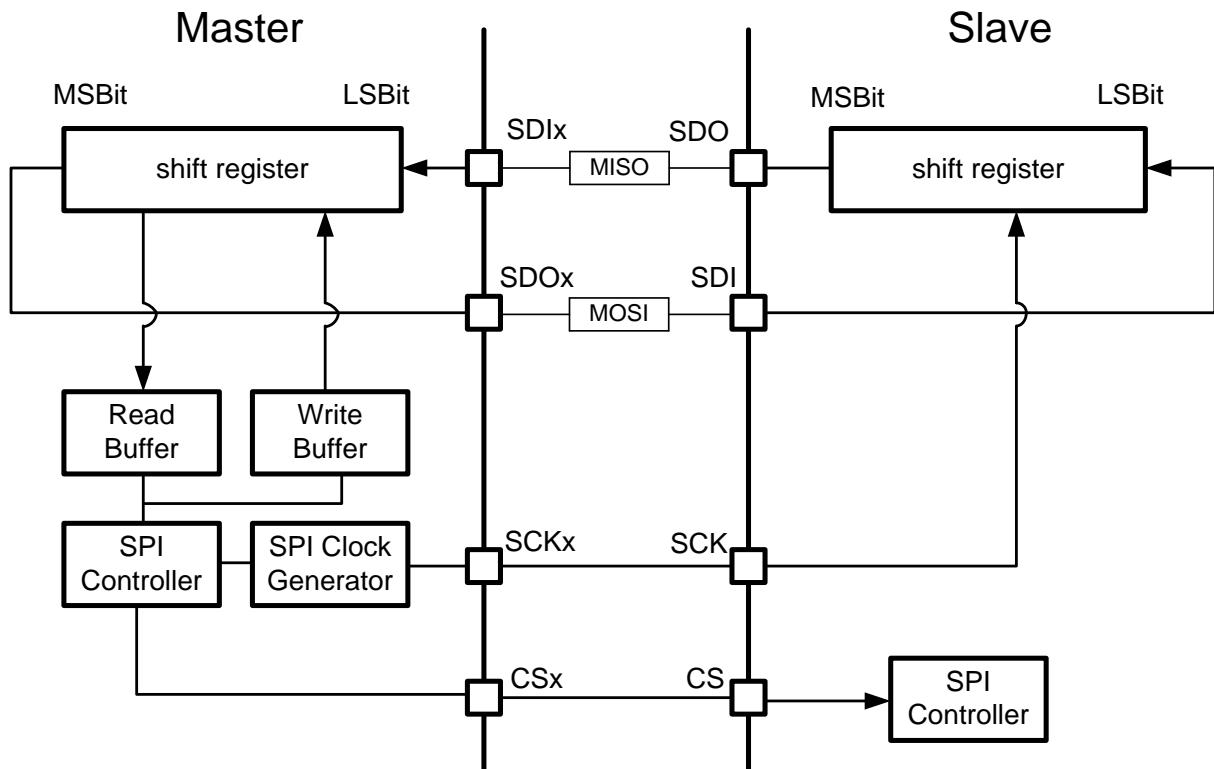


CP1PS[3:0]	CPI1 Divider	CP1PS[3:0]	CPI1 Divider
0000	CPI1/1	1000	CPI1/256
0001	CPI1/2	1001	CPI1/512
0010	CPI1/4	1010	CPI1/1024
0011	CPI1/8	1011	CPI1/2048
0100	CPI1/16	1100	CPI1/4096
0101	CPI1/32	1101	CPI1/8192
0110	CPI1/64	1110	CPI1/16384
0111	CPI1/128	1111	CPI1/32768

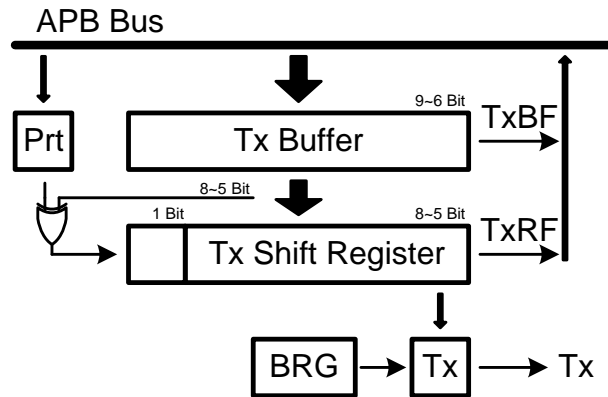
4.14. Timer B2 Network



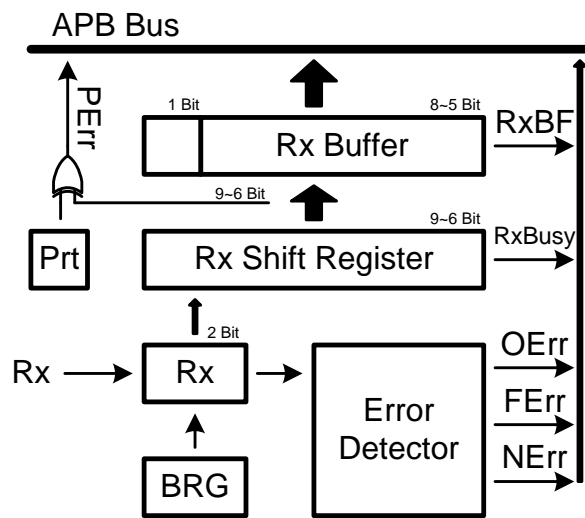
4.15. 32-bit SPI Diagram



4.16. UART Block Diagram

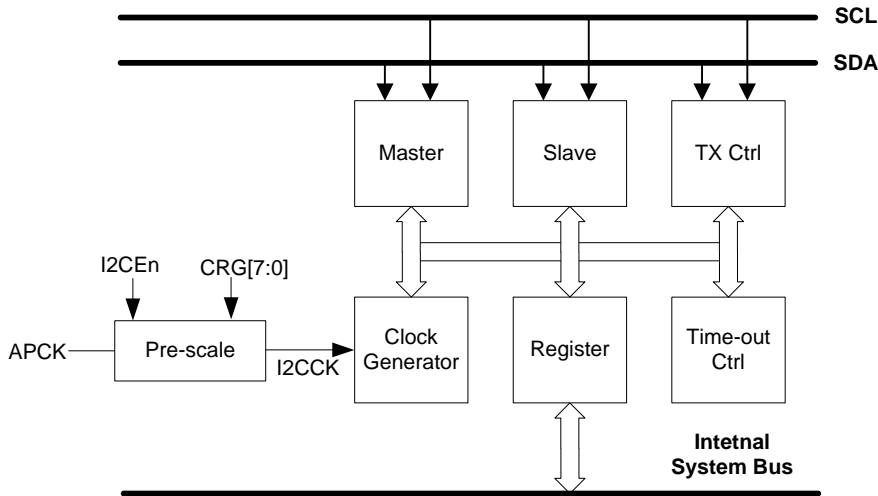


UART Transmit Block Diagram

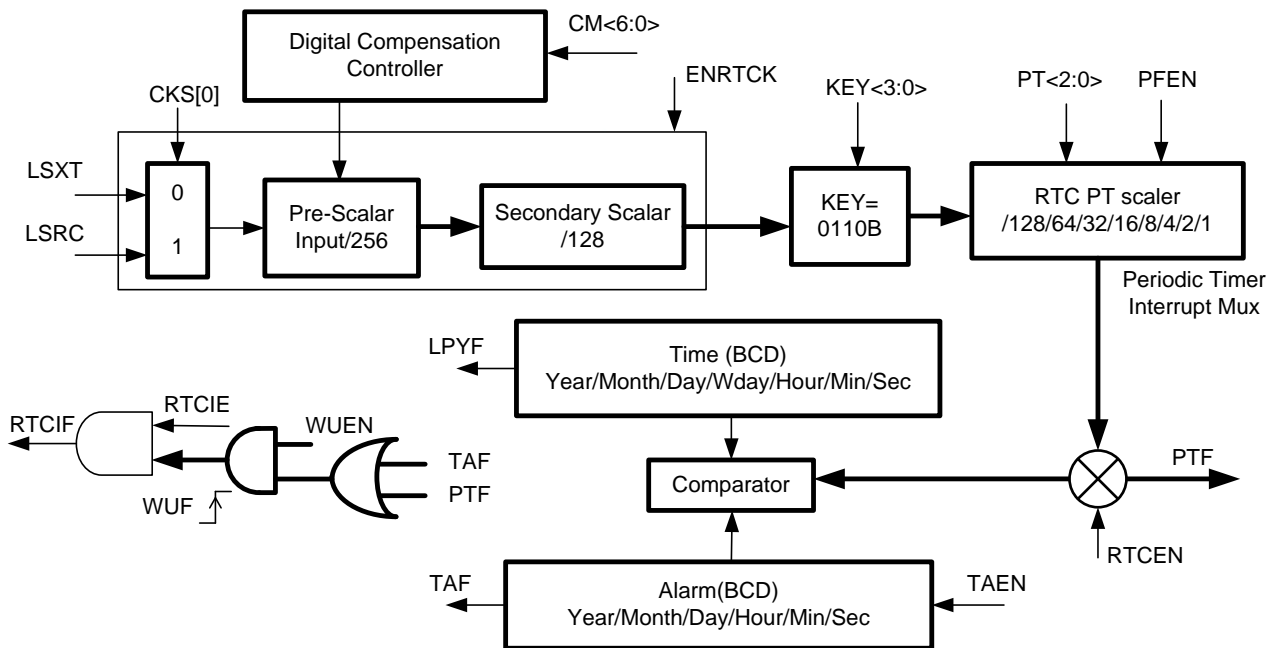


UART Receive Block Diagram

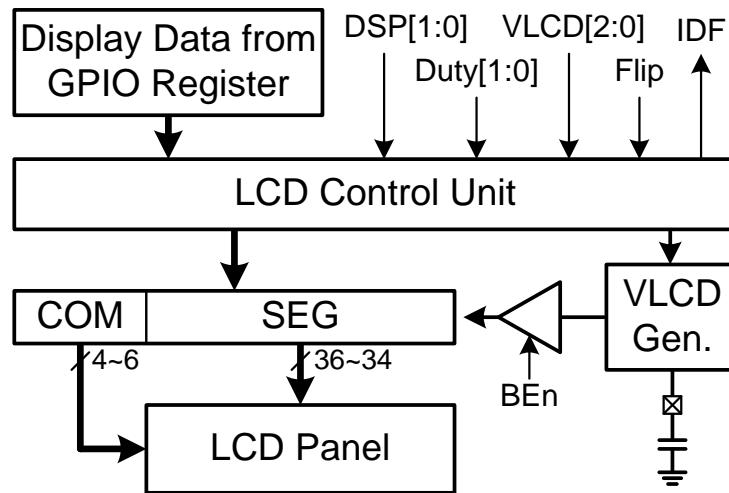
4.17. I²C Block Diagram



4.18. Hardware RTC Block Diagram



4.19. LCD Function Configuration



5. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD3V to VSS	-0.2 V to 4.0 V
Voltage applied to any pin	-0.2 V to VDD3V + 0.3 V
Diode current at any device terminal	±2mA
Storage temperature, Tstg: (UN programmed device)	-55°C to 150°C
(Programmed device)	-40°C to 85°C
Operating Temperature	-40°C to 85°C
Soldering Temperature (10 Sec)	+260°C
Maximum output current sink by any PORT1 to PORT10 I/O PIN	10mA

5.1. Recommended Operating Conditions

VDD3V=2.2V to 3.6V.TA=25°C, Unless Otherwise Noted

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD3V	Digital Application	2.2	3.0	3.6	V
Supply Current	I_Sleep	Sleep Mode ,VDD18 LDO OFF Sleep Mode ,VDD18 LDO ON		2.5 3.5		uA
	I_Idle01	LSRC=35KHz+IDLE Mode		5.0		uA
	I_Idle02	HSRC=2MHz+IDLE Mode		50		uA
	I_Wait	LSRC=35KHz+Wait Mode		130		uA
	Free Run_01MHz	HSRC=2MHz@CPU_CK:2MHz/2		0.6		mA
	Free Run_02MHz	HSRC=2MHz@CPU_CK:2MHz		1.0		mA
	Free Run_04MHz	HSRC=4MHz@CPU_CK:4MHz		1.8		mA
	Free Run_10MHz	HSRC=10MHz@CPU_CK:10MHz		3.0		mA
	Free Run_16MHz	HSRC=16MHz@CPU_CK:16MHz		4.0		mA
Power Up Delay	t _{PU,DLY}	Wake Up From Sleep		64		ms

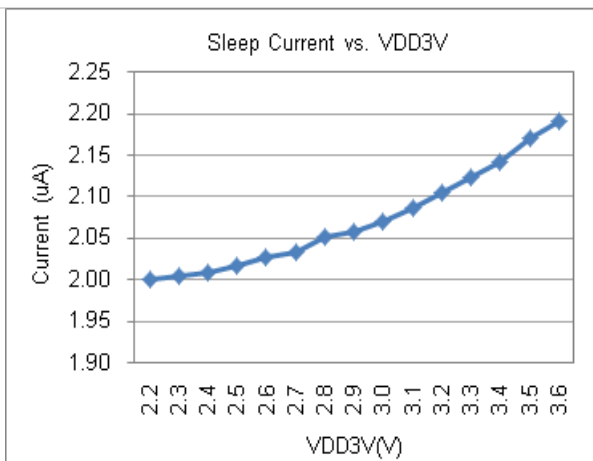


Figure5.1-1 Sleep Current vs. VDD3V

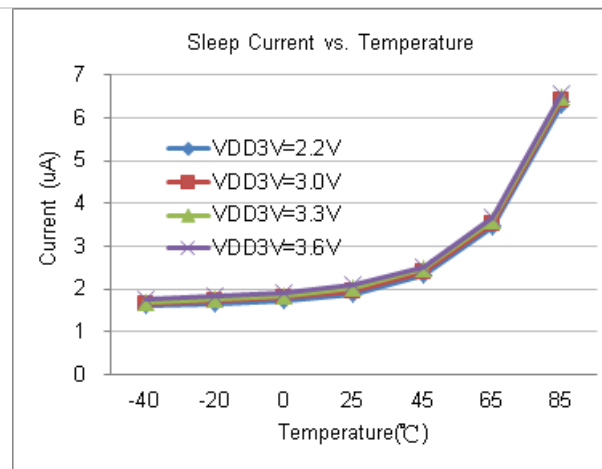


Figure5.1-2 Sleep Current vs. Temperature

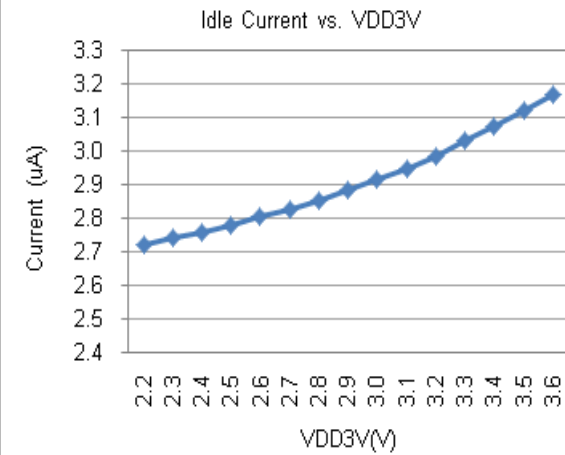


Figure 5.1-3 Idle Current vs. VDD3V

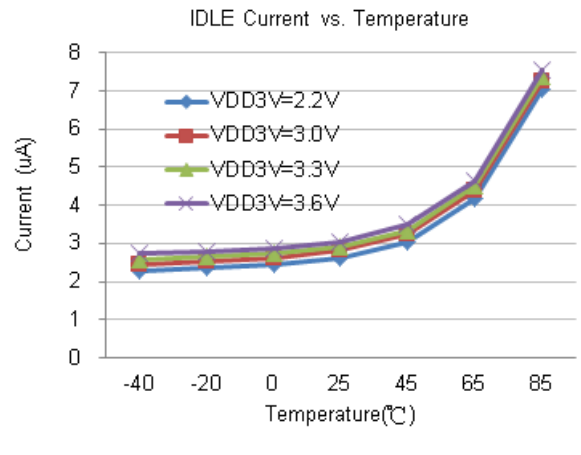


Figure 5.1-4 Idle Current vs. Temperature

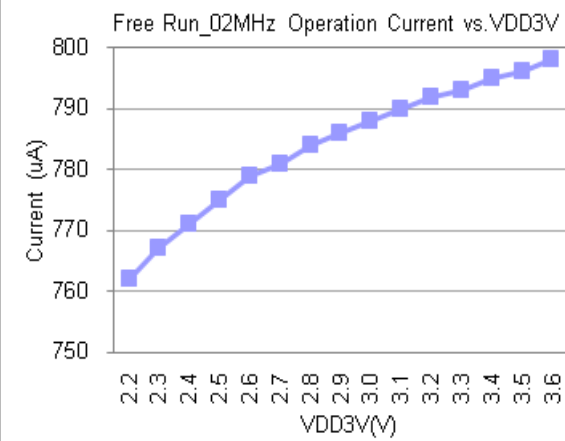


Figure 5.1-5 Free Run_02MHz Operation Current vs. VDD3V

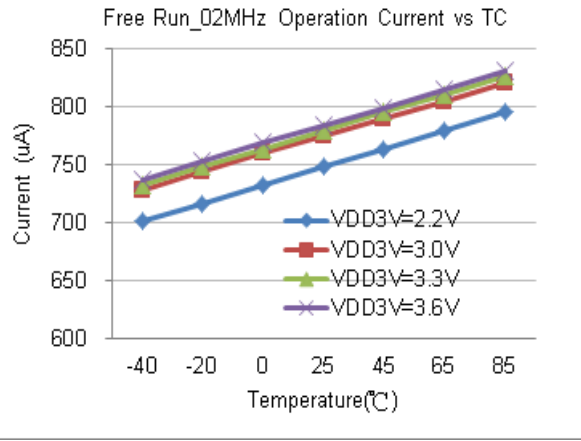


Figure 5.1-6 Free Run_02MHz Current vs. Temperature

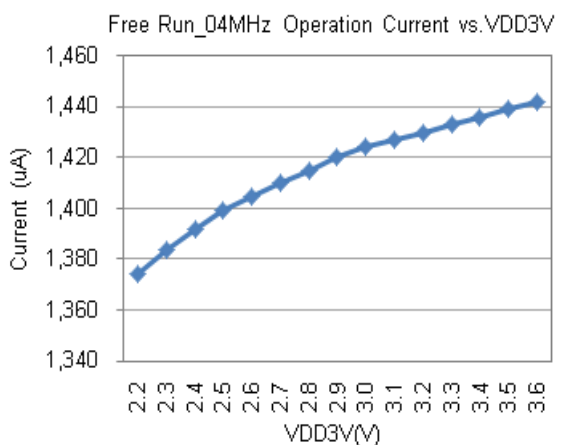


Figure 5.1-7 Free Run_04MHz Operation Current vs. VDD3V

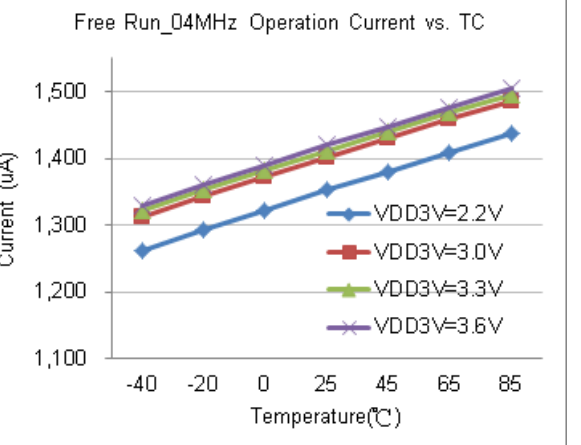


Figure 5.1-8 Free Run_04MHz Current vs. Temperature

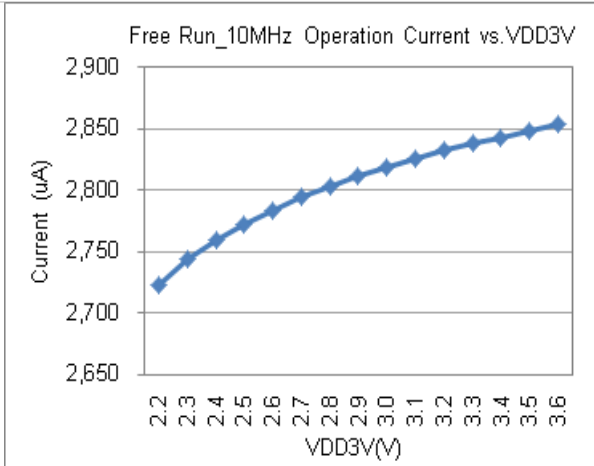


Figure5.1-9 Free Run_10MHz Operation Current vs. VDD3V

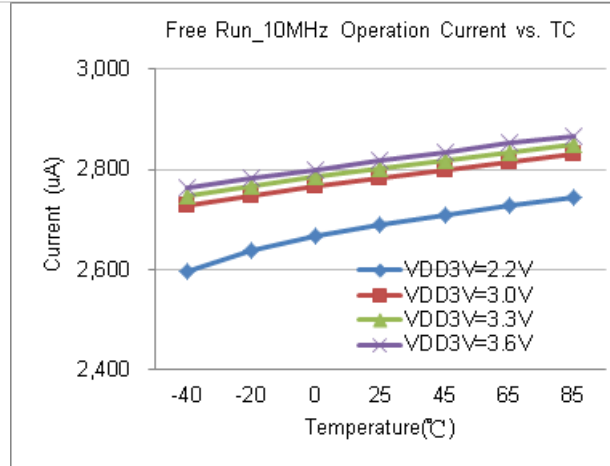


Figure5.1-10 Free Run_10MHz Current vs. Temperature

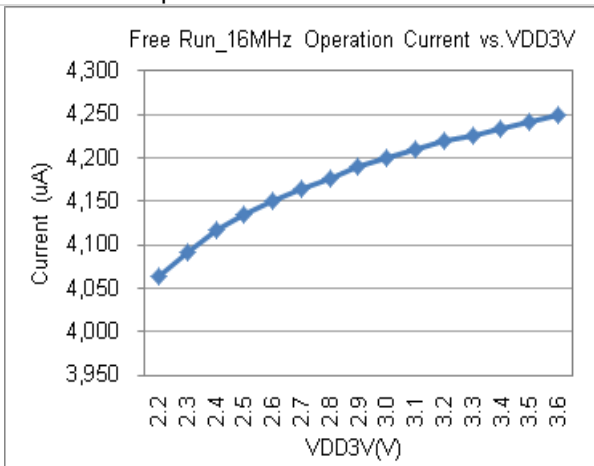


Figure5.1-11 Free Run_16MHz Operation Current vs. VDD3V

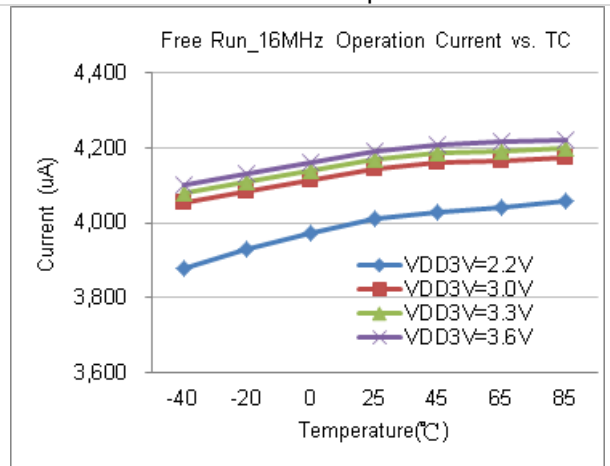


Figure5.1-12 Free Run_16MHz Current vs. Temperature

5.2. Clock System

Typical values are at $T_A=25^{\circ}\text{C}$ and $V_{DD3V} = 3.0\text{V}$. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
External High Speed Oscillator						
VDD3V	Operation voltage		2.2		3.6	V
HSXT	High speed oscillator frequency	VDD3V = 2.2V ~ 3.6V OHS_HS = 1b	4		16	MHz
		VDD3V = 2.2V ~ 3.6V OHS_HS = 0b	2		4	MHz
I _{XHS}	High speed oscillator current	HSXT = 16MHz		100		uA
D _{XHS}	Duty of high oscillator		40		60	%
External Low Speed Oscillator						
LSXT	Low speed oscillator frequency	VDD3V = 2.2V ~ 3.6V		32.768		KHz
I _{XLS}	Low speed oscillator current			2		uA
D _{XLS}	Duty of low speed oscillator		40		60	%
RTC	Normal Mode	VDD3V=3.3V @Flash Run		10		uA
Internal High Speed Oscillator						
F _{HAO}	Internal high speed oscillator frequency	F _{HAO} = 2MHz F _{HAO} = 2MHz, after trim ^{Note1}	-10% -2%	2 1.843	+10% +2%	MHz
		F _{HAO} = 4MHz F _{HAO} = 4MHz, after trim ^{Note1}	-10% -2%	4 4.147	+10% +2%	MHz
		F _{HAO} = 10MHz F _{HAO} = 10MHz, after trim ^{Note1}	-10% -2%	10 9.216	+10% +2%	MHz
		F _{HAO} = 16MHz F _{HAO} = 16MHz, after trim ^{Note1}	-10% -2%	16 15.667	+10% +2%	MHz
V _{HAO}	Voltage coefficient	VDD3V = 2.2V ~ 3.6V	-0.2		+0.2	%
T _{HAO}	Temperature coefficient	-40~85 ^o C	-1.5		+1.5	%
I _{HAO}	Internal high speed oscillator current	F _{HAO} = 2MHz		20		uA
		F _{HAO} = 16MHz		75		uA
D _{HAO}	Duty of oscillator		40		60	%
WT _{HAO}	Wake up time	F _{HAO} = 2MHz		30		us
Internal Low Speed Oscillator						
F _{LPO}	Internal low speed oscillator frequency	VDD3V = 3.3V	-20%	35	+20%	KHz
V _{LPO}	Voltage coefficient	VDD3V = 2.2V ~ 3.6V	-2.5		+2.5	%
T _{LPO}	Temperature coefficient	-40~85 ^o C	-2.5		+2.5	%
I _{LPO}	Internal low speed oscillator current			0.35	0.7	uA
D _{LPO}	Duty of low speed oscillator		40		60	%

Note1

After trim: According to the factory calibration parameters of HAO to calibrate HAO, and need to correspond to the selected HAO frequency. Configure the register 0x40304[7:0]. Please refer to the chapter 6.1.2 “UG-HY16F198B_EN” to know how to use that in detail.

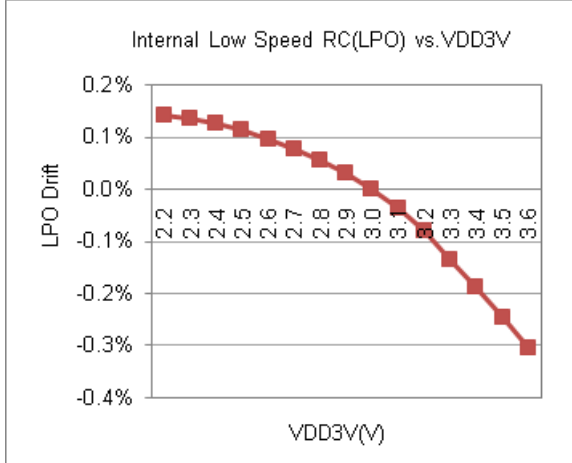


Figure5.2-1 LPO vs. VDD3V

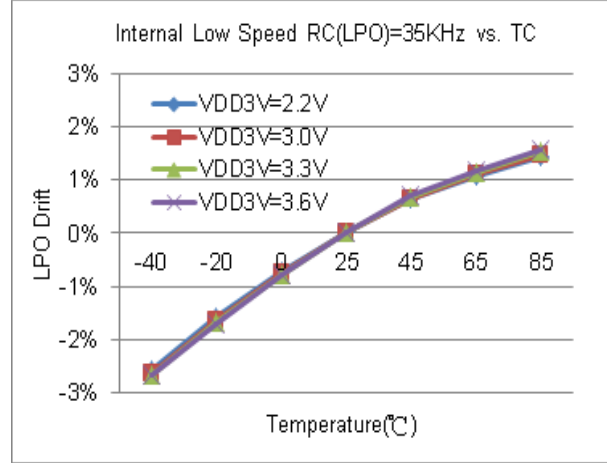


Figure5.2-2 LPO vs. Temperature

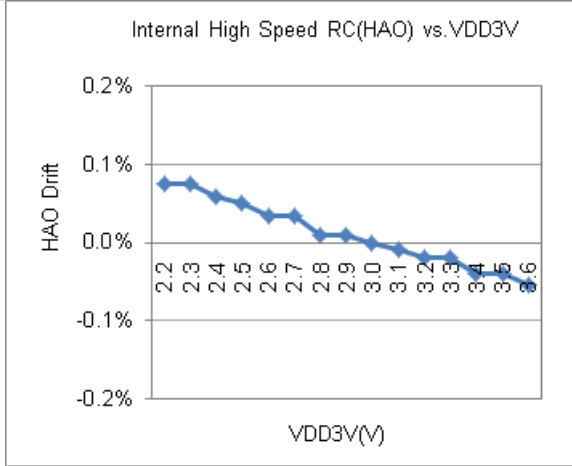


Figure5.2-3 HAO vs. VDD3V

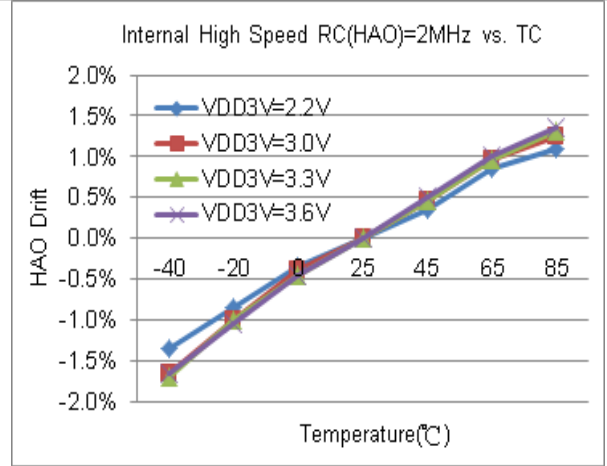


Figure5.2-4 HAO vs. VDD3V

5.3. Power Management System

Typical values are at $T_A=25^{\circ}\text{C}$ and $V_{DD3V} = 3.0\text{V}$. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA LDO						
	Output voltage error		-5		5	%
	Capacitor loading		0.1	1	10	uF
	Settling time	Capacitor loading = 0.1uF, 99% of VDDA		50		us
	Operation current	Bias + Band gap + VDDA LDO		35	50	uA
	Dropout voltage	$I_L=10\text{mA}$		0.2		V
	Voltage coefficient	$V_{DD3V} = 2.5 \sim 3.6\text{V}$		0.1		%/V
	VDDA voltage 1	$I_L = 0.1\text{mA}$		2.4		V
	VDDA voltage 2	$I_L = 0.1\text{mA}$		2.7		V
	VDDA voltage 3	$I_L = 0.1\text{mA}$		3.0		V
	VDDA voltage 4	$I_L = 0.1\text{mA}$		3.3		V
	Temperature coefficient	By using BRG $V_{DDA}=3.0\text{V}$		100		ppm/ $^{\circ}\text{C}$
VDD18 LDO						
	Output voltage		1.7	1.8	1.9	V
	Capacitor loading			1000		nF
	Voltage coefficient	$V_{DD3V}= 2.2 \sim 3.6\text{V}$		1		%/V
	Temperature coefficient			100		ppm/ $^{\circ}\text{C}$
	Load regulation	Load = 0.1~10mA		0.1		V/A
	Dropout voltage	Load = 10mA		0.2		V
REFO Buffer						
	Capacitor loading		22	100	1000	nF
	Operation current			20		uA
	Output current	1% change voltage	-1		1	mA
	Temperature coefficient	$V_{DDA}=3.0\text{V}$		80		ppm/ $^{\circ}\text{C}$
	Offset voltage	$REFO = 1.2\text{V}$		± 3	± 12	mV
	Voltage coefficient	$V_{DDA}= 2.4\text{V} \sim 3.6\text{V}$		0.1		%/V

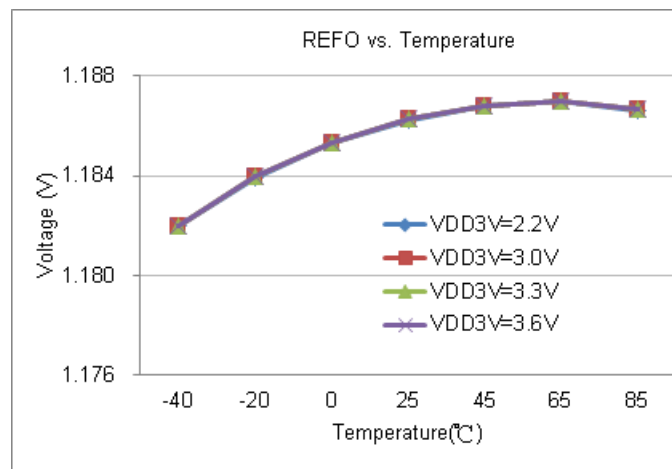


Figure5.3-1 REFO vs. Temperature

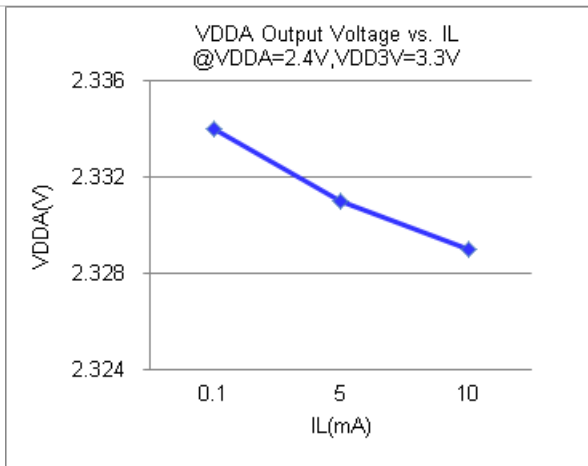


Figure5.3-2 VDDA vs. IL

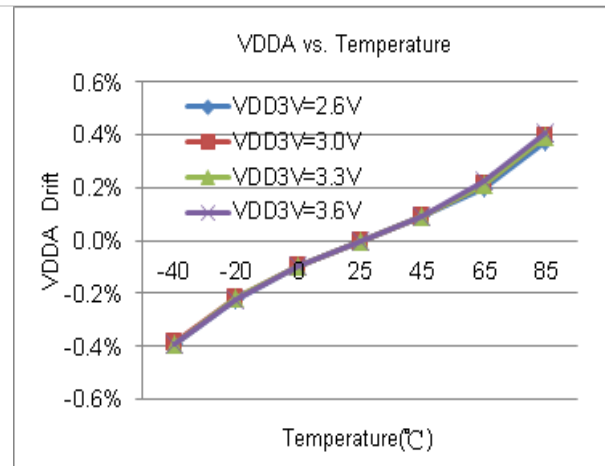


Figure5.3-3 VDDA vs. Temperature

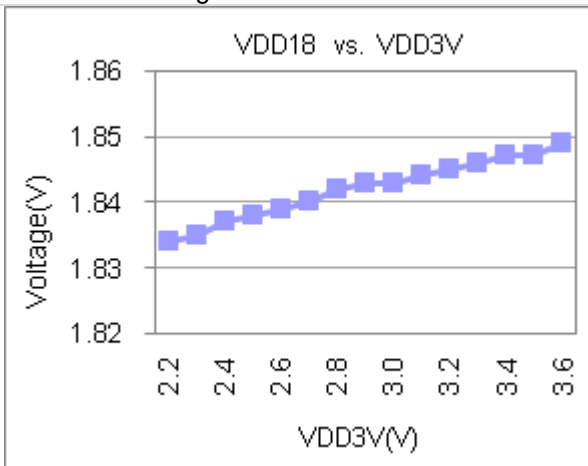


Figure5.3-4 VDD18 vs. VDD3V

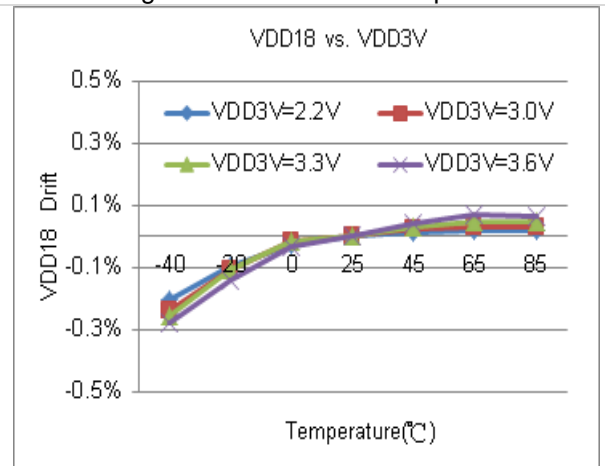


Figure5.3-5 VDD18 vs. Temperature

5.4. Charge Pump System

Typical values are at $T_A=25^\circ\text{C}$, $V_{DD3V} = 3.0\text{V}$, and $C_{CP_O}:10\mu\text{F}$. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CP_I	VDD supply voltage		2.4		3.6	V
CP_O	Backlight voltage	$C_{CP_O}:10\mu\text{F}$, $C_{HL}:1\mu\text{F}$, $V_{DD3V}=3\text{V}$, Loading $\leq 15\text{mA}$		3.3		V
I_{LED}	Driving current	$V_{DD3V} = 2.4\text{V}$			15	mA

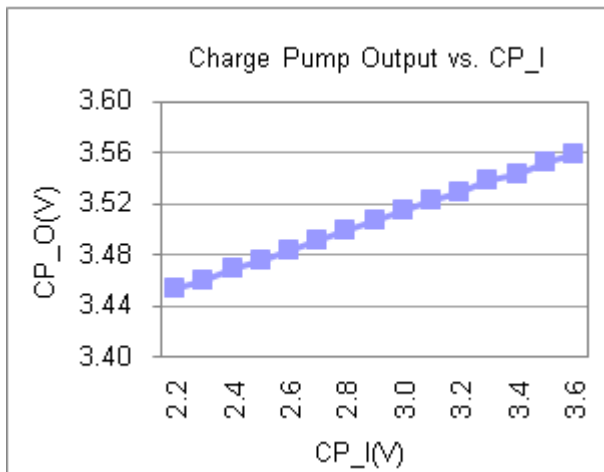


Figure5.4-1 CP_O vs. CP_I

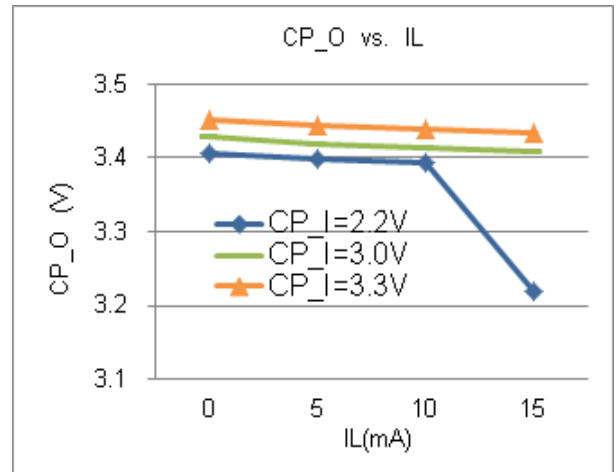


Figure5.4-2 CP_O vs. IL

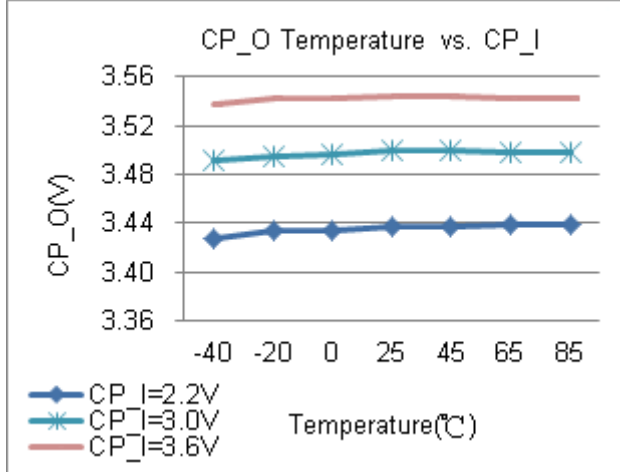


Figure5.4-3 CP_O vs. Temperature

5.5. Reset Management System

Reset Management System includes Brownout/External RST Pin/Low Voltage Detect.
 Typical values are at $T_A=25^{\circ}\text{C}$ and $V_{DD3V} = 3.0\text{V}$, unless otherwise noted.

Sym.	Parameter	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}	2			us
	VDD Start Voltage to accepted reset internally (L→H), V_{LVR}	1.8	1.95	2.1	V
	Temperature drift, $T_A=-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$	-50		+50	mV
	Hysteresis, $V_{HYS-LVR}$		50		mV
POR	Operation Slew Rate			0.1	V/us
	Start Voltage to accepted reset	0.6			V

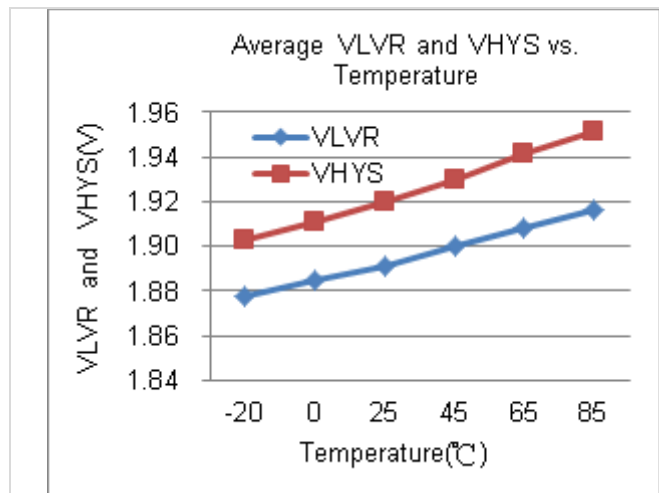


Figure5.5 Average VLVR and VHYS vs. Temperature

5.6. GPIO Port

Typical values are at $T_A=25^{\circ}\text{C}$ and $V_{DD3V} = 3.3\text{V}$. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
PT 1.0 ~ 3.7 GPIO Port						
R_{PU}	Internal pull high resistor		65	85	105	k Ω
V_{IH}	Input high voltage		$0.7 \cdot V_{DD3V}$			V
V_{IL}	Input low voltage				$0.3 \cdot V_{DD3V}$	V
I_{OH}	Source current			10		mA
I_{OL}	Sink current			10		mA
PT 6.0 ~ 10.1 GPIO Port						
V_{IH}	Input high voltage		$0.6 \cdot V_{DD3V}$			V
V_{IL}	Input low voltage				$0.3 \cdot V_{DD3V}$	V
I_{OH}	Source current	$V_{DD3V}-0.3\text{V}$		10		mA
I_{OL}	Sink current	$V_{SS}+0.3\text{V}$		10		mA

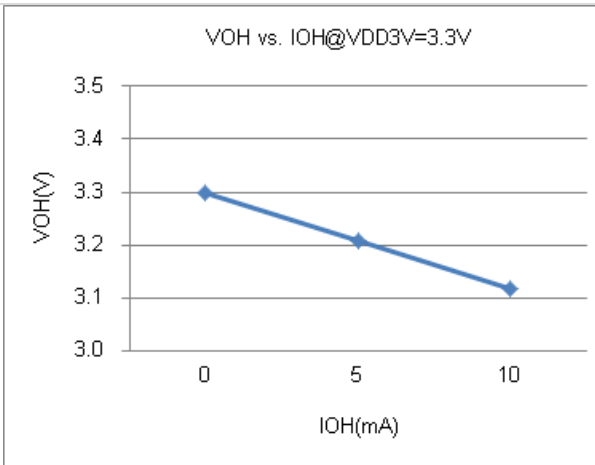


Figure5.6-1 VOH vs. IOH

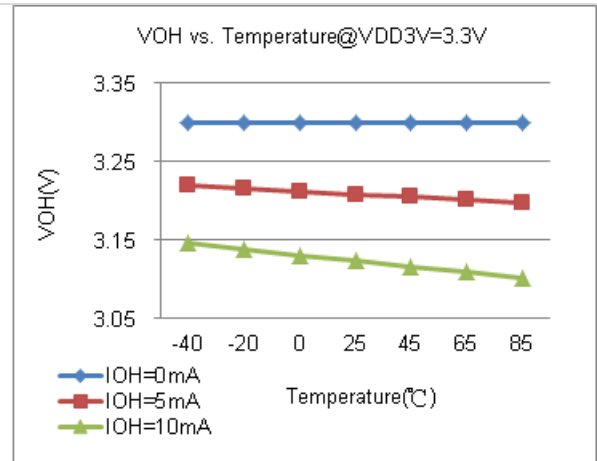


Figure5.6-2 VOH vs. Temperature

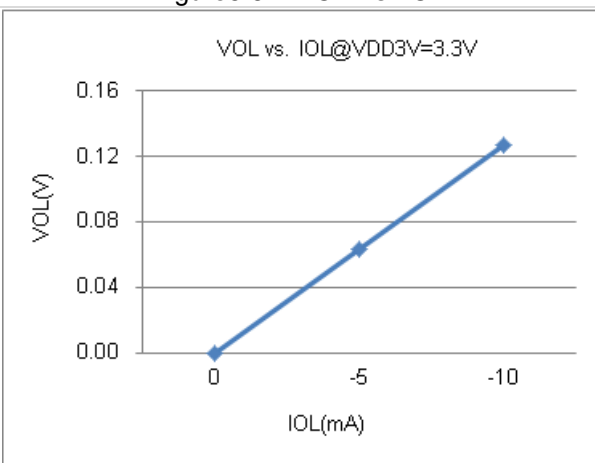


Figure5.6-3 VOL vs. IOL

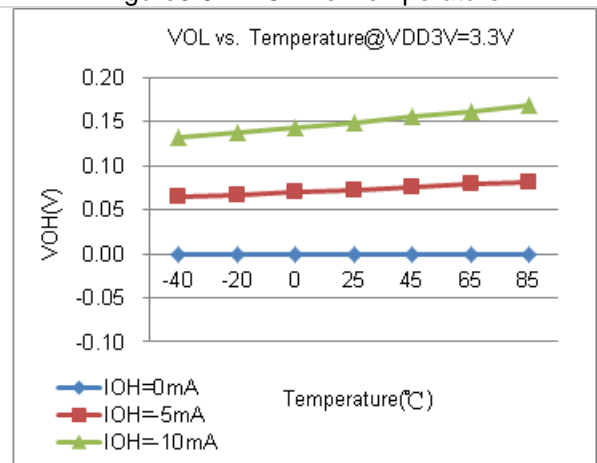


Figure5.6-4 VOL vs. Temperature

5.7. $\Sigma\Delta$ ADC ENOB and RMS Noise

Typical values are at TA=25°C and VDD3V = 3.3V, VDDA=2.4V unless otherwise noted. HY16F198B provides important input noise specification that aims at $\Sigma\Delta$ ADC. Table 5.6-1 and Table 5.7-2 lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

<i>ENOB(RMS) with OSR/GAIN at A/D Clock=333Khz, VDDA=2.4V, VREF=1.2V</i>																
Max. Vin(mV) =0.9*VREF (1)	OSR				32	64	128	256	512	1024	2048	4096	8192	16384	32768	
	Output rate(HZ)				10417	5208	2604	1302	651	326	163	81	41	20	10	
	Gain	=	PGA	x												ADGN
±1080	1	=	1	x	1	12.3	14.2	16.3	16.8	17.4	17.9	18.3	18.8	19.4	19.9	20.3
±540	2	=	1	x	2	11.8	13.1	16.0	16.6	17.0	17.4	18.0	18.7	19.3	19.7	20.2
±270	4	=	1	x	4	11.1	14.6	16.0	16.5	16.9	17.3	17.9	18.6	19.1	19.5	20.1
±33.75	32	=	8	x	4	11.1	12.2	14.9	15.4	15.7	16.1	16.7	17.6	18.1	18.6	19.1
±16.875	64	=	16	x	4	11.1	12.7	14.6	15.1	15.4	15.9	16.4	17.1	17.6	18.1	18.6
±8.4375	128	=	32	x	4	11.1	13.4	14.1	14.6	15.1	15.5	16.1	16.7	17.1	17.6	18.2

(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).

Table 5.7-1 $\Sigma\Delta$ ADC ENOB Table

<i>RMS Noise(uV) with OSR/GAIN at A/D Clock=333Khz, VDDA=2.4V, VREF=1.2V</i>																
Max. Vin(mV) =0.9*VREF	OSR				32	64	128	256	512	1024	2048	4096	8192	16384	32768	
	Output rate(HZ)				10417	5208	2604	1302	651	326	163	81	41	20	10	
	Gain	=	PGA	x												ADGN
±1080	1	=	1	x	1	459	124	28.7	19.97	13.95	9.93	7.17	5.03	3.49	2.49	1.812
±540	2	=	1	x	2	323	136	17.6	11.62	9.08	6.97	4.60	2.78	1.88	1.39	0.966
±270	4	=	1	x	4	260	23.9	8.7	6.51	4.71	3.72	2.47	1.47	1.05	0.78	0.541
±33.75	32	=	8	x	4	33.1	15.9	2.4	1.69	1.38	1.09	0.70	0.38	0.26	0.19	0.132
±16.875	64	=	16	x	4	16.2	5.4	1.5	1.06	0.83	0.61	0.42	0.26	0.18	0.13	0.092
±8.4375	128	=	32	x	4	8.4	1.8	1.0	0.75	0.53	0.39	0.27	0.17	0.13	0.09	0.063

Table 5.7 -2 $\Sigma\Delta$ ADC RMS Table

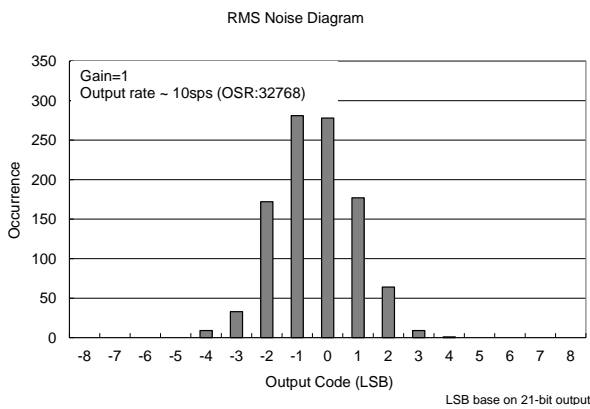


Figure5.7-1(a) RMS Noise Diagram

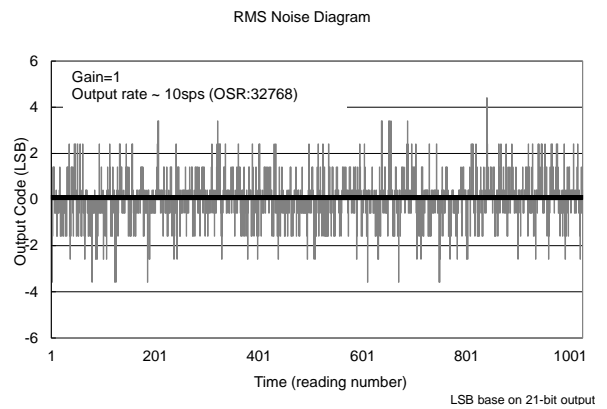


Figure5.7-1(b) Output Code Diagram

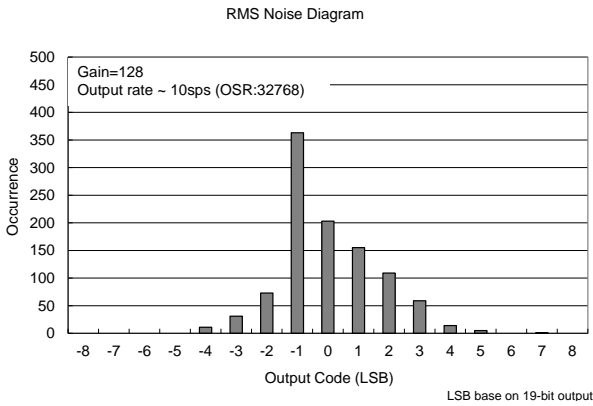


Figure5.7-2(a) RMS Noise Diagram

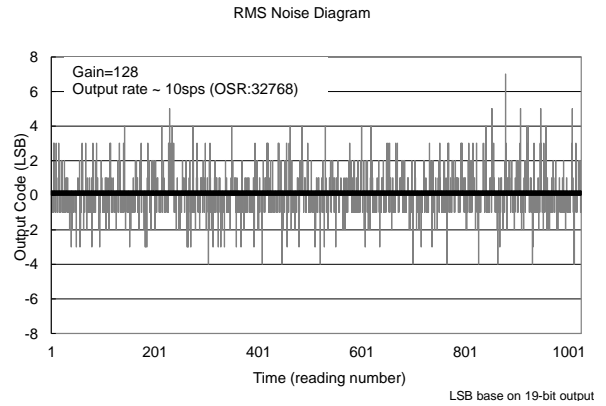


Figure5.7-2(b) Output Code Diagram

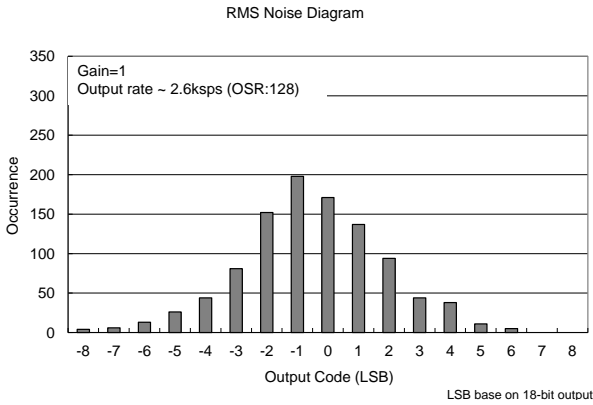


Figure5.7-3(a) RMS Noise Diagram

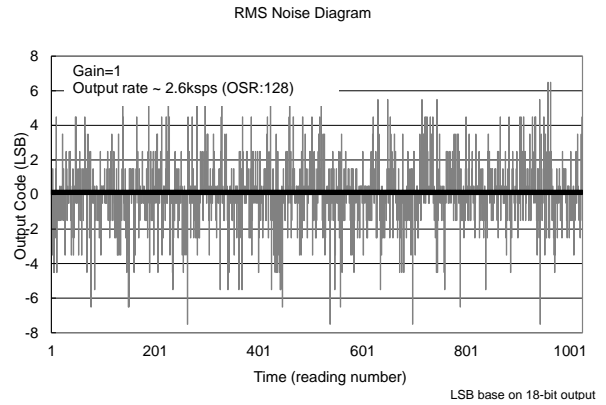


Figure5.7-3(b) Output Code Diagram

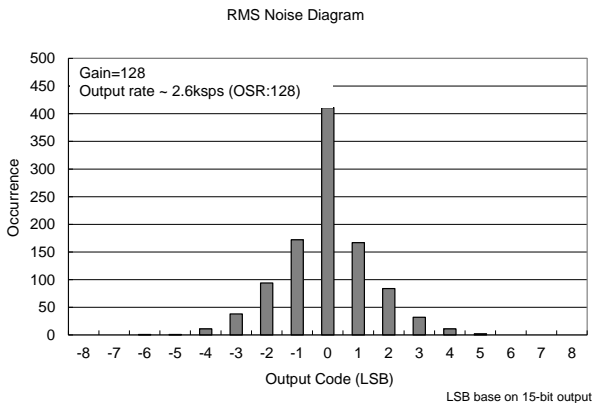


Figure5.7-4(a) RMS Noise Diagram

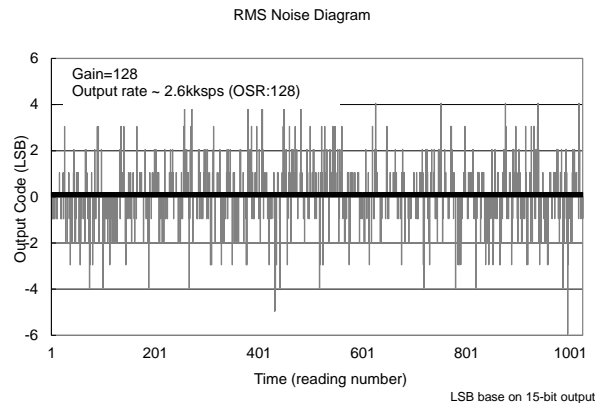


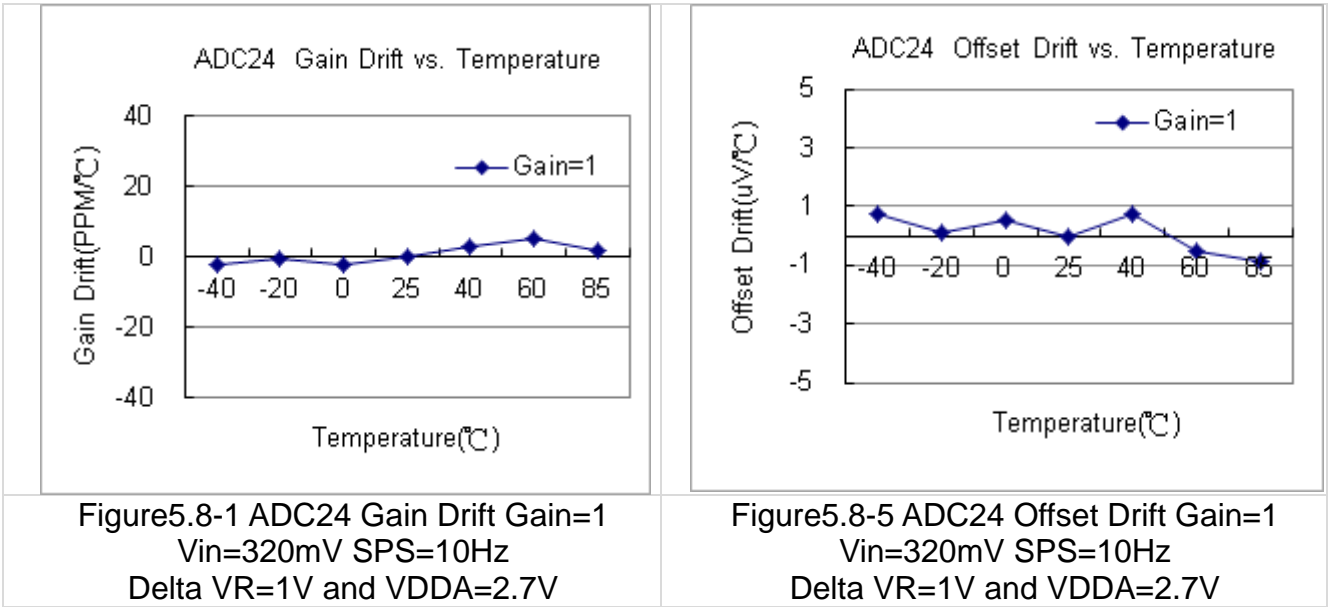
Figure5.7-4(b) Output Code Diagram

5.8. ADC Management System

All specifications at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$,

$V_{DDA} = \text{REFP} = 3.0\text{V}$, $\text{REFN} = \text{VSS}$, and $\text{Gain} = 128$. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Analog Inputs						
	Full-scale input voltage (VINP - VINN)	Considering ADC performance matches ADC ENOB table. REFP=VDDA, REFN=VSS VREF be set to 1/2 only	$\pm 0.5 * \text{VREF} / \text{Gain}$			V
		Considering ADC performance matches ADC ENOB table. REFP=REFO_I REFN=VSS VREF be set to 1 only				
	Common-mode input range	Gain = 1, @25°C	VSS-0.2V		VDDA	V
Analog Inputs						
	Full-scale input voltage (VINP - AINN)		$\pm 0.5 * \text{VREF} / \text{Gain}$			V
	Common-mode input range	Gain = 1, @25°C	VSS-0.2V		VDDA	V
System Performance						
	Resolution	No missing codes		24		Bits
	Data rate	ADC Clock		ADC Clock /OSR		SPS
	Digital filter settling time	Full setting		3		Data
	Integral nonlinearity (INL)	Differential input End-point fit, OSR=32768		15		PPM
	ADC Gain drift	40°C to +85°C,		5		ppm/ °C
	Normal-mode rejection	$f_{IN} = 60\text{Hz}$ $\pm 1\text{Hz}$, Output rate = 10 SPS	Internal OSC	70		dB
			External OSC	80		dB
	Common-mode rejection	$\Delta V_{DDA} = 0.1\text{V @ DC}$		80		dB
	Input-referred noise	Output rate= 10 SPS		65		nV, rms
	Power-supply rejection	$\Delta V_{DDA} = 0.1\text{V @ DC}$		80		dB
Voltage Reference Input						
	Voltage reference input	$\text{VREF} = \text{REFP} - \text{REFN}$			VDDA	V
	Positive Reference Input	REFP, @25°C	VDDA/2		VDDA	V
	Negative Reference Input	REFN, @25°C	VSS		VDDA/2	V
ADC Modulator Current						
ADC	ADC Modulator	$V_{DD3V} = 3.3\text{V}, V_{DDA} = 2.4\text{V}$		150		uA
PGA	ADC PGA	$V_{DD3V} = 3.3\text{V}, V_{DDA} = 2.4\text{V}$		625		uA



5.9. Temperature Sensor

Typical values are at $T_A=25^{\circ}\text{C}$, $VDD3V = 3.0\text{V}$, and $VDDA=2.4\text{V}$. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			173		$\mu\text{V}/^{\circ}\text{C}$
KT	Absolute temperature scale 0°K			-288		$^{\circ}\text{C}$
TC_{ERR}	One point calibrate error temperature	Calibration at 25°C of $-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$		± 2		$^{\circ}\text{C}$

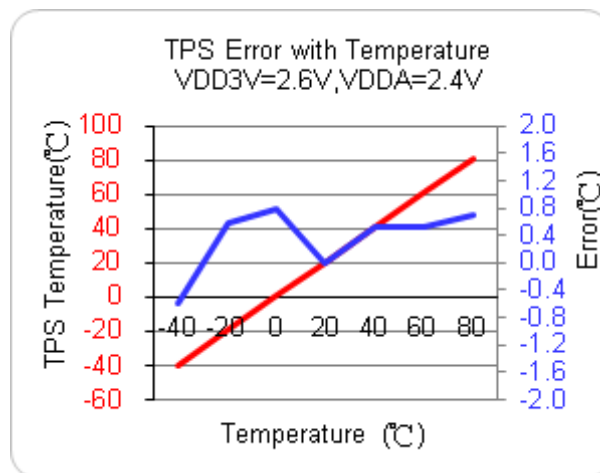


Figure5.9 TPS Performance

5.10.8-Bit Resistance Ladders

Typical values are at $T_A=25^{\circ}\text{C}$ and $V_{DD3V} = 3.0\text{V}$. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Resolution	Monotonic		8		Bit
	Power Supply		2.4		V_{DD3V}	V
V_{OUT}	Output range	DA output is between V_{R-} and V_{R+}	0		V_{DD3V}	V
V_{REFP}	Positive reference voltage range	$V_{REFP} > V_{REFN}$	0		V_{DD3V}	V
V_{REFN}	Negative reference voltage range		0		V_{DD3V}	V
R_{ON}	8-Bit Resistance ladders. output switch	$V_{DDA}=2.4\text{V}$ $0.5\text{V} < DA_OP < V_{DD3V}-0.5\text{V}$			200	Ω
		$V_{DDA}=2.4\text{V}$ $0.5\text{V} > DA_OP,$ $DA_OP > V_{DD3V}-0.5\text{V}$		10		Ω
R_{RSW}	Reference voltage switch	$V_{REFP} = 2.2\text{V}, V_{REFN} = 0\text{V},$ $V_{DDA} = 2.4\text{V}$		15	30	Ω
R_{LADDER}	One LSB resistance ladder		621	730	840	Ω
INL	Integral linearity error	$V_{R+} = 2.4\text{V}, V_{R-} = 0\text{V}$		± 0.5	± 1	LSB
DNL	Differential linearity error	$V_{R+} = 2.4\text{V}, V_{R-} = 0\text{V}$		± 0.5	± 1	LSB
E_{OS}	Offset error	$V_{R+} = 2.4\text{V}, V_{R-} = 0\text{V}$			1	LSB
8-Bit Resistance Ladders	(V_{in} Floating)	$V_{DD3V}=3.3\text{V}, V_{DDA}=2.4\text{V}$		0.1		μA

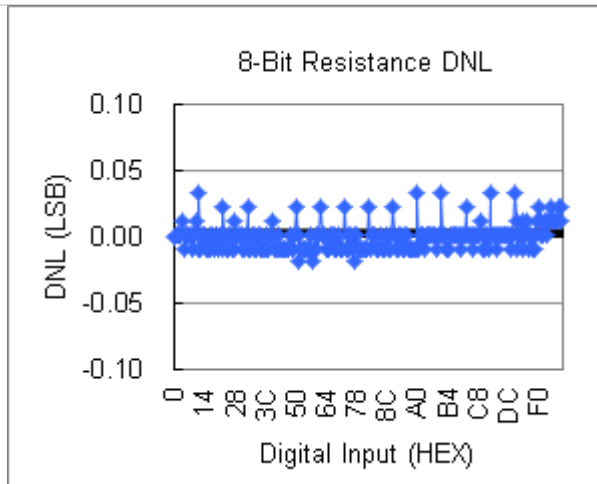


Figure5.10-1 8-Bit Resistance vs. DNL

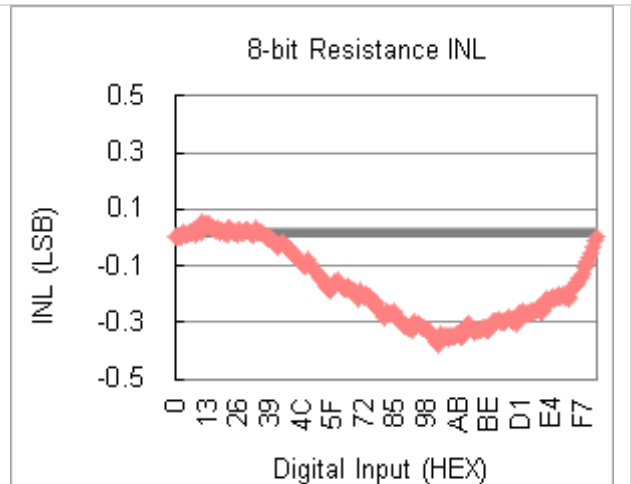


Figure5.10-2 8-Bit Resistance vs. INL

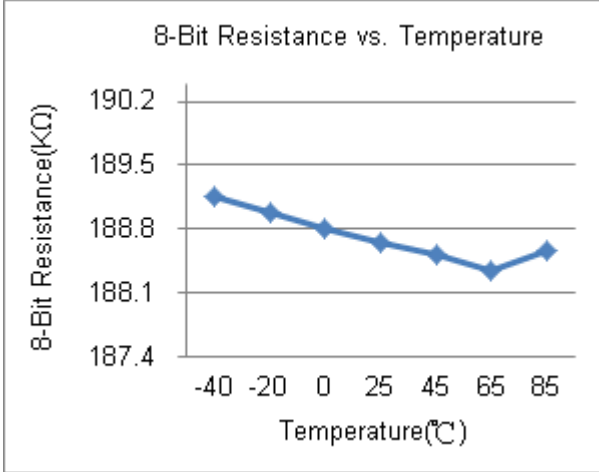
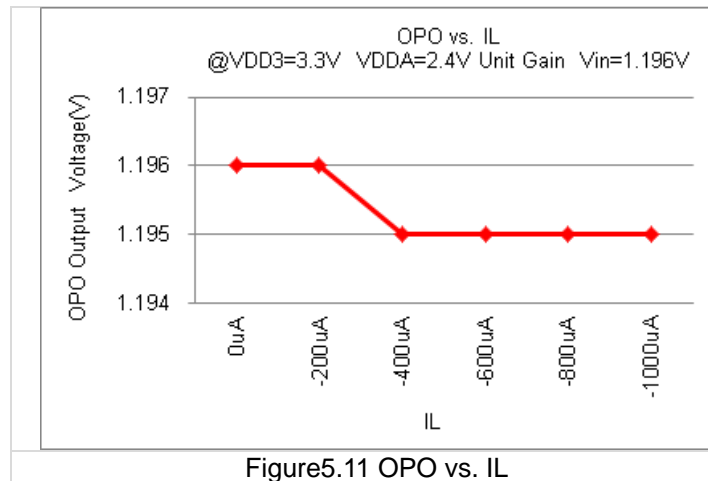


Figure5.10-3 8-bit Resistance vs. Temperature

5.11. OPA Management System

Typical values are at $T_A=25^{\circ}\text{C}$, $V_{DD3V} = 3.0\text{V}$, and $C_{V_{LCD}}=10\mu\text{F}$. Unless otherwise noted.

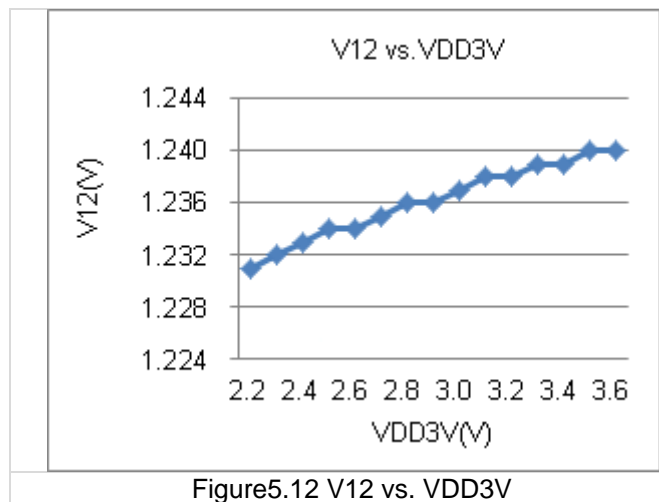
Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA	Power supply		2.4		3.6	V
V _{OUT}	Output range		0		VDDA	V
V _{IN}	Input common range		0		VDDA	V
I _{OPA}	OPAMP current			120		uA
I _{OPA_LOAD}	Output current loading (push or pull)	VDDA = 3.0V, 0.3V < Output voltage < VDDA-0.3V			1	mA
		VDDA = 2.4V, 0.3V < Output voltage < VDDA-0.3V			0.5	mA
C _{LOAD}	Max output capacitor load				1	nF
SR	Slew rate	Loading R=10K, C=100pF, 0.3V → VDDA-0.3V		0.6		V/us
UGB	Unit gain bandwidth	Loading C=100pF		1000		KHz
V _{OS}	Offset error	V _{in} = 1.2V	-5		+5	mV
DFD	Digital filter delay	VDDA = 3.0V		2		us
C _{SA}	Sample capacitor			10		pF



5.12. CMP Management System

Typical values are at $T_A=25^\circ\text{C}$ and $V_{DD3V} = 3.0\text{V}$. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{MC}	Operation supply current	ENCMP[0]=1, CMPHS[0]=1b		10		uA
	Low Power Mode	ENCMP[0]=1, CMPHS[0]=0b		1		
V_{IC}	Common-mode input voltage		0		$V_{DD3V}-1$	V
V_{OS}	Offset voltage		-5		5	mV
V_{hys}	Input hysteresis		0	0.7	1.5	mV
V_{REF}	Reference voltage	CPPS[1:0]=11b	1	1.2	1.4	V
	Temperature drift	CPPS[1:0]=11b		80		ppm/ $^\circ\text{C}$
I_R	Multi-node resistor current	CPRL[0]=0b		10		uA
		CPRL[0]=1b		30		



5.13. LCD System

Typical values are at TA=25°C, VDD3V = 3.3V, and CVLCD=10uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
I _{LCD}	Operation Current Charge Pump Mode	VDD3V=3.3V VLCD=3.0V (VLCD<VDD3V)		10		uA	
VLCD	Supply Voltage Range	VLCD	2.50		3.80	V	
VLCD	Embedded Charge Pump Output Voltage @ VLCD Pin	VDD3V = 2.4V CVLCD = 10uF	Mode1: Data ¹ =00_011B (After trim) ^{Note1}	-5%	3.43	+5%	V
			Mode1: Data ¹ =00_011B	-10%	3.30	+10%	
			Mode2: Data ¹ =00_100B (After trim) ^{Note1}	-5%	3.16	+5%	
			Mode2: Data ¹ =00_100B	-10%	3.00	+10%	
			Mode3: Data ¹ =00_101B (After trim) ^{Note1}	-5%	2.93	+5%	
			Mode3: Data ¹ =00_101B	-10%	3.00	+10%	
			Mode4: Data ¹ =11_101B (After trim) ^{Note1}	-5%	2.73	+5%	
			Mode4: Data ¹ =11_101B	-10%	2.80	+10%	
			Mode5: Data ¹ =01_101B (After trim) ^{Note1}	-5%	2.55	+5%	
			Mode5: Data ¹ =01_101B	-10%	2.6	+10%	
Z _{LCD}	Output Impedance With LCD Buffer	FLCD = 128Hz, VLCD = 3.0V		10		KΩ	

Note1

After trim: According to the factory calibration parameters of VLCD to calibrate VLCD, and need to correspond to the selected VLCD voltage. User can refer to the document “UG-HY16F198B_EN” or “APD-HY16IDE007_EN” to know how to use that in detail.

Data1 Bit: 0X41F24 [EN_Rshift1, EN_Rshift0], 0X41B00 [VLCD2, VLCD1, VLCD0]

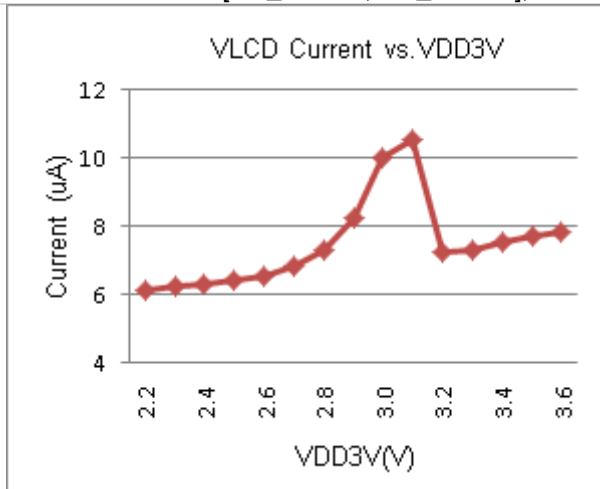


Figure5.13-1 VLCD Current vs. VDD3V @ VLCD=3.16V

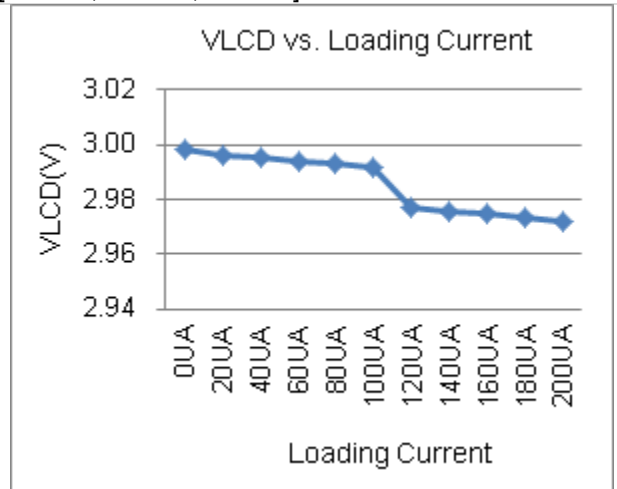


Figure5.13-2 VLCD With Load @ VLCD=3.0V

6. Ordering Information

6.1. HY16F19xB Series Device No. Selection

Order Name	Package Type	Pin	PKG Type		Code No.	Shipment Type	Quantity Per Package	Material	MSL ³
			Description ²						
HY16F198B-D000	Die	-	D	000	-	-	100	Green ⁴	-
HY16F198B-N088	QFN	88	N	088	-	Tray	168	Green ⁴	MSL-3
HY16F198B-L100	LQFP	100	L	100	-	Tray	90	Green ⁴	MSL-3
HY16F198B-L064	LQFP	64	L	064	-	Tray	250	Green ⁴	MSL-3
HY16F197B-L064	LQFP	64	L	064	-	Tray	250	Green ⁴	MSL-3
HY16F197B-N068	QFN	68	N	068	-	Tray	348	Green ⁴	MSL-3
HY16F196B-L064	LQFP	64	L	064	-	Tray	250	Green ⁴	MSL-3

¹ Device No.: Model No. – Package Type Description

HY16F198B-L100

IC part Number | IC PKG Type

EX : You request in LQFP 100 package.

The device No. will be HY16F198B-L100.

And please clearly indicate the shipment packing type when placing orders.

³ MSL:

The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

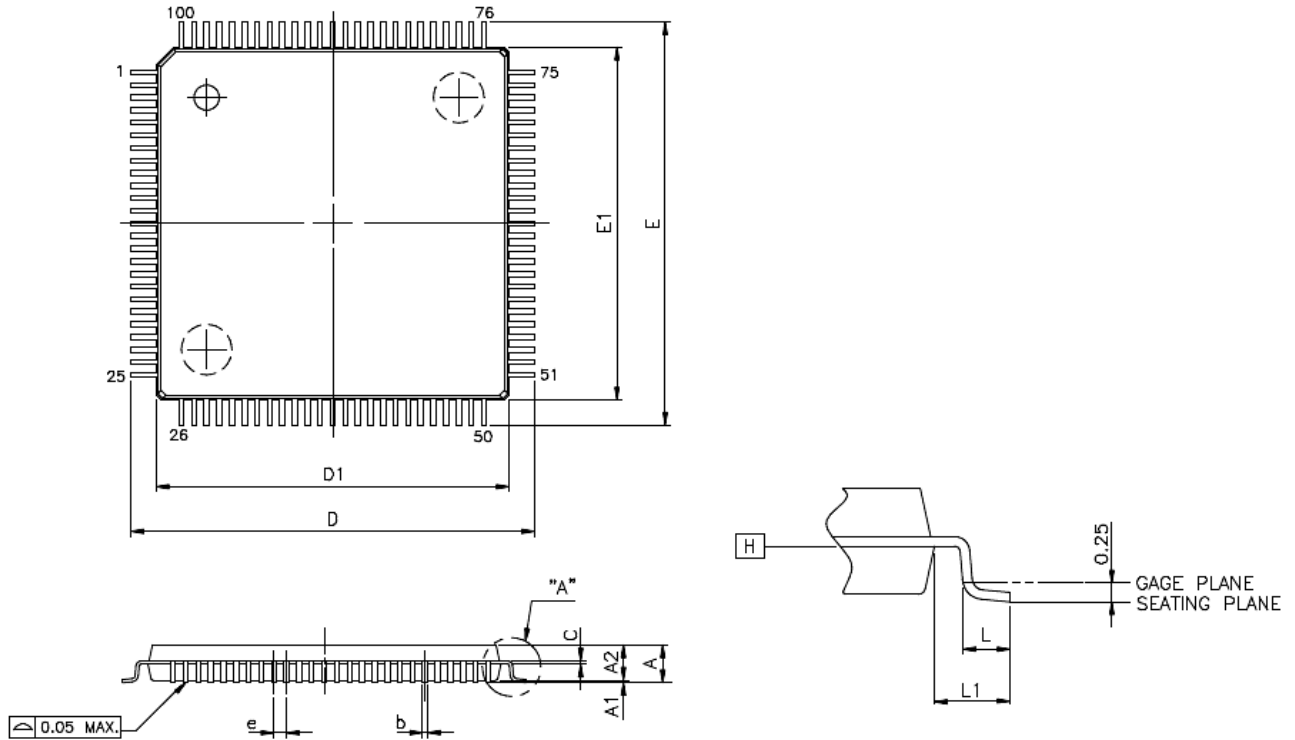
⁴ Green (RoHS & no Cl/Br):

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br<900ppm or Cl<900ppm or (Br+Cl)<1500ppm)

7. Package Information

7.1. LQFP100 PKG Diagram

Unit: mm



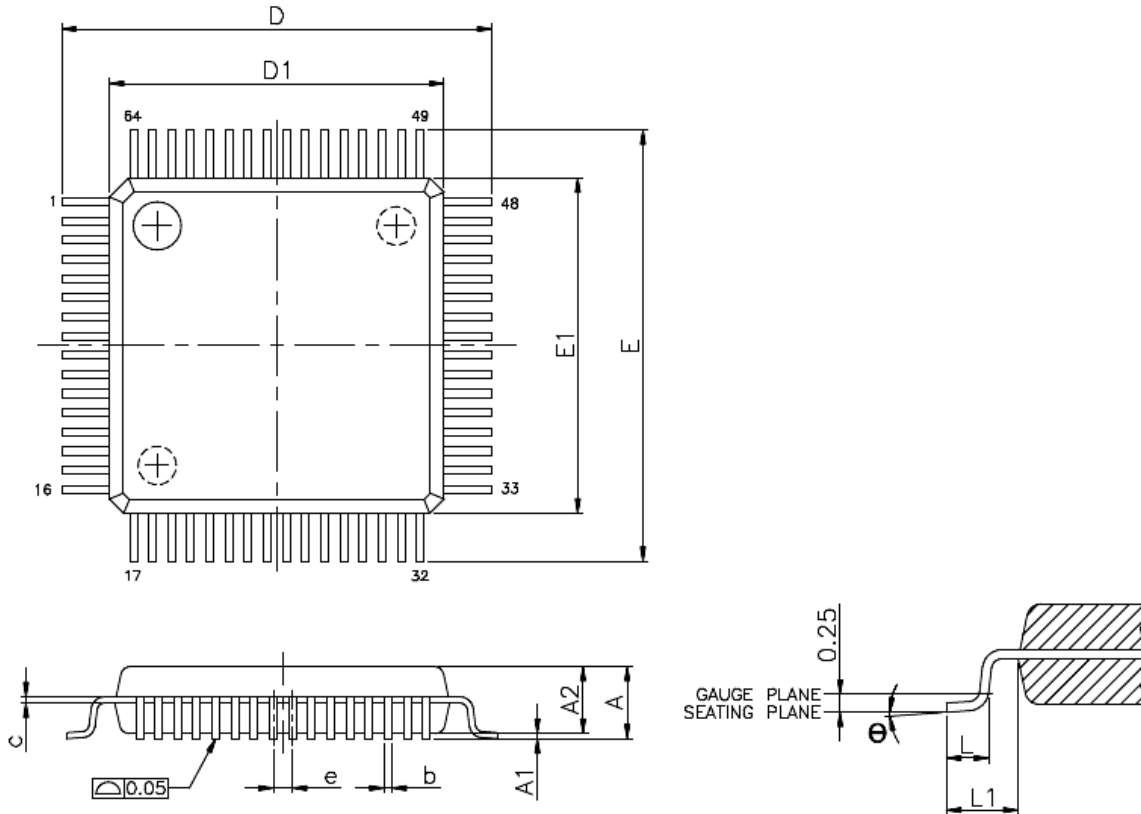
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

Note: JEDEC MS-026 compliant

7.2. LQFP64 PKG Diagram

Unit: mm



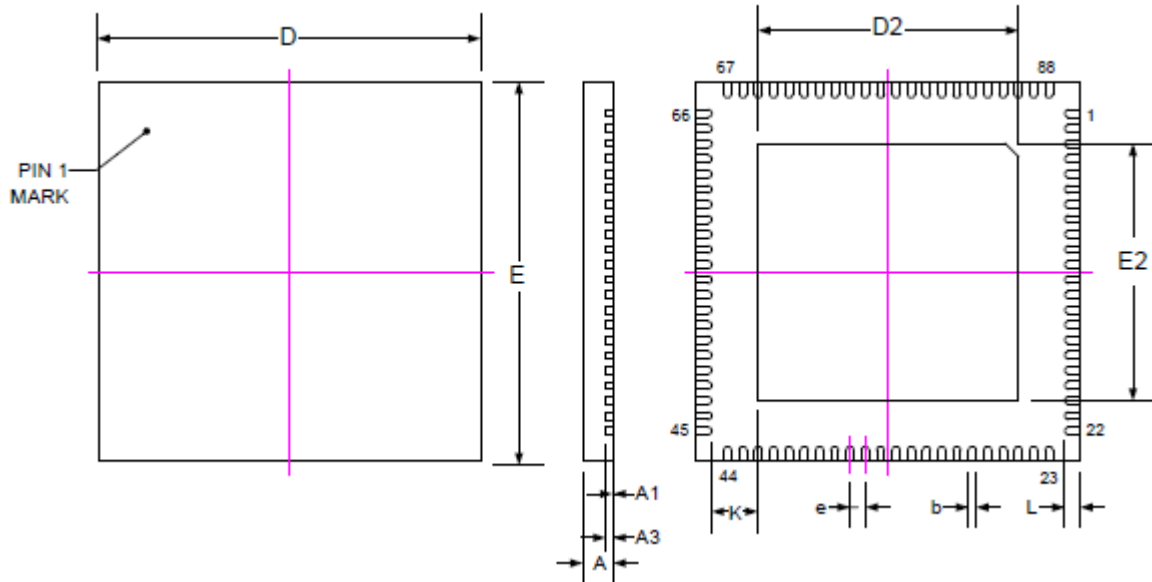
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note: JEDEC MS-026 compliant

7.3. QFN88 PKG Diagram

Unit: mm



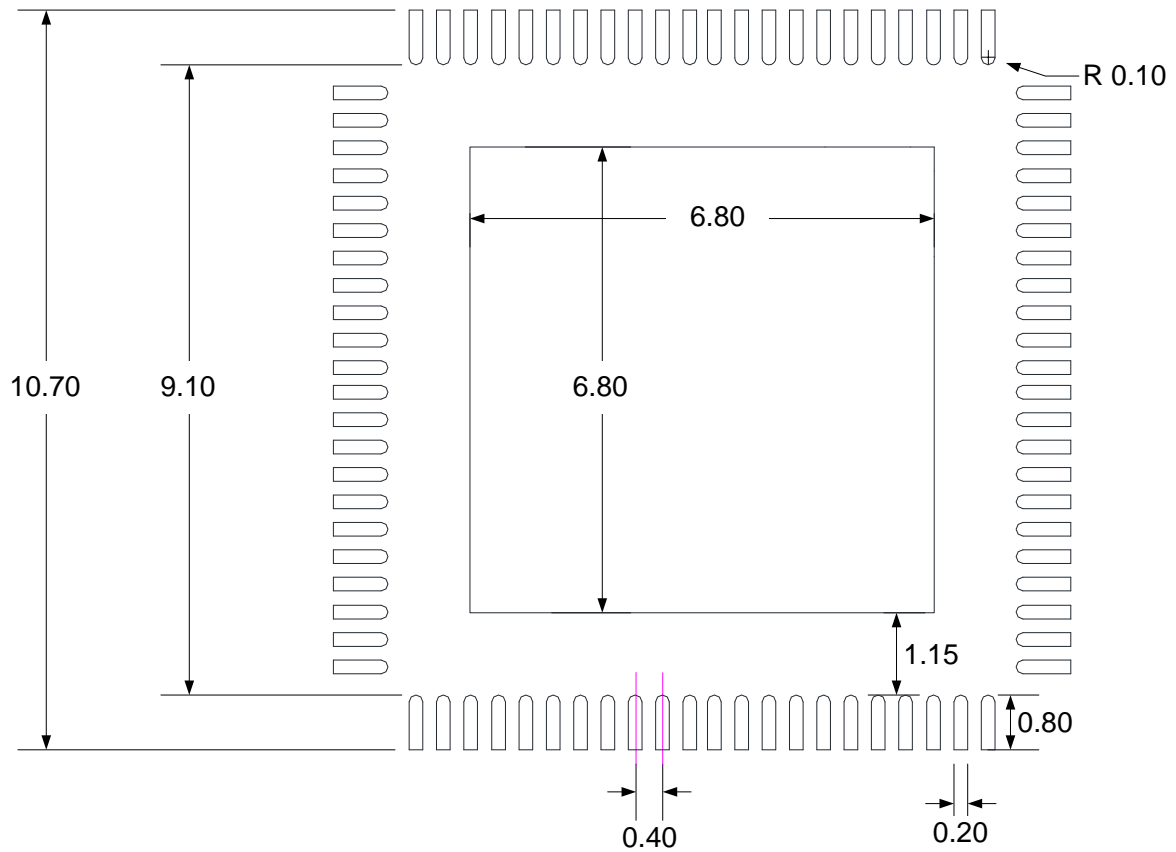
SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.15	0.20	0.25
D	10.00 BSC		
E	10.00 BSC		
e	0.40 BSC		
D2	6.75	6.80	6.85
E2	6.75	6.80	6.85
L	0.30	0.40	0.50
K	1.08	1.20	1.33

Note: All dimensions refer to JEDEC OUTLINE MO-220.

Package Outline Drawing--- QFN 10x10 88

7.4. Land Pattern Design Recommendations

Unit: mm

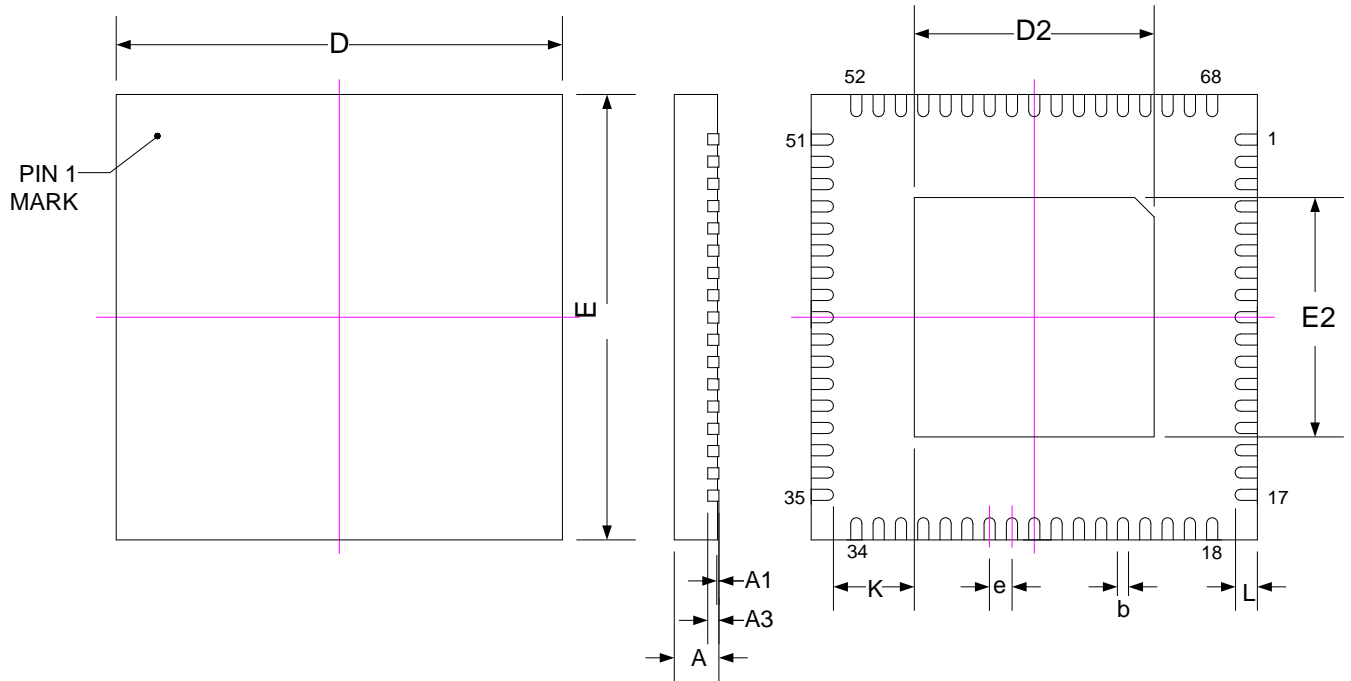


Note:

1. Publication IPC-7351 is recommended for alternate designs
2. Unit : mm
3. http://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB.pdf

7.5. QFN68 PKG Diagram

Unit: mm

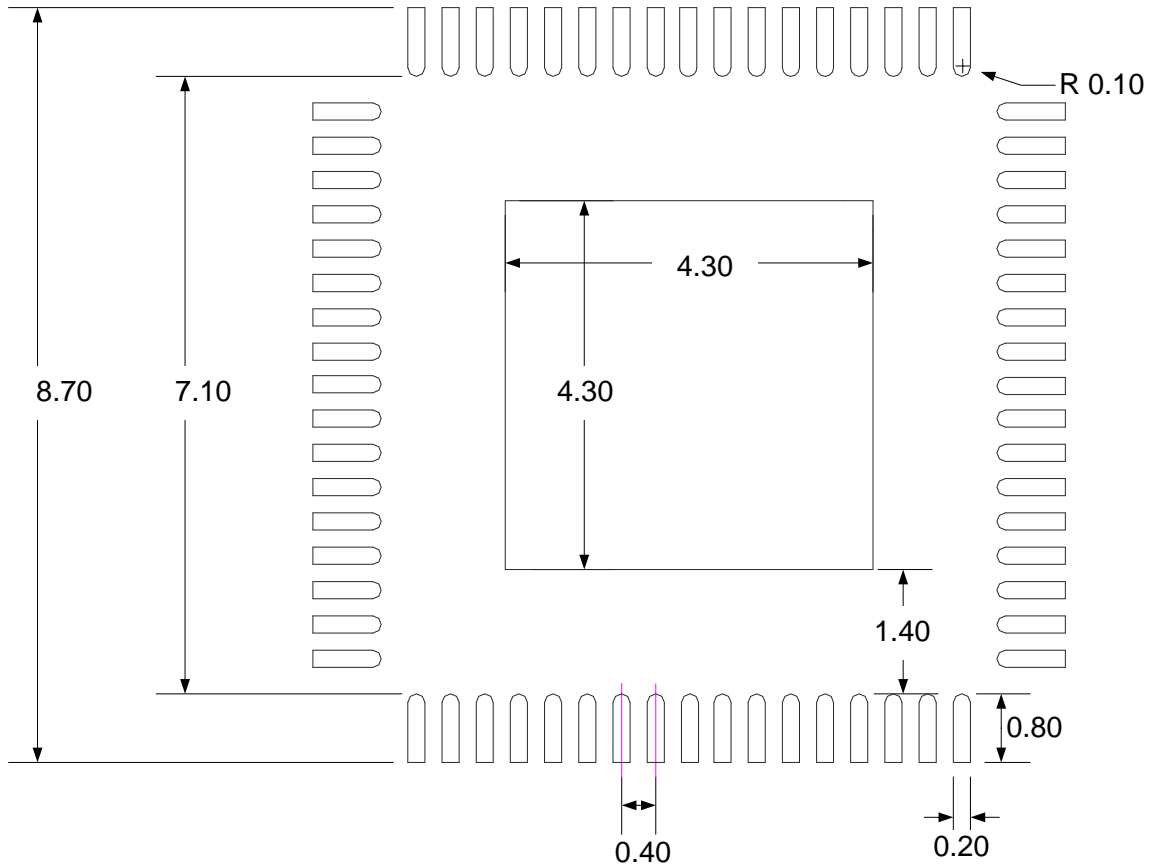


SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.15	0.20	0.25
D	8.00 BSC		
E	8.00 BSC		
e	0.40 BSC		
D2	4.20	4.30	4.40
E2	4.20	4.30	4.40
L	0.35	0.40	0.45
K	1.35	1.45	1.55

Note: All dimensions refer to JEDEC OUTLINE MO-220.
 Package Outline Drawing--- QFN 8x8 68

7.6. Land Pattern Design Recommendations

Unit: mm



Note:

1. Publication IPC-7351 is recommended for alternate designs
2. Unit: mm
3. http://www.hycontek.com/wp-content/uploads/QFN_DFN_PCB.pdf

8. Revision Record

Major differences are stated thereafter:

Version	Page	Revision Summary	Date
V01	ALL	First edition	2017/02/13
V02	ALL	<ol style="list-style-type: none">1. Remove PT3.2 & PT3.3 Multiplexing pin function, only to retain AIO4 & AIO5 analog function.2. Modify the VDDA description: Analog voltage source input / output (connect 1 ~ 10 uF capacitor to VSS)3. Modify the Note.3 links in sections 7.4 and 7.64. Modify 5.6 sections R_{PU} (Internal pull high resistor) Specifications.5. Modify the contents of Table 2-1 (full range of package description)	2017/09/08