HYCON TECHNOLOGY

HY16F198/HY16F198B

Datasheet

High Precision Mixed-Signal Controller
4x36 ~ 6x34 LCD Driver
32-Bit Low Power MCU
21-bit ENOB ΣΔADC
64Kb Flash

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1. Features

Digital Circuit

- 32-bit MCU 1T Andes Core N801
- C Complier & User Friendly Development Tools
- 2.2V to 3.6V operational voltage.
- -40 to 85℃ operational environment
- Low power operation:
  - MCU: 350uA/MIPS@3.3V
  - Low speed mode: 10uA@17Khz & 3.3V
  - Sleep mode: 2.5uA@3.3V
- 64K Byte Flash ROM
- 8K Byte SRAM
- 16-bit Timer A, Timer B(x2), Timer C
- 16-bit PWM controller
- I^2C/SPI/ UART(x2) communication Hardware IP
- RTC Hardware IP
- Low voltage detection/BOR circuit
- 32 programmable digital I/O ports
  - 16 general propose digital I/O ports
  - 16 programmable digital I/O ports multiplexed with LCD Segment
- 4x36 ~ 6x34 LCD Driver
  - Support 1/3, 1/4, 1/5, 1/6 duty @ 1/3 bias mode
  - R-type, External VLCD Application
  - 3.3V, 3.0V, 2.8V, or 2.6V internal charge pump VLCD

Analog Circuit

- An ultra low noise 24-bit SD ADC
  - Down to 65nVrms input refer noise
  - Conversion rate up to 350KSPS
  - Input amplification gain up to 128
  - Operation voltage 2.4V to 3.6V
- External High Speed Oscillator Max 16MHz
- External Low Speed Oscillator Mode 32768Hz
- Internal High Speed Oscillator Max 16MHz
- Internal Low Speed Oscillator 35KHz
- Power management
  - Charge Pump regulation
  - Build-in selectable VDDA voltage LDO
  - 1.2V Band gap reference output
- A resistor ladders can be used as 8-bit Resistance Ladder
  - Programmable potentiometer
  - Monotonic guarantee
- A rail-to-rail operation amplifier
  - CMOS input, 1MHz bandwidth
  - Unit Gain Buffer, Integrator
  - S/H circuit, software SAR ADC
  - Can use as comparator
- Multi-function Analog Comparator
  - support touch key
  - Low Voltage Detection

art No.	Flash ROM (kb)	SRAM (kb)	ΣΔADC VIN Ch.	I/O	Touch Key (Ch.)	LCD		Charge pump	ISP Mode	Package	Others: (All the products have the same IP)
						COM	SEG				
HY16F196-L064	16	2	8	20+22	6	4~6	24~22	Y	N	LQFP64	Analog Parts: One hardware RTC and calendar. One 8-bit resistance ladders for DAC. One rail-to-rail OPAMP. One multi-function comparator. One built-in temperature sensor. Digital Parts: One 32-bit programmable SPI One IIC(master and slave mode.) Two enhanced UART Four channels PWM function,
HY16F196-N068	16	2	8	20+26	6	4~6	28~26	Y	N	QFN68	
HY16F197-L064	32	4	5	20+24	6	4~6	26~24	Y	N	LQFP64	
HY16F197-N068	32	4	5	20+28	6	4~6	30~28	Y	N	QFN68	
HY16F198-L100	64	8	8	24+34	8	4~6	36~34	Y	N	LQFP100	
HY16F198-N088	64	8	8	24+34	8	4~6	36~34	Y	N	QFN88	
HY16F198-L064	64	8	6	24+24	8	4~6	26~24	N	N	LQFP64	
HY16F196B-L064	16	2	8	20+22	6	4~6	24~22	Y	Y	LQFP64	
HY16F196B-N068	16	2	8	20+26	6	4~6	28~26	Y	Y	QFN68	
HY16F197B-L064	32	4	5	20+24	6	4~6	26~24	Y	Y	LQFP64	
HY16F197B-N068	32	4	5	20+28	6	4~6	30~28	Y	Y	QFN68	
HY16F198B-L100	64	8	8	24+34	8	4~6	36~34	Y	Y	LQFP100	
HY16F198B-N088	64	8	8	24+34	8	4~6	36~34	Y	Y	QFN88	
HY16F198B-L064	64	8	6	24+24	8	4~6	26~24	N	Y	LQFP64	

- Note: HY16F19xB and HY16F19x are same package type, update characteristics descriptions please refer to Chapter 8.

2. Pin Definition

2.1. HY16F198 LQFP100 Pin Diagram

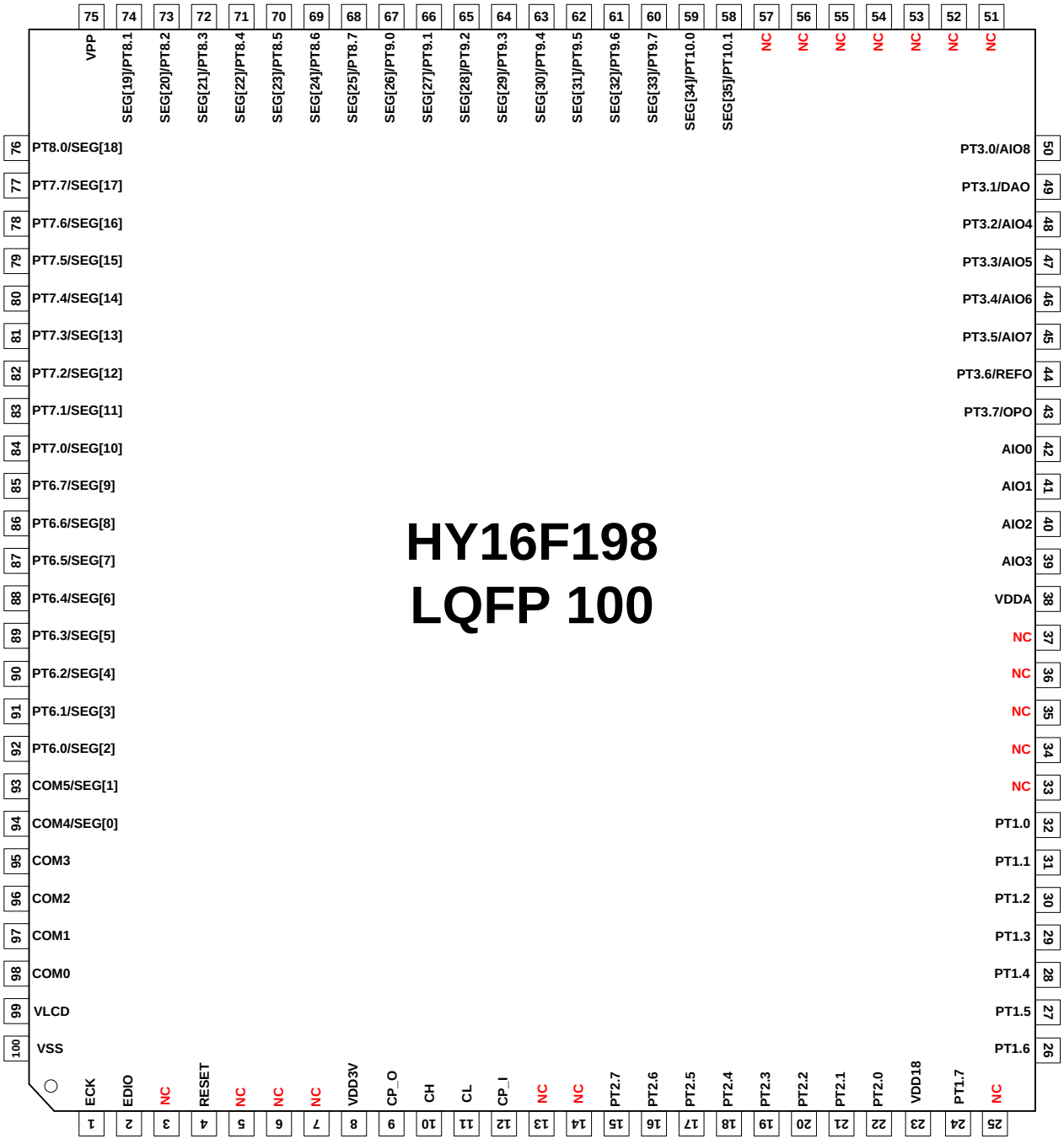


Figure 2-1-1 HY16F198/HY16F198B LQFP100 Pin Diagram

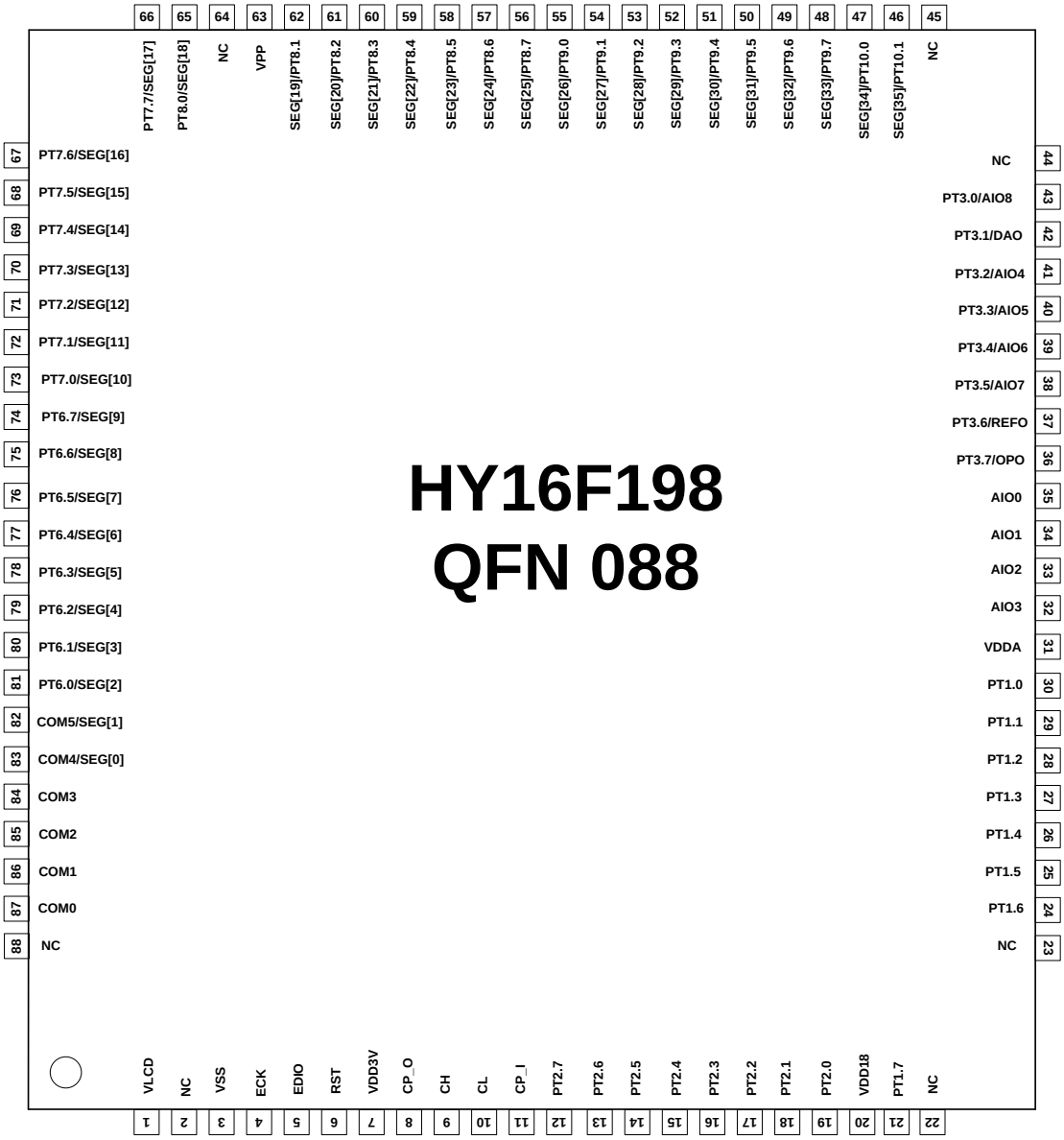


Figure 2-1-2 HY16F198/HY16F198B QFN88 Diagram

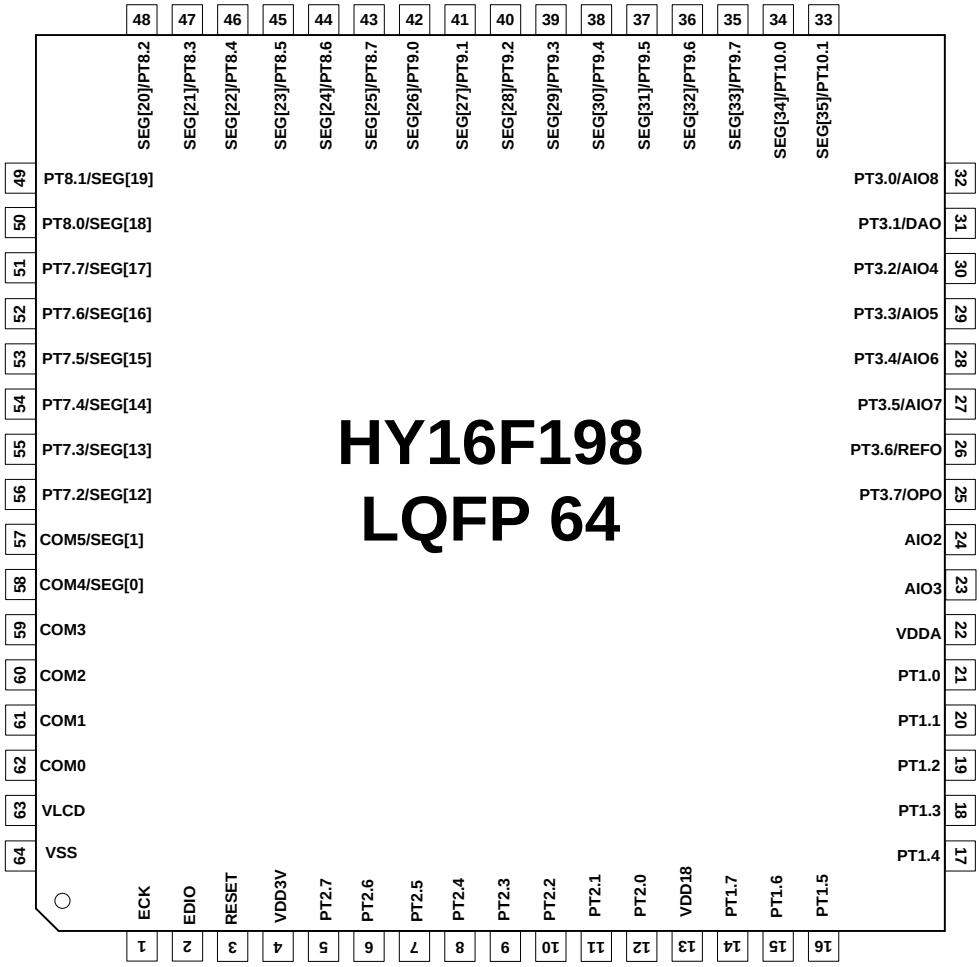


Figure 2-1-3 HY16F198/HY16F198B LQFP64 Diagram

2.2. HY16F197 Series Pin Diagram

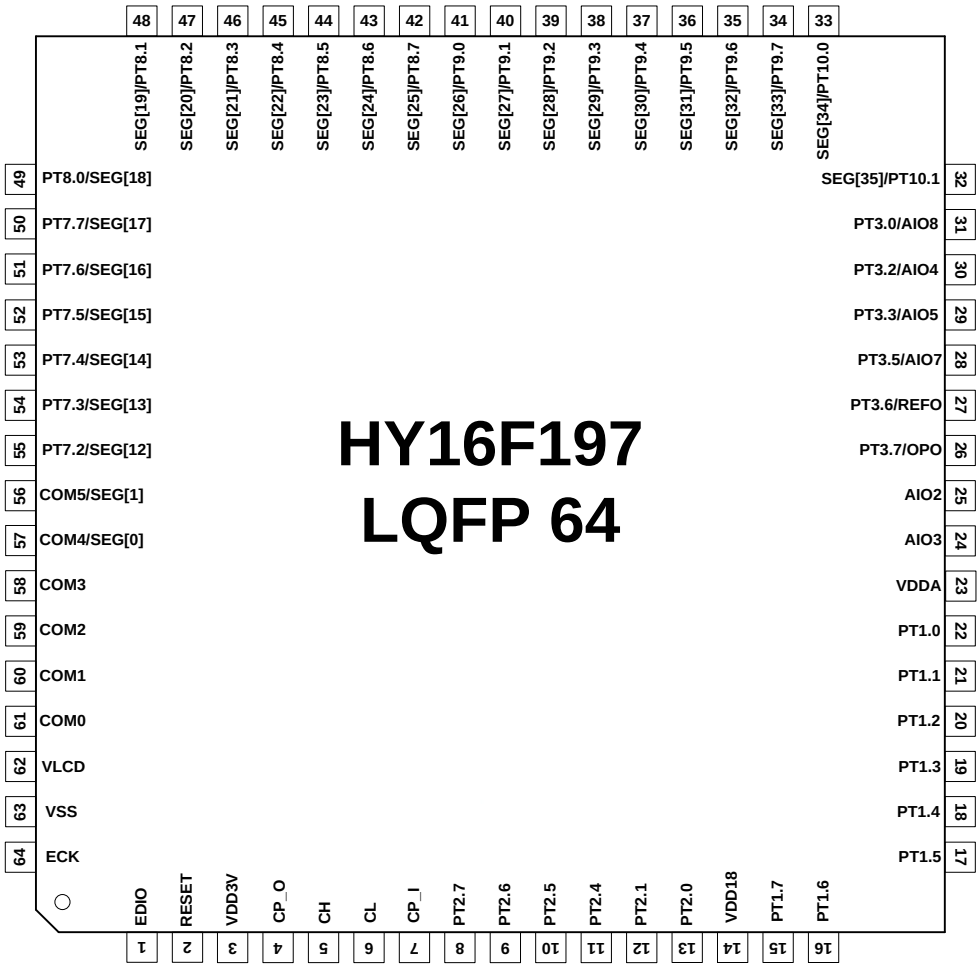


Figure 2-2-1 HY16F197 HY16F197B LQFP64 Pin Diagram

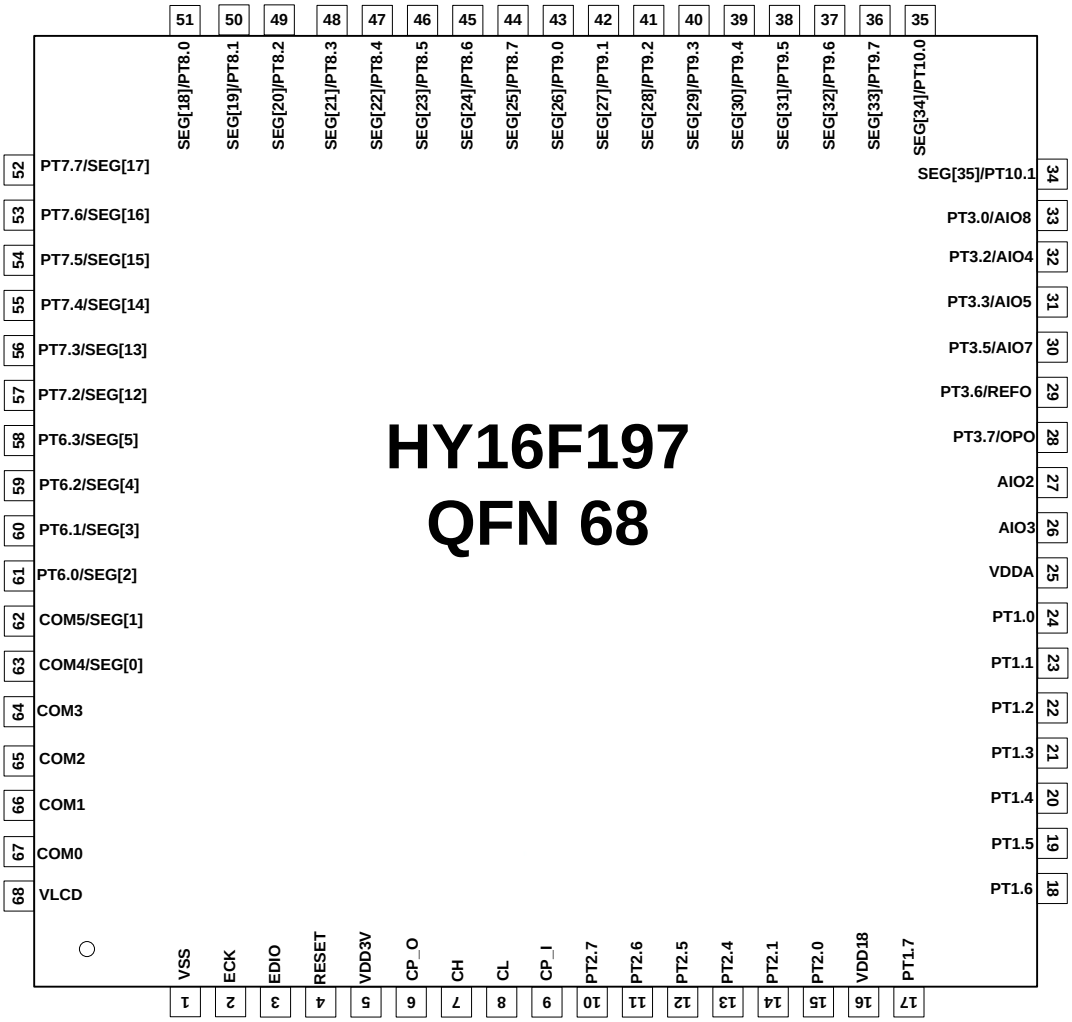


Figure 2-2-2 HY16F197 HY16F197B QFN 68 Pin Diagram

2.3. HY16F196 Series Pin Diagram

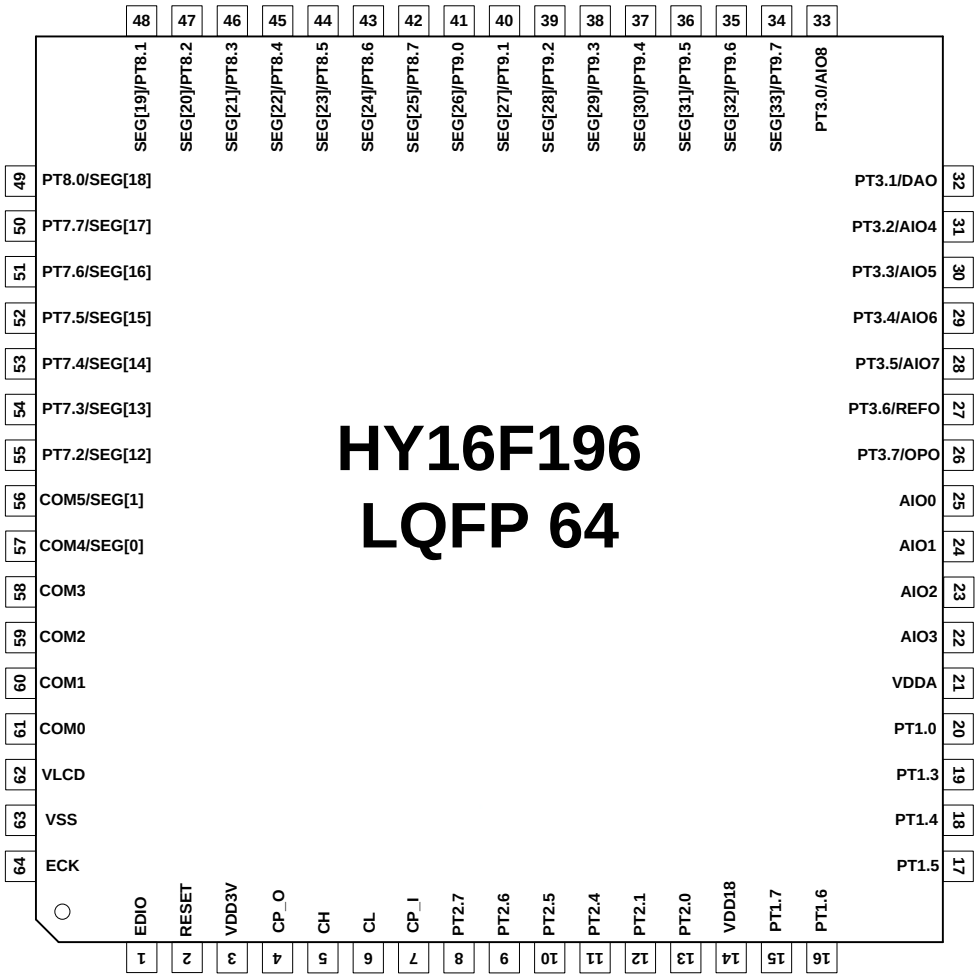


Figure 2-3-1 HY16F196/HY16F196B LQFP 64 Pin Diagram

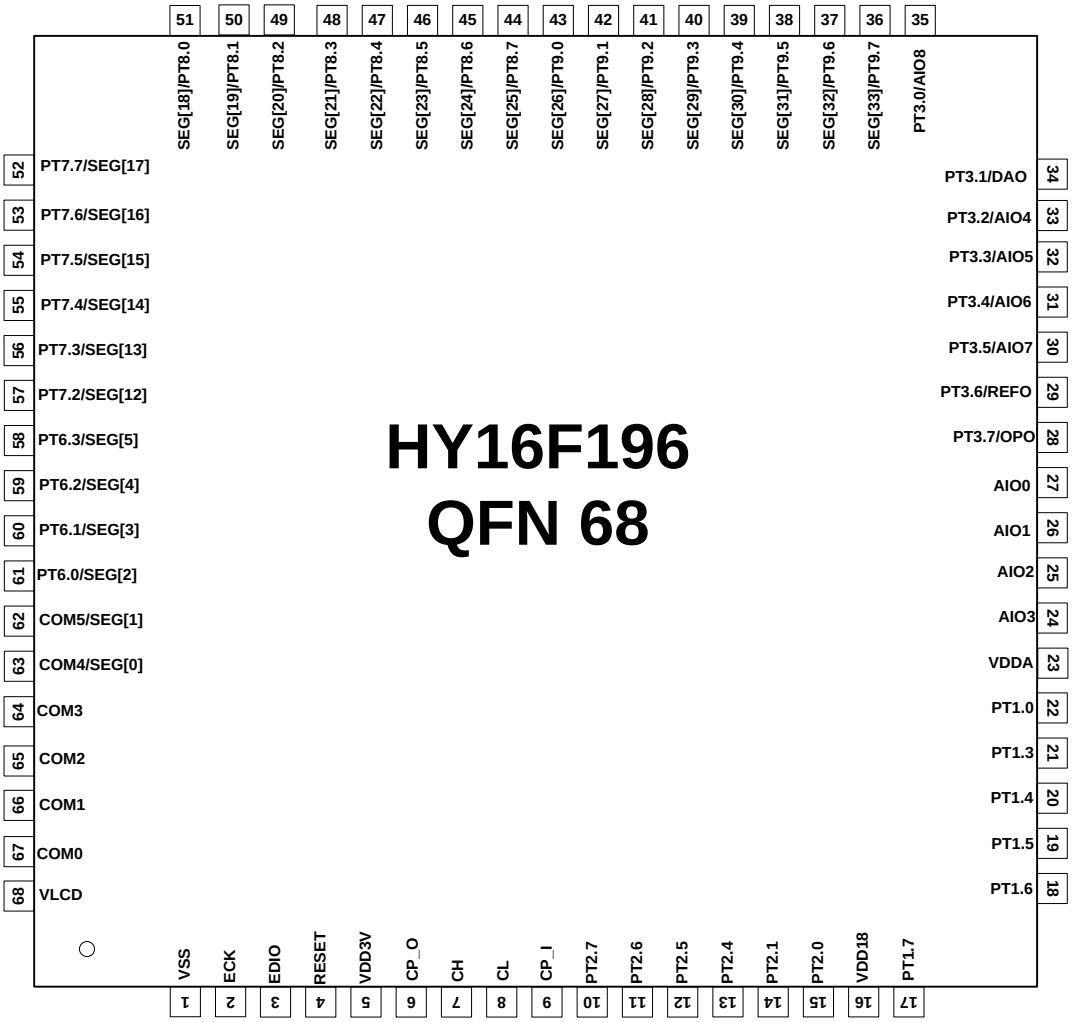


Figure 2-3-2 HY16F196/HY16F196B QFN 68 Pin Diagram

2.4. Pin Description

2.4.1 HY16F19x and HY16F19xB Series

TYPE Definition：I = Digital Input. O = Digital Output. OD = Open-drain Output.
AI = Analog Input. AO = Analog Output. P = Power Connection.

Name	HY16F198-L100 HY16F198B-100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	Type	Pin Name	Description
ECK	1	64	64	DIO	ECK	Embedded Debug Module (EDM) Clock Input PIN. 100K Resistance to VSS.
EDIO	2	1	1	DIO	EDIO	Embedded Debug Module (EDM) Data Input/ Output PIN. 100K Resistance to VSS.
RESET	4	2	2	DI	RESET	Active Low Reset 100K Resistance to VDD3V, 100nF Cap to VSS.
VDD3V	8	3	3	PI	VDD3V	Power Input For System, 10uF Cap to VSS.
CP_O	9	4	4	PO	CP_O	Charge pump output 3.3V, 10uF Cap to VSS.
CH	10	5	5	PIO	CH	Charge Pump Capacitor High Voltage Plate, 1uF Cap to CL
CL	11	6	6	PIO	CL	Charge Pump Capacitor Low Voltage Plate, 1uF Cap to CH
CP_I	12	7	7	PI	CP_I	Charge Pump Power Input, 10uF Cap to VSS.
PT2.7	15	8	8	IO XO I O O I I IO	PT2.7 HS_XOUT INT2.7 PWM3_4 MOSI_4 RX2_4 TCI2_8 SDA_8	Digital Input/ Output Pin High Speed Crystal XOUT ,2~16MHZ Interrupt Source INT 2.7 TimerB2, PWM3_4 Output Pin SPI Interface MOSI_4(Master output, Slave input) EUART2 Interface RX2_4 Timer C Capture Module PIN TCI2_8 I2C Interface SDA_8

Name	HY16F198-L100 HY16F198B-100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	Type	Pin Name	Description
PT2.6	16	9	9	IO XI I O I IO I IO	PT2.6 HS_XIN INT2.6 PWM2_4 MISO_4 TX2_4 TCI1_8 SCL_8	Digital Input/ Output Pin High Speed Crystal XIN ,2~16MHZ Interrupt Source INT 2.6 TimerB2, PWM2_4 Output Pin SPI Interface MISO_4(Master input, Slave output) EUART2 Interface TX2_4 Timer C Capture Module PIN TCI1_8 I2C Interface SCL_8
PT2.5	17	10	10	IO XO I O I I I IO	PT2.5 LS_XIN INT2.5 PWM1_4 CK_4 RX_4 TCI2_7 SDA_7	Digital Input/ Output Pin Low Speed Crystal XIN 32768HZ Interrupt Source INT 2.5 TimerB, PWM1_4 Output Pin SPI Interface CK_4 EUART Interface RX_4 Timer C Capture Module PIN TCI2_7 I2C Interface SDA_7
PT2.4	18	11	11	IO XI I O I IO I IO	PT2.4 LS_XOUT INT2.4 PWM0_4 CS_4 TX_4 TCI1_7 SCL_7	Digital Input/ Output Pin Low Speed Crystal XOUT 32768HZ Interrupt Source INT 2.4 TimerB, PWM0_4 Output Pin SPI Interface CS_4 EUART Interface TX_4 Timer C Capture Module PIN TCI1_7 I2C Interface SCL_7
PT2.3	19	-	-	IO I O O I I IO AI	PT2.3 INT2.3 PWM3_3 MOSI_3 RX2_3 TCI2_6 SDA_6 CL8	Digital Input/ Output Pin Interrupt Source INT 2.3 TimerB2, PWM3_3 Output Pin SPI Interface MOSI_3(Master output, Slave input) EUART2 Interface RX2_3 Timer C Capture Module PIN TCI2_6 I2C Interface SDA_6 Comparator Analog Input CL8
PT2.2	20	-	-	IO I	PT2.2 INT2.2	Digital Input/ Output Pin Interrupt Source INT 2.2

Name	HY16F198-L100 HY16F198B-100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	Type	Pin Name	Description
				O I IO I IO AI	PWM2_3 MISO_3 TX2_3 TCI1_6 SCL_6 CL7	TimerB2, PWM2_3 Output Pin SPI Interface MISO_3(Master input, Slave output) EUART2 Interface TX2_3 Timer C Capture Module PIN TCI1_6 I2C Interface SCL_6 Comparator Analog Input CL7
PT2.1	21	12	12	IO I O I I I IO AI	PT2.1 INT2.1 PWM1_3 CK_3 RX_3 TCI2_5 SDA_5 CL6	Digital Input/ Output Pin Interrupt Source INT 2.1 TimerB, PWM1_3 Output Pin SPI Interface CK_3 EUART Interface RX_3 Timer C Capture Module PIN TCI2_5 I2C Interface SDA_5 Comparator Analog Input CL6
PT2.0	22	13	13	IO I O I IO I IO AI	PT2.0 INT2.0 PWM0_3 CS_3 TX_3 TCI1_5 SCL_5 CL5	Digital Input/ Output Pin Interrupt Source INT 2.0 TimerB, PWM0_3 Output Pin SPI Interface CS_3 EUART Interface TX_3 Timer C Capture Module PIN TCI1_5 I2C Interface SCL_5 Comparator Analog Input CL5
VDD18	23	14	14	PI	VDD18	Digital Power Supply output 1.8V, 1uF Cap to VSS
PT1.7	24	15	15	IO AO I O O I I IO	PT1.7 CMPO INT1.7 PWM3_2 MOSI_2 RX2_2 TCI2_4 SDA_4	Digital Input/ Output Pin Comparator Output (Digital) Interrupt Source INT 1.7 TimerB2, PWM3_2 Output Pin SPI Interface MOSI_2(Master output, Slave input) EUART2 Interface RX2_2 Timer C Capture Module PIN TCI2_4 I2C Interface SDA_4
PT1.6	26	16	16	IO I	PT1.6 INT1.6	Digital Input/ Output Pin Interrupt Source INT 1.6

Name	HY16F198-L100 HY16F198B-100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	Type	Pin Name	Description
				O I IO I IO AI	PWM2_2 MISO_2 TX2_2 TCI1_4 SCL_4 CL4	TimerB2, PWM2_2 Output Pin SPI Interface MISO_2(Master input, Slave output) EUART2 Interface TX2_2 Timer C Capture Module PIN TCI1_4 I2C Interface SCL_4 Comparator Analog Input CL4
PT1.5	27	17	17	IO I O I I I IO AI	PT1.5 INT1.5 PWM1_2 CK_2 RX_2 TCI2_3 SDA_3 CL3	Digital Input/ Output Pin Interrupt Source INT 1.5 TimerB, PWM1_2 Output Pin SPI Interface CK_2 EUART Interface RX_2 Timer C Capture Module PIN TCI2_3 I2C Interface SDA_3 Comparator Analog Input CL3
PT1.4	28	18	18	IO I O I IO I IO AI	PT1.4 INT1.4 PWM0_2 CS_2 TX_2 TCI1_3 SCL_3 CL2	Digital Input/ Output Pin Interrupt Source INT 1.4 TimerB, PWM0_2 Output Pin SPI Interface CS_2 EUART Interface TX_2 Timer C Capture Module PIN TCI1_3 I2C Interface SCL_3 Comparator Analog Input CL2
PT1.3	29	19	19	IO I O O I I IO AI	PT1.3 INT1.3 PWM3_1 MOSI_1 RX2_1 TCI2_2 SDA_2 CL1	Digital Input/ Output Pin Interrupt Source INT1.3 TimerB2, PWM3_1 Output Pin SPI Interface MOSI_1(Master output, Slave input) EUART2 Interface RX2_1 Timer C Capture Module PIN TCI2_2 I2C Interface SDA_2 Comparator Analog Input CL1
PT1.2	30	20	-	IO I O I	PT1.2 INT1.2 PWM2_1 MISO_1	Digital Input/ Output Pin Interrupt Source INT 1.2 TimerB2, PWM2_1 Output Pin SPI Interface MISO_1(Master input,

Name	HY16F198-L100 HY16F198B-100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	Type	Pin Name	Description
				IO I IO AI	TX2_1 TCI1_2 SCL_2 CH3	Slave output) EUART2 Interface TX2_1 Timer C Capture Module PIN TCI1_2 I2C Interface SCL_2 Comparator Analog Input CH3
PT1.1	31	21	-	IO I O I I I IO AI	PT1.1 INT1.1 PWM1_1 CK_1 RX_1 TCI2_1 SDA_1 CH2	Digital Input/ Output Pin Interrupt Source INT 1.1 TimerB, PWM1_1 Output Pin SPI Interface CK_1 EUART Interface RX_1 Timer C Capture Module PIN TCI2_1 I2C Interface SDA_1 Comparator Analog Input CH2
PT1.0	32	22	20	IO I O I IO I IO AI	PT1.0 INT1.0 PWM0_1 CS_1 TX_1 TCI1_1 SCL_1 CH1	Digital Input/ Output Pin Interrupt Source INT 1.0 TimerB, PWM0_1 Output Pin SPI Interface CS_1 EUART Interface TX_1 Timer C Capture Module PIN TCI1_1 I2C Interface SCL_1 Comparator Analog Input CH1
VDDA	38	23	21	PIO	VDDA	Analog Power Supply, LDO Output, or Analog Power Input , 1uF Cap to VSS.
AIO3	39	24	22	AI	AIO3	ADC Analog Input Signal Port AIO3
AIO2	40	25	23	AI	AIO2	ADC Analog Input Signal Port AIO2
AIO1	41	-	24	AI	AIO1	ADC Analog Input Signal Port AIO1
AIO0	42	-	25	AI	AIO0	ADC Analog Input Signal Port AIO0
PT3.7	43	26	26	IO AO	PT3.7 OPO	Digital Input/ Output Pin Rail-to-rail OPAMP Analog Output Pin
PT3.6	44	27	27	IO PIO	PT3.6 REFO	Digital Input/ Output Pin Reference Voltage output 1.2V, 0.1uF Cap to VSS.
PT3.5	45	28	28	IO AI	PT3.5 AIO7	Digital Input/ Output Pin ADC Analog Input Signal Port AIO7
PT3.4	46	-	29	IO	PT3.4	Digital Input/ Output Pin

Name	HY16F198-L100 HY16F198B-100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	Type	Pin Name	Description
				AI	AIO6	ADC Analog Input Signal Port AIO6
PT3.3	47	29	30	IO AI	PT3.3 AIO5	Digital Input/ Output Pin ADC Analog Input Signal Port AIO5
PT3.2	48	30	31	IO AI	PT3.2 AIO4	Digital Input/ Output Pin ADC Analog Input Signal Port AIO4
PT3.1	49	-	32	IO AO AO	PT3.1 OPO2 DAO	Digital Input/ Output Pin Rail-to-rail OPAMP Digital Output Pin 8-BIT Resistance Ladders Output Pin
PT3.0	50	31	33	IO AO AI	PT3.0 OPO1 AIO8	Digital Input/ Output Pin Rail-to-rail OPAMP Digital Output Pin ADC Analog Input Signal Port AIO8
SEG35	58	32	-	IO AO	PT10.1 SEG35	Digital Input/ Output Pin LCD Segment Output
SEG34	59	33	-	IO AO	PT10.0 SEG34	Digital Input/ Output Pin LCD Segment Output
SEG33	60	34	34	IO AO O O I	PT9.7 SEG33 PWM3_8 MOSI_8 RX2_8	Digital Input/ Output Pin LCD Segment Output TimerB2, PWM3_8 Output Pin SPI Interface MOSI_8(Master output, Slave input) EUART2 Interface RX2_8
SEG32	61	35	35	IO AO O O I	PT9.6 SEG32 PWM2_8 MISO_8 TX2_8	Digital Input/ Output Pin LCD Segment Output TimerB2, PWM2_8 Output Pin SPI Interface MISO_8(Master input, Slave output) EUART2 Interface TX2_8
SEG31	62	36	36	IO AO O O I	PT9.5 SEG31 PWM1_8 CK_8 RX_8	Digital Input/ Output Pin LCD Segment Output TimerB, PWM1_8 Output Pin SPI Interface CK_8 EUART Interface RX_8
SEG30	63	37	37	IO AO O	PT9.4 SEG30 PWM0_8	Digital Input/ Output Pin LCD Segment Output TimerB, PWM0_8 Output Pin

Name	HY16F198-L100 HY16F198B-100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	Type	Pin Name	Description
				O I	CS_8 TX_8	SPI Interface CS_8 EUART Interface TX_8
SEG29	64	38	38	IO AO O O I	PT9.3 SEG29 PWM3_7 MOSI_7 RX2_7	Digital Input/ Output Pin LCD Segment Output TimerB2, PWM3_7 Output Pin SPI Interface MOSI_7(Master output, Slave input) EUART2 Interface RX2_7
SEG28	65	39	39	IO AO O O I	PT9.2 SEG28 PWM2_7 MISO_7 TX2_7	Digital Input/ Output Pin LCD Segment Output TimerB2, PWM2_7 Output Pin SPI Interface MISO_7(Master input, Slave output) EUART2 Interface TX2_7
SEG27	66	40	40	IO AO O O I	PT9.1 SEG27 PWM1_7 CK_7 RX_7	Digital Input/ Output Pin LCD Segment Output TimerB, PWM1_7 Output Pin SPI Interface CK_7 EUART Interface RX_7
SEG26	67	41	41	IO AO O O I	PT9.0 SEG26 PWM0_7 CS_7 TX_7	Digital Input/ Output Pin LCD Segment Output TimerB, PWM0_7 Output Pin SPI Interface CS_7 EUART Interface TX_7
SEG25	68	42	42	IO AO O O I I	PT8.7 SEG25 PWM3_6 MOSI_6 RX2_6 TCI3_8	Digital Input/ Output Pin LCD Segment Output Pin TimerB2, PWM3_6 Output SPI Interface MOSI_6(Master output, Slave input) EUART2 Interface RX2_6 Timer B2 Clock Trigger PIN TCI3_8
SEG24	69	43	43	IO AO O O I	PT8.6 SEG24 PWM2_6 MISO_6 TX2_6	Digital Input/ Output Pin LCD Segment Output TimerB2, PWM2_6 Output Pin SPI Interface MISO_6(Master input, Slave output)

Name	HY16F198-L100 HY16F198B-100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	Type	Pin Name	Description
						EUART2 Interface TX2_6
SEG23	70	44	44	IO AO O O I I	PT8.5 SEG23 PWM1_6 CK_6 RX_6 TCI3_7	Digital Input/ Output Pin LCD Segment Output TimerB, PWM1_6 Output Pin SPI Interface CK_6 EUART Interface RX_6 Timer B2 Clock Trigger PIN TCI3_7
SEG22	71	45	45	IO AO O O I	PT8.4 SEG22 PWM0_6 CS_6 TX_6	Digital Input/ Output Pin LCD Segment Output TimerB, PWM0_6 Output Pin SPI Interface CS_6 EUART Interface TX_6
SEG21	72	46	46	IO AO O O I I	PT8.3 SEG21 PWM3_5 MOSI_5 RX2_5 TCI3_6	Digital Input/ Output Pin LCD Segment Output TimerB2, PWM3_5 Output Pin SPI Interface MOSI_5(Master output, Slave input) EUART2 Interface RX2_5 Timer B2 Clock Trigger PIN TCI3_6
SEG20	73	47	47	IO AO O O I	PT8.2 SEG20 PWM2_5 MISO_5 TX2_5	Digital Input/ Output Pin LCD Segment Output TimerB2, PWM2_5 Output Pin SPI Interface MISO_5(Master input, Slave output) EUART2 Interface TX2_5
SEG19	74	48	48	IO AO O O I I	PT8.1 SEG19 PWM1_5 CK_5 RX_5 TCI3_5	Digital Input/ Output Pin LCD Segment Output TimerB, PWM1_5 Output Pin SPI Interface CK_5 EUART Interface RX_5 Timer B2 Clock Trigger PIN TCI3_5
VPP	75	-	-	PI	VPP	Reserve (can't connect to any pin)
SEG18	76	49	49	IO AO O	PT8.0 SEG18 PWM0_5	Digital Input/ Output Pin LCD Segment Output TimerB, PWM0_5 Output

Name	HY16F198-L100 HY16F198B-100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	Type	Pin Name	Description
				O	CS_5	SPI Interface CS_5
				I	TX_5	EUART Interface TX_5
SEG17	77	50	50	IO	PT7.7	Digital Input/ Output Pin
				AO	SEG17	LCD Segment Output
				I	TCI3_4	Timer B2 Clock Trigger PIN TCI3_4
SEG16	78	51	51	IO	PT7.6	Digital Input/ Output Pin
				AO	SEG16	LCD Segment Output
SEG15	79	52	52	IO	PT7.5	Digital Input/ Output Pin
				AO	SEG15	LCD Segment Output
				I	TCI3_3	Timer B2 Clock Trigger PIN TCI3_3
SEG14	80	53	53	IO	PT7.4	Digital Input/ Output Pin
				AO	SEG14	LCD Segment Output
SEG13	81	54	54	IO	PT7.3	Digital Input/ Output Pin
				AO	SEG13	LCD Segment Output
				I	TCI3_2	Timer B2 Clock Trigger PIN TCI3_2
SEG12	82	55	55	IO	PT7.2	Digital Input/ Output Pin
				AO	SEG12	LCD Segment Output
SEG11	83	-	-	IO	PT7.1	Digital Input/ Output Pin
				AO	SEG11	LCD Segment Output
				I	TCI3_1	Timer B2 Clock Trigger PIN TCI3_1
SEG10	84	-	-	IO	PT7.0	Digital Input/ Output Pin
				AO	SEG10	LCD Segment Output
SEG9	85	-	-	IO	PT6.7	Digital Input/ Output Pin
				AO	SEG9	LCD Segment Output
SEG8	86	-	-	IO	PT6.6	Digital Input/ Output Pin
				AO	SEG8	LCD Segment Output
SEG7	87	-	-	IO	PT6.5	Digital Input/ Output Pin
				AO	SEG7	LCD Segment Output
SEG6	88	-	-	IO	PT6.4	Digital Input/ Output Pin
				AO	SEG6	LCD Segment Output
SEG5	89	-	-	IO	PT6.3	Digital Input/ Output Pin
				AO	SEG5	LCD Segment Output
SEG4	90	-	-	IO	PT6.2	Digital Input/ Output Pin
				AO	SEG4	LCD Segment Output
SEG3	91	-	-	IO	PT6.1	Digital Input/ Output Pin

Name	HY16F198-L100 HY16F198B-100	HY16F197-L064 HY16F197B-L064	HY16F196-L064 HY16F196B-L064	Type	Pin Name	Description
				AO	SEG3	LCD Segment Output
SEG2	92	-	-	IO AO	PT6.0 SEG2	Digital Input/ Output Pin LCD Segment Output
SEG1	93	56	56	IO AO AO	PT10.3 SEG1 COM5	Digital Input/ Output Pin LCD Segment Output LCD Common Output
SEG0	94	57	57	IO AO AO	PT10.2 SEG0 COM4	Digital Input/ Output Pin LCD Segment Output LCD Common Output
COM3	95	58	58	AO	COM3	LCD Common Output
COM2	96	59	59	AO	COM2	LCD Common Output
COM1	97	60	60	AO	COM1	LCD Common Output
COM0	98	61	61	AO	COM0	LCD Common Output
VLCD	99	62	62	PIO	VLCD	LCD Power Supply Output, or Power Supply Input, 10uF Cap to VSS.
VSS	100	63	63	PI	VSS	System Power Ground
Others	-	-	-	-	NC	Not Connect

Table 2-1 HY16F198/198B/197/197B/196/196B Pin definition and description

2.4.2 GPIO Port Function Configuration

Function	INT	Timer C Capture	Special Function	SPI	I²C	UART	AIP	Analog	Timer B/B2 PWM
Output Priority	I/P	I/P	0	1	2	3	4	5	6
PT1.0	INT1.0	TCI1_1		CS_1	SCL_1	Tx_1		CH1	PWM0_1
PT1.1	INT1.1	TCI2_1		CK_1	SDA_1	Rx_1		CH2	PWM1_1
PT1.2	INT1.2	TCI1_2		MISO_1	SCL_2	Tx2_1		CH3	PWM2_1
PT1.3	INT1.3	TCI2_2		MOSI_1	SDA_2	Rx2_1		CL1	PWM3_1
PT1.4	INT1.4	TCI1_3		CS_2	SCL_3	Tx_2		CL2	PWM0_2
PT1.5	INT1.5	TCI2_3		CK_2	SDA_3	Rx_2		CL3	PWM1_2
PT1.6	INT1.6	TCI1_4		MISO_2	SCL_4	Tx2_2		CL4	PWM2_2
PT1.7	INT1.7	TCI2_4		MOSI_2	SDA_4	Rx2_2	CMPO		PWM3_2
PT2.0	INT2.0	TCI1_5		CS_3	SCL_5	Tx_3		CL5	PWM0_3
PT2.1	INT2.1	TCI2_5		CK_3	SDA_5	Rx_3		CL6	PWM1_3
PT2.2	INT2.2	TCI1_6		MISO_3	SCL_6	Tx2_3		CL7	PWM2_3
PT2.3	INT2.3	TCI2_6		MOSI_3	SDA_6	Rx2_3		CL8	PWM3_3
PT2.4	INT2.4	TCI1_7	LS_XOUT	CS_4	SCL_7	Tx_4			PWM0_4
PT2.5	INT2.5	TCI2_7	LS_XIN	CK_4	SDA_7	Rx_4			PWM1_4
PT2.6	INT2.6	TCI1_8	HS_XIN	MISO_4	SCL_8	Tx2_4			PWM2_4
PT2.7	INT2.7	TCI2_8	HS_XOUT	MOSI_4	SDA_8	Rx2_4			PWM3_4
PT3.0							OPO1	AIO8	
PT3.1							OPO2	DAO	
PT3.2								AIO4	
PT3.3								AIO5	
PT3.4								AIO6	
PT3.5								AIO7	
PT3.6								REFO	
PT3.7								OPO	
RESET	RESET								
AIO0								AIO0	
AIO1								AIO1	
AIO2								AIO2	
AIO3								AIO3	
COM0			COM 0						
COM1			COM 1						
COM2			COM 2						
COM3			COM 3						
PT10.2			COM 4/SEG 0						

PT10.3			COM 5/SEG 1						
PT6.0			SEG 2						
PT6.1			SEG 3						
PT6.2			SEG 4						
PT6.3			SEG 5						
PT6.4			SEG 6						
PT6.5			SEG 7						
PT6.6			SEG 8						
PT6.7			SEG 9						
PT7.0			SEG 10						
PT7.1		TCI3_1	SEG 11						
PT7.2			SEG 12						
PT7.3		TCI3_2	SEG 13						
PT7.4			SEG 14						
PT7.5		TCI3_3	SEG 15						
PT7.6			SEG 16						
PT7.7		TCI3_4	SEG 17						
PT8.0			SEG 18	CS_5		Tx_5			PWM0_5
PT8.1		TCI3_5	SEG 19	CK_5		Rx_5			PWM1_5
PT8.2			SEG 20	MISO_5		Tx2_5			PWM2_5
PT8.3		TCI3_6	SEG 21	MOSI_5		Rx2_5			PWM3_5
PT8.4			SEG 22	CS_6		Tx_6			PWM0_6
PT8.5		TCI3_7	SEG 23	CK_6		Rx_6			PWM1_6
PT8.6			SEG 24	MISO_6		Tx2_6			PWM2_6
PT8.7		TCI3_8	SEG 25	MOSI_6		Rx2_6			PWM3_6
PT9.0			SEG 26	CS_7		Tx_7			PWM0_7
PT9.1			SEG 27	CK_7		Rx_7			PWM1_7
PT9.2			SEG 28	MISO_7		Tx2_7			PWM2_7
PT9.3			SEG 29	MOSI_7		Rx2_7			PWM3_7
PT9.4			SEG 30	CS_8		Tx_8			PWM0_8
PT9.5			SEG 31	CK_8		Rx_8			PWM1_8
PT9.6			SEG 32	MISO_8		Tx2_8			PWM2_8
PT9.7			SEG 33	MOSI_8		Rx2_8			PWM3_8
PT10.0			SEG 34						
PT10.1			SEG 35						

3. Application Circuit

3.1. Bridge Sensor

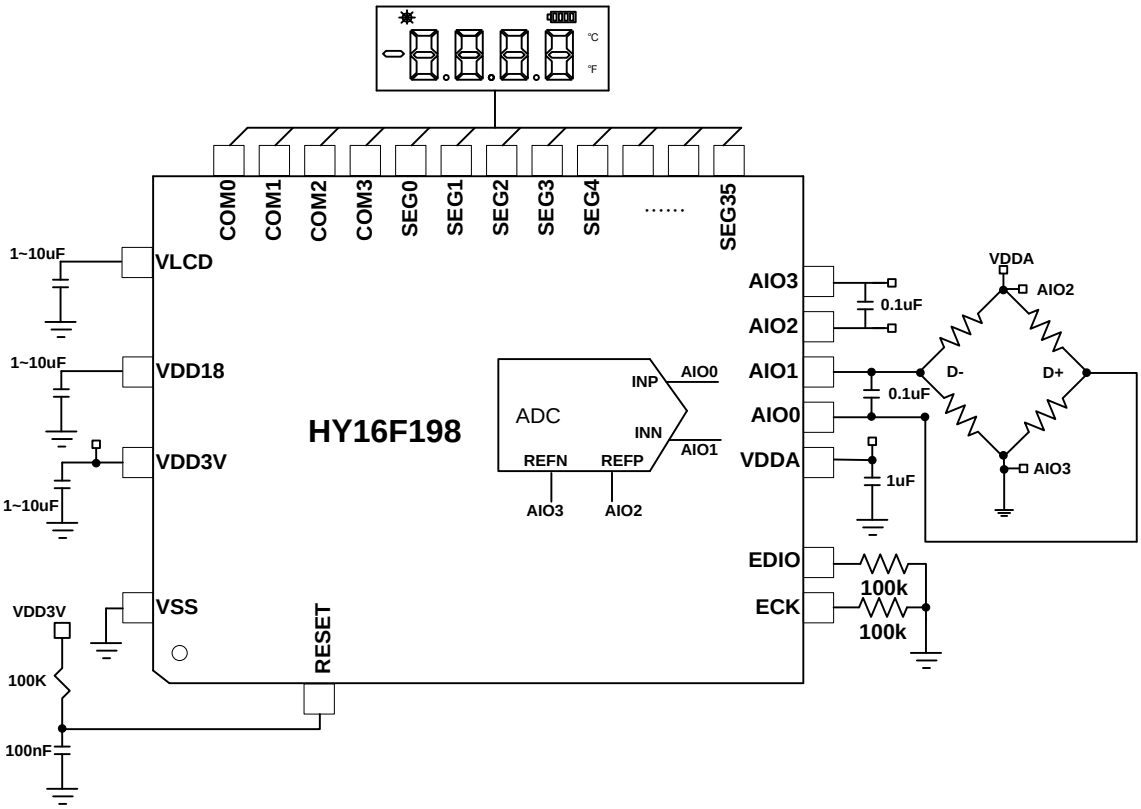


Figure 3-1 Bridge Sensor Circuit

3.2. Blood Pressure Sensor

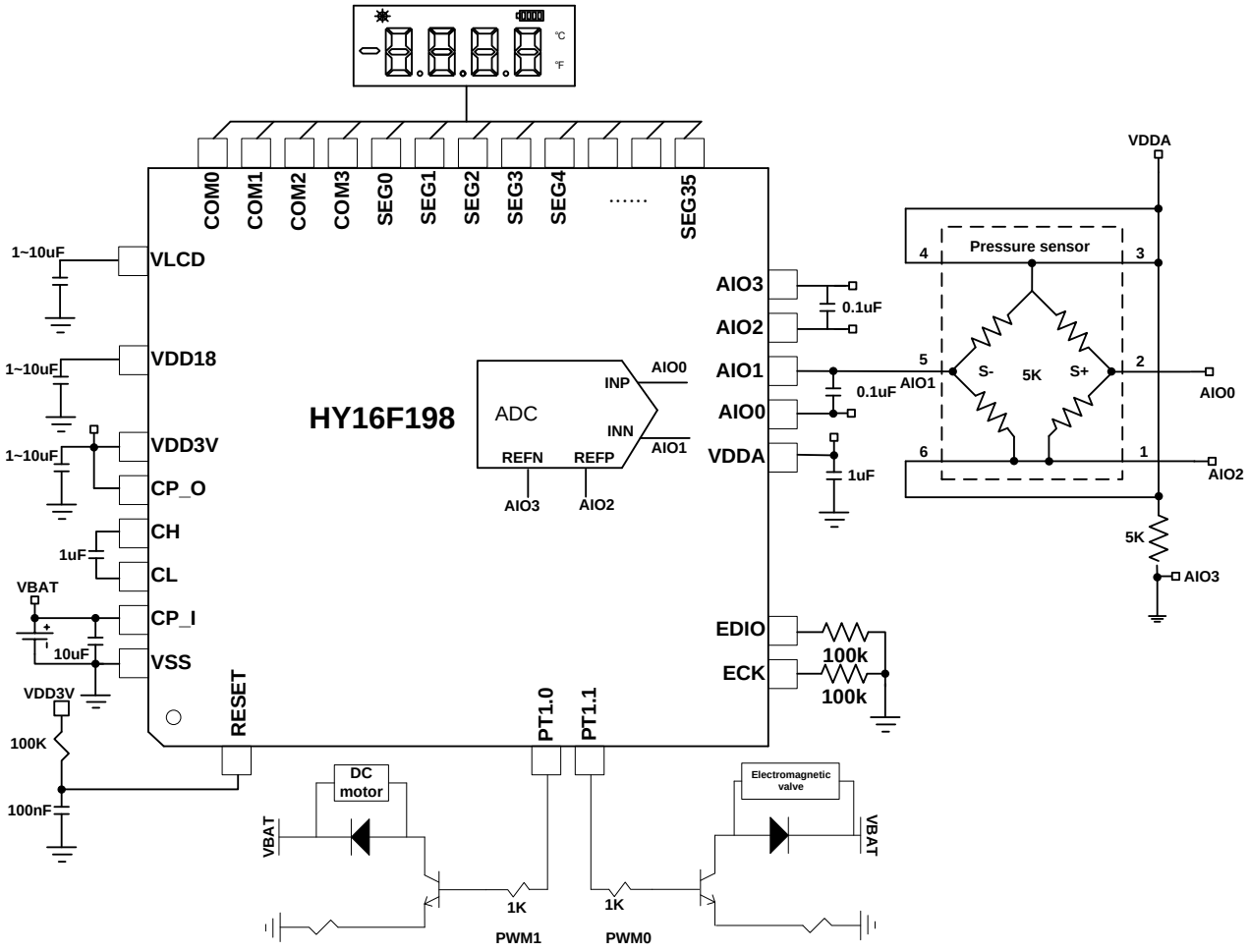


Figure 3-2 Blood Pressure Sensor Circuit

3.3. Electrochemical Sensor

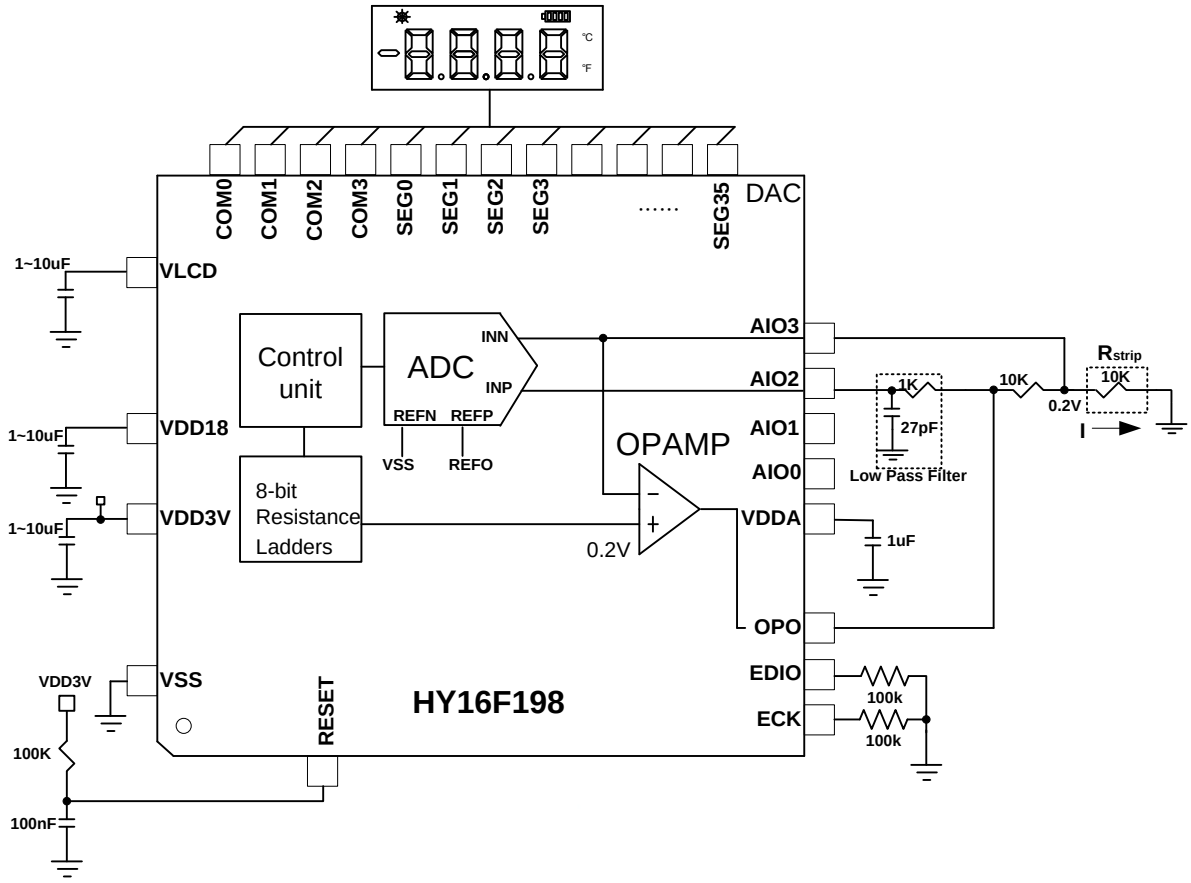


Figure 3-3 Electrochemical Sensor Circuit

3.4. Touch Key Sensor

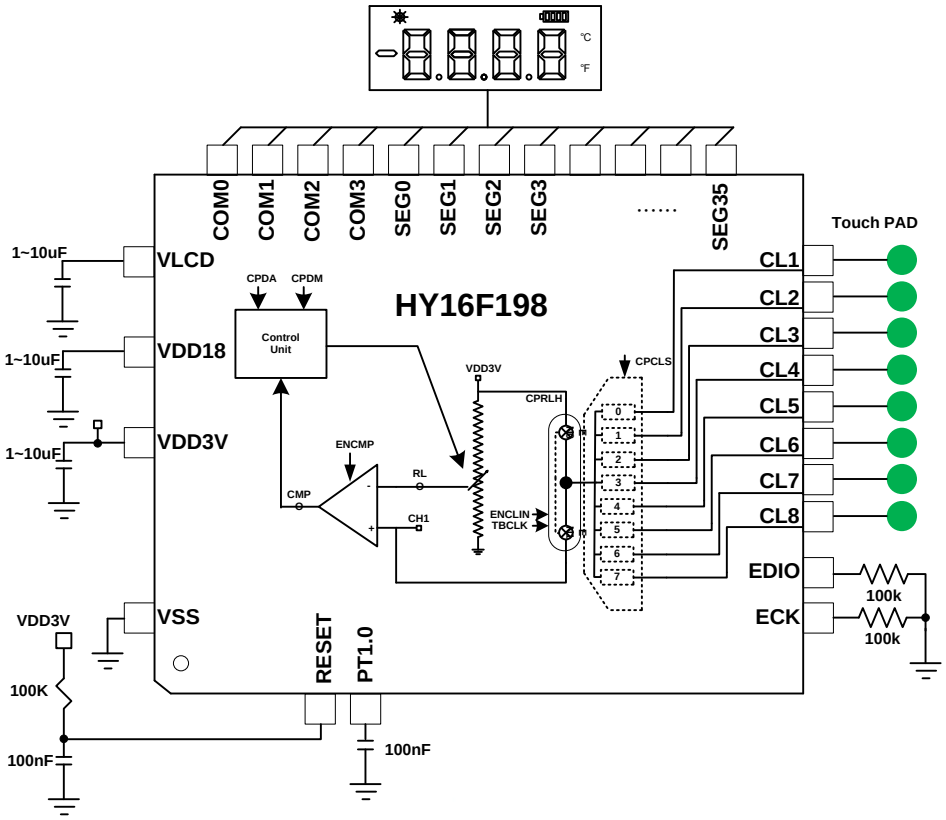


Figure 3-4 Touch Key Sensor Circuit

3.5. 3-in-1 Blood Glucose Meter

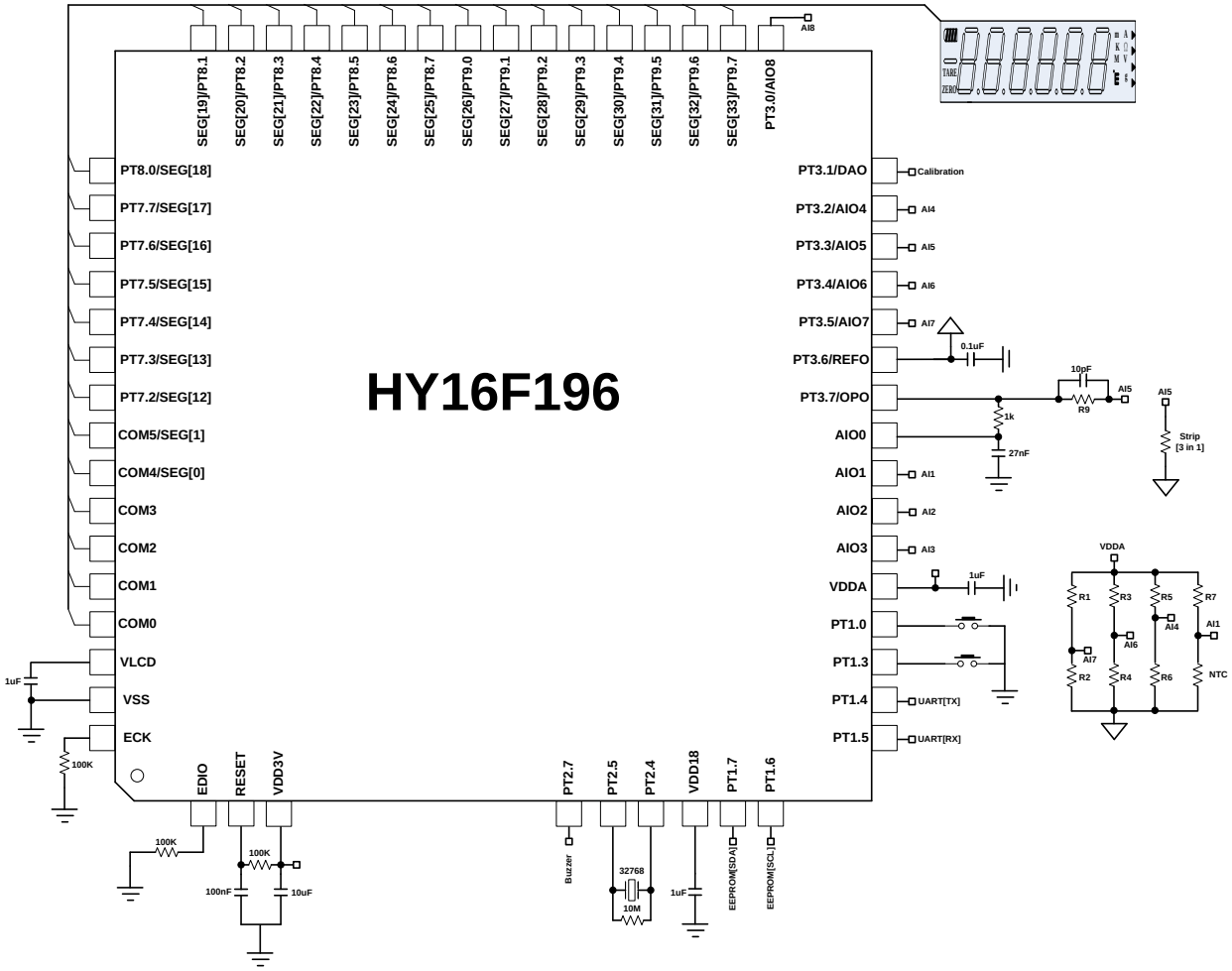


Figure 3-5 3-in-1 Blood Glucose Meter Circuit

4. Function Outline

4.1. Internal Block Diagram

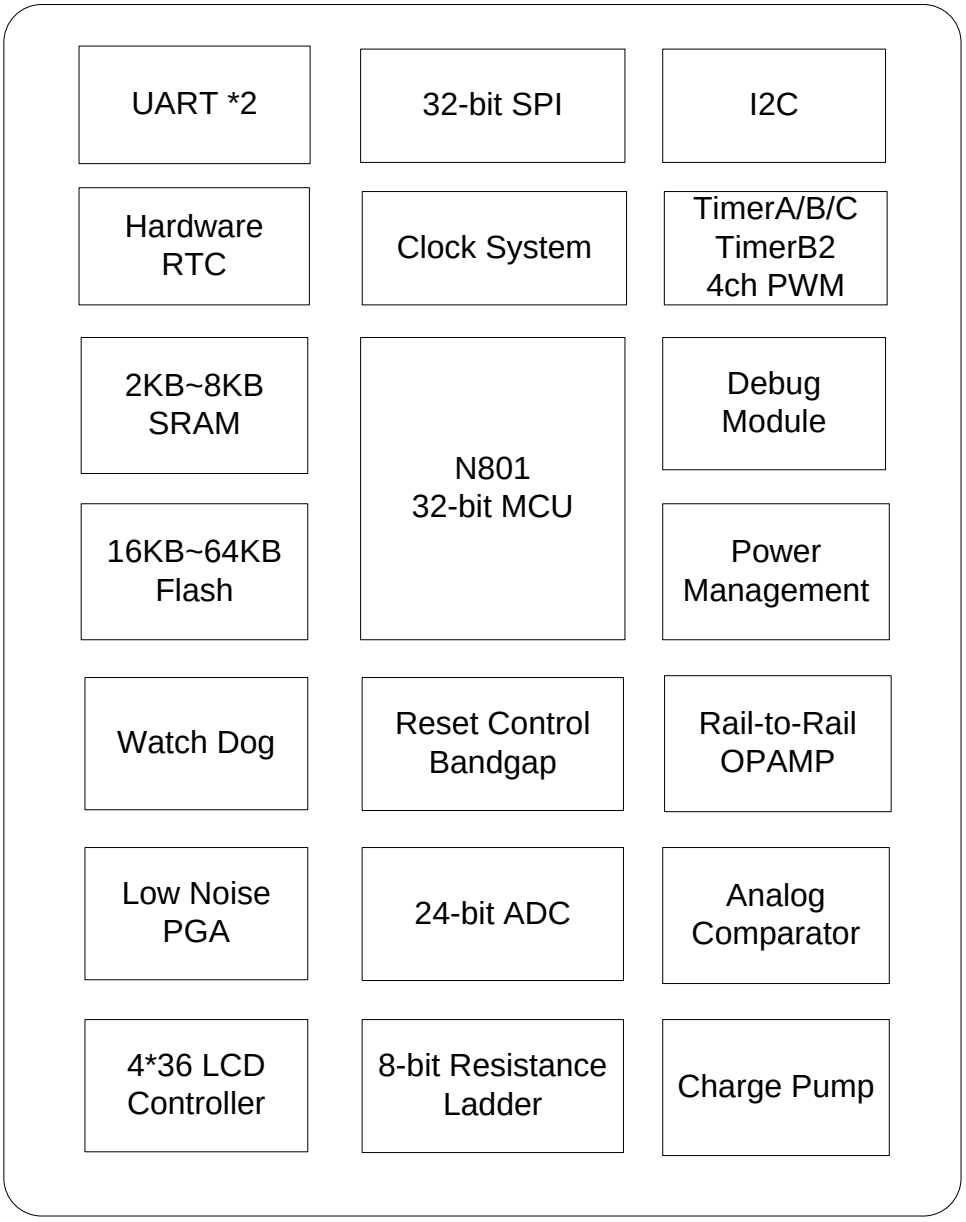


Figure 4-1 HY16F198 Internal Block Diagram

4.2. Building Block Diagram

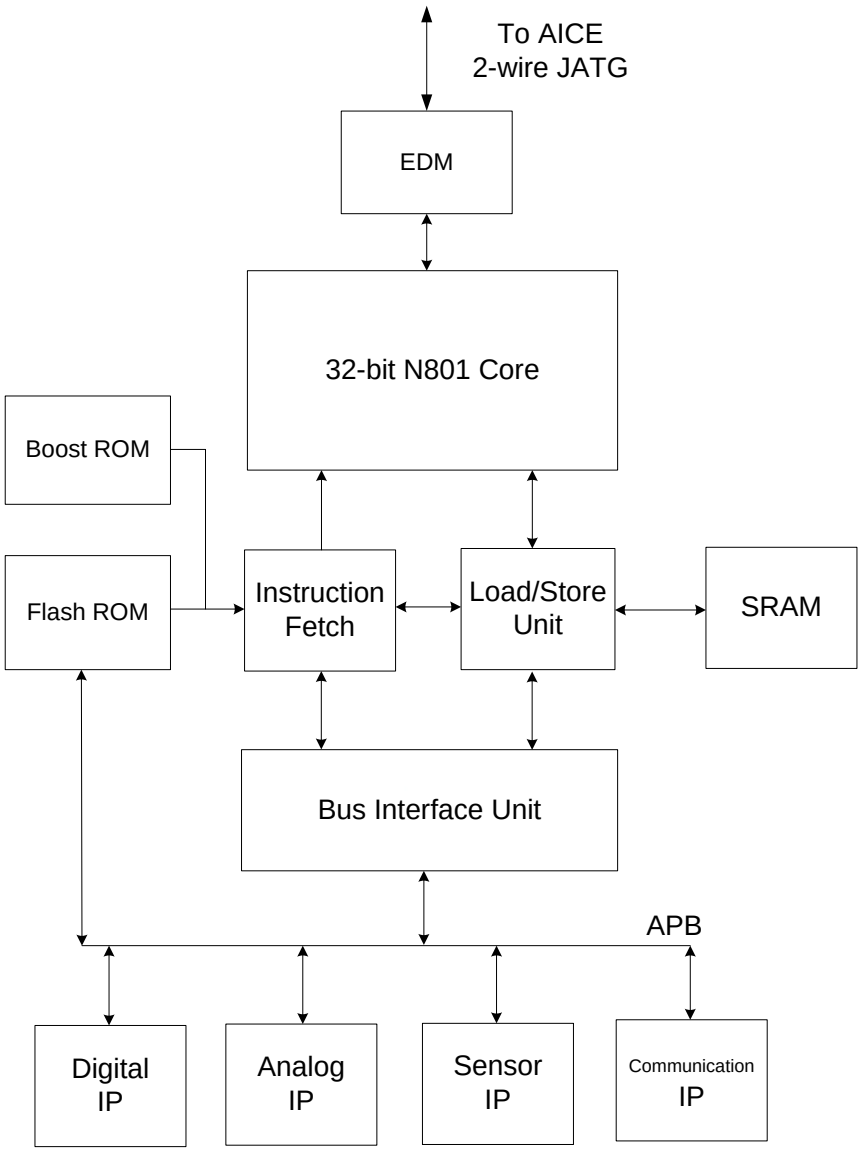
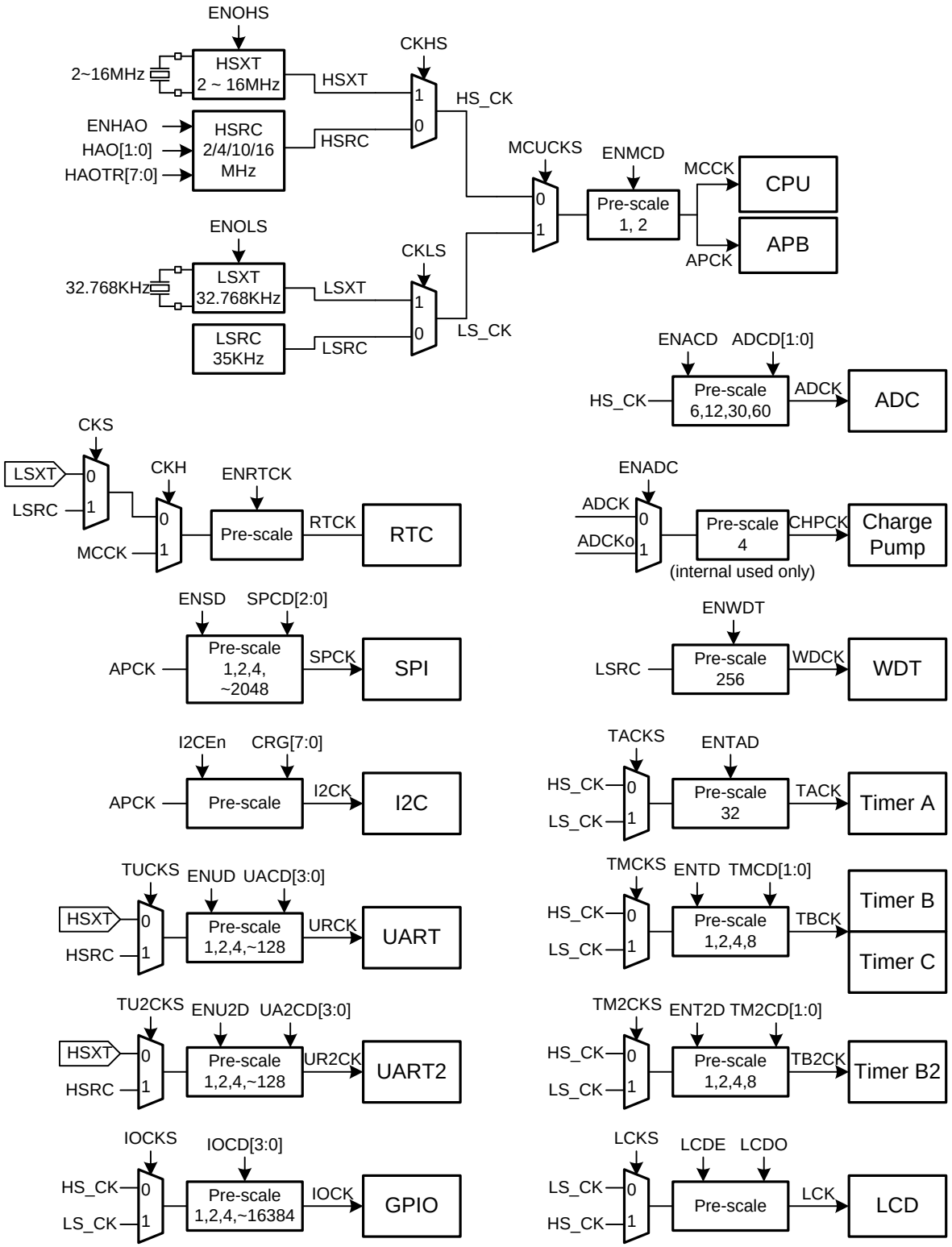


Figure 4-2 Building Block Diagram

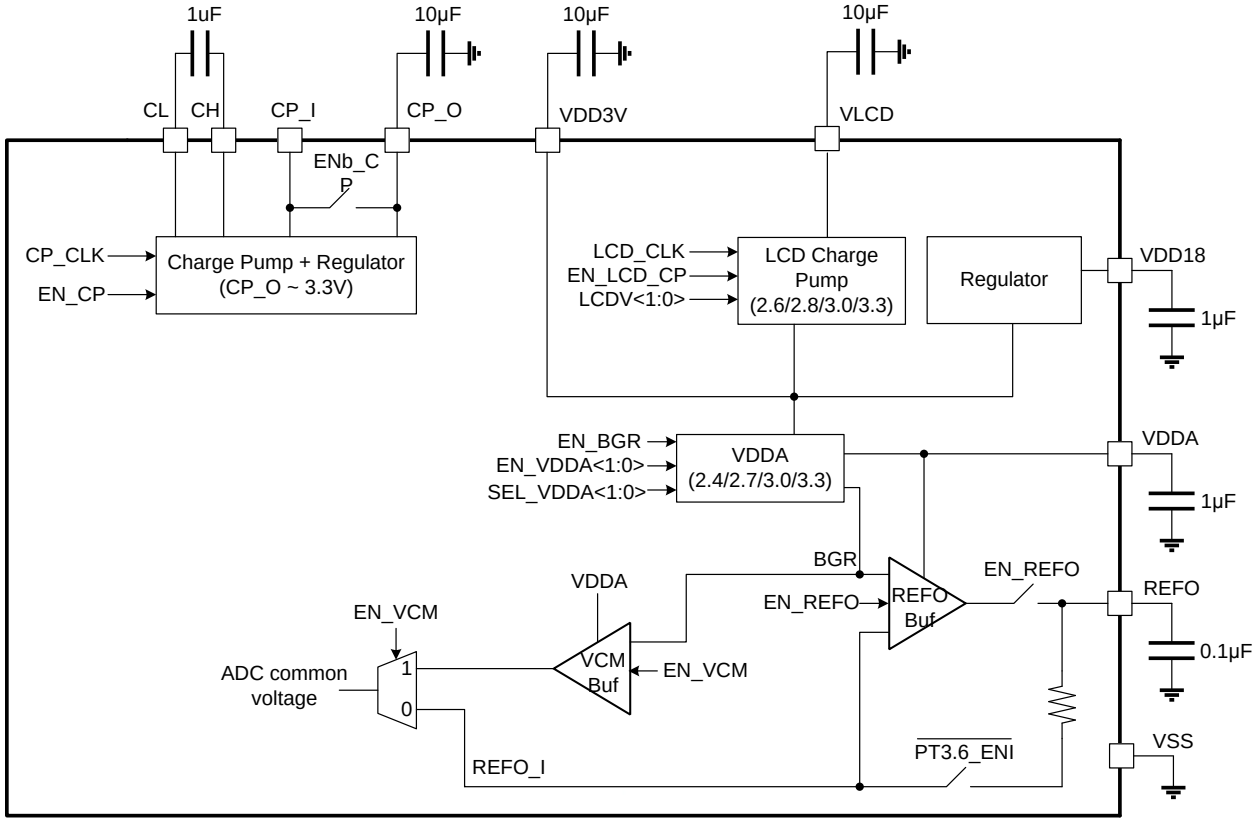
4.3. Related Description and Supporting Document

File Name	Description
UG-HY16F198	HY16F19 User Guide
APD-HY16IDE007	HY16F19X C Library Manual
APD-HY16IDE005	HY16F19X C Compile operation description
APD-HY16IDE008	HY16F19X IP User Manual
APD-HY16IDE001	HY16F Series IDE Software User Manual/ HY16F Series Device setup file
APD-HY16IDE009	HY16F Series IDE Hardware User Manual
APD-HY16IDE006	HY16F Series Writer kit User Manual

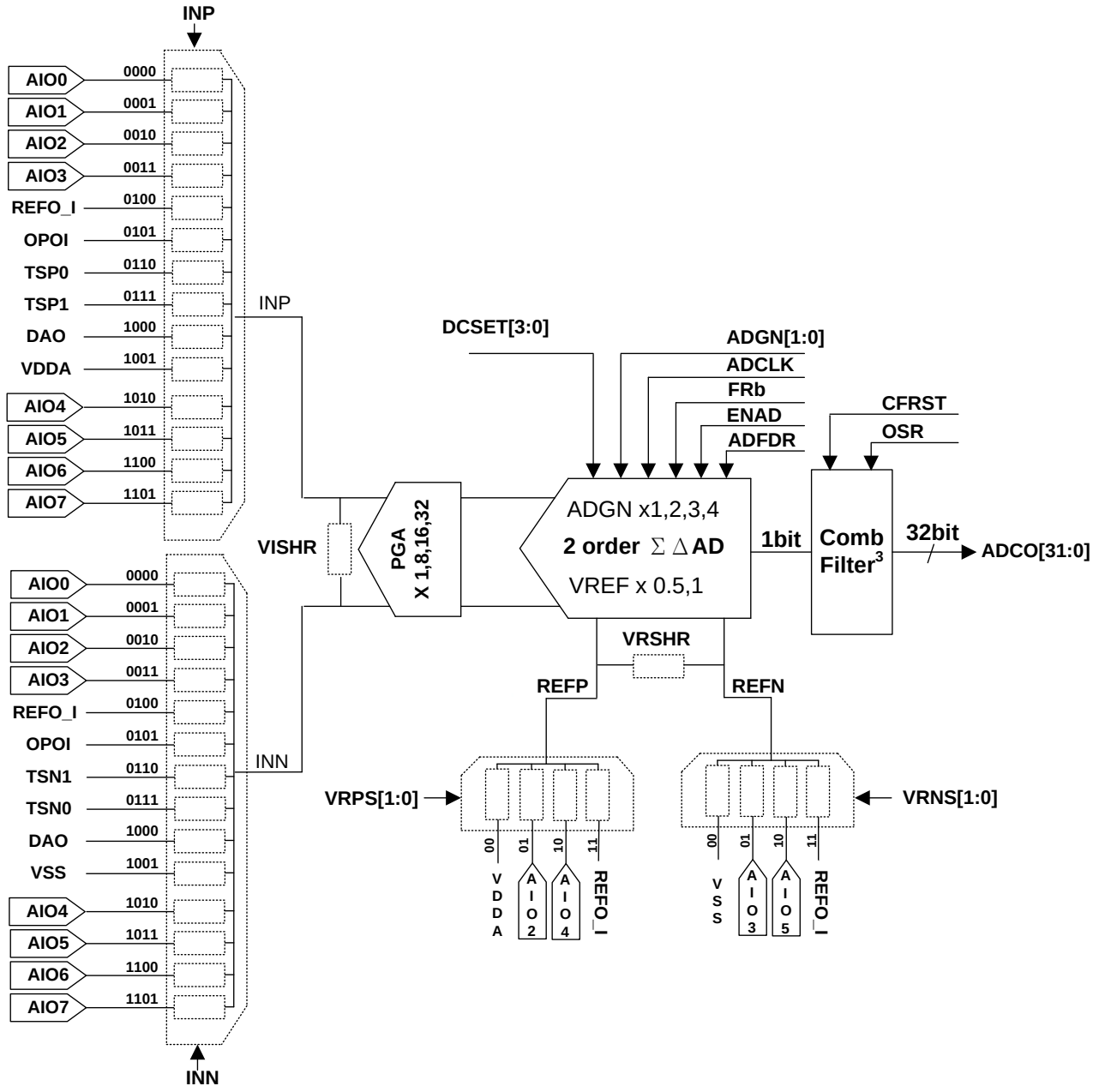
4.4. Clock System Network



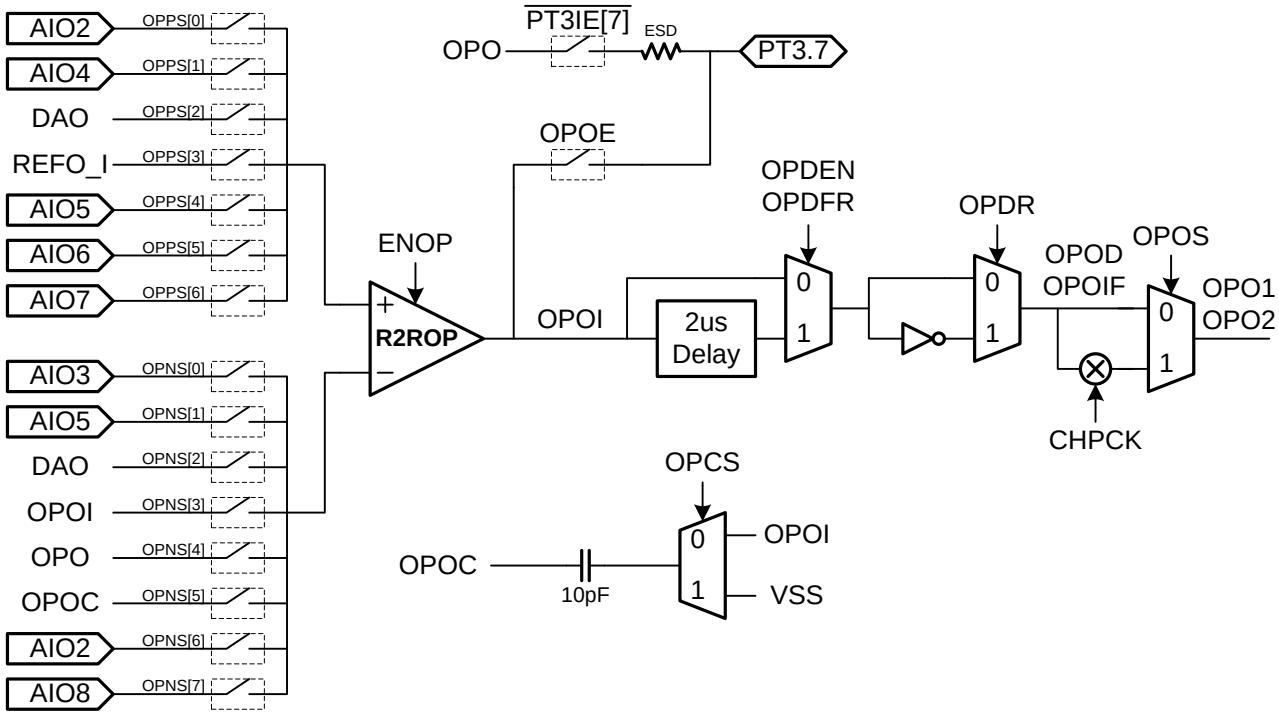
4.5. Power System Network



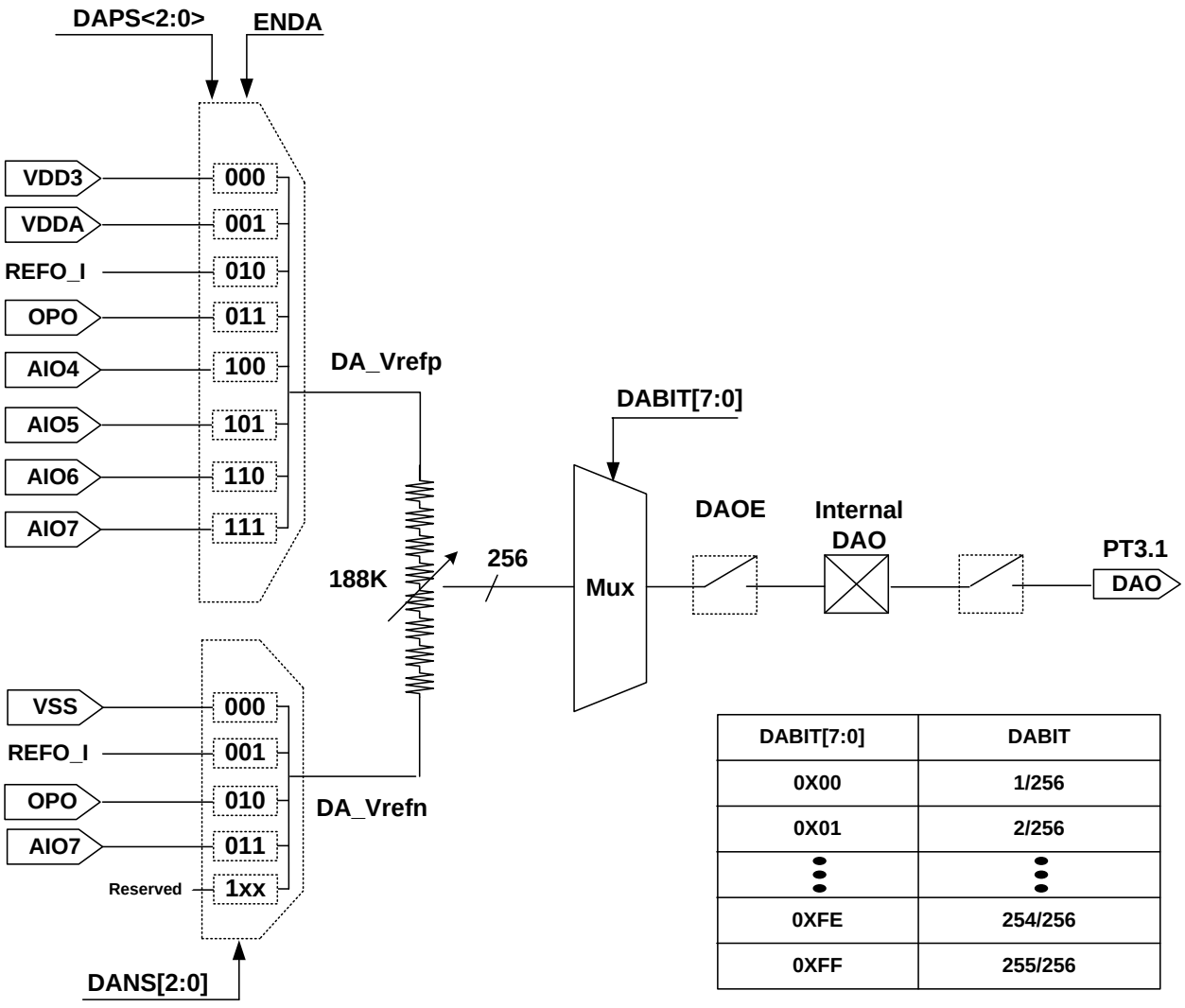
4.6. 24-bit ΣΔADC Network



4.7. Rail to Rail OPAMP Network

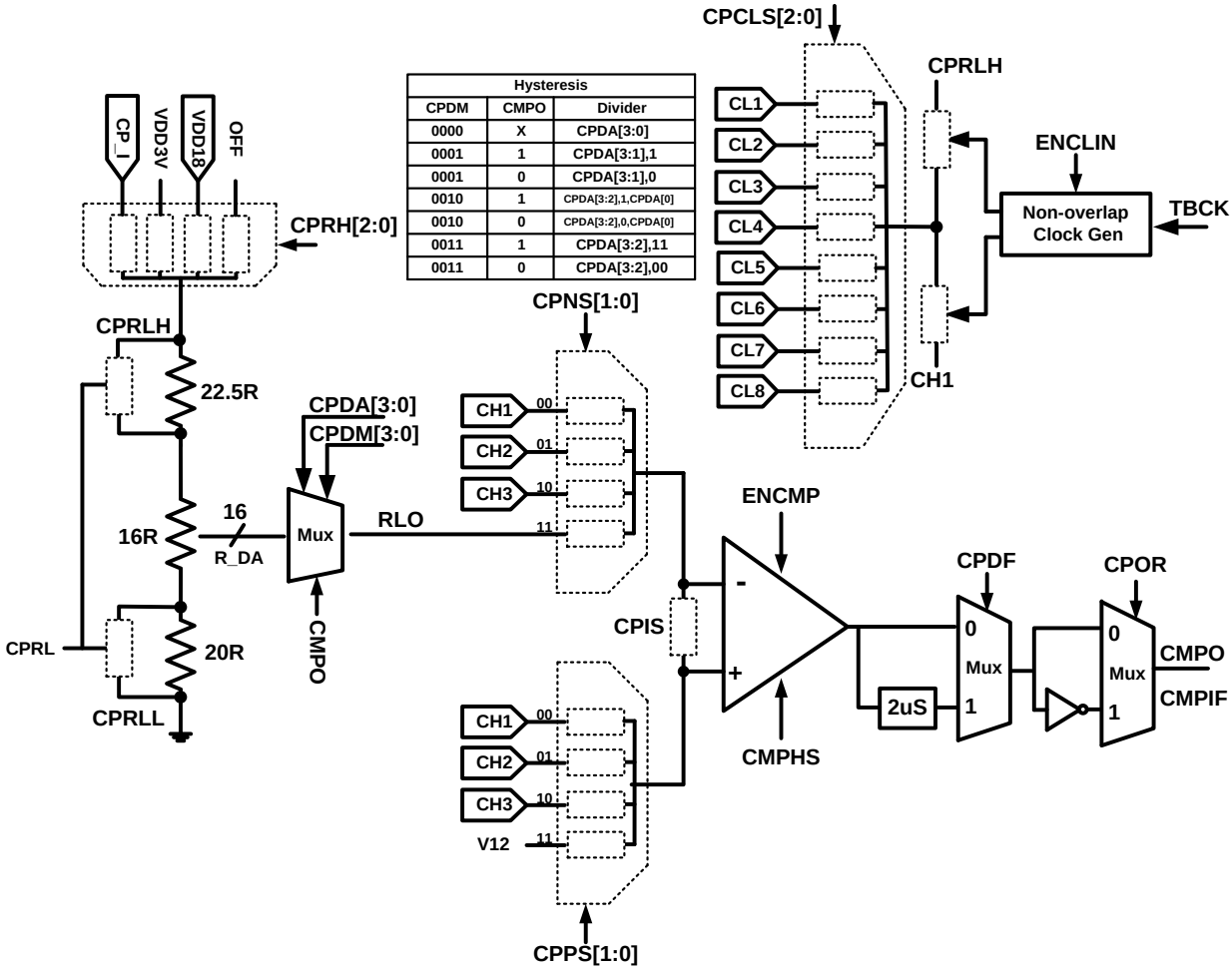


4.8. 8-bit Resistance Ladder Network



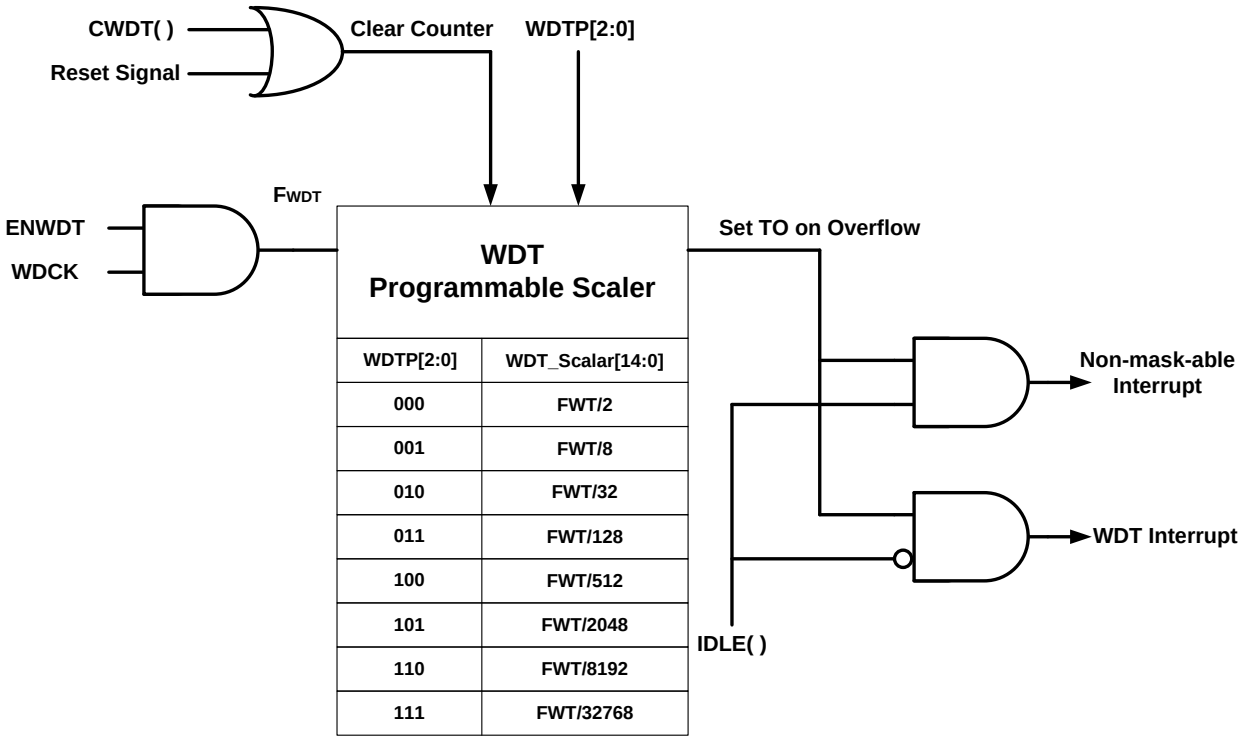
DABIT[7:0]	DABIT
0X00	1/256
0X01	2/256
⋮	⋮
0XFE	254/256
0XFF	255/256

4.9. Analog Comparator Network



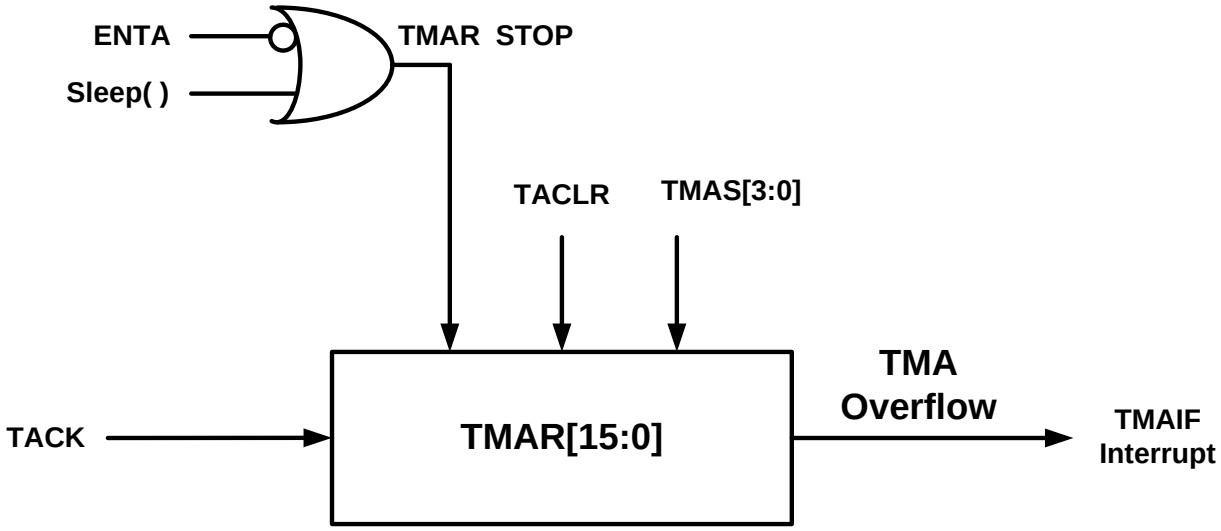
Hysteresis		
CPDM	CMPO	Divider
0000	X	CPDA[3:0]
0001	1	CPDA[3:1],1
0001	0	CPDA[3:1],0
0010	1	CPDA[3:2],1,CPDA[0]
0010	0	CPDA[3:2],0,CPDA[0]
0011	1	CPDA[3:2],11
0011	0	CPDA[3:2],00

4.10. Watch Dog Timer Network



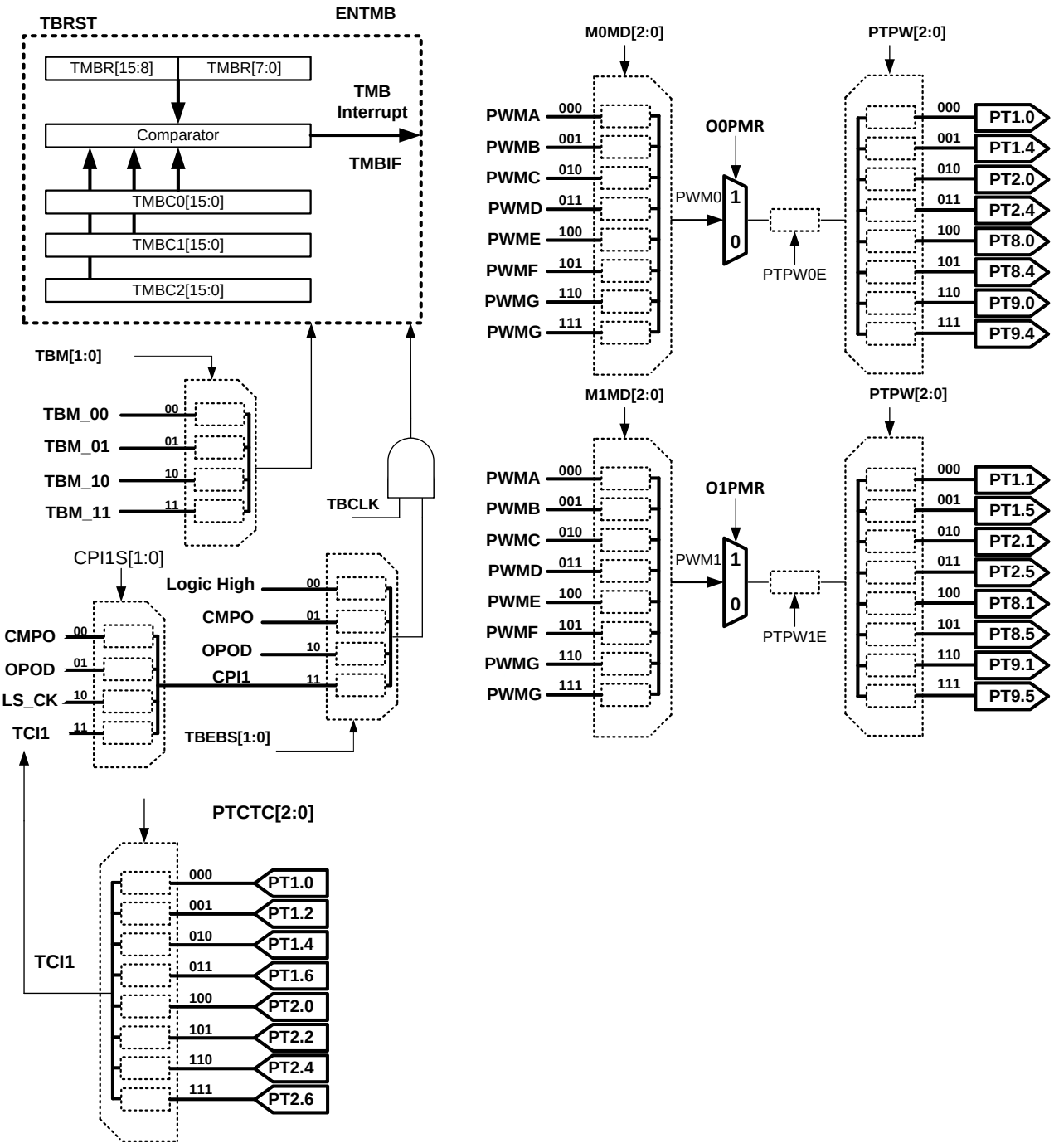
WDTP[2:0]	WDT_Scalar[14:0]
000	FWT/2
001	FWT/8
010	FWT/32
011	FWT/128
100	FWT/512
101	FWT/2048
110	FWT/8192
111	FWT/32768

4.11. Timer A Network

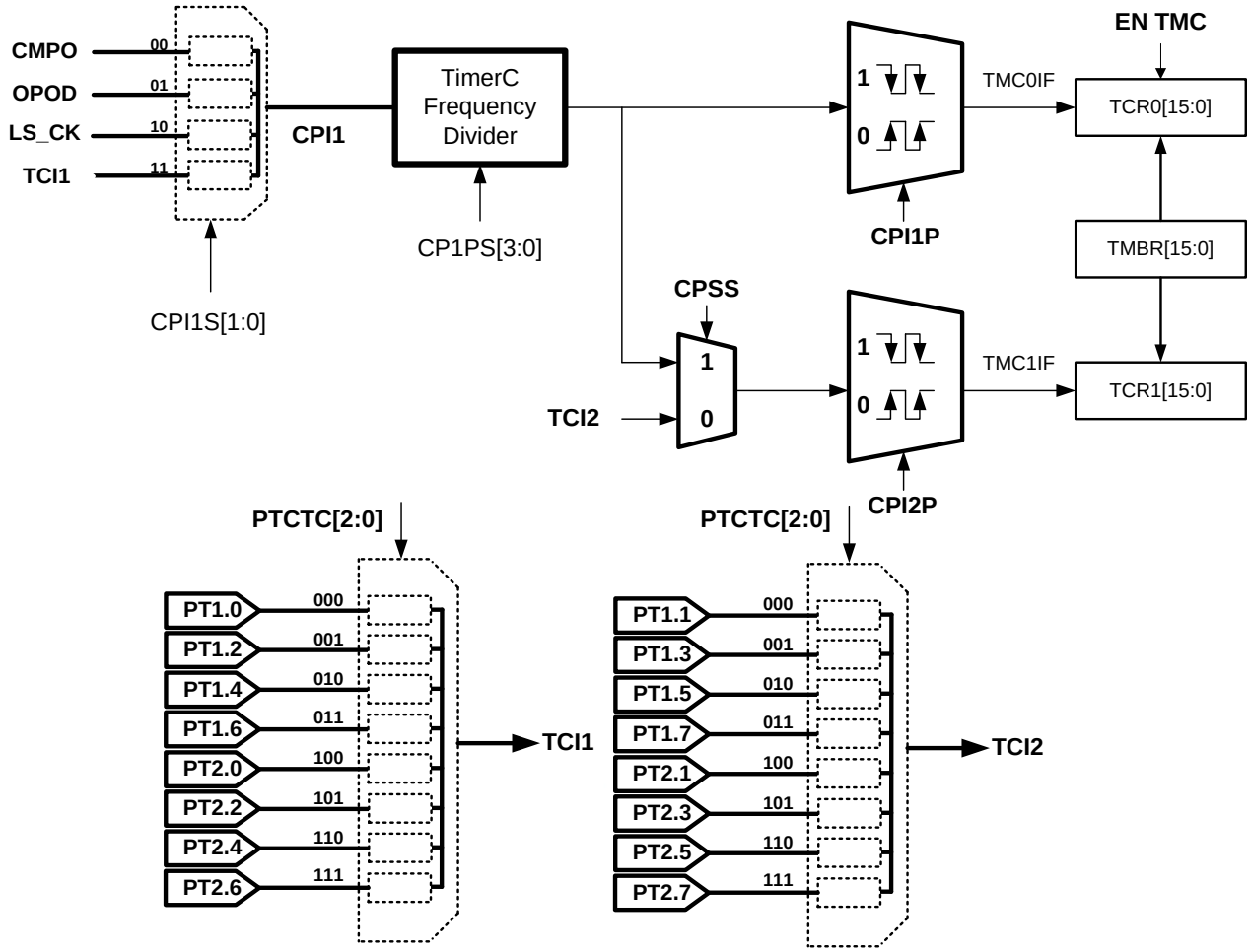


TMAS[3:0]	TMAR[15:0]	TMAS[3:0]	TMAR[15:0]
0000	TACK/2	1000	TACK/512
0001	TACK/4	1001	TACK/1024
0010	TACK/8	1010	TACK/2048
0011	TACK/16	1011	TACK/4096
0100	TACK/32	1100	TACK/8192
0101	TACK/64	1101	TACK/16384
0110	TACK/128	1110	TACK/32768
0111	TACK/256	1111	TACK/65536

4.12. Timer B Network

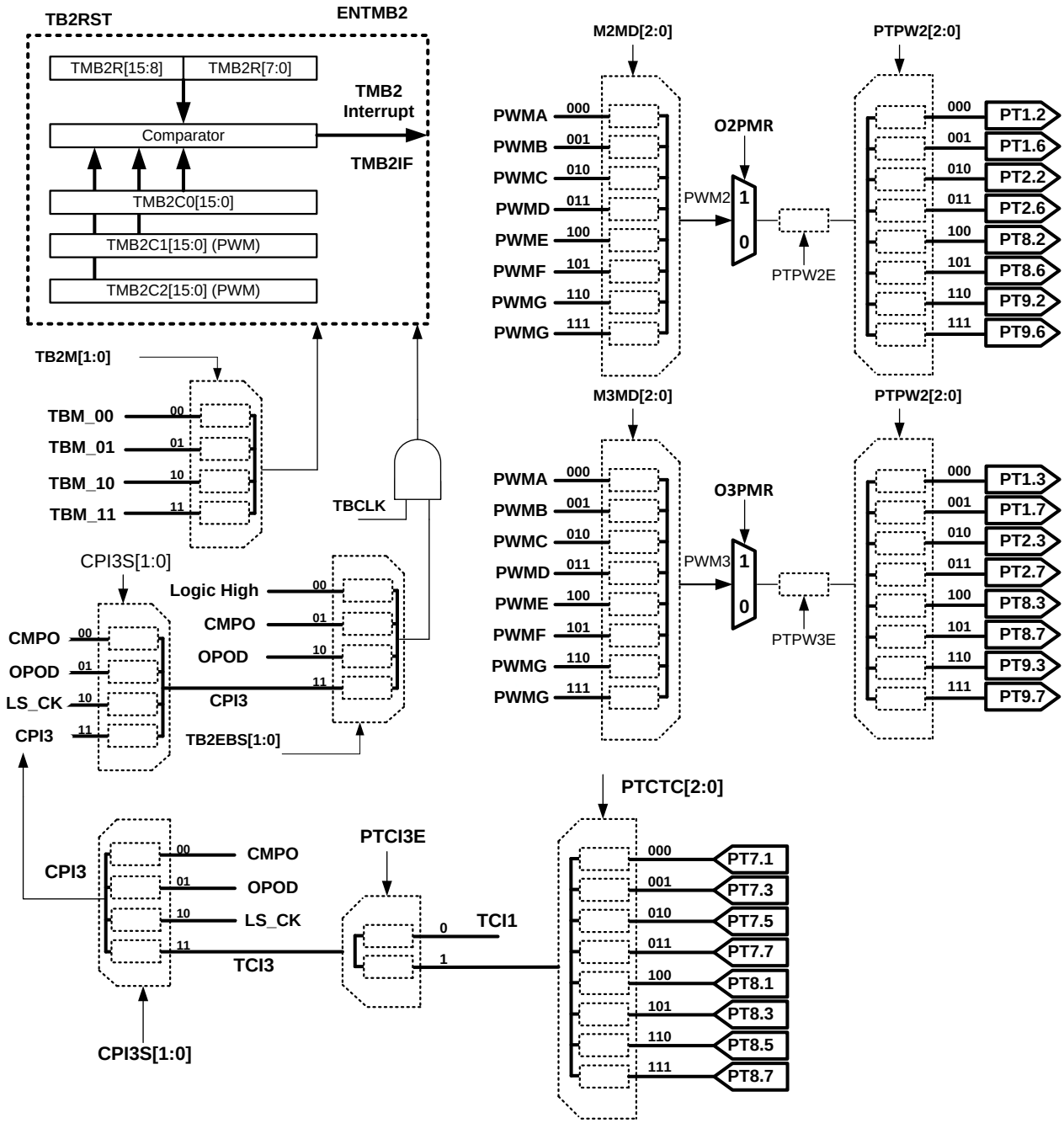


4.13. Timer C Network

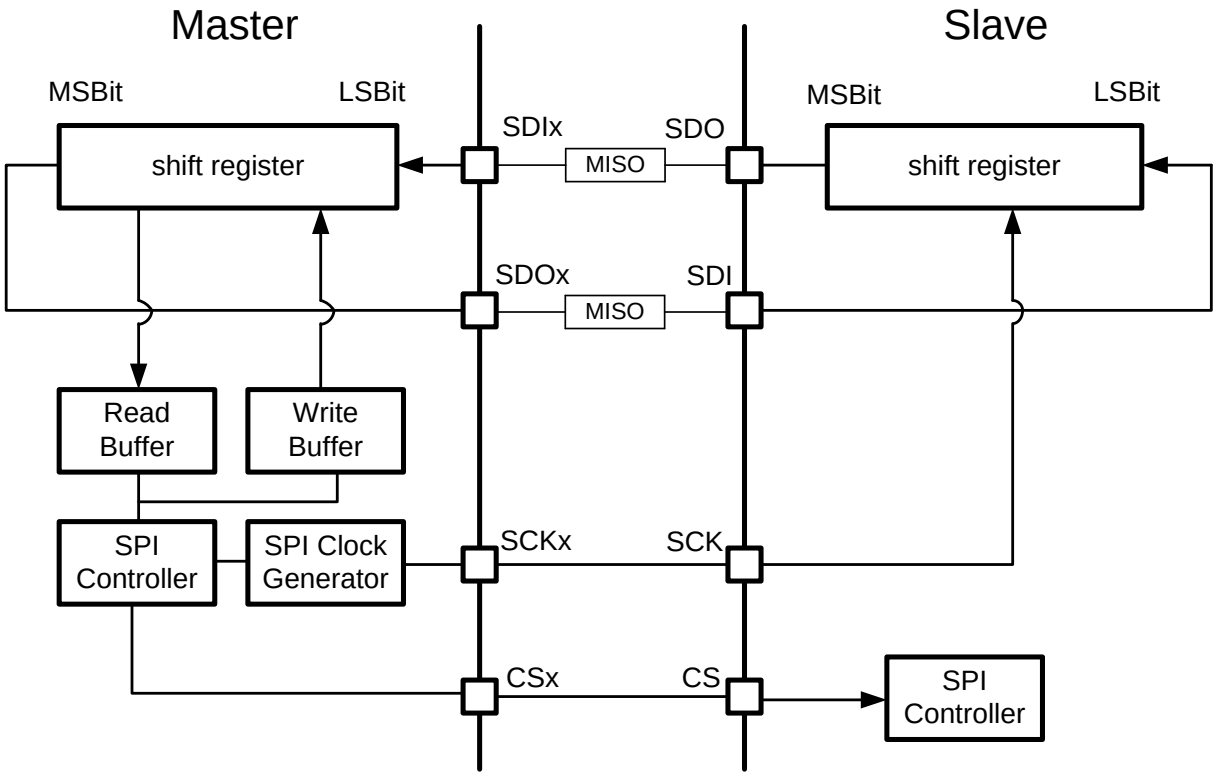


CP1PS[3:0]	CPI1 Divider	CP1PS[3:0]	CPI1 Divider
0000	CPI1/1	1000	CPI1/256
0001	CPI1/2	1001	CPI1/512
0010	CPI1/4	1010	CPI1/1024
0011	CPI1/8	1011	CPI1/2048
0100	CPI1/16	1100	CPI1/4096
0101	CPI1/32	1101	CPI1/8192
0110	CPI1/64	1110	CPI1/16384
0111	CPI1/128	1111	CPI1/32768

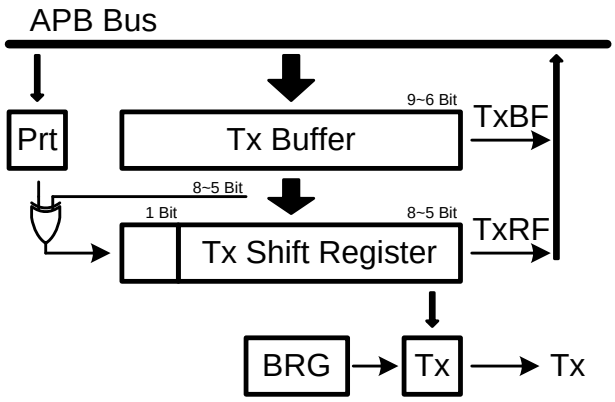
4.14. Timer B2 Network



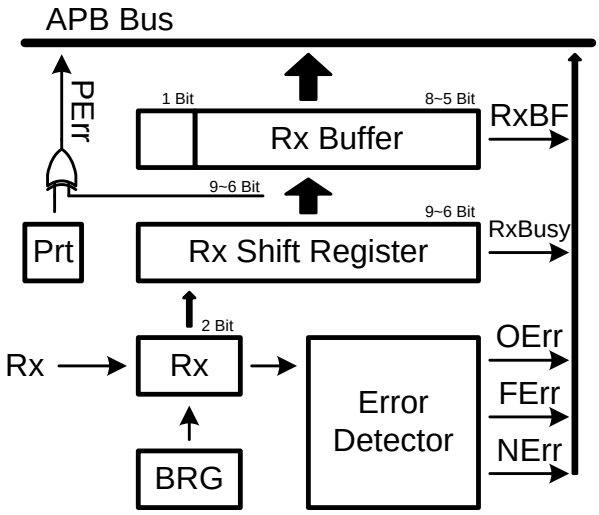
4.15. 32-bit SPI Diagram



4.16. UART Block Diagram

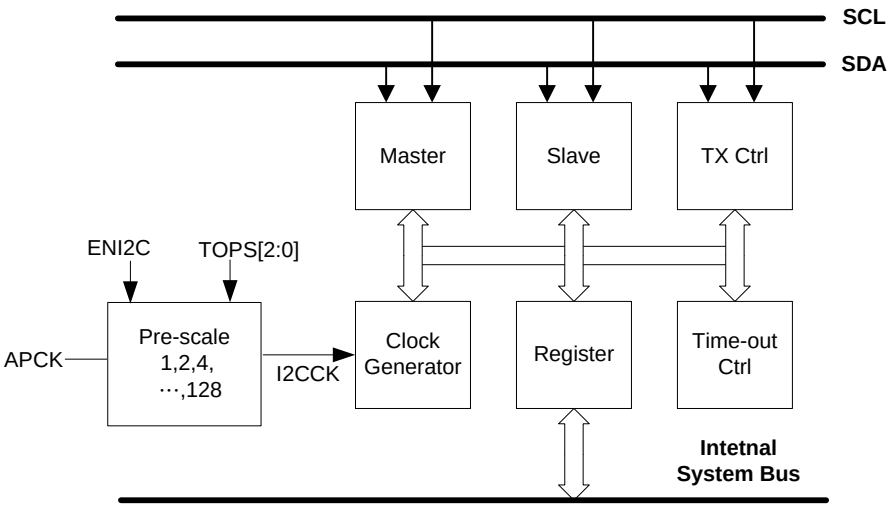


UART Transmit Block Diagram

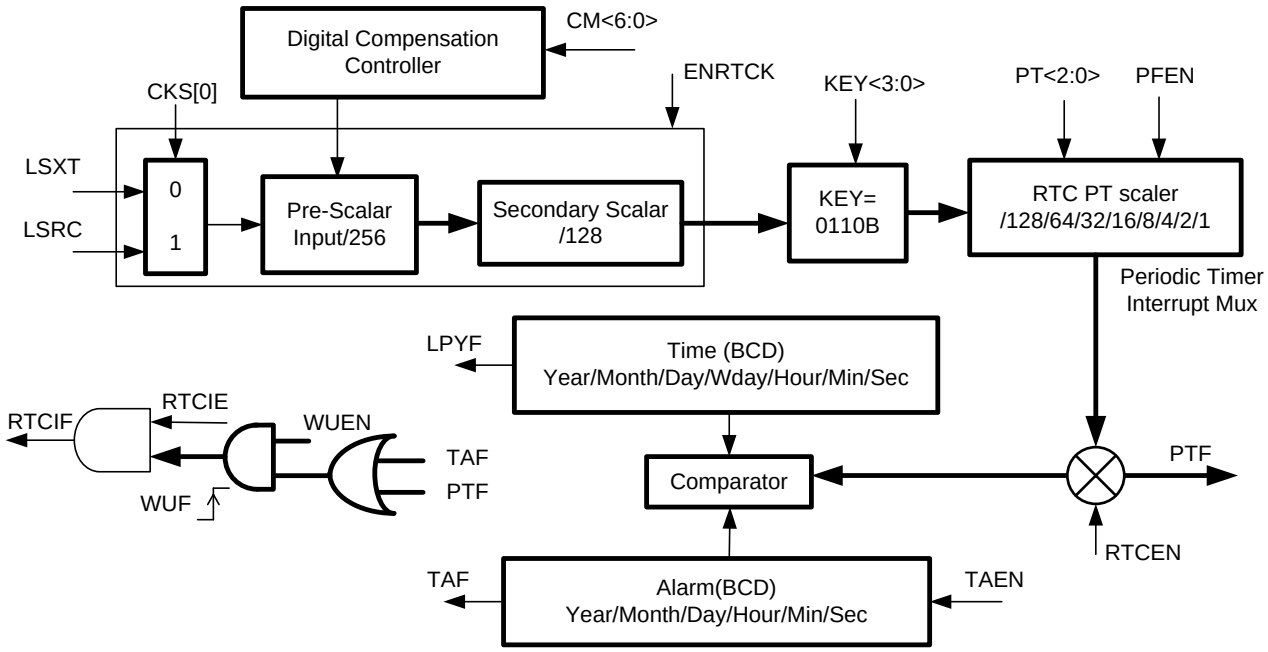


UART Receive Block Diagram

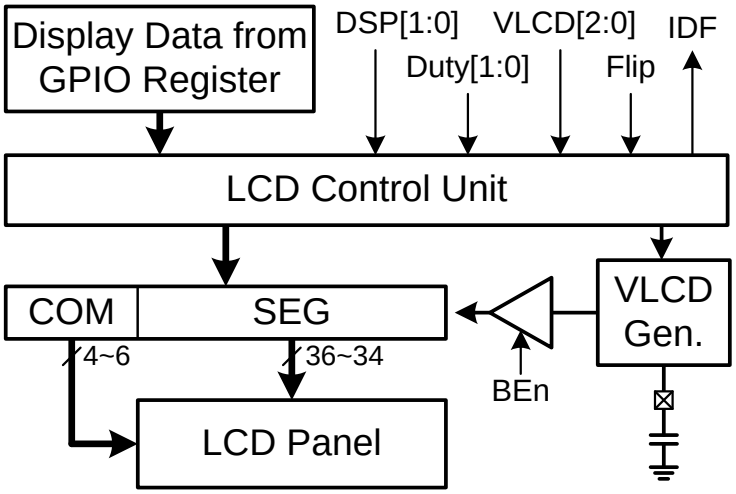
4.17. I2C Block Diagram



4.18. Hardware RTC Block Diagram



4.19. LCD Function Configuration



5. Electrical Characteristics

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at VDD3V to VSS . . . . . −0.2 V to 4.0 V
Voltage applied to any pin . . . . . −0.2 V to VDD3V + 0.3 V
Diode current at any device terminal . . . . . ±2mA
Storage temperature, Tstg: (UN programmed device) . . . . . −55℃ to 150℃
(Programmed device) . . . . . −40℃ to 85℃
Soldering Temperature (10 Sec) . . . . . +260°C
Maximum output current sink by any PORT1 to PORT10 I/O PIN 10mA

5.1. Recommended Operating Conditions

VDD3V=2.2V to 3.6V.TA=-40℃~85℃,Unless Otherwise Noted

Parameter	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	VDD3V	Digital Application	2.2	3.0	3.6	V
Supply Current	I_Sleep	Sleep Mode		2.5		uA
	I_Idle01	LSRC=34KHz+IDLE Mode		5.0		uA
	I_Idle02	HSRC=2MHz+IDLE Mode		50		uA
	I_Wait	LSRC=34KHz+Wait Mode		130		uA
	Free Run_01MHz	HSRC=2MHz@CPU_CK:2MHz/2		0.6		mA
	Free Run_02MHz	HSRC=2MHz@CPU_CK:2MHz		1.0		mA
	Free Run_04MHz	HSRC=4MHz@CPU_CK:4MHz		1.8		mA
	Free Run_10MHz	HSRC=10MHz@CPU_CK:10MHz		3.0		mA
	Free Run_16MHz	HSRC=16MHz@CPU_CK:16MHz		4.0		mA
Power Up Delay	$t_{PU,DLY}$	Wake Up From Sleep		64		ms

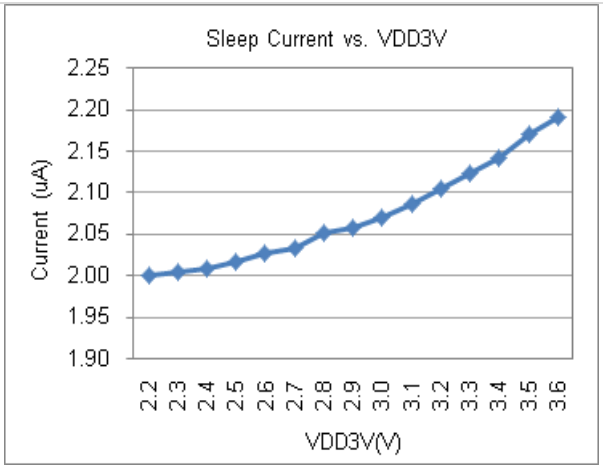


Figure5.1-1 Sleep Current vs. VDD3V

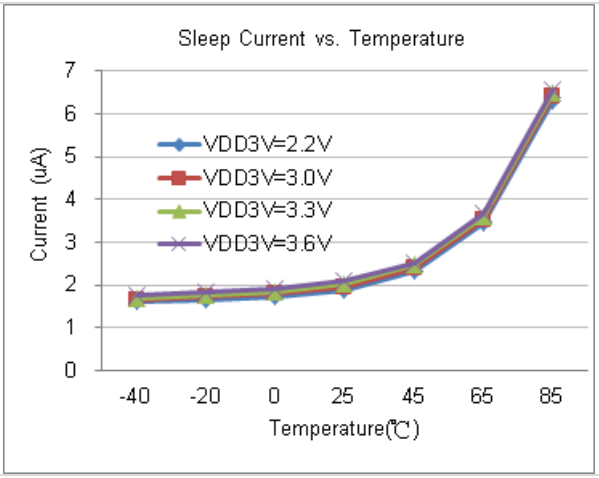


Figure5.1-2 Sleep Current vs. Temperature

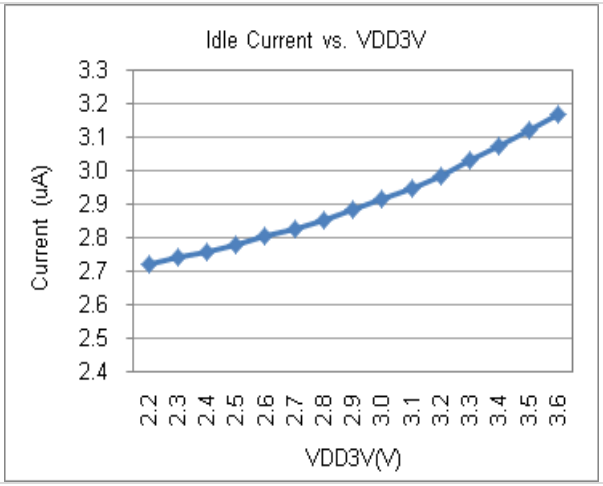


Figure5.1-3 Idle Current vs. VDD3V

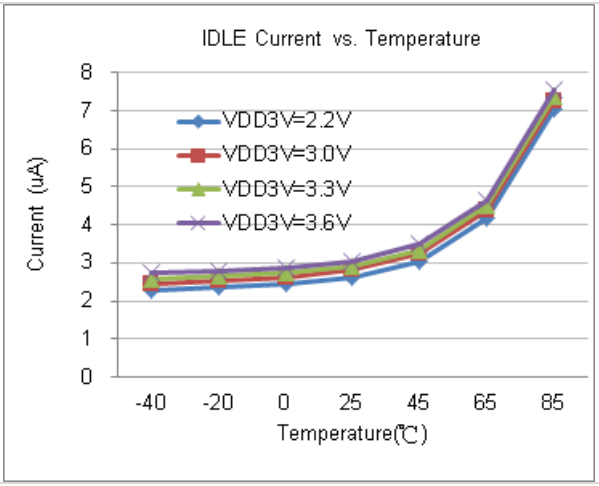


Figure5.1-4 Idle Current vs. Temperature

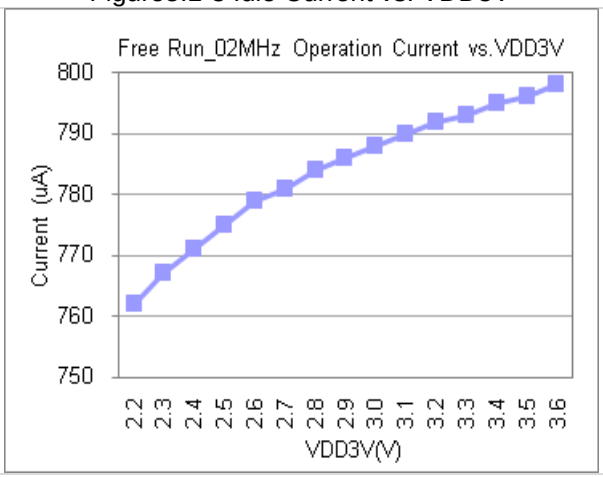


Figure5.1-5 Free Run_02MHz Operation Current vs. VDD3V

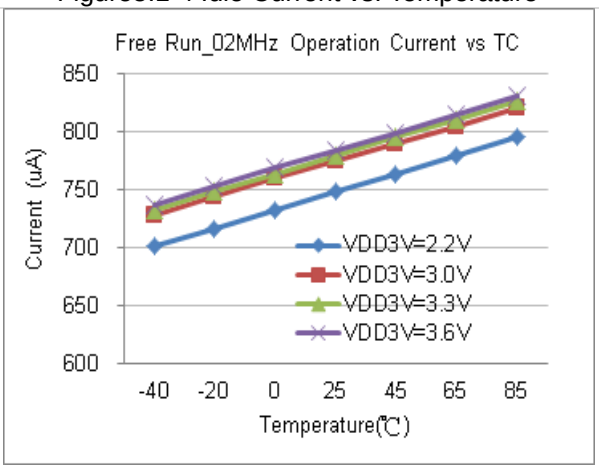


Figure5.1-6 Free Run_02MHz Current vs. Temperature

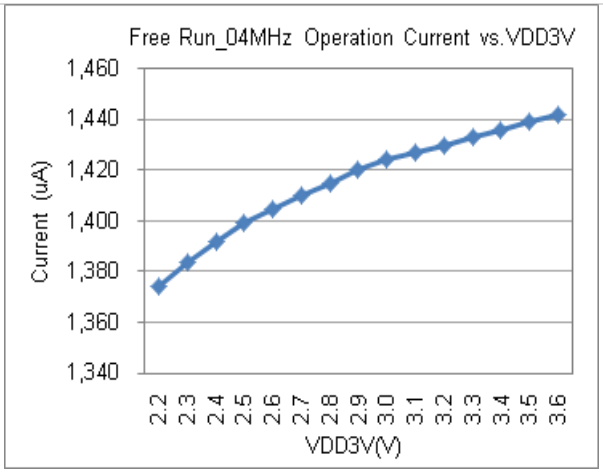


Figure5.1-7 Free Run_04MHz Operation Current vs. VDD3V

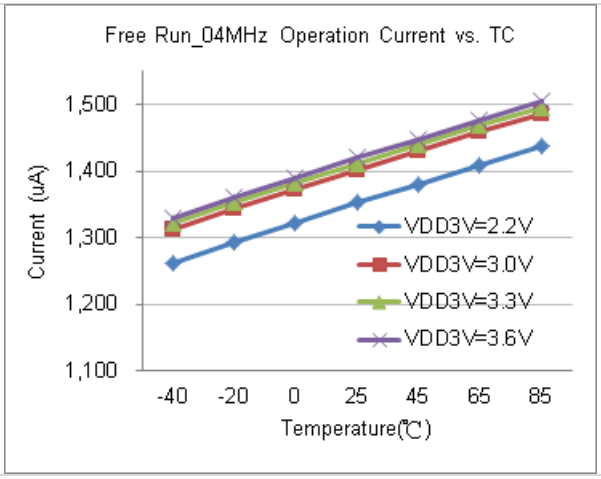


Figure5.1-8 Free Run_04MHz Current vs. Temperature

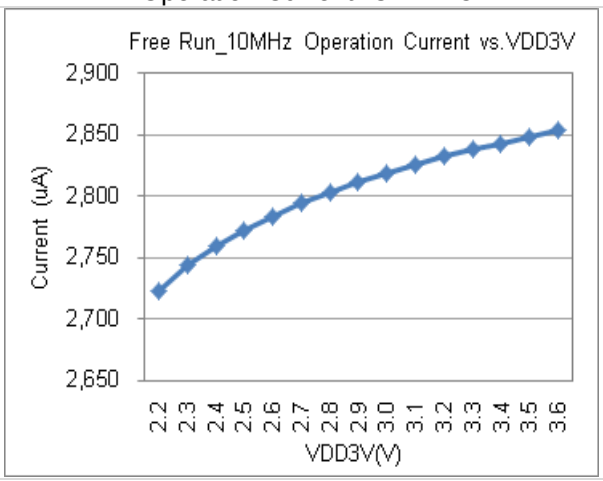


Figure5.1-9 Free Run_10MHz Operation Current vs. VDD3V

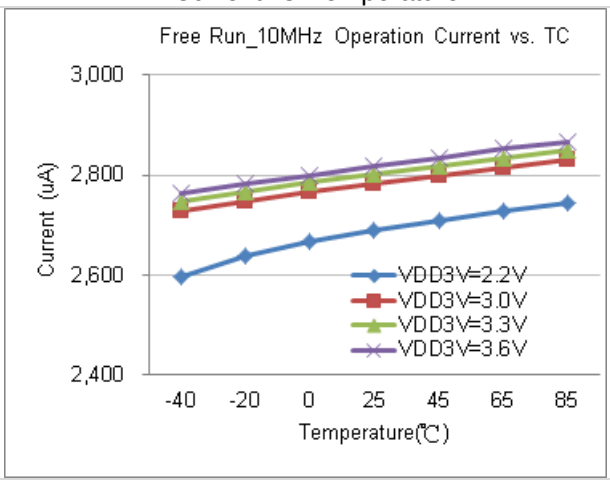


Figure5.1-10 Free Run_10MHz Current vs. Temperature

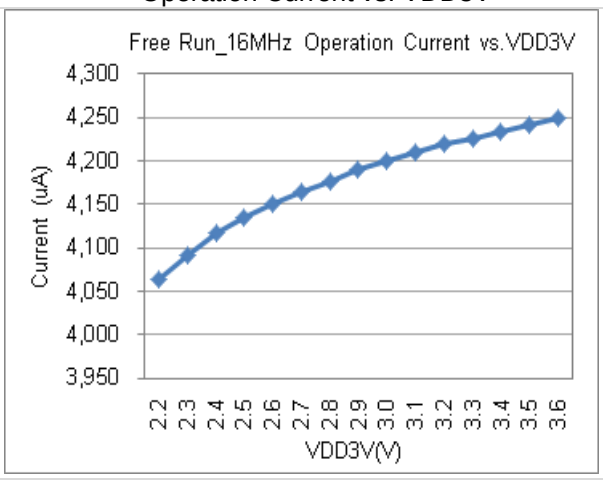


Figure5.1-11 Free Run_16MHz Operation Current vs. VDD3V

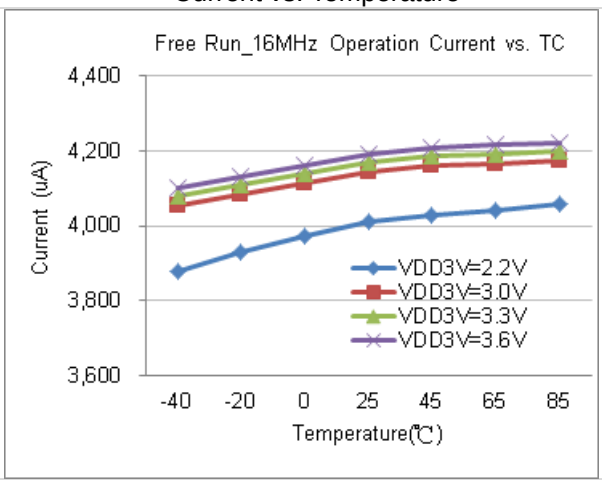


Figure5.1-12 Free Run_16MHz Current vs. Temperature

5.2. Clock System

Typical values are at T_A=25℃ and VDD3V = 3.0V.Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
External High Speed Oscillator						
VDD3V	Operation voltage		2.2		3.6	V
F_{XHS}	High speed oscillator frequency	VDD3V = 2.2V ~ 3.6V OHS_HS = 1b	4		16	MHz
		VDD3V = 2.2V ~ 3.6V OHS_HS = 0b	2		4	MHz
I_{XHS}	High speed oscillator current	F_{XHS} = 16MHz		100		uA
D_{XHS}	Duty of high oscillator		40		60	%
External Low Speed Oscillator						
F_{XLS}	Low speed oscillator frequency	VDD3V = 2.2V ~ 3.6V		32.768		KHz
I_{XLS}	Low speed oscillator current			2		uA
D_{XLS}	Duty of low speed oscillator		40		60	%
Internal High Speed Oscillator						
F_{HAO}	Internal high speed oscillator frequency	F_{HAO} = 2MHz, after trim	-2%	2	+2%	MHz
		F_{HAO} = 4MHz, after trim	-2%	4	+2%	MHz
		F_{HAO} = 10MHz, after trim	-2%	10	+2%	MHz
		F_{HAO} = 16MHz, after trim	-2%	16	+2%	MHz
	Voltage coefficient	VDD3V = 2.2V ~ 3.6V	-0.2		+0.2	%
T_{HAO}	Temperature coefficient	-40~85℃	-1.5		+1.5	%
I_{HAO}	Internal high speed oscillator current	F_{HAO} = 2MHz		20		uA
		F_{HAO} = 16MHz		75		uA
D_{HAO}	Duty of oscillator		40		60	%
WT_{HAO}	Wake up time	F_{HAO} = 2MHz		30		us
Internal Low Speed Oscillator						
F_{LPO}	Internal low speed oscillator frequency	VDD3V = 3.3V	-10%	35	+10%	KHz
	Voltage coefficient	VDD3V = 2.2V ~ 3.6V	-2.5		+2.5	%
T_{LPO}	Temperature coefficient	-40~85℃	-2.5		+2.5	%
I_{LPO}	Internal low speed oscillator current			0.35	0.7	uA
D_{LPO}	Duty of low speed oscillator		40		60	%

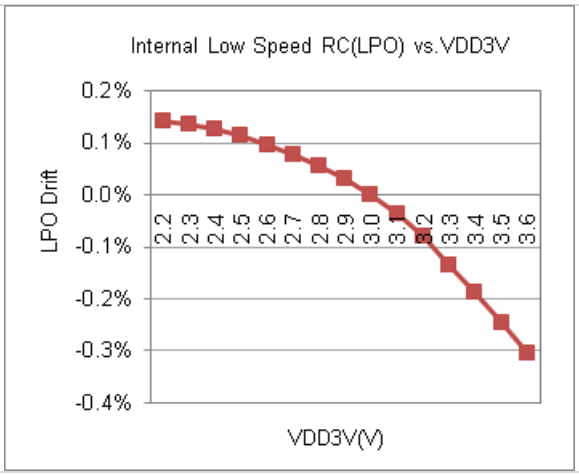


Figure5.2-1 LPO vs. VDD3V

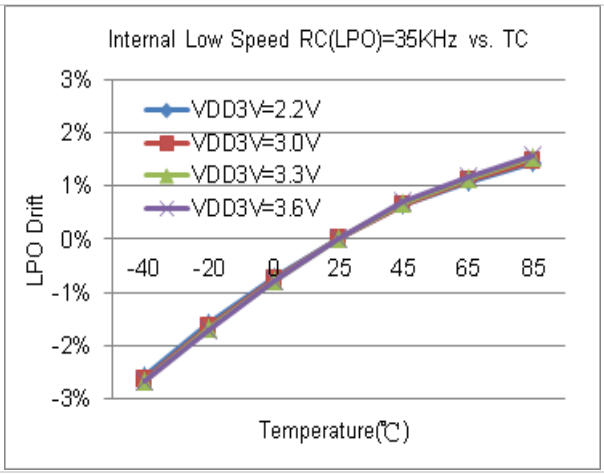


Figure5.2-2 LPO vs. Temperature

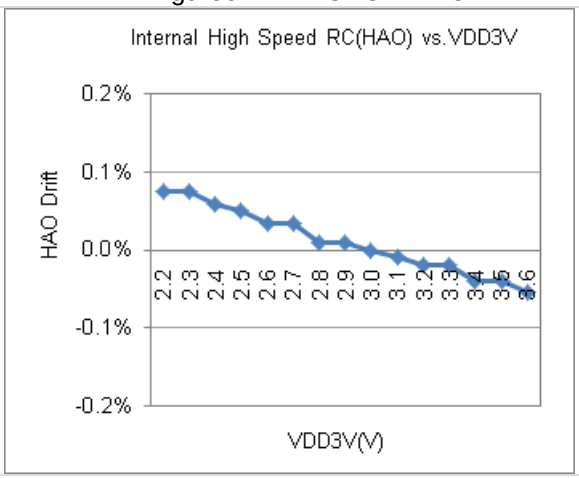


Figure5.2-3 HAO vs. VDD3V

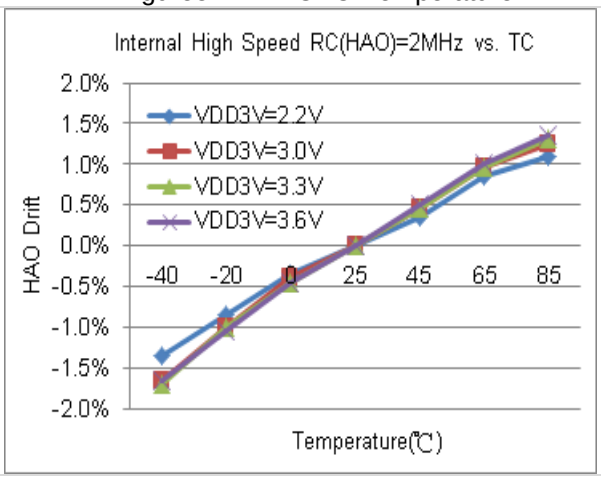


Figure5.2-4 HAO vs. VDD3V

5.3. Power Management System

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA LDO						
	Output voltage error		-5		5	%
	Capacitor loading		0.1	1	10	uF
	Settling time	Capacitor loading = 0.1uF, 99% of VDDA		50		us
	Operation current	Bias + Band gap + VDDA LDO		35	50	uA
	Dropout voltage	I_L=10mA		0.2		V
	Voltage coefficient	VDD3V = 2.5 ~ 3.6V		0.1		%/V
	VDDA voltage 1	I_L = 0.1mA		2.4		V
	VDDA voltage 2	I_L = 0.1mA		2.7		V
	VDDA voltage 3	I_L = 0.1mA		3.0		V
	VDDA voltage 4	I_L = 0.1mA		3.3		V
	Temperature coefficient	By using BRG VDDA=3.0V		100		ppm/°C
VDD18 LDO						
	Output voltage		1.7	1.8	1.9	V
	Capacitor loading		100	1000	10,000	nF
	Voltage coefficient	VDD3V= 2.2 ~ 3.6V		1		%/V
	Temperature coefficient			100		ppm/°C
	Load regulation	Load = 0.1~10mA		0.1		V/A
	Dropout voltage	Load = 10mA		0.2		V
REFO Buffer						
	Capacitor loading		22	100	1000	nF
	Operation current			15		uA
	Output current	1% change voltage	-1		1	mA
	Temperature coefficient	VDDA=3.0V		80		ppm/°C
	Offset voltage	REFO = 1.2V		±3	±12	mV
	Voltage coefficient	VDDA= 2.4V ~ 3.6V		0.1		%/V

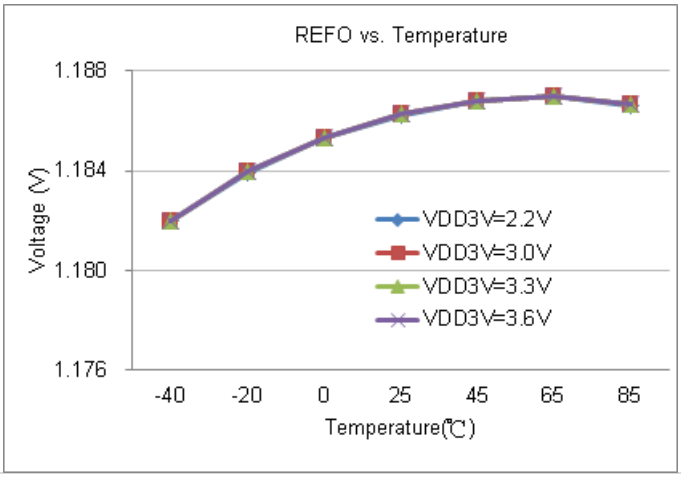


Figure5.3-1 REFO vs. Temperature

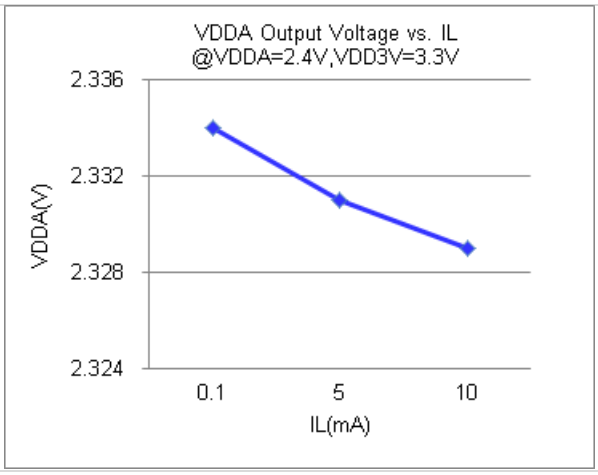


Figure5.3-2 VDDA vs. IL

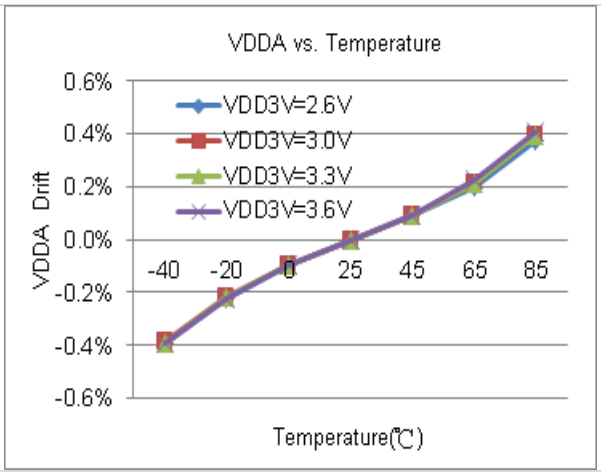


Figure5.3-3 VDDA vs. Temperature

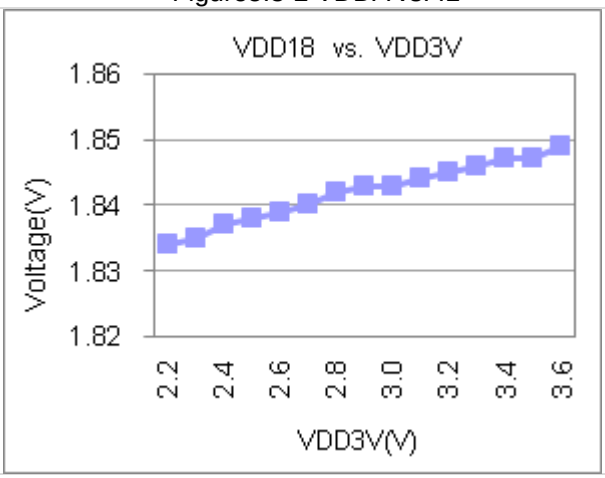


Figure5.3-4 VDD18 vs. VDD3V

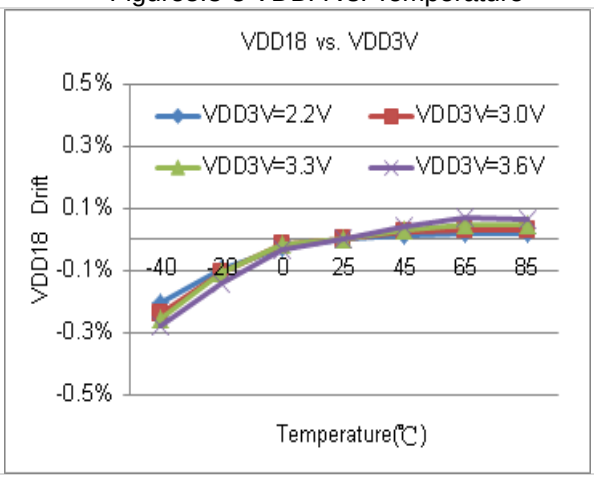


Figure5.3-5 VDD18 vs. Temperature

5.4. Charge Pump System

Typical values are at T_A=25℃, VDD3V = 3.0V, and C_{CP_O}:10uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CP_I	VDD supply voltage		2.4		3.6	V
CP_O	Backlight voltage	C_{CPO}:10uF, C_{HL}:1uF, VDD3V=3V, Loading≦15mA		3.3		V
I_{LED}	Driving current	VDD3V = 2.4V			15	mA

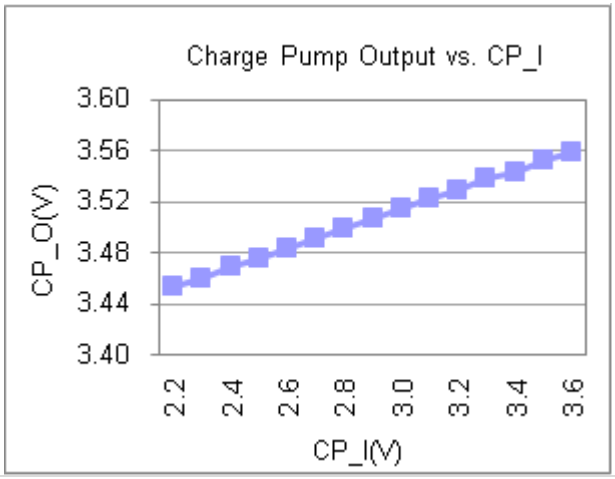


Figure5.4-1 CP_O vs. CP_I

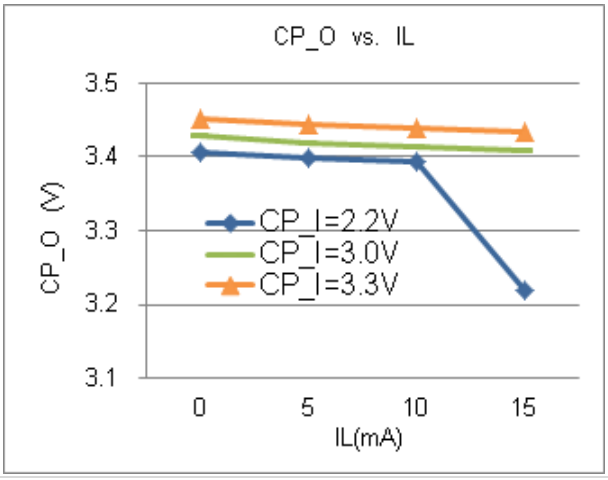


Figure5.4-2 CP_O vs. IL

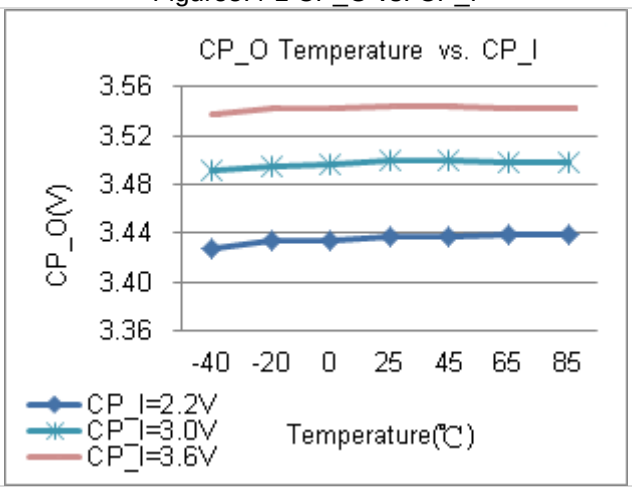


Figure5.4-3 CP_O vs. Temperature

5.5. Reset Management System

Typical values are at T_A=25℃ and VDD3V = 3.0V. unless otherwise noted.

Sym.	Parameter	Min.	Typ.	Max.	unit
BOR	Pulse length needed to accepted reset internally, t_{d-LVR}	2			us
	VDD Start Voltage to accepted reset internally (L→H),V_{LVR}	1.8	1.95	2.1	V
	Temperature drift, T_A=-40℃~85℃	-50		+50	mV
	Hysteresis, $V_{HYS-LVR}$		50		mV
POR	Operation Slew Rate			0.1	V/us
	Start Voltage to accepted reset	0.6			V

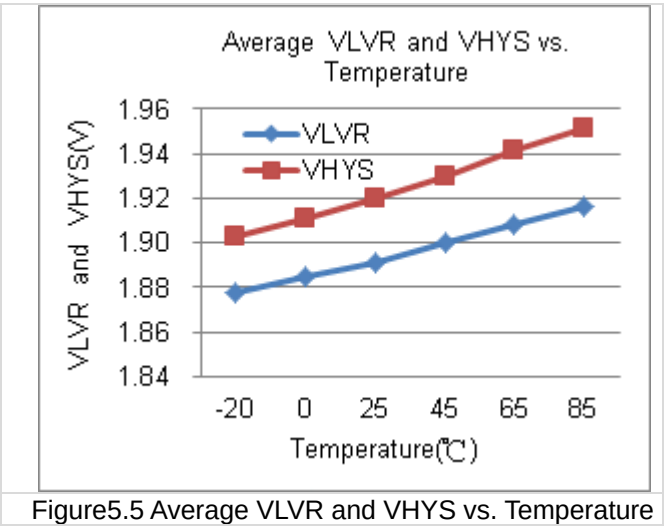


Figure5.5 Average VLVR and VHYS vs. Temperature

5.6. GPIO Port

Typical values are at T_A=25℃ and VDD3V = 3.3V. unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
PT 1.0 ~ 4.0 GPIO Port						
R_{PU}	Internal pull high resistor			75		kΩ
V_{IH}	Input high voltage		0.7*VDD3V			V
V_{IL}	Input low voltage				0.3*VDD3V	V
I_{OH}	Source current			10		mA
I_{OL}	Sink current			10		mA
PT 6.0 ~ 10.1 GPIO Port						
V_{IH}	Input high voltage		0.6*VDD3V			V
V_{IL}	Input low voltage				0.3*VDD3V	V
I_{OH}	Source current	VDD3V-0.3V		10		mA
I_{OL}	Sink current	VSS+0.3V		10		mA

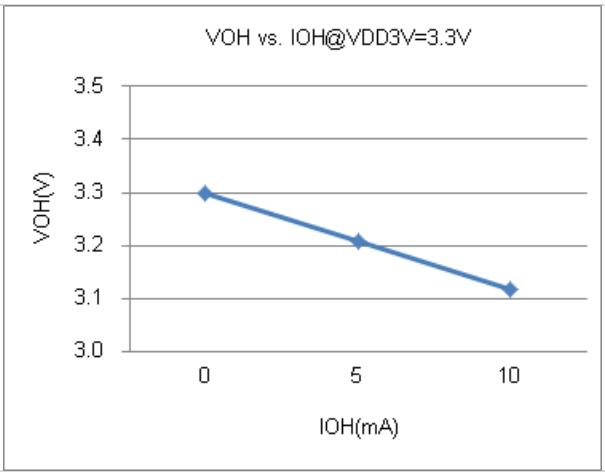


Figure5.6-1 VOH vs. IOH

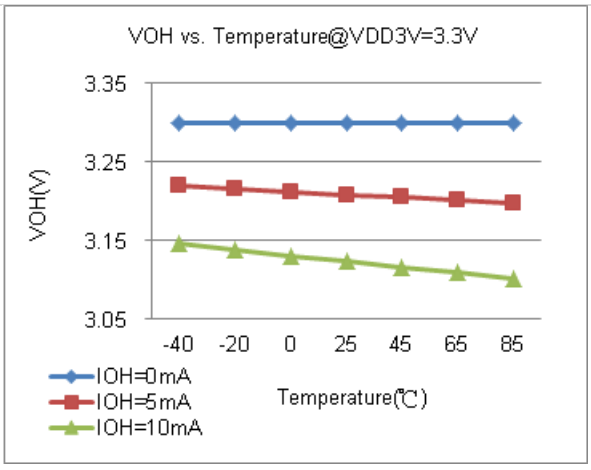


Figure5.6-2 VOH vs. Temperature

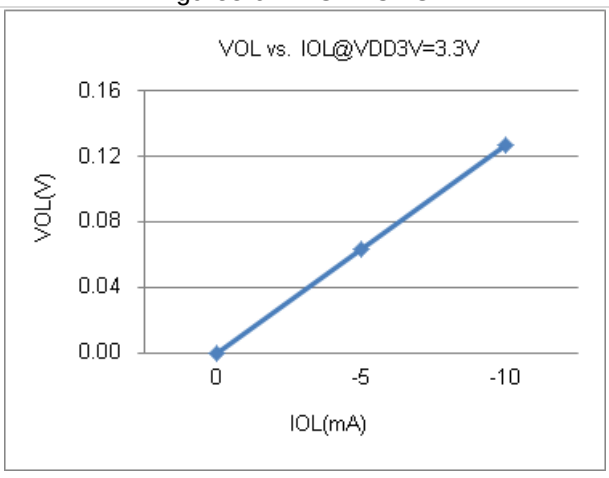


Figure5.6-3 VOL vs. IOL

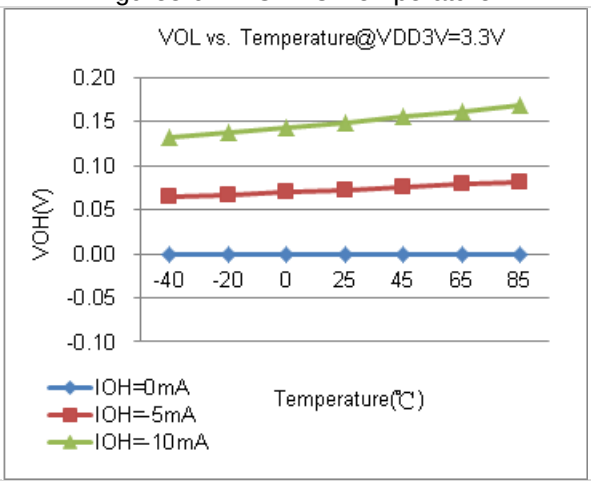


Figure5.6-4 VOL vs. Temperature

5.7. ΣΔADC ENOB and RMS Noise

Typical values are at TA=25℃ and VDD3V = 3.3V, VDDA=2.4V unless otherwise noted. HY16F198 provides important input noise specification that aims at ΣΔADC. Table 5.6-1 and Table 5.7-2 lists out the relations of typical noise specification, Gain, Output rate, and maximum input voltage of single end. Test condition configuration and external input signal short, voltage reference: 1.2V and 1024 records were sampled.

ENOB(RMS) with OSR/GAIN at A/D Clock=333Khz, VDDA=2.4V, VREF=1.2V															
Max. Vin(mV) =0.9*VREF (1)	OSR					32	64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					10417	5208	2604	1302	651	326	163	81	41	20	10
	Gain	=	PGA	×	ADGN											
±1080	1	=	1	×	1	12.3	14.2	16.3	16.8	17.4	17.9	18.3	18.8	19.4	19.9	20.3
±540	2	=	1	×	2	11.8	13.1	16.0	16.6	17.0	17.4	18.0	18.7	19.3	19.7	20.2
±135	4	=	1	×	4	11.1	14.6	16.0	16.5	16.9	17.3	17.9	18.6	19.1	19.5	20.1
±33.75	32	=	8	×	4	11.1	12.2	14.9	15.4	15.7	16.1	16.7	17.6	18.1	18.6	19.1
±16.875	64	=	16	×	4	11.1	12.7	14.6	15.1	15.4	15.9	16.4	17.1	17.6	18.1	18.6
±11.25	96	=	24	×	4	11.1	12.1	14.3	14.8	15.3	15.7	16.3	16.9	17.4	17.9	18.4
±8.435	128	=	32	×	4	11.1	13.4	14.1	14.6	15.1	15.5	16.1	16.7	17.1	17.6	18.2
(1) Max.Vin (mV) is the max. input voltage of single end to ground (VSS).																

Table 5.7-1 ΣΔADC ENOB Table

RMS Noise(uV) with OSR/GAIN at A/D Clock=333Khz, VDDA=2.4V, VREF=1.2V															
Max. Vin(mV) =0.9*VREF	OSR					32	64	128	256	512	1024	2048	4096	8192	16384	32768
	Output rate(HZ)					10417	5208	2604	1302	651	326	163	81	41	20	10
	Gain	=	PGA	×	ADGN											
±1080	1	=	1	×	1	459	124	28.7	19.97	13.95	9.93	7.17	5.03	3.49	2.49	1.812
±540	2	=	1	×	2	323	136	17.6	11.62	9.08	6.97	4.60	2.78	1.88	1.39	0.966
±135	4	=	1	×	4	260	23.9	8.7	6.51	4.71	3.72	2.47	1.47	1.05	0.78	0.541
±33.75	32	=	8	×	4	33.1	15.9	2.4	1.69	1.38	1.09	0.70	0.38	0.26	0.19	0.132
±16.875	64	=	16	×	4	16.2	5.4	1.5	1.06	0.83	0.61	0.42	0.26	0.18	0.13	0.092
±11.25	96	=	24	×	4	11.3	5.5	1.2	0.85	0.60	0.45	0.30	0.20	0.14	0.10	0.071
±8.435	128	=	32	×	4	8.4	1.8	1.0	0.75	0.53	0.39	0.27	0.17	0.13	0.09	0.063

Table 5.7 -2 ΣΔADC RMS Table

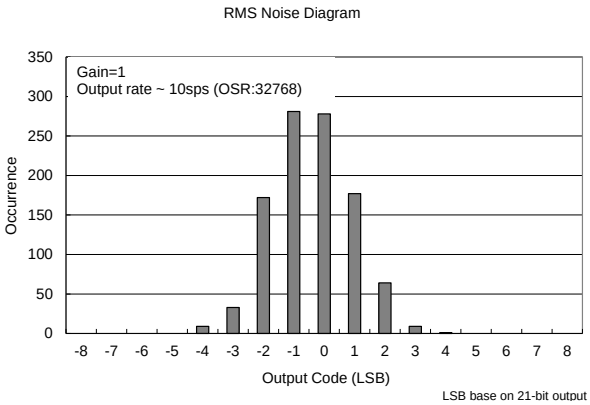


Figure5.7-1(a) RMS Noise Diagram

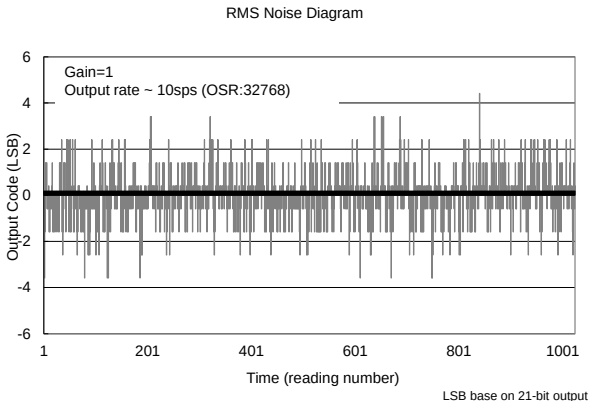


Figure5.7-1(b) Output Code Diagram

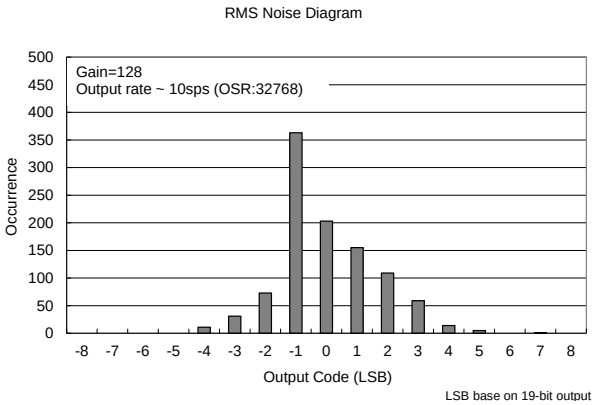


Figure5.7-2(a) RMS Noise Diagram

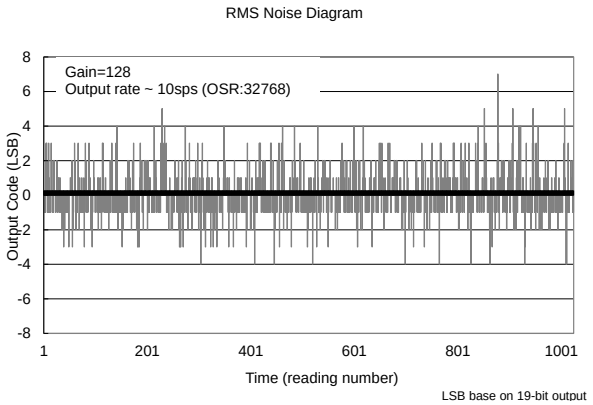


Figure5.7-2(b) Output Code Diagram

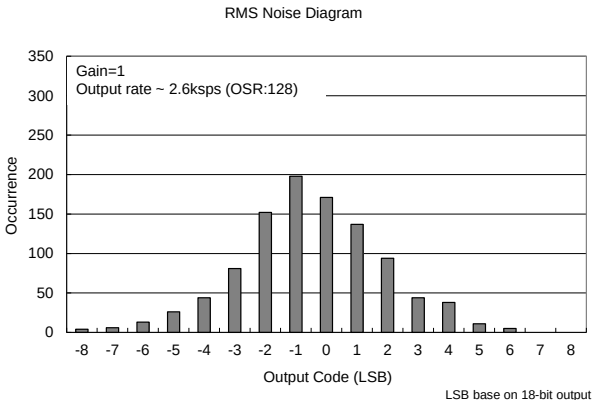


Figure5.7-3(a) RMS Noise Diagram

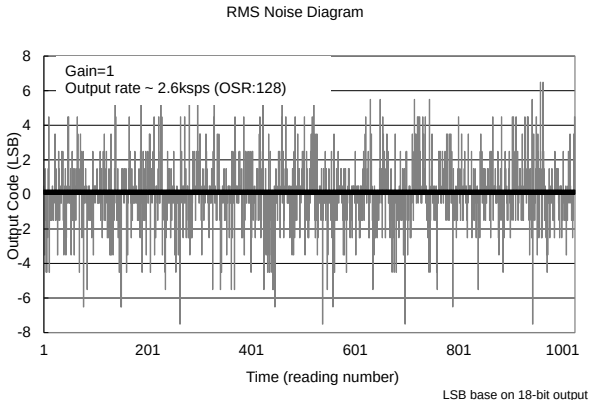


Figure5.7-3(b) Output Code Diagram

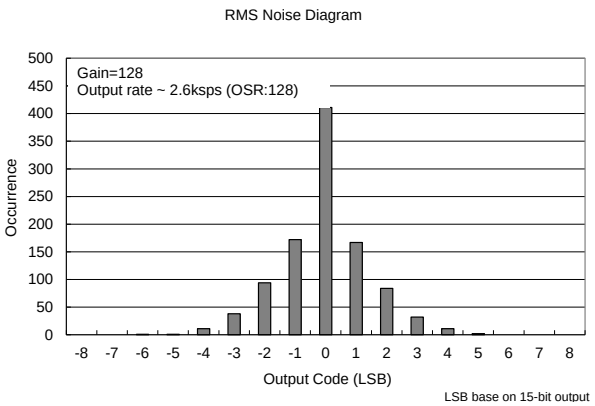


Figure5.7-4(a) RMS Noise Diagram

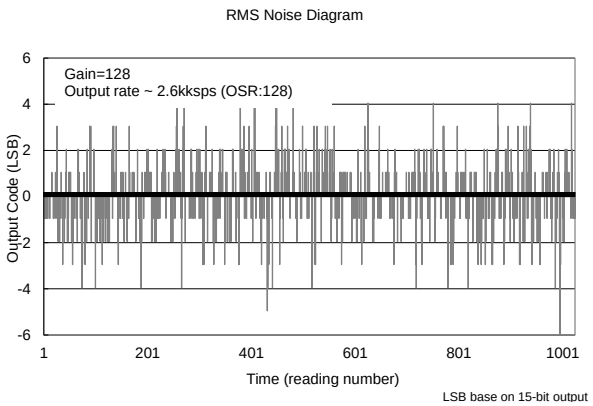


Figure5.7-4(b) Output Code Diagram

5.8. ADC Management System

All specifications at T_A=-40℃ to +85℃,
VDDA=REFP=3.0V, REFN=VSS, and Gain=128. Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
Analog Inputs							
	Full-scale input voltage (VINP - AINN)			±0.5*VREF/Gain			V
	Common-mode input range	Gain = 1		VSS-0.2V		VDDA	V
System Performance							
	Resolution	No missing codes			24		Bits
	Data rate				ADC Clock /OSR		SPS
	Digital filter settling time	Full setting			3		Data
	Integral nonlinearity (INL)	Differential input End-point fit,OSR=32768			15		PPM
	Gain drift				5		ppm/℃
	Normal-mode rejection	f_{IN}=60Hz ±1Hz, Output rate = 10 SPS	Internal OSC		70		dB
			External OSC		80		dB
	Common-mode rejection	ΔVDDA = 0.1V @ DC			80		dB
	Input-referred noise	Output rate= 10 SPS			65		nV, rms
	Power-supply rejection	ΔVDDA = 0.1V @ DC			80		dB
Voltage Reference Input							
	Voltage reference input	VREF = REFP - REFN				VDDA	V
	Positive Reference Input	REFP		VDDA/2		VDDA+0.1	V
	Negative Reference Input	REFN		VSS-0.1V		VDDA/2	V
ADC Modulator Current							
ADC	ADC Modulator	VDD3V=3.3V,VDDA=2.4V			150		uA
PGA	ADC PGA	VDD3V=3.3V,VDDA=2.4V			625		uA

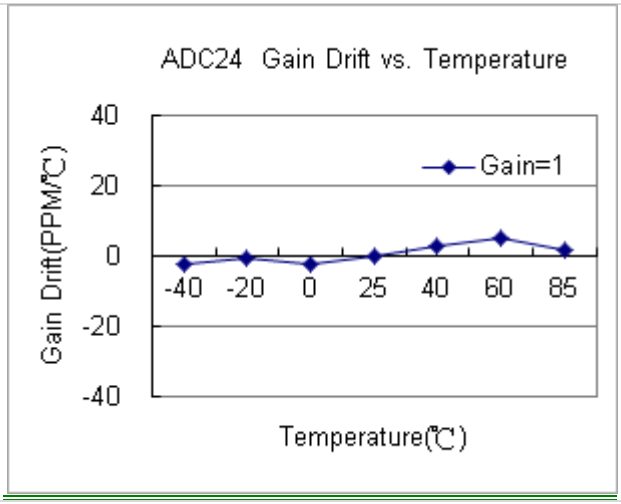


Figure5.8-1 ADC24 Gain Drift Gain=1
Vin=320mV SPS=10Hz
Delta VR=1V and VDDA=2.7V

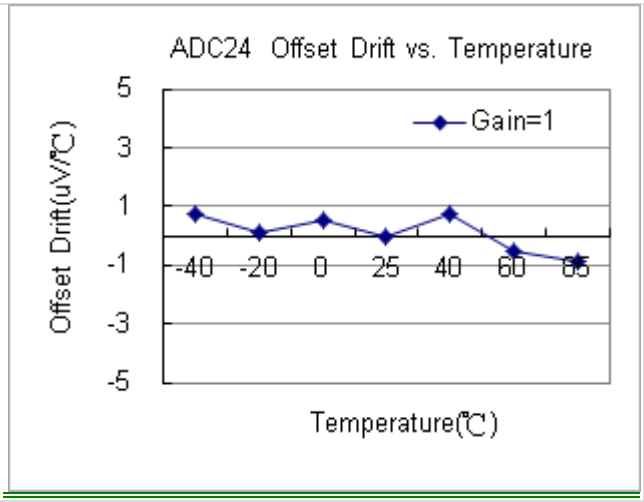


Figure5.8-5 ADC24 Offset Drift Gain=1
Vin=320mV SPS=10Hz
Delta VR=1V and VDDA=2.7V

5.9. Temperature Sensor

Typical values are at T_A=25℃, VDD3V = 3.0V, and VDDA=2.4V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
TC_S	Sensor temperature drift			173		uV/℃
KT	Absolute temperature scale 0°K			-288		℃
TC_{ERR}	One point calibrate error temperature	Calibration at 25℃ of -40℃~85℃		±2		℃

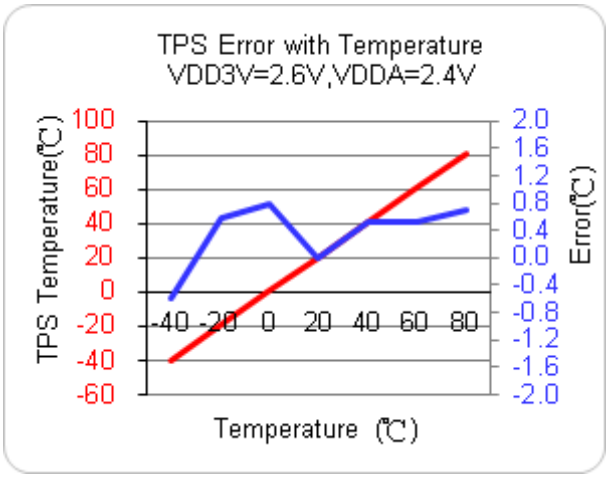


Figure5.9 TPS Performance

5.10. 8-Bit Resistance Ladders

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Resolution	Monotonic		8		Bit
	Power Supply		2.4		VDD3V	V
V_{OUT}	Output range	DA output is between VR- and VR+	0		VDD3V	V
V_{REFP}	Positive reference voltage range	$V_{REFP} > V_{REFN}$	0		VDD3V	V
V_{REFN}	Negative reference voltage range		0		VDD3V	V
R_{ON}	8-Bit Resistance ladders. output switch	VDDA=2.4V 0.5V < DA_OP < VDD3V-0.5V			200	Ω
		VDDA=2.4V 0.5V > DA_OP, DA_OP > VDD3V-0.5V		10		Ω
R_{RSW}	Reference voltage switch	V_{REFP} = 2.2V, V_{REFN} = 0V, VDDA = 2.4V		15	30	Ω
R_{LADDER}	One LSB resistance ladder			600		Ω
INL	Integral linearity error	VR+ = 2.4V, VR- = 0V		±0.5	±1	LSB
DNL	Differential linearity error	VR+ = 2.4V, VR- = 0V		±0.5	±1	LSB
E_{OS}	Offset error	VR+ = 2.4V, VR- = 0V			1	LSB
8-Bit Resistance Ladders	(Vin Floating)	VDD3V=3.3V,VDDA=2.4V		0.1		uA

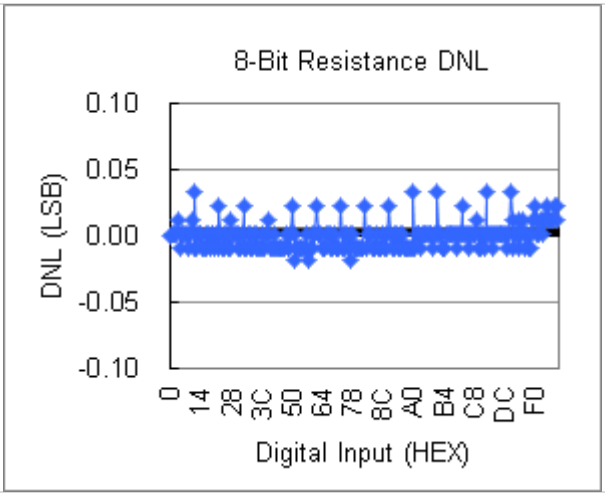


Figure5.10-1 8-Bit Resistance vs. DNL

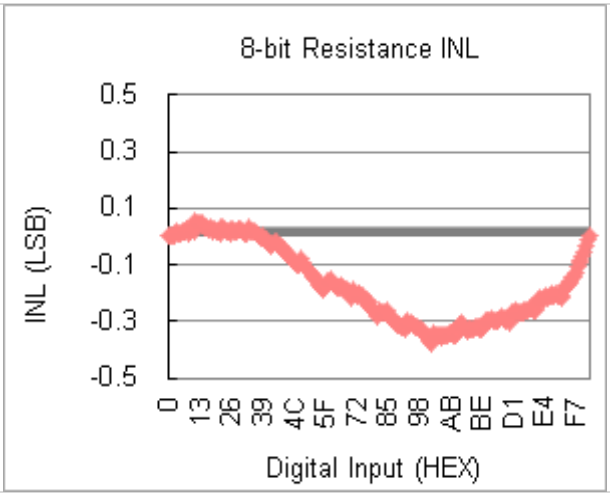


Figure5.10-2 8-Bit Resistance vs. INL

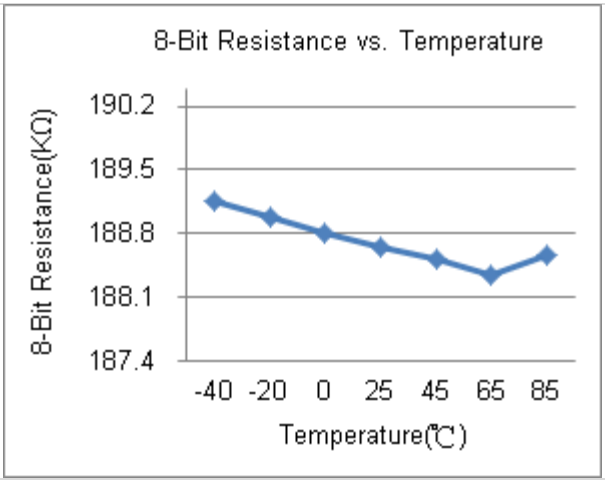


Figure5.10-3 8-bit Resistance vs. Temperature

5.11. OPA Management System

Typical values are at T_A=25℃, VDD3V = 3.0V, and C_{VLCD}=10uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VDDA	Power supply		2.4		3.6	V
V_{OUT}	Output range		0		VDDA	V
V_{IN}	Input common range		0		VDDA	V
I_{OPA}	OPAMP current			120		uA
I_{OPA_LOAD}	Output current loading (push or pull)	VDDA = 3.0V, 0.3V< Output voltage <VDDA-0.3V			1	mA
		VDDA = 2.4V, 0.3V< Output voltage <VDDA-0.3V			0.5	mA
C_{LOAD}	Max output capacitor load				1	nF
SR	Slew rate	Loading R=10K, C=100pF, 0.3V → VDDA-0.3V		0.6		V/us
UGB	Unit gain bandwidth	Loading C=100pF		1000		KHz
V_{OS}	Offset error	Vin = 1.2V	-5		+5	mV
DFD	Digital filter delay	VDDA = 3.0V		2		us
C_{SA}	Sample capacitor			10		pF

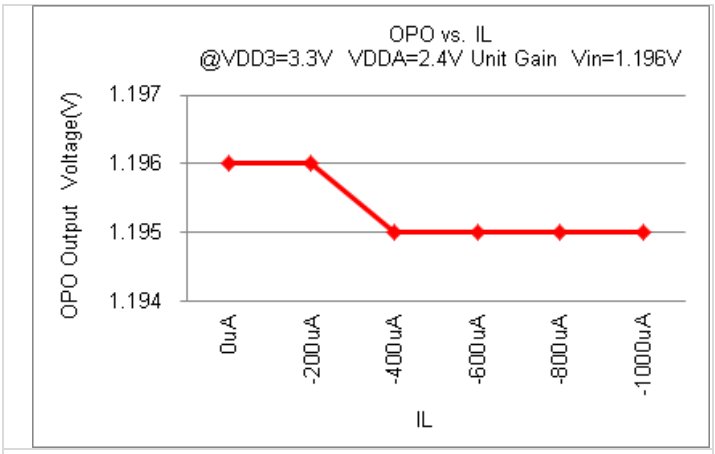


Figure5.11 OPO vs. IL

5.12. CMP Management System

Typical values are at T_A=25℃ and VDD3V = 3.0V. Unless otherwise noted.

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{MC}	Operation supply current	ENCMP[0]=1, CMPHS[0]=1b		10		uA
	Low Power Mode	ENCMP[0]=1, CMPHS[0]=0b		1		
V_{IC}	Common-mode input voltage		0		VDD3V-1	V
V_{OS}	Offset voltage		-5		5	mV
V_{hys}	Input hysteresis		0	0.7	1.5	mV
V_{REF}	Reference voltage	CPPS[1:0]=11b		1.2		V
	Temperature drift	CPPS[1:0]=11b		80		ppm/℃
I_R	Multi-node resistor current	CPRL[0]=0b		10		uA
		CPRL[0]=1b		30		

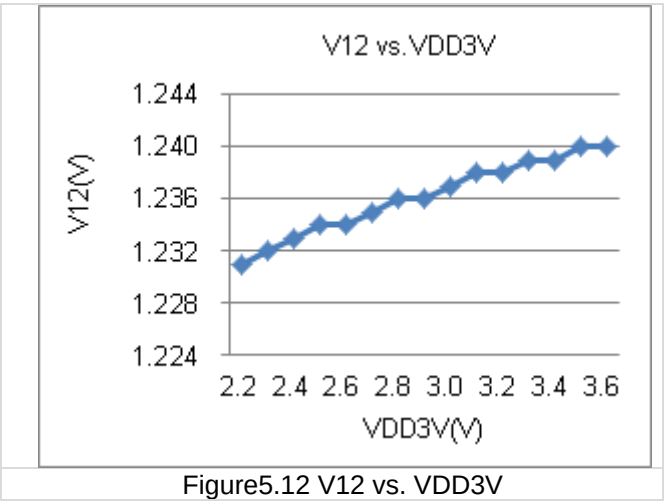


Figure5.12 V12 vs. VDD3V

5.13. LCD System

Typical values are at TA=25℃, VDD3V = 3.3V, and CVLCD=10uF. Unless otherwise noted.

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{LCD}	Operation Current Charge Pump Mode	VDD3V=3.3V VLCD=3.0V	W/O Panel		10		uA
VLCD	Supply Voltage Range	VLCD	With Buffer	2.50		3.80	V
VLCD	Embedded Charge Pump Output Voltage @ VLCD Pin	VDD3V = 2.4V CVLCD = 10uF	Mode1: Data[1]=00_011B	3.26	3.43	3.60	V
			Mode2: Data[1]=00_100B	3.00	3.16	3.32	
			Mode3: Data[1]=00_101B	2.78	2.93	3.08	
			Mode4: Data[1]=11_101B	2.59	2.73	2.87	
			Mode5: Data[1]=01_101B	2.42	2.55	2.68	
Z_{LCD}	Output Impedance With LCD Buffer	FLCD = 128Hz, VLCD = 3.0V			10		KΩ

Data1 Bit: 0X41F24 [EN_Rshift1, EN_Rshift0], 0X41B00 [VLCD2, VLCD1, VLCD0]

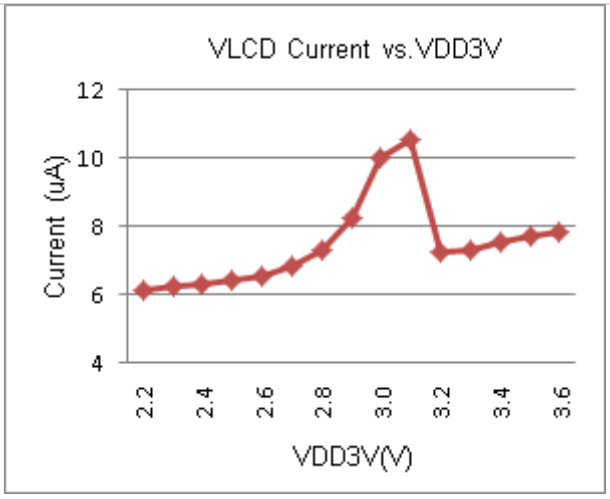


Figure5.13-1 VLCD Current vs. VDD3V @VLCD=3.16V

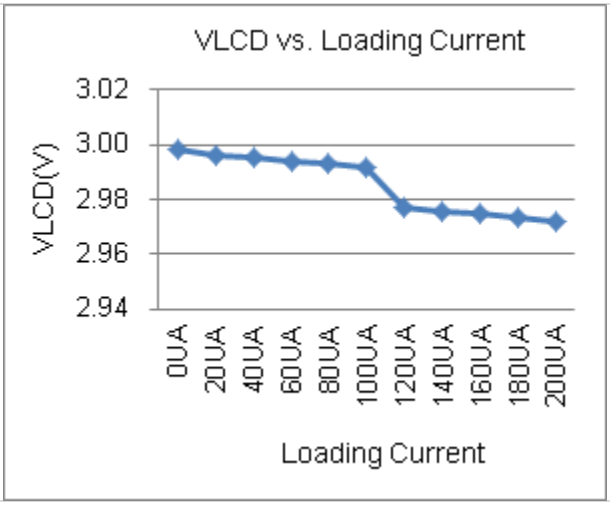


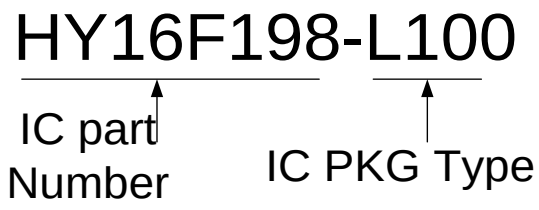
Figure5.13-2 VLCD With Load @VLCD=3.0V

6. Ordering Information

6.1. HY16F19X Series Device No. Selection

Device No.[1]	Package Type	Pins	Package Drawing		Code[2]	Shipment Packing Type	Unit Q'ty	Material Composition	MSL[3]
HY16F198-D000	Die	-	D	000	-	-	100	Green[4]	-
HY16F198-N088	QFN	88	N	088	-	Tray	168	Green[4]	MSL-3
HY16F198-L100	LQFP	100	L	100	-	Tray	90	Green[4]	MSL-3
HY16F198-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F197-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F197-N068	QFN	68	N	068	-	Tray	348	Green[4]	MSL-3
HY16F196-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F196-N068	QFN	68	N	068	-	Tray	348	Green[4]	MSL-3

[1] Device No.: Model No. – Package Type Description



EX：You request in LQFP 100 package.
The device No. will be HY16F198-L100.
And please clearly indicate the shipment packing type when placing orders.

[3] MSL:
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization.
The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[4] Green (RoHS & no Cl/Br):
HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%).

6.2. HY16F19xB Series Device No. Selection

Order Name	Package Type	Pin	PKG Type Description		Code No.[2]	Shipment Type	Quantity Per Packge	Material	MSL[3]
HY16F198B-D000	Die	-	D	000	-	-	100	Green[4]	-
HY16F198B-N088	QFN	88	N	088	-	Tray	168	Green[4]	MSL-3
HY16F198B-L100	LQFP	100	L	100	-	Tray	90	Green[4]	MSL-3
HY16F198B-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F197B-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3
HY16F197B-N068	QFN	68	N	068	-	Tray	348	Green[4]	MSL-3
HY16F196B-L064	LQFP	64	L	064	-	Tray	250	Green[4]	MSL-3

[1] Device No.: Model No. – Package Type Description

EX：You request in LQFP 100 package.
The device No. will be HY16F198B-L100.
And please clearly indicate the shipment packing type when placing orders.

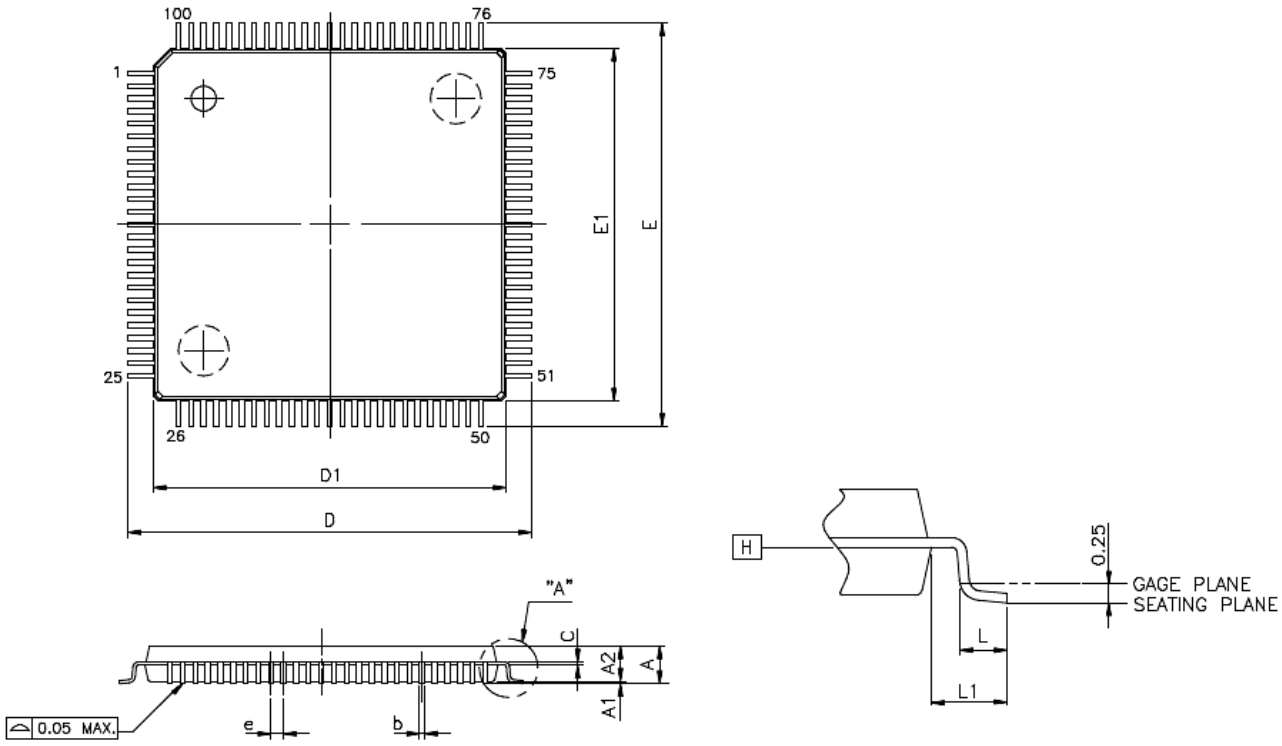
[3] MSL:
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization.
The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[4] Green (RoHS & no Cl/Br):
HYCON products are Green products that compliant with RoHS directive and are
Halogen free (Br/Cl<0.1%).

7. Package Information

7.1. LQFP100 PKG Diagram

Unit: mm



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		

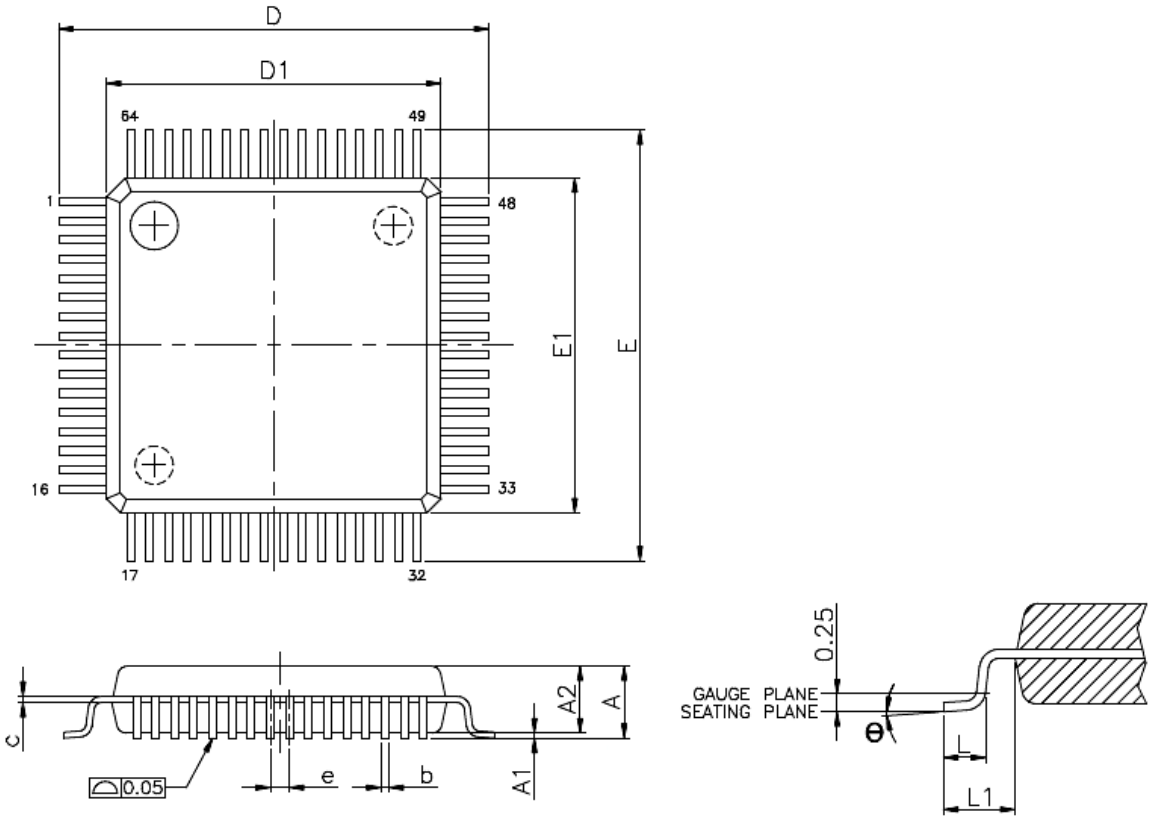
Note:

(1) All dimensions refer to JEDEC OUTLINE MS-026.

(2) Do not include Mold Flash or Protrusions.

7.2. LQFP64 PKG Diagram

Unit: mm



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

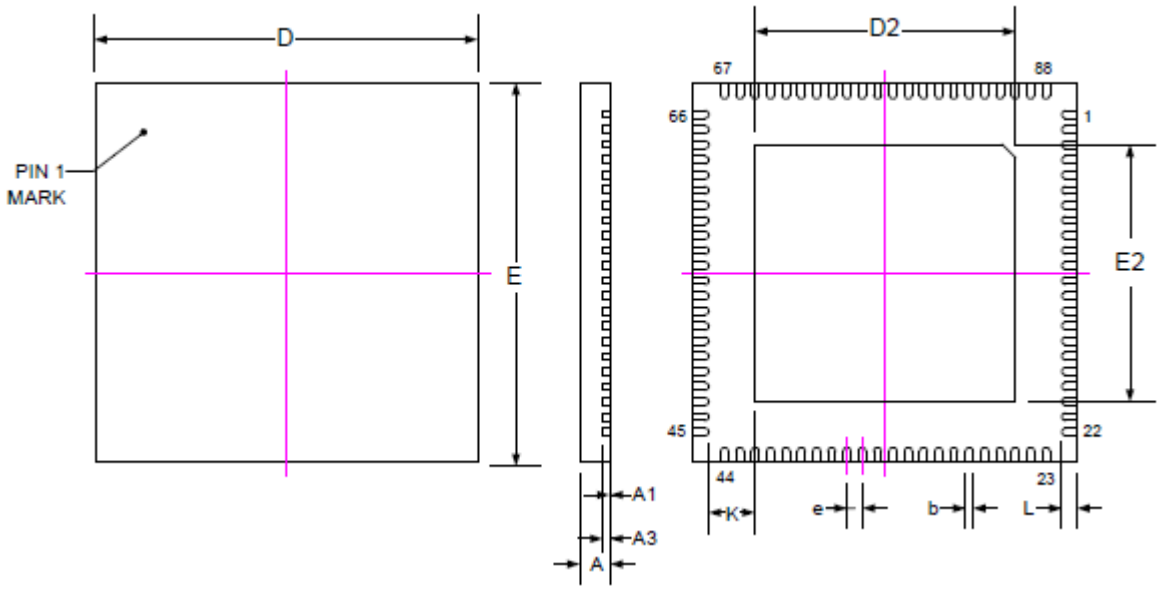
Note:

(1) All dimensions refer to JEDEC OUTLINE MS-026.

(2) Do not include Mold Flash or Protrusions.

7.3. QFN88 PKG Diagram

Unit:mm



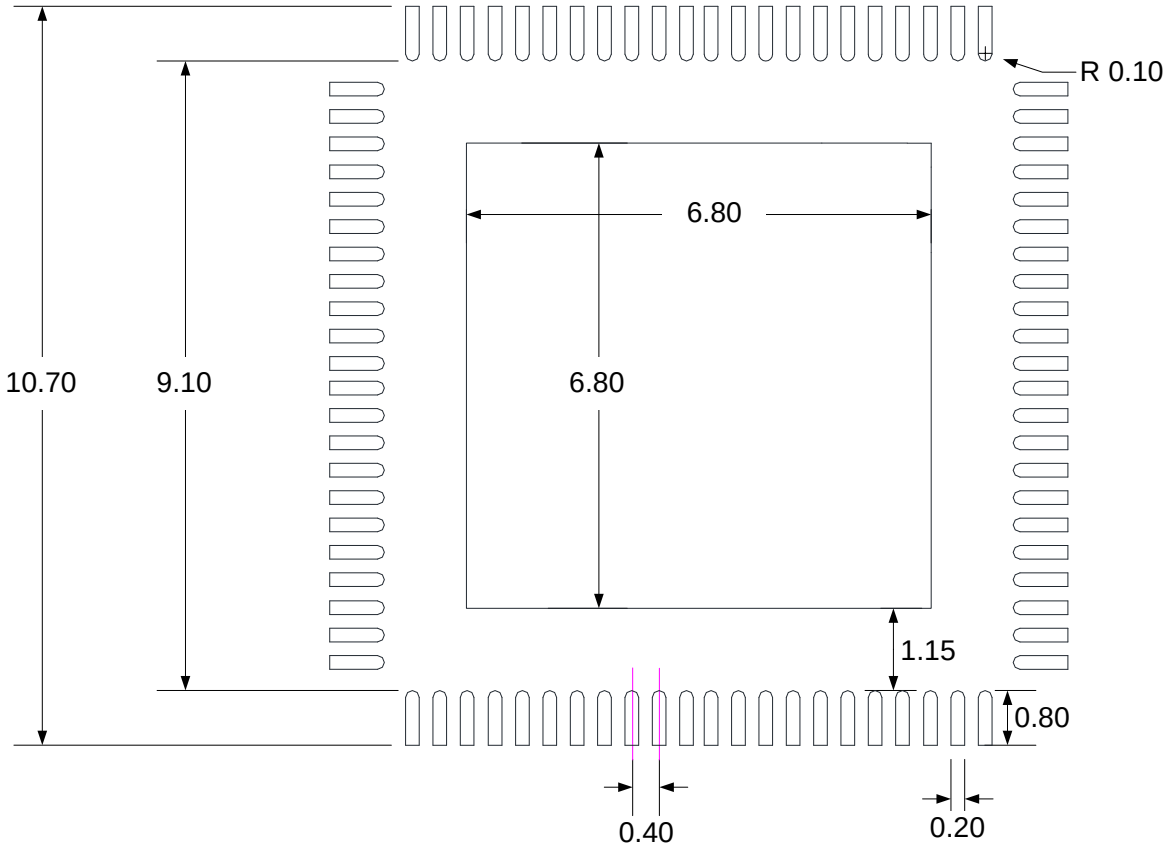
SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		10.00 BSC	
E		10.00 BSC	
e		0.40 BSC	
D2	6.75	6.80	6.85
E2	6.75	6.80	6.85
L	0.30	0.40	0.50
K	1.08	1.20	1.33

Note: All dimensions refer to JEDEC OUTLINE MO-220.

Package Outline Drawing--- QFN 10x10 88

Land Pattern Design Recommendations

Unit : mm

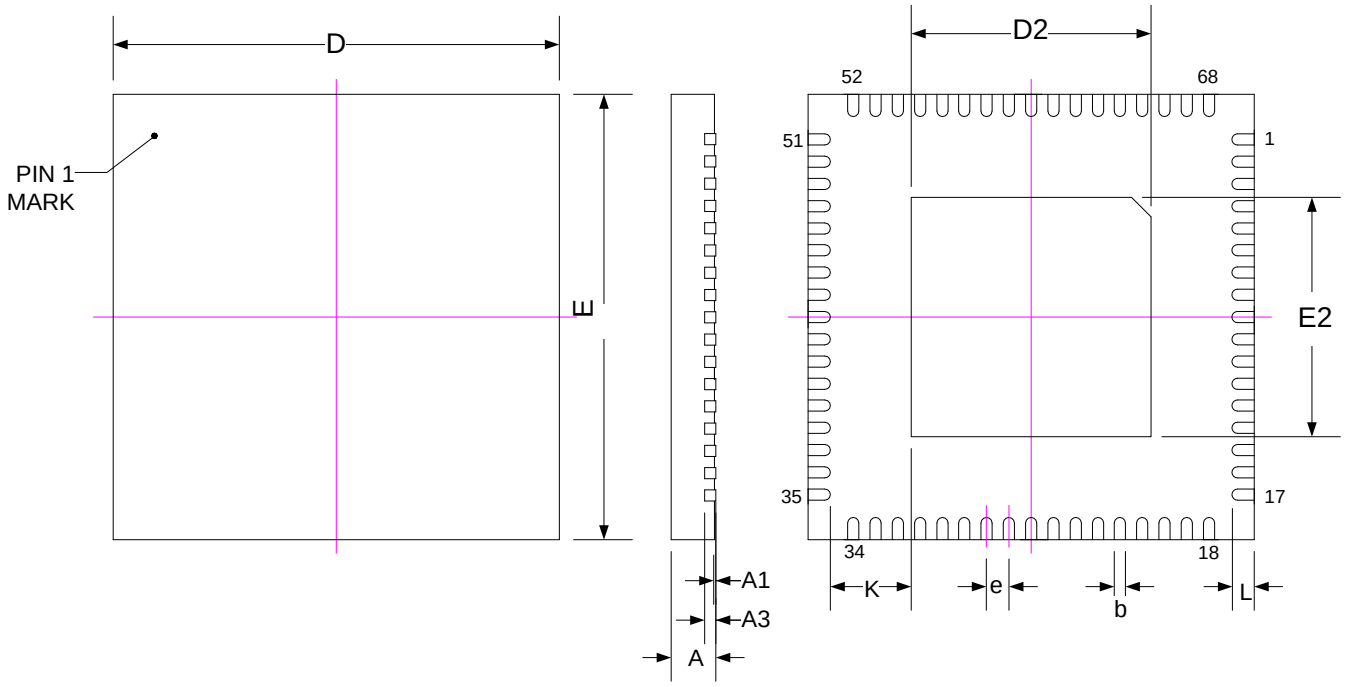


Note:

1. Publication IPC-7351 is recommended for alternate designs
2. Unit : mm
3. http://www.hycontek.com/attachments/MSP/OJTI-HM-2013-002.pdf

7.4. QFN68 PKG Diagram

Unit:mm

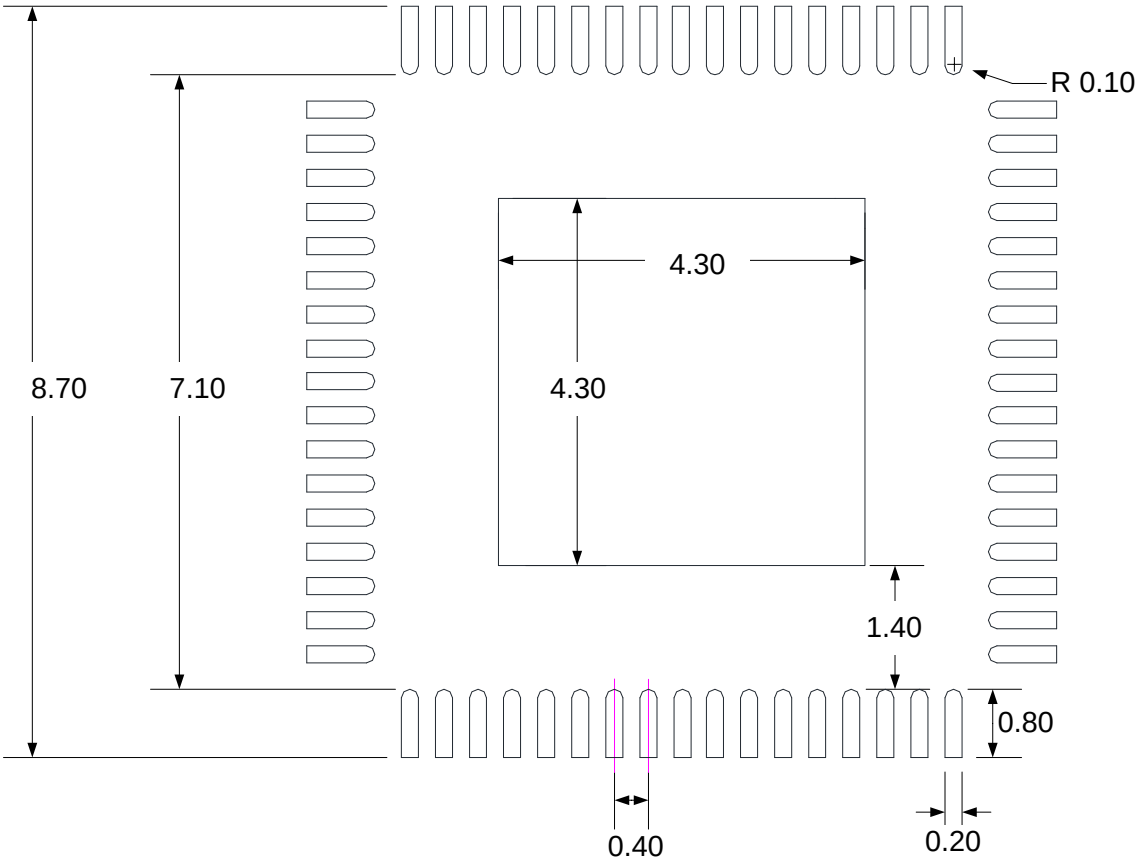


SYMBOLS	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		8.00 BSC	
E		8.00 BSC	
e		0.40 BSC	
D2	4.20	4.30	4.40
E2	4.20	4.30	4.40
L	0.35	0.40	0.45
K	1.35	1.45	1.55

Note: All dimensions refer to JEDEC OUTLINE MO-220.
Package Outline Drawing--- QFN 8x8 68

Land Pattern Design Recommendations

Unit : mm



Note:

1. Publication IPC-7351 is recommended for alternate designs
2. Unit : mm
3. http://www.hycontek.com/attachments/MSP/OJTI-HM-2013-002.pdf

8. HY16F19xB Upgrade Description

HY16F19xB is an upgrade version of HY16F19x. With the same package type, it's not only backward compatible but enhanced for specific applications. Followings are the upgrade description:

1. SPI Slave Mode Improvement:

- HY16F19x with SPI Slave Mode configuration doesn't support the Wake-up function when in Sleep mode.
- HY16F19xB supports the Wake-up function through SPI CS pin when in Sleep mode.

2. VLCD Power Reduction:

- HY16F19x limits VLCD voltage to the level lower than VDD3V to avoid unnecessary current drain.
- HY16F19xB supports VLCD voltage usage regardless of VDD3V level without unnecessary current drain.

3. Flash Erase Function Improvement:

- HY16F19x needs a correct password when conducting Flash Erase command to erase program by using the Writer Kit.
- HY16F19xB supports Flash Erase command to erase program without the need for password.

4. ISP Bootloader Support:

- HY16F19x doesn't support ISP Bootloader.
- HY16F19xB supports ISP to updating user program through UART interface.

5. Flash Self-Burn Function Improvement:

- HY16F19x only supports following functions:
  - ROM_BurnWord: Including process of Erase and Word Write, takes around 30msec.
  - ROM_BurnPage: Including process of Erase and Page Write, takes around 30msec.
  - PageErase: Process of Page Erase, takes around 25msec.
  - SectorErase: Process of Sector Erase , takes around 25msec.

- HY16F19xB adds following functions (without Erasing operation) to shorten writing time.:
  - ROM_BurnWordonly: Only conduct process of Word Write, takes around 3msec.
  - ROM_BurnPageWriteonly: Only conduct process of Page Write, takes around

3msec.

6. Notes of Compatibility between HY16F19x and HY16F19xB:

- HY16F19x and HY16F19xB are compatible in hardware level. A Source code needs to be compiled for the target hardware. Following are either ways to port source code to target hardware.
  - Create a new project for the target hardware then copy your source code to the new project and compile.
  - In current project, configure the Linker file path to the one corresponding to the target hardware and compile.

9. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary	Date
V01	ALL	First edition	2014/06/06
V02	P55/P52/P06	Add QFN88 Pin Figure Information	2014/10/06
	P51	Revise LCD Spec Description	
V03	ALL	8-bit DAC change to 8-bit Resistance Ladder	2015/01/12
	CH5	Add Spec Curve Diagram	
	CH7.4	Add QFN68 Pin Figure Information	
V04	CH4.1	IC Diagram “8-bit DAC: change to “8-bit Resistance Ladder”	2015/06/09
	CH4.6	ADC Network output change OPO to OPOI, REFO Revise as REFO_I	
	CH4.7	OPAMP Network Input REFO Revise as REFO_I	
	CH4.8	8-bit Resistance Ladder Network Input REFO Revise as REFO_I	
	CH5.3	REFO Buffer Capacitor loading revise unit: pF to nF, and add Min Value 22nF	
V05	CH1&2&CH6.2	Add HY16F19xB related information	2015/8/6
	CH7.3&CH7.4	Add QFN68 and QFN88 Land Pattern design recommendations	
	CH8	Add CH8, HY16F19xB upgrade descriptions	2015/11/20