HY2613A/B/C
Datasheet

RAM Mapping 4x36
LCD Controller Driver
With LED Backlight
Built-in Charge Pump

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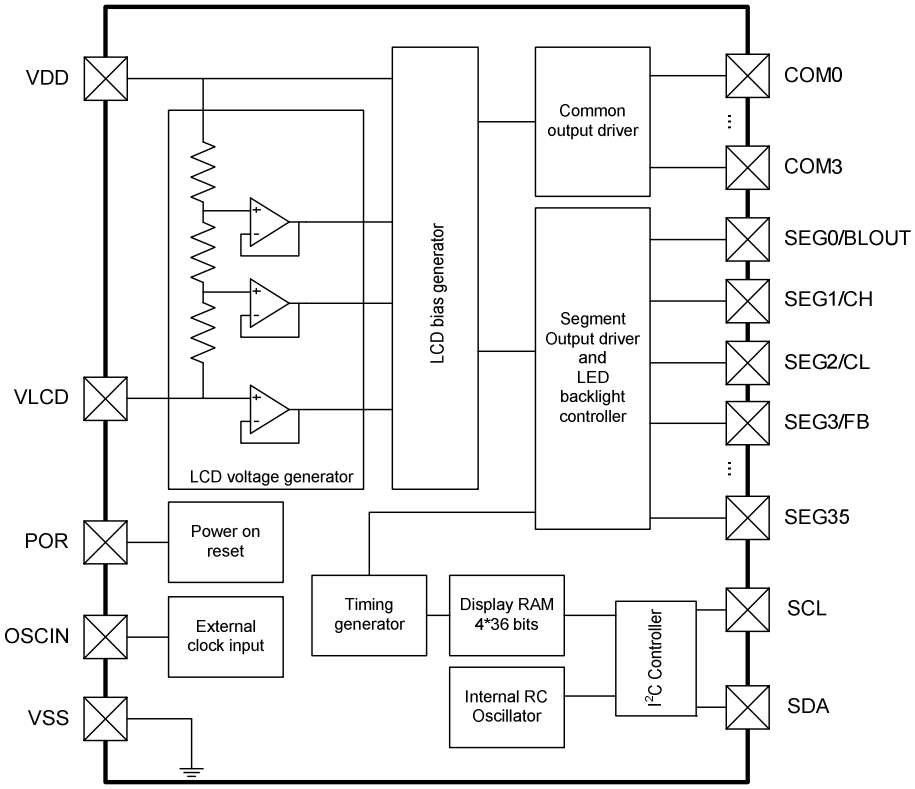
1. FEATURES

- Integrated RAM LCD Display Function
  - Driver output type
    - 4*36 segments
    - 4*32 segments (LED back light)
    - Integrated blinking function
  - Bias Circuit and Cycle
    - 1/2 or 1/3 Bias,1/4 Duty
    - High side or low side driver
    - Built-in Buffer AMP
  - Power
    - Contrast adjust function
    - Micro contrast function
    - Built-in voltage pump has 8 output voltage
  - LED Back Light Function
    - Constant current: 15mA/4.2V
- Digital Function
  - Built-in display data ram (DDRAM) 4*36=144BIT
  - 2-wire I^2C serial communication interface （SCL,SDA）
  - Built-in 33KHz LPO oscillation circuit
  - Low power consumption and Idle mode
  - IRQ pin function (HY2613A/C only)
    - Time Base output
    - WDT NMI output
- Operation Environment
  - Operation voltage: 2.4V to 5.5V
  - Operation temperature: –40℃ to +85℃
  - No external components
  - Integrated Power on reset circuit



Model No.	LCD Segment	LED Driver	VLCD Charge pump	LCD Mode	LCD Bias	IRQ	LCD Duty	Serial Interface	PIN
HY2613A	4x36	-	Yes	High Side	1/2, 1/3	Yes	1/4	I^2C	TSSOP48/LQFP48
HY2613B	4x36	-	-	Low Side	1/2, 1/3	-	1/4	I^2C	TSSOP48/LQFP48
HY2613C	4x32	Yes	Yes	High Side	1/2, 1/3	Yes	1/4	I^2C	TSSOP48/LQFP48

2. PIN DEFINITION

2.1. TSSOP48 Pin Diagram

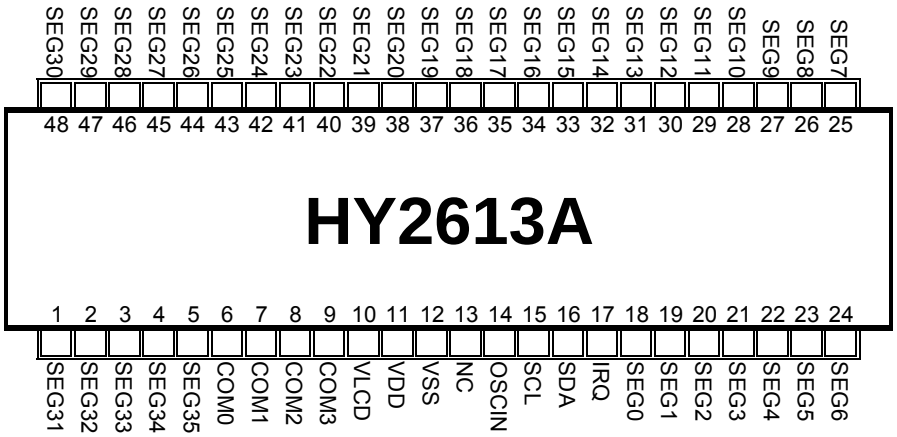


Figure 1 HY2613A TSSOP48 Pin Diagram

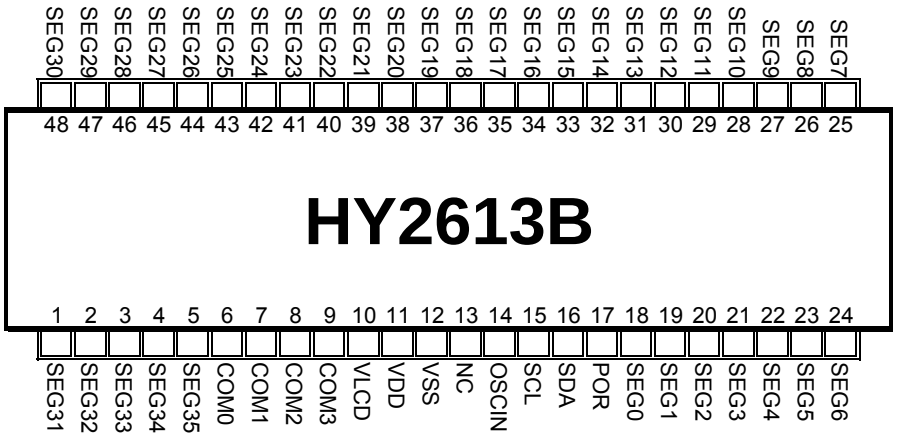


Figure 2 HY2613B TSSOP48 Pin Diagram

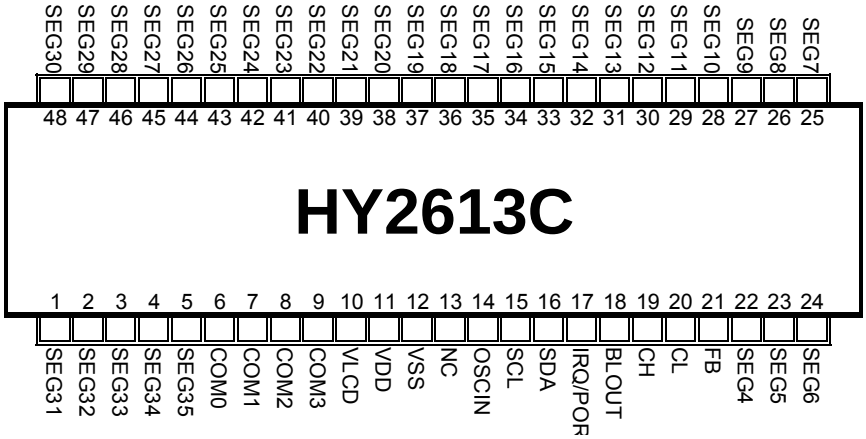


Figure 3 HY2613C TSSOP48 Pin Diagram

2.2. LQFP48 Pin Diagram

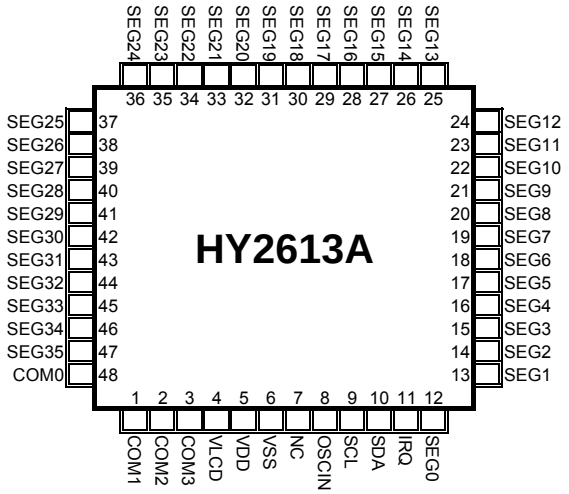


Figure 4 HY2613A LQFP48 Pin Diagram

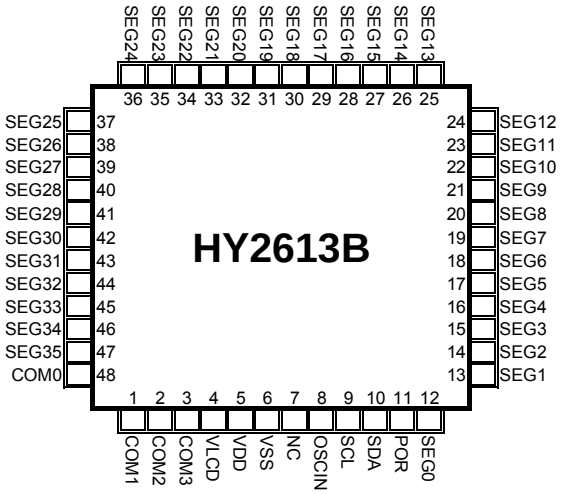


Figure 5 HY2613B LQFP48 Pin Diagram

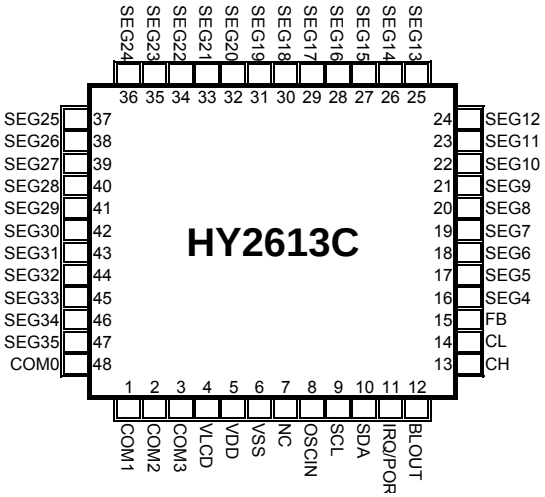


Figure 6 HY2613C LQFP48 Pin Diagram

2.3. TSSOP48 Description

"I/O" Output/Input, "I" Input, "O" Output, "S" Smith trigger, "C" CMOS character with output and input, "P" power, "A" Analog channel

No.	PIN NAME	Pin characteristic		Function Description
	HY2613	Buffer Type	Buffer Type	
1	SEG31	O	A	LCD Segment Output
2	SEG32	O	A	LCD Segment Output
3	SEG33	O	A	LCD Segment Output
4	SEG34	O	A	LCD Segment Output
5	SEG35	O	A	LCD Segment Output
6	COM0	O	A	LCD COM Output
7	COM1	O	A	LCD COM Output
8	COM2	O	A	LCD COM Output
9	COM3	O	A	LCD COM Output
10	VLCD (For HY2613A) (For HY2613B) (For HY2613C)	P P P P	P P P P	LCD power supply LCD power voltage input or charge pump power output LCD ground voltage input LCD power voltage input or charge pump power output
11	VDD	P	P	Power supply for IC operation
12	VSS	P	P	Grounding pin for IC operation voltage
13	NC	O	A	RESERVE
14	OSCIN OSCIN	 I	 A	 External clock input
15	SCL	I	C	I^2C clock input
16	SDA	I/O	C	I^2C Data input/output
17	IRQ/POR IRQ(HY2613A/C only) POR(HY2613B/C only)	 O I	 C C	 IRQ flag status output Power on reset function pin
18	SEG0/BLOUT SEG0(HY2613A/B only) BLOUT(HY2613C only)	 O P	 A P	 LCD Segment Output Charge pump power source F
19	SEG1/CH SEG1(HY2613A/B only) CH(HY2613C only)	 O I/O	 A A	 LCD Segment Output Charge pump fly capacitor port

20	SEG2/CL SEG2(HY2613A/B only) CL(HY2613C only)	 O I/O	 A A	 LCD Segment Output Charge pump fly capacitor port
21	SEG3/FB SEG3(HY2613A/B only) FB(HY2613C only)	 O I	 A A	 LCD Segment Output Constant current feedback port
22	SEG4	O	A	LCD Segment Output
23	SEG5	O	A	LCD Segment Output
24	SEG6	O	A	LCD Segment Output
25	SEG7	O	A	LCD Segment Output
26	SEG8	O	A	LCD Segment Output
27	SEG9	O	A	LCD Segment Output
28	SEG10	O	A	LCD Segment Output
29	SEG11	O	A	LCD Segment Output
30	SEG12	O	A	LCD Segment Output
31	SEG13	O	A	LCD Segment Output
32	SEG14	O	A	LCD Segment Output
33	SEG15	O	A	LCD Segment Output
34	SEG16	O	A	LCD Segment Output
35	SEG17	O	A	LCD Segment Output
36	SEG18	O	A	LCD Segment Output
37	SEG19	O	A	LCD Segment Output
38	SEG20	O	A	LCD Segment Output
39	SEG21	O	A	LCD Segment Output
40	SEG22	O	A	LCD Segment Output
41	SEG23	O	A	LCD Segment Output
42	SEG24	O	A	LCD Segment Output
43	SEG25	O	A	LCD Segment Output
44	SEG26	O	A	LCD Segment Output
45	SEG27	O	A	LCD Segment Output
46	SEG28	O	A	LCD Segment Output
47	SEG29	O	A	LCD Segment Output
48	SEG30	O	A	LCD Segment Output

Table 1 HY2613A/B/C TSSOP48 Pin Description

2.4. LQFP48 Description

"I/O" Output/Input, "I" Input, "O" Output, "S" Smith trigger, "C" CMOS character with output and input, "P" power, "A" Analog channel

No.	PIN NAME	Pin characteristic		Function Description
	HY2613	Buffer Type	Buffer Type	
1	COM1	O	A	COM output for LCD
2	COM2	O	A	COM output for LCD
3	COM3	O	A	COM output for LCD
4	VLCD (For HY2613A) (For HY2613B) (For HY2613C)	P P P P	P P P P	LCD power supply LCD power voltage input or charge pump power output LCD ground voltage input LCD power voltage input or charge pump power output
5	VDD	P	P	Power supply for IC operation
6	VSS	P	P	Grounding pin for IC operation voltage
7	NC	O	A	RESERVE
8	OSCIN OSCIN	 I	 AA	 External clock input
9	SCL	I	C	I^2C clock input
10	SDA	I/O	C	I^2C Data input/output
11	IRQ/POR IRQ(HY2613A/C only) POR(HY2613B/C only)	 O I	 C C	 IRQ flag status output Power on reset function pin
12	SEG0/BLOUT SEG0(HY2613A/B only) BLOUT(HY2613C only)	 O P	 A P	 COM Output for LCD Charge pump power source
13	SEG1/CH SEG1(HY2613A/B only) CH(HY2613C only)	 O I/O	 A A	 COM Output for LCD Charge pump capacitor port
14	SEG2/CL SEG2(HY2613A/B only) CL(HY2613C only)	 O I/O	 A A	 COM Output for LCD Charge pump capacitor port
15	SEG3/FB SEG3(HY2613A/B only) FB(HY2613C only)	 O I	 A A	 COM Output for LCD Constant current feedback port

16	SEG4	O	A	Segment output for LCD
17	SEG5	O	A	Segment output for LCD
18	SEG6	O	A	Segment output for LCD
19	SEG7	O	A	Segment output for LCD
20	SEG8	O	A	Segment output for LCD
21	SEG9	O	A	Segment output for LCD
22	SEG10	O	A	Segment output for LCD
23	SEG11	O	A	Segment output for LCD
24	SEG12	O	A	Segment output for LCD
25	SEG13	O	A	Segment output for LCD
26	SEG14	O	A	Segment output for LCD
27	SEG15	O	A	Segment output for LCD
28	SEG16	O	A	Segment output for LCD
29	SEG17	O	A	Segment output for LCD
30	SEG18	O	A	Segment output for LCD
31	SEG19	O	A	Segment output for LCD
32	SEG20	O	A	Segment output for LCD
33	SEG21	O	A	Segment output for LCD
34	SEG22	O	A	Segment output for LCD
35	SEG23	O	A	Segment output for LCD
36	SEG24	O	A	Segment output for LCD
37	SEG25	O	A	Segment output for LCD
38	SEG26	O	A	Segment output for LCD
39	SEG27	O	A	Segment output for LCD
40	SEG28	O	A	Segment output for LCD
41	SEG29	O	A	Segment output for LCD
42	SEG30	O	A	Segment output for LCD
43	SEG31	O	A	Segment output for LCD
44	SEG32	O	A	Segment output for LCD
45	SEG33	O	A	Segment output for LCD
46	SEG34	O	A	Segment output for LCD
47	SEG35	O	A	Segment output for LCD
48	COM0	O	A	COM output for LCD

Table 2 HY2613A/B/C LQFP48 Pin Description

3. APPLICATION CIRCUIT

3.1. VLCD Connect to VDD

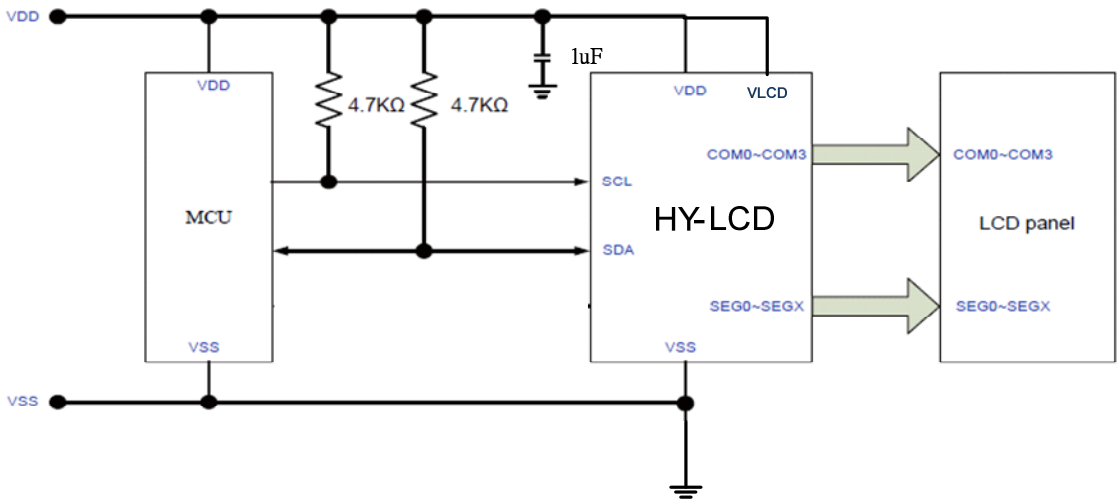


Figure 7 HY2613A/HY2613C Application Circuit I

3.2. VLCD Connect to VSS

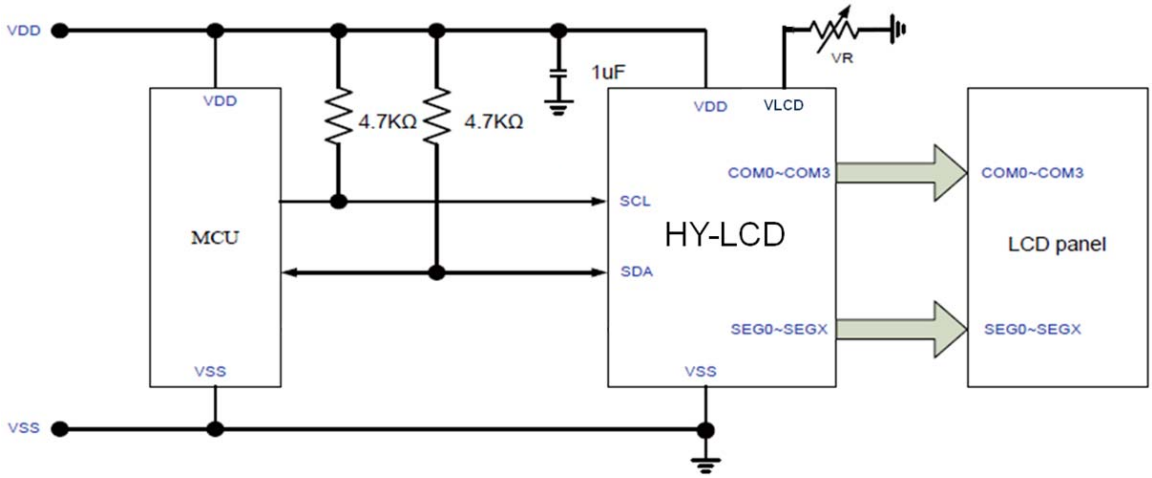


Figure 8 HY2613B Application Circuit II

3.3. VLCD Internal Charge Pump

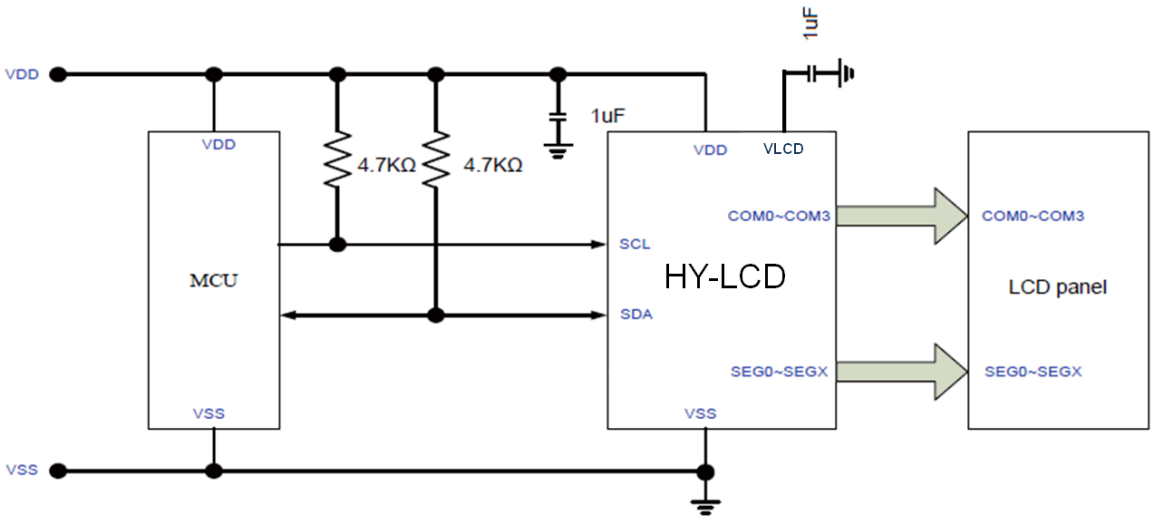


Figure 9 HY2613A/HY2613C Application CircuitⅢ

3.4. LED Back Light + VLCD Internal Charge Pump

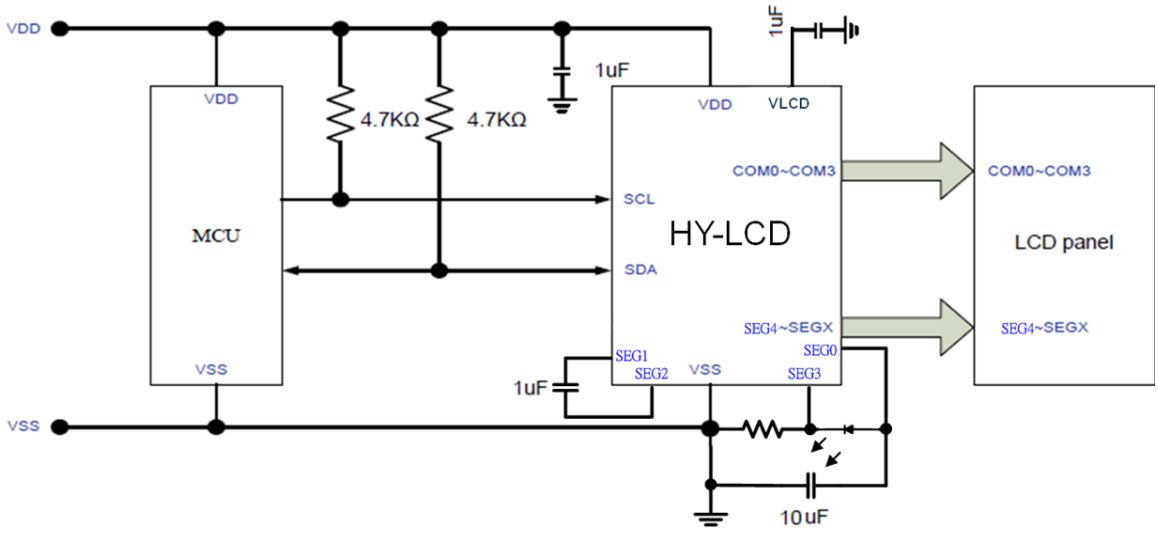


Figure 10 HY2613C Application CircuitⅣ

4. FUNCTION OUTLINE

4.1. Communicating interface

HY2613 uses I^2C interface to transfer data, communication form and description will be given in this chapter.

4.1.1. Start and Stop

Start command must be sent as to initiate data transmission. When the transmission completed, a Stop command must be given, as shown in Figure 11.

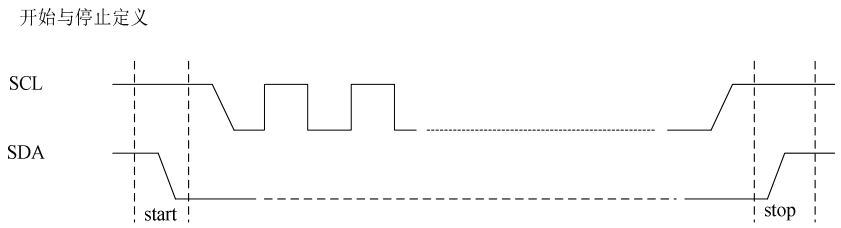
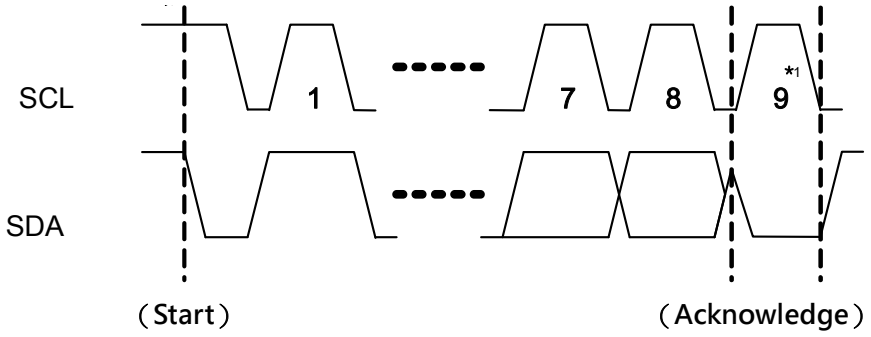


Figure 11 Start and Stop Command

4.1.2. ACK Sign

During actual data transmission process, the master end must receive an acknowledged signal, indicating the data transmission was completed and to proceed the next transmission. The ACK sign definition as shown as Figure 12.



* When Master sends the eighth clock of SCL signal to Slave, SDA pin of Master must change from output status to input status as to receive ACK signal from the Slave end.

Figure 12 ACK Sign

4.1.3. Transfer Form

I^2C data transmission procedures are as shown in Figure 13.

1. Initialization starts condition.
2. Send Slave address
3. Command, display data transfer.

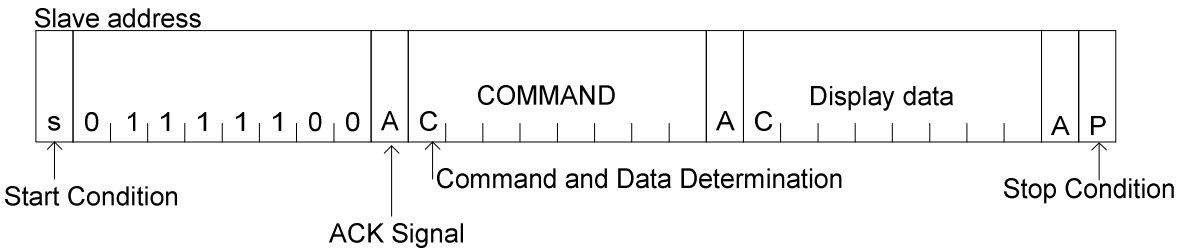


Figure 13 I²C Transfer Form

4.1.4. Order Transfer Rules

When start condition was set, sending slave address (“01111100”). After sending slave address, input 1 byte command. The MSB bit of command is to determine whenter the next one was command or display data.

Command or data determine bit=1, can input the following command.

Command or data determine bit=0, can input the following disply data.

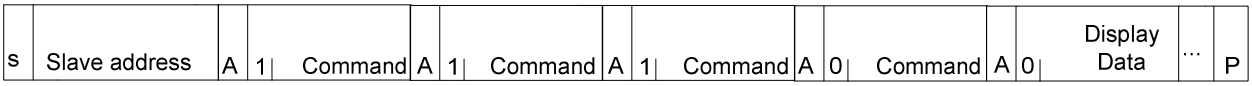


Figure 14 I²C Command Form

Command cannot be given under input display data status. To reinput command, the start condition must be formed again.

During command transmission status, inputting start condition or stop condition, the command in transfer will be canceled. Inputting start confition during transmission process, the next inputted Slave address will be converted to command input status.

After the start condition was formed, please Slave Address data first. If the initial Slave Address was not identified, no Acknowledge signal would return, the following transmission data will no be received. It would go back to input start condition when the data receiving was declined.

4.1.5. Display Data Write In and Transfer Rules

HY2613 built in 36×4=144bit Display Data RAM (DDRAM). Write in display data and DDRAM data and its corresponding address display is shown in below.

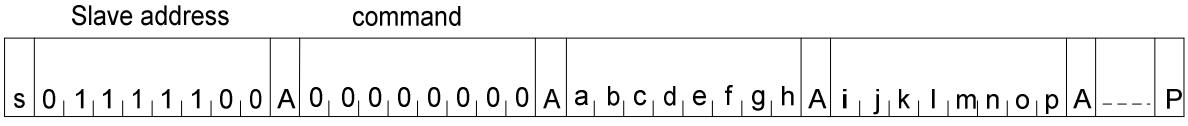


Figure 15 Data Write in and I²C Transfer Form

Write in Binary 8bit data to DDRAM. Writein area is pointed by Address set order, every 4bit data address will automatically increase. Thus, using continuous data transmission method can write date into DDRAM continuously.

bit	00h	01h	02h	03h	04h	05h	06h	.....	21h	22h	23h	
0	a	e	i	m								COM0
1	b	f	j	n								COM0
2	c	g	k	o								COM0
3	d	h	l	p								COM0
	SEG	SEG	SEG	SEG	SEG	SEG	SEG	.....	SEG	SEG	SEG	

Table 3 DDRAM Form

DDRAM data was written every 4bit, data writein will stop for not waiting ACK signal.

4.1.6. Advanced Function Data Write In and Transfer Rules

HY2613 embedded with LED driver, High side or Low side LCD driver, ...etc. function contol bit in SDRAM. It requires high level data writein and transmission way to start and stop function. Moreover, users must execute command『Extend Control (EXCTL)』to start advanced data operation. Please refer to *Chapter 5* for detailed description.

Advanced data memory has 20×4 = 80-bits control bit, there are two ways of writing in data, single data writein and continuous data writein. After completion of data writein, users must execute『I^2C Stop』command to exist advanced data writein mode, please refer to Figure 16 and Figure 17.

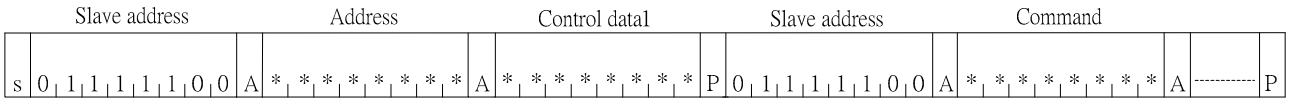


Figure 16 Advanced Single Data Write-in and Transmission Form

Example: Start, 0x7C, Ack, 0xE1, Ack, Stop, Start, 0x7C, Ack, Extend control address (0x00~0x05), Ack, Control data, Ack, Stop

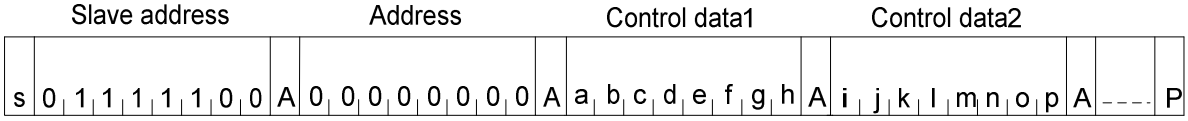


Figure 17 Advanced Continuous Data Write-in and Transmission Form

Binary 8bit advanced function controls write-in data to SDRAM. Writein field is appointed by command,『Extend Control (EXCTL)』+ 『Slave address + address + conrtol data1 + control data2 +...+ P』...I^2C transmission forms. Every 4bit data writein address will increased automatically. Thus, using continuous data sending way can write data continuously to SDRAM.

bit	00h	01h	02h	03h	04h	05h	06h	…	21h	22h	23h
0											
1											
2											
3											

Table 4 DDRAM form

SDRAM data was written every 4bit, data writein will stop for not waiting ACK signal.

Example: Start, 0x7C, Ack, 0xE1, Ack, Stop, Start, 0x7C, Ack, Extend control address (0x00~0x05), Ack, Control data1, Ack, Control data2, Ack, ..., Ack, Stop

4.2. Oscillation Feature, Oscillator

HY2613 can use internal oscillation circuit or external clock signal to generate internal operation and clock signal forLCD operation. Using internal oscillation circuit to operate, OSCIN pin and VSS pin must be short.

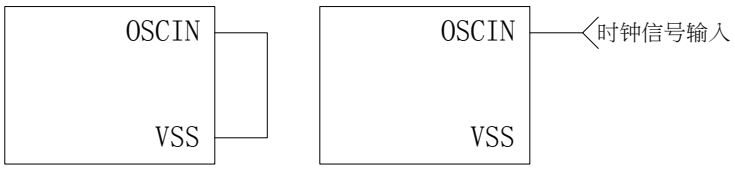


Figure 18 Circuit of Internal and External Clock Source

When the clock signal is provided extermally, using Set IC Operation (ICSET) command to switch and input external clock signal from OSCIN pin.

When using external input clock source, keeping f_{CLK} frequency as 80Hz, as shown in Figure 19. Pleas refer to *Chapter 5* for detailed description.

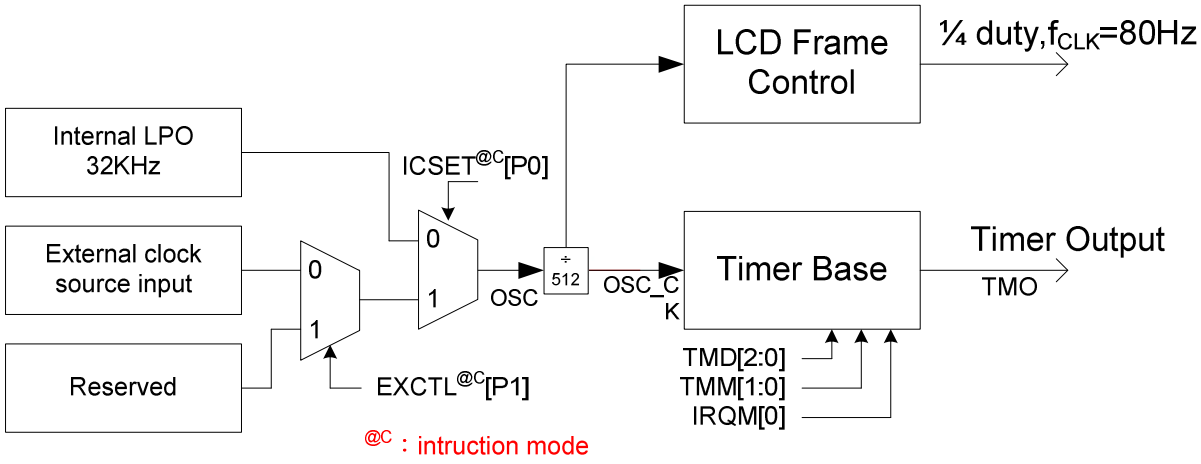


Figure 19 System Frequency Source

4.3. LCD Driver (Bias Circuit and Wave)

LCD DRIVE circuit generates LCD drive voltage. Low power consumption LCD drive display can be achieved by passing through internal BUFFER AMP:

- The setting of 1/3,1/2 Bias is settled by Mode Set (MODE SET) command.
- The setting of LINE,FRAME Inversion is settled by Display control (DISCTL) command.
- The Chapter 5 gives details of settinig up, for further reference.

4.3.1. 1/3-bias,1/4-duty LINE Inversion

	Segn	Segn+1	Segn+2	Segn+3	…
COM0	State A				…
COM1	State B				…
COM2					…
COM3					…
…	…	…	…	…	…

Figure 20 1/3-bias, 1/4-duty LINE Inversion

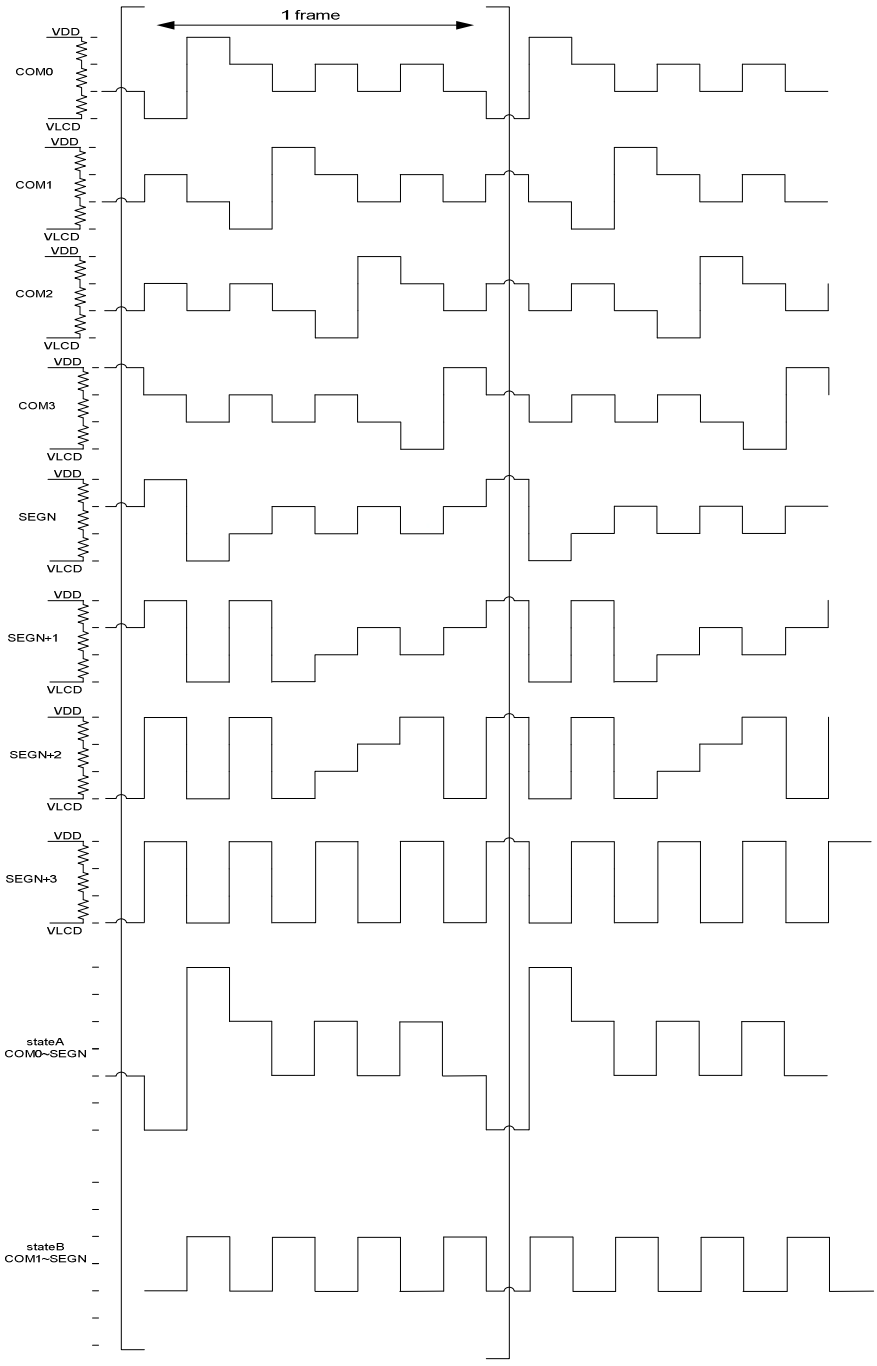


Figure 21 1/3-bias, 1/4-duty LINE Inversion

4.3.2. 1/3-bias,1/4-duty FRAME Inversion

	Segn	Segn+1	Segn+2	Segn+3	…
COM0	State A				…
COM1	State B				…
COM2					…
COM3					…
…	…	…	…	…	…

Figure 22 1/3-bias, 1/4-duty FRAME Inversion

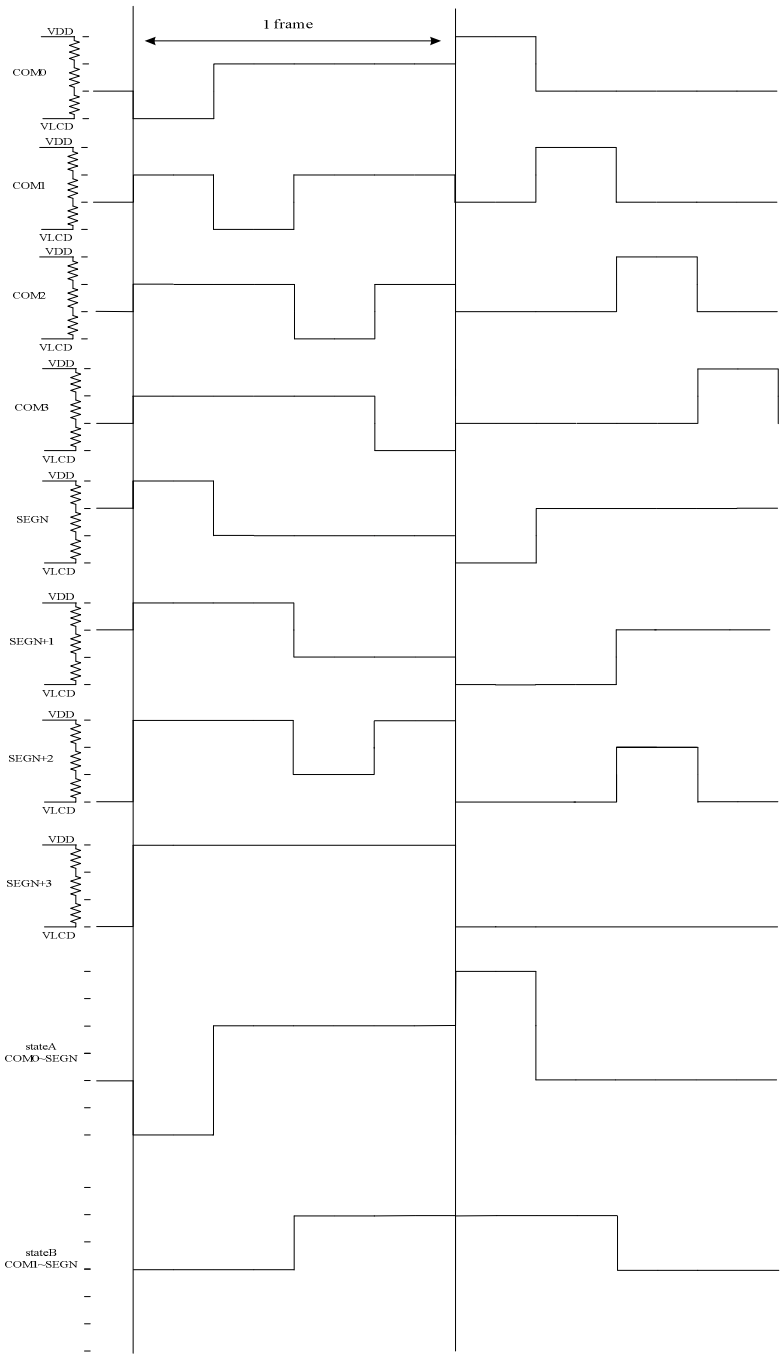


Figure 23 1/3-bias, 1/4-duty FRAM Inversion

4.3.3. 1/2-bias,1/4-duty LINE Inversion

	Segn	Segn+1	Segn+2	Segn+3	…
COM0	State A				…
COM1	State B				…
COM2					…
COM3					…
…	…	…	…	…	…

Figure 24 1/2-bias, 1/4-duty LINE Inversion

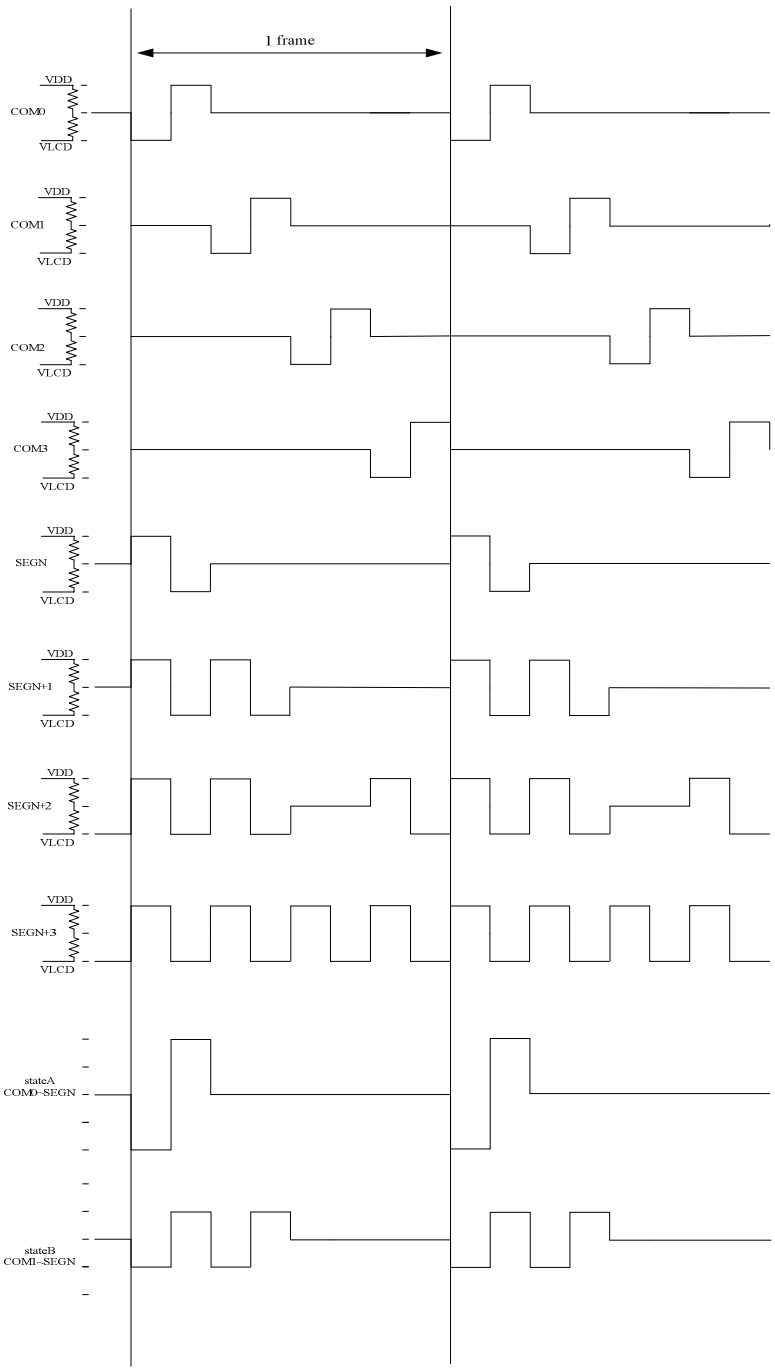


Figure 25 1/2-bias,1/4-duty LINE Inversion

4.3.4. 1/2-bias,1/4-duty FRAME Inversion

	Segn	Segn+1	Segn+2	Segn+3	…
COM0	State A				…
COM1	State B				…
COM2					…
COM3					…
…	…	…	…	…	…

Figure 26 1/2-bias, 1/4-duty FRAME Inversion

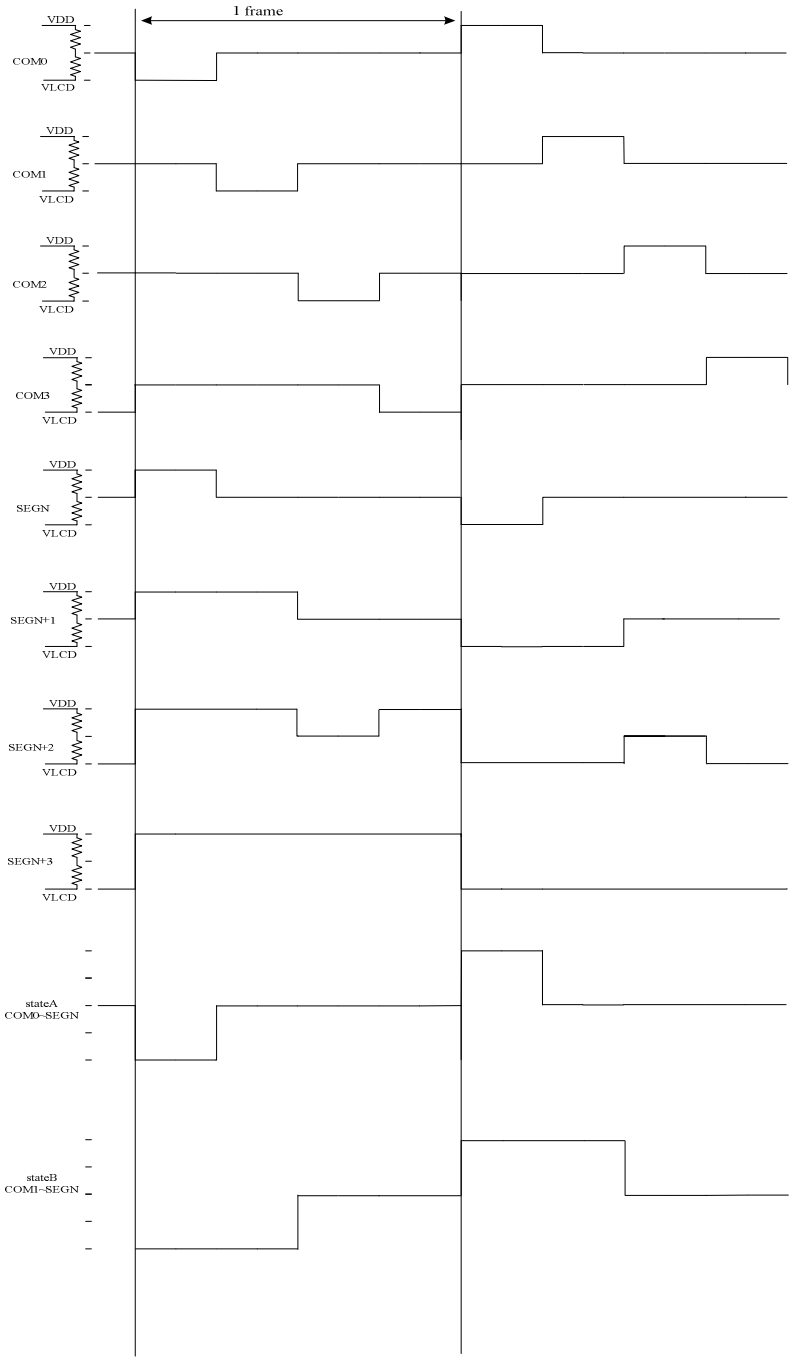


Figure 27 1/2-bias, 1/4-duty FRAM Inversion

4.4. Blinking Function

HY2613 has display blink function. Blink model is settled by Blink control (BLKCTL) command. Adjusting blink cycle in addcordance with f_{CLK} features when using internal oscillation cirucit. For detailed f_{CLK} features please refer to *Chapter 4.2Oscillation Feature, Oscillator*. *Chapter 5 Command* gives details of settinig up, for further reference.

4.5. LED Back Light Function

HY2613 offers LED driver function. Back light mode is configured by Backlight control command,『Extend Control (EXCTL)』. This function uses SEG0～SEG3, providing 4.2V/15mA output LED driver. *Chapter 5 Command* gives details of settinig up, for further reference.

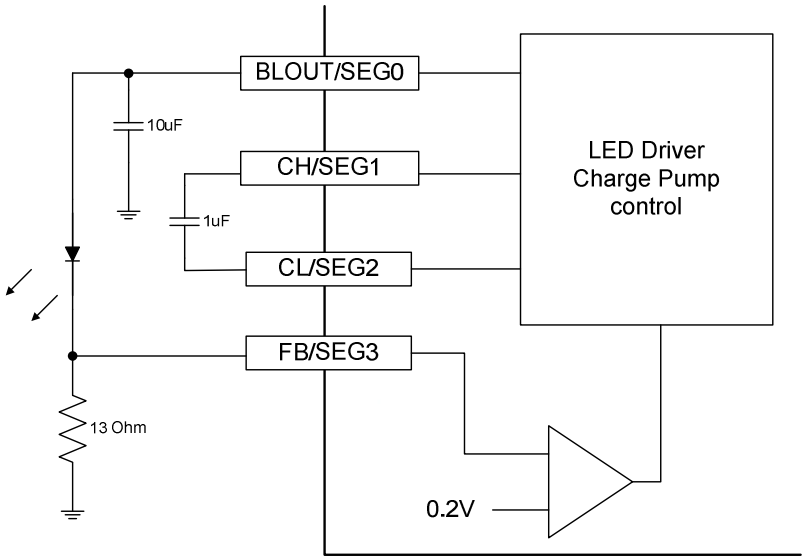


Figure 28 LED back light frame

4.5.1. LED Back Light Circuit

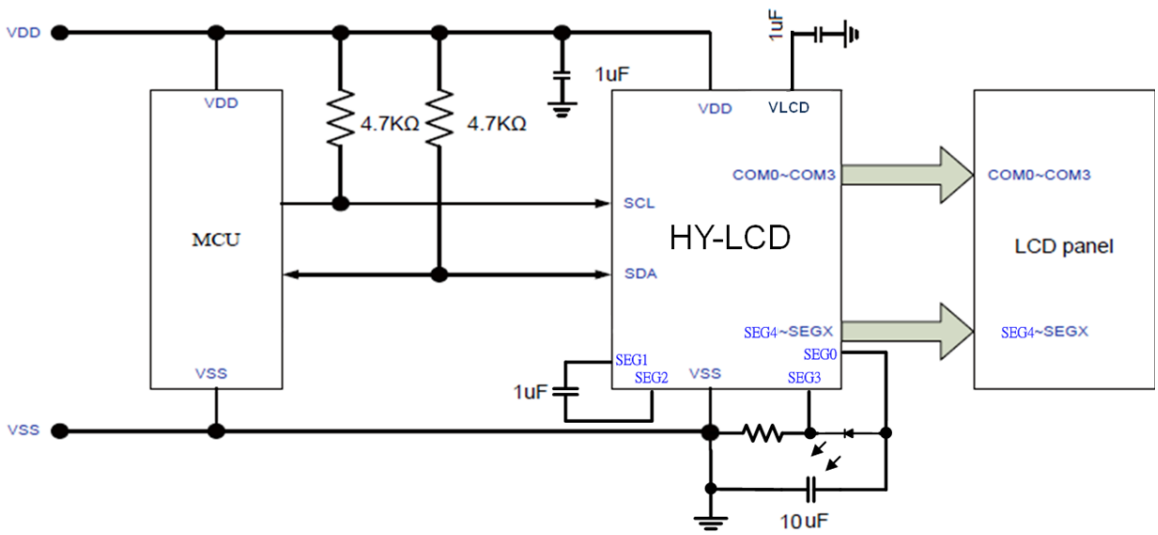


Figure 29 LED back light circuit

4.6. LCD Operate Voltage and Contrast Adjustment

LCD drive voltage has three modes and built-in 16-step voltage adjust function, through VLCD contoller can select VLCD pin to connect to VDD (HY2613A/HY2613C), VSS (HY2613B) or using internal charge pump (HY2613A/HY2613C) way. Through CTVR[3:0] contrast adjust controller can adjust VLCD pin equivalent voltage. *Chapter 5 Command* gives details of settinig up, for further reference.

4.6.1. VLCD Connects to VDD without External Contrast Adjustment

Connecting VLCD to VDD mode does not support external Contrast adjust function. Users can use embedded contrast to adjust CTVR controller.

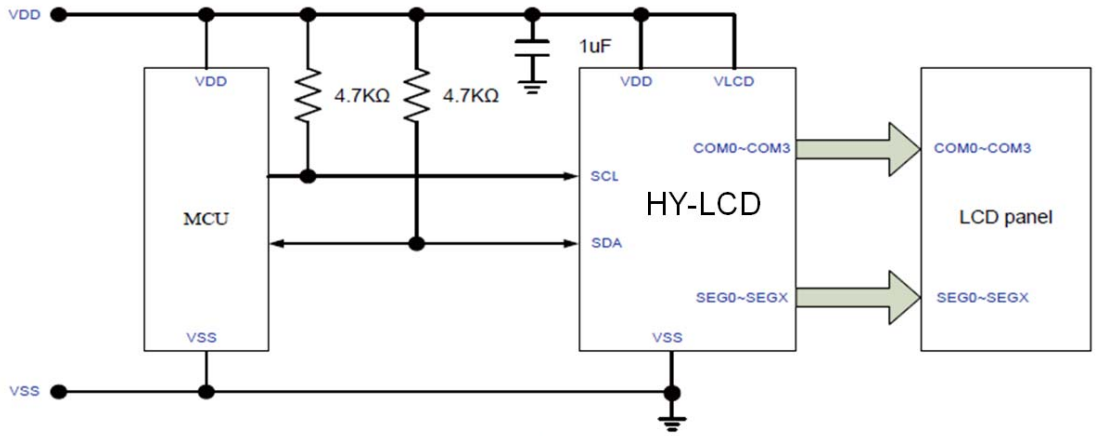


Figure 30 HY2613A/HY2613C VLCD Connect to VDD

4.6.2. VLCD Connects to VDD without External Contrast Adjustment

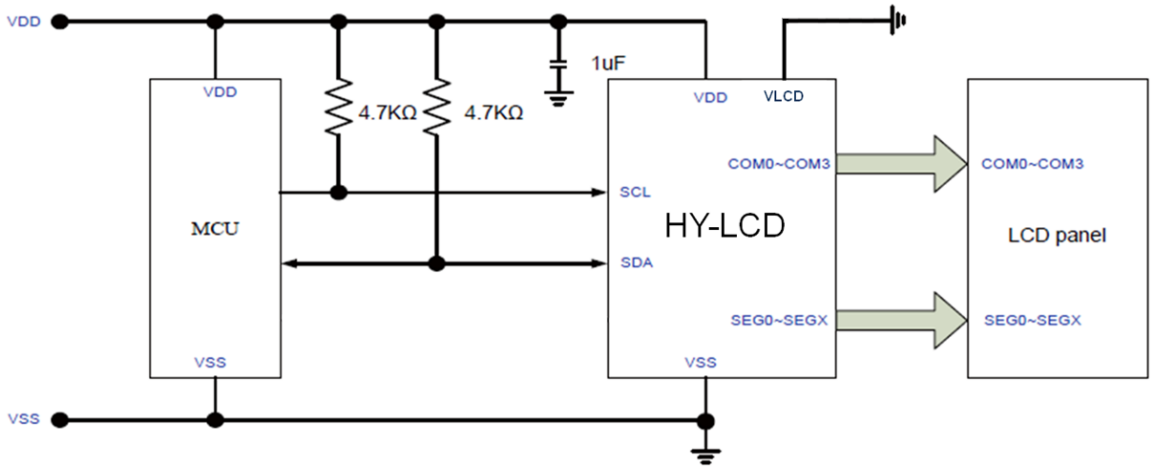


Figure 31 HY2613A/HY2613C VLCD Connect to VDD with outside contrast adjustment

4.6.3. VLCD Through Resistance Connect to VSS with Outside Contrast Adjustment

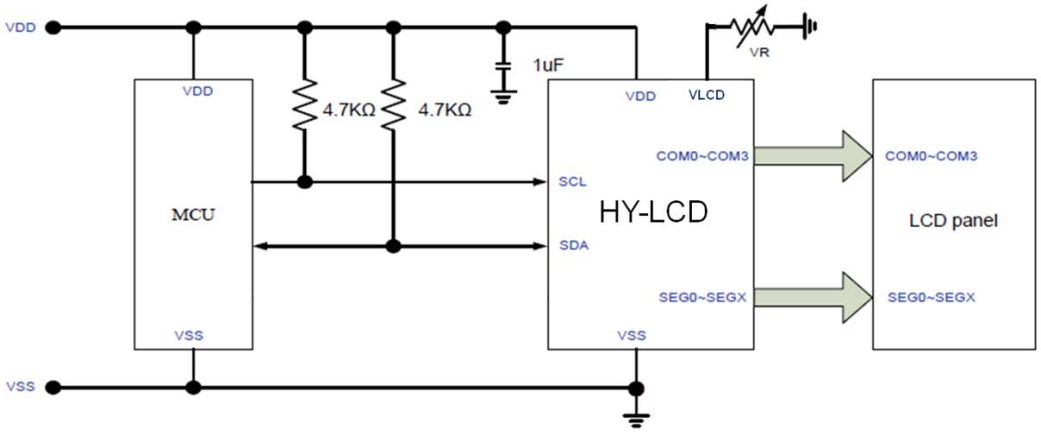


Figure 32 HY2613B VLCD connect to VSS with outside contrast adjustment

4.6.4. VLCD Adopts Internal Charge Pump

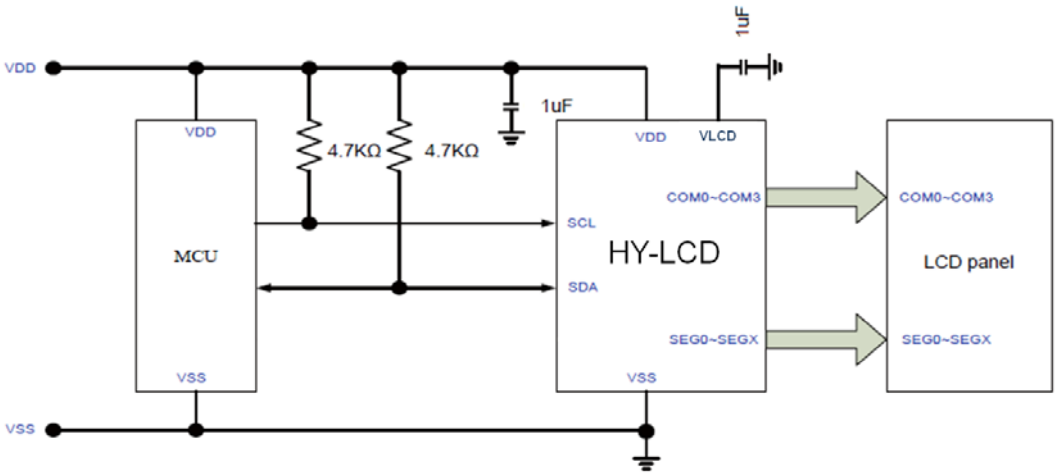


Figure 333 HY2613A/HY2613C LCD Adopts Internal VLCD Charge Pump Way

4.6.5. Contrast Adjust Function Description

Connecting a variable resistor between VLCD～VSS to realize external CONTRAST adjust function (applicable to HY2613B version IC).

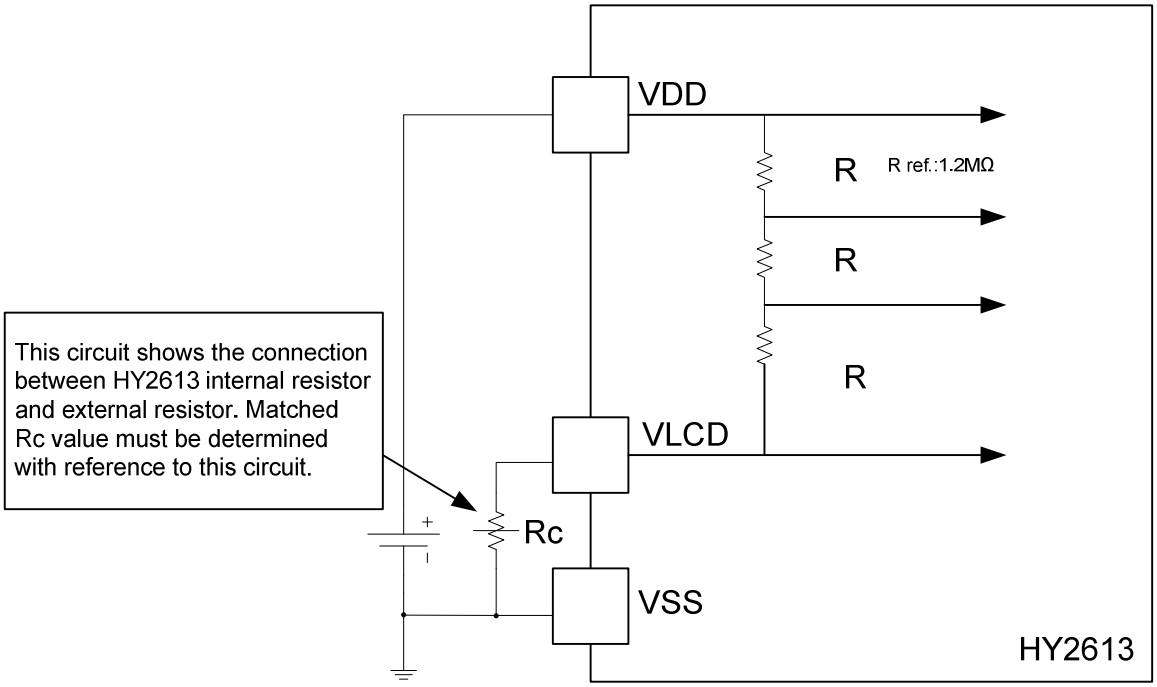


Figure 34 1/3-bias use CONTRAST

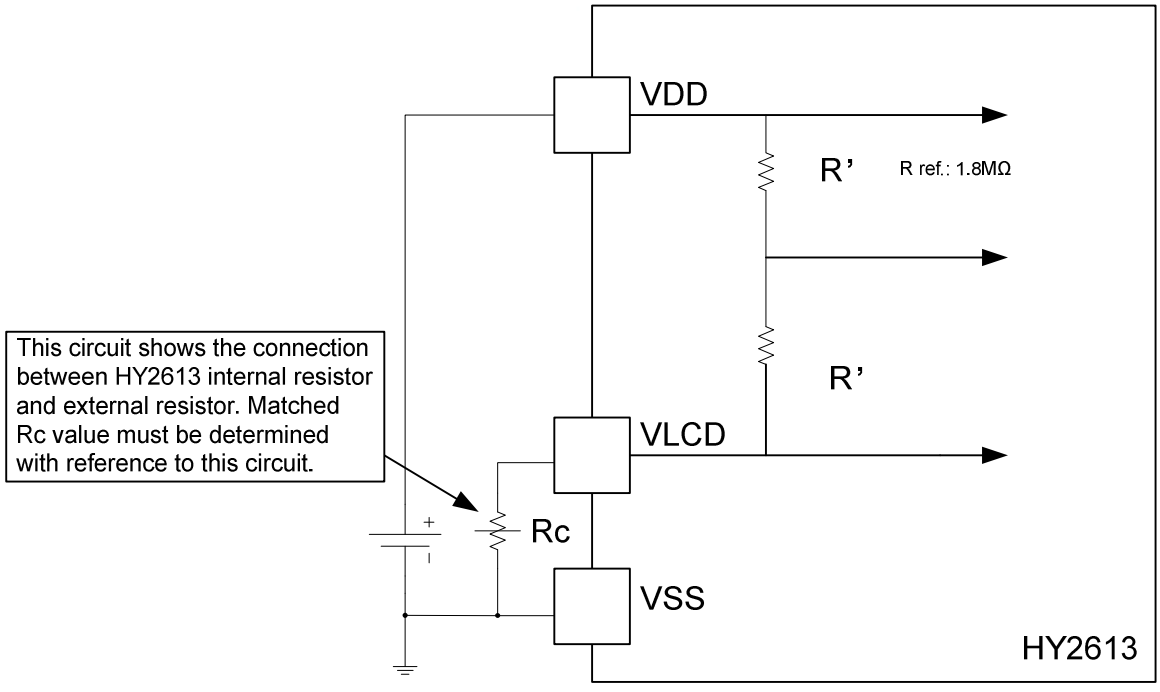


Figure 35 1/2-bias use CONTRAST

Reference circuits without using CONTRAST function are shown in below:

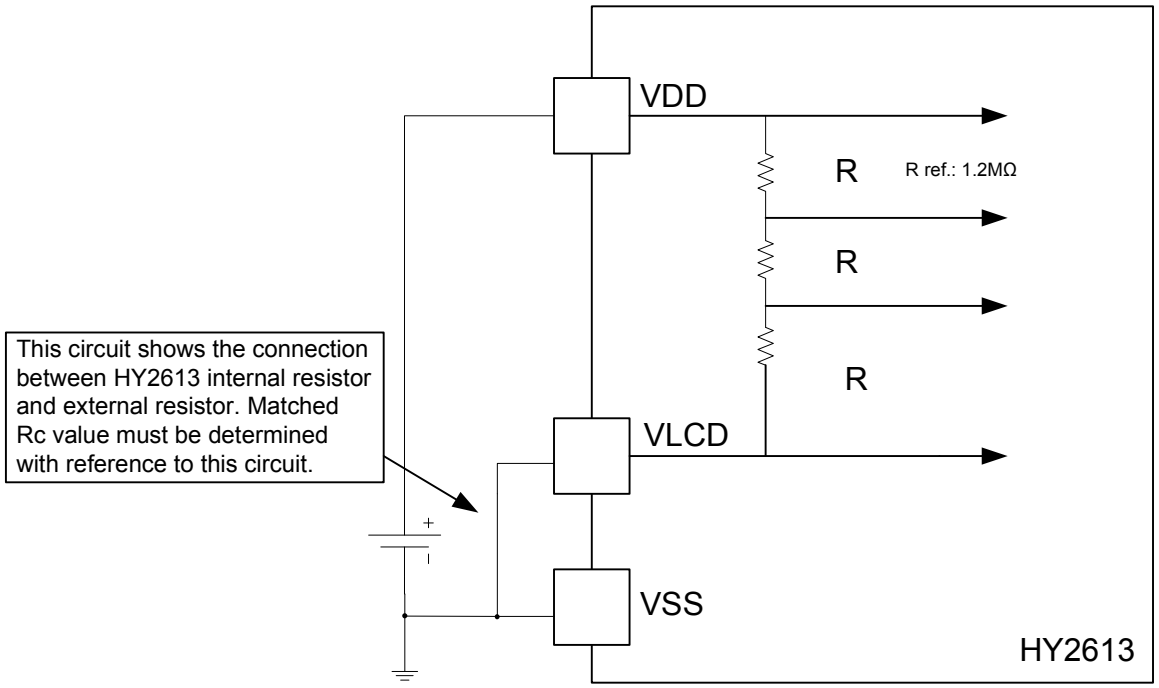


Figure 36 1/3-bias without us CONTRAST

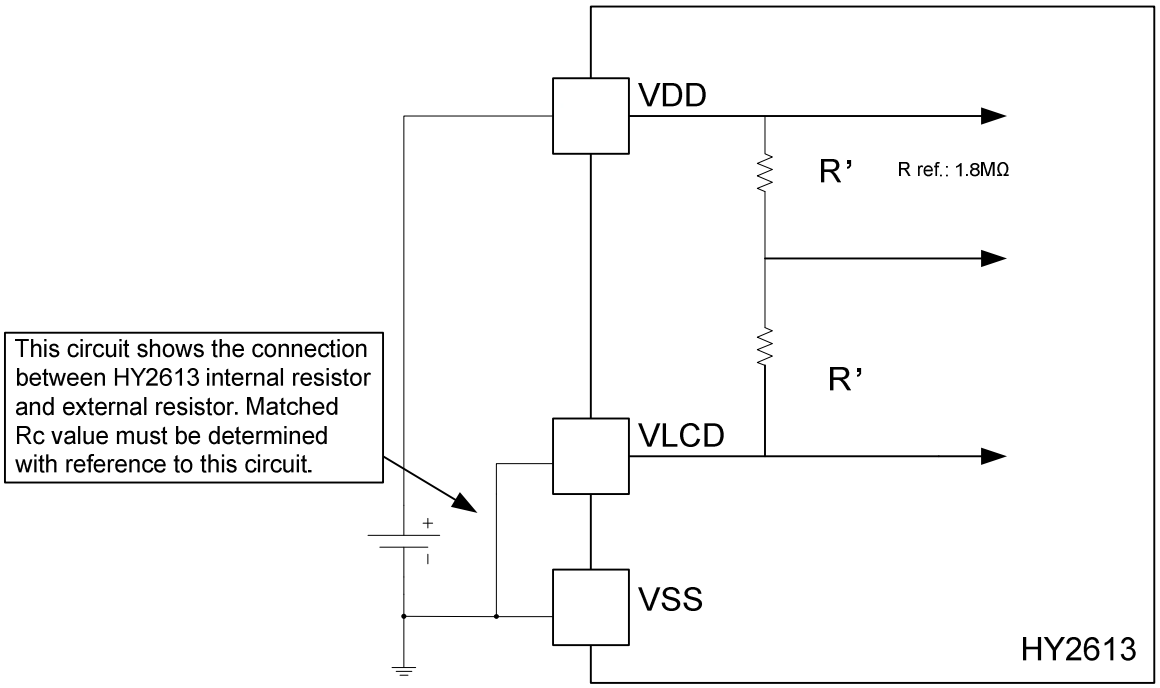


Figure 37 1/2-bias without us CONTRAST

4.6.6. VLCD Built-in CONTRAST Adjust controller

HY2613A/HY2613C embedded with contrast adjust controller to change LCD drive voltage, adjusting contrast display effect. Contrast adjust controller equivalent output voltage and calculation method, please refer to Figure and Table 5.

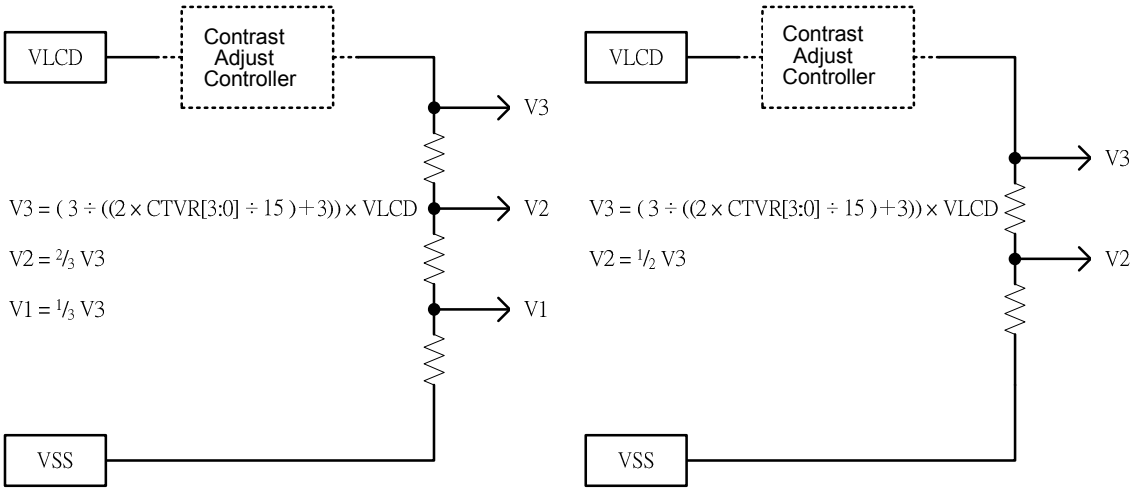


Figure 38 LCD contrast adjust circuit

CTVR[3:0]	1/3 , 1/2 Bias Voltage Display			1/2 Bias Voltage Display		Remark
	V3	V2	V1	V3	V2	
0000	5.000V	3.333V	1.667V	5.000V	2.500V	
0001	4.787V	3.191V	1.596V	4.787V	2.394V	
0010	4.592V	3.061V	1.531V	4.592V	2.296V	
0011	4.412V	2.941V	1.471V	4.412V	2.206V	
0100	4.245V	2.830V	1.415V	4.245V	2.123V	
0101	4.091V	2.727V	1.364V	4.091V	2.045V	
0110	3.947V	2.632V	1.316V	3.947V	1.974V	
0111	3.814V	2.542V	1.271V	3.814V	1.907V	
1000	3.689V	2.459V	1.230V	3.689V	1.844V	
1001	3.571V	2.381V	1.190V	3.571V	1.786V	
1010	3.462V	2.308V	1.154V	3.462V	1.731V	
1011	3.358V	2.239V	1.119V	3.358V	1.679V	
1100	3.261V	2.174V	1.087V	3.261V	1.630V	
1101	3.169V	2.113V	1.056V	3.169V	1.585V	
1110	3.082V	2.055V	1.027V	3.082V	1.541V	
1111	3.000V	2.000V	1.000V	3.000V	1.500V	

Table 5 Table of LCD Contrast Adjust Equivalent Voltage

4.7. Counter Output

Both HY2613A/HY2613C has two counter sets output. One of them is Time Base, the other is NMI signal. Detailed configurations please refer to *Chapter 5*

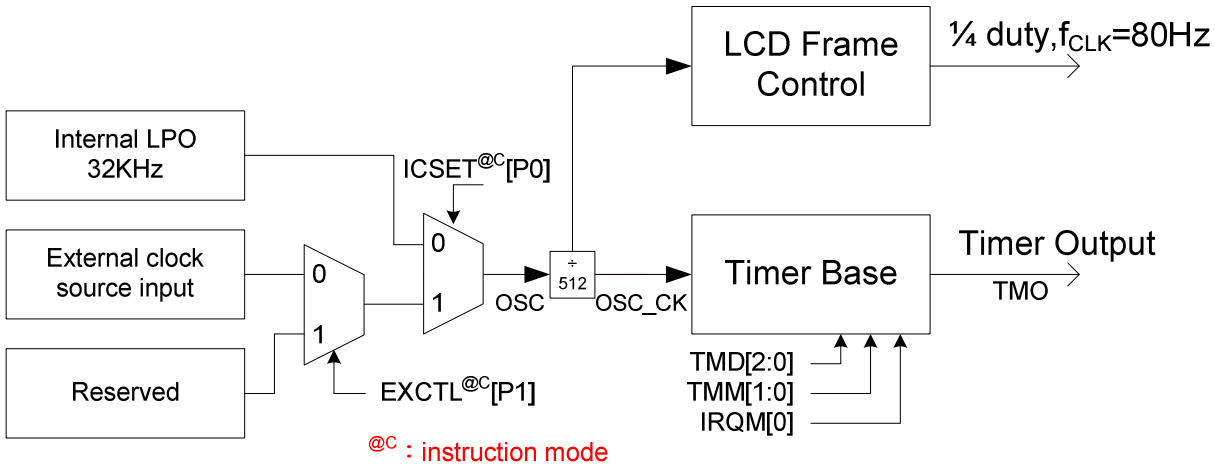


Figure 39 Timer Output Structure

4.8. Initialization Flow

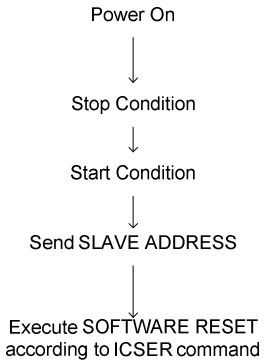


Figure 39 Initialization Flow

Please execute the following procedures after power on. Reset HY2613 initial value. DDRAM data of all registers are unknown.

4.9. Reset Initialization Status

RESET initialization status after executing Software Reset:

- Display is close.
- Initialzation DDRAM address (Do not initialize DDRAM data).
- Register initial value is illustrated in *Chapter 5*.

4.10. Table of RAM

"u"：不變更,"."：未使用,"*"：可讀/寫,"$"：0→1→0

Address	Name	Bit 3	Bit 2	Bit 1	Bit 0	POR	non-POR	R/W
00h	**SEG0**	SEG0[3]	SEG0[2]	SEG0[1]	SEG0[0]	uuuu	uuuu	*,*,*
01h	**SEG1**	SEG1[3]	SEG1[2]	SEG1[1]	SEG1[0]	uuuu	uuuu	*,*,*
02h	**SEG2**	SEG2[3]	SEG2[2]	SEG2[1]	SEG2[0]	uuuu	uuuu	*,*,*
03h	**SEG3**	SEG3[3]	SEG3[2]	SEG3[1]	SEG3[0]	uuuu	uuuu	*,*,*
04h	**SEG4**	SEG4[3]	SEG4[2]	SEG4[1]	SEG4[0]	uuuu	uuuu	*,*,*
05h	**SEG5**	SEG5[3]	SEG5[2]	SEG5[1]	SEG5[0]	uuuu	uuuu	*,*,*
06h	**SEG6**	SEG6[3]	SEG6[2]	SEG6[1]	SEG6[0]	uuuu	uuuu	*,*,*
07h	**SEG7**	SEG7[3]	SEG7[2]	SEG7[1]	SEG7[0]	uuuu	uuuu	*,*,*
08h	**SEG8**	SEG8[3]	SEG8[2]	SEG8[1]	SEG8[0]	uuuu	uuuu	*,*,*
09h	**SEG9**	SEG9[3]	SEG9[2]	SEG9[1]	SEG9[0]	uuuu	uuuu	*,*,*
0Ah	**SEG10**	SEG10[3]	SEG10[2]	SEG10[1]	SEG10[0]	uuuu	uuuu	*,*,*
0Bh	**SEG11**	SEG11[3]	SEG11[2]	SEG11[1]	SEG11[0]	uuuu	uuuu	*,*,*
0Ch	**SEG12**	SEG12[3]	SEG12[2]	SEG12[1]	SEG12[0]	uuuu	uuuu	*,*,*
0Dh	**SEG13**	SEG13[3]	SEG13[2]	SEG13[1]	SEG13[0]	uuuu	uuuu	*,*,*
0Eh	**SEG14**	SEG14[3]	SEG14[2]	SEG14[1]	SEG14[0]	uuuu	uuuu	*,*,*
0Fh	**SEG15**	SEG15[3]	SEG15[2]	SEG15[1]	SEG15[0]	uuuu	uuuu	*,*,*
10h	**SEG16**	SEG16[3]	SEG16[2]	SEG16[1]	SEG16[0]	uuuu	uuuu	*,*,*
11h	**SEG17**	SEG17[3]	SEG17[2]	SEG17[1]	SEG17[0]	uuuu	uuuu	*,*,*
12h	**SEG18**	SEG18[3]	SEG18[2]	SEG18[1]	SEG18[0]	uuuu	uuuu	*,*,*
13h	**SEG19**	SEG19[3]	SEG19[2]	SEG19[1]	SEG19[0]	uuuu	uuuu	*,*,*
14h	**SEG20**	SEG20[3]	SEG20[2]	SEG20[1]	SEG20[0]	uuuu	uuuu	*,*,*
15h	**SEG21**	SEG21[3]	SEG21[2]	SEG21[1]	SEG21[0]	uuuu	uuuu	*,*,*
16h	**SEG22**	SEG22[3]	SEG22[2]	SEG22[1]	SEG22[0]	uuuu	uuuu	*,*,*
17h	**SEG23**	SEG23[3]	SEG23[2]	SEG23[1]	SEG23[0]	uuuu	uuuu	*,*,*
18h	**SEG24**	SEG24[3]	SEG24[2]	SEG24[1]	SEG24[0]	uuuu	uuuu	*,*,*
19h	**SEG25**	SEG25[3]	SEG25[2]	SEG25[1]	SEG25[0]	uuuu	uuuu	*,*,*
1Ah	**SEG26**	SEG26[3]	SEG26[2]	SEG26[1]	SEG26[0]	uuuu	uuuu	*,*,*
1Bh	**SEG27**	SEG27[3]	SEG27[2]	SEG27[1]	SEG27[0]	uuuu	uuuu	*,*,*
1Ch	**SEG28**	SEG28[3]	SEG28[2]	SEG28[1]	SEG28[0]	uuuu	uuuu	*,*,*
1Dh	**SEG29**	SEG29[3]	SEG29[2]	SEG29[1]	SEG29[0]	uuuu	uuuu	*,*,*
1Eh	**SEG30**	SEG30[3]	SEG30[2]	SEG30[1]	SEG30[0]	uuuu	uuuu	*,*,*
1Fh	**SEG31**	SEG31[3]	SEG31[2]	SEG31[1]	SEG31[0]	uuuu	uuuu	*,*,*
20h	**SEG32**	SEG32[3]	SEG32[2]	SEG32[1]	SEG32[0]	uuuu	uuuu	*,*,*
21h	**SEG33**	SEG33[3]	SEG33[2]	SEG33[1]	SEG33[0]	uuuu	uuuu	*,*,*
22h	**SEG34**	SEG34[3]	SEG34[2]	SEG34[1]	SEG34[0]	uuuu	uuuu	*,*,*
23h	**SEG35**	SEG35[3]	SEG35[2]	SEG35[1]	SEG35[0]	uuuu	uuuu	*,*,*
Extend Control Register								
000h	**VLCD**	VLCD[3]	VLCD[2]	VLCD[1]	VLCD[0]	0000	uuuu	*,*,*
001h	**CTVR**	CTVR[3]	CTVR[2]	CTVR[1]	CTVR[0]	0000	uuuu	*,*,*
002h	**LCDM**					0000	0000	*,*,*
003h	**LCDM**			VLCDEN[1]	VLCDEN[0]	0000	00uu	*,*,*
004h	**TM**	IRQM	TMD[2]	TMD[1]	TMD[0]	0000	uuuu	*,*,*
005h	**TM**		TMEN[1]	TMEN[0]	TMCR[0]	0000	0uu$	*,*,*

Table 6 Table of RAM

5. ORDER PRECISE DESCRIPTION

D7（MSB）is command or data determination bit, users can refer to *Chapter 4.1 Commnunication Interface* for sending data in detailed description:

0：Next Byte (D7-D0) is the data to be written to RAM.

1：Next Byte is Order.

Input	DATA								描述
	D7	D6	D5	D4	D3	D2	D1	D0	
Mode Set	C	1	0	*	P3	P2	*	*	MODE SET
Address set	C	0	0	P4	P3	P2	P1	P0	ADSET
Display control	C	0	1	P4	P3	P2	P1	P0	DISCTL
Set IC Operarion	C	1	1	0	1	*	P1	P0	ICSET
Blink control	C	1	1	1	0	*	P1	P0	BLKCTL
All pixel control	C	1	1	1	1	1	P1	P0	APCTL
Extend Control	C	1	1	0	0	P2	P1	P0	EXCTL

Table 7 Display ON/OFF

5.1. Mode Set (MODE SET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	*	P3	P2	*	*

Figure 40 Mode Set Byte

P3：Setting display off or on

Setting	P3	Initial Value
Display off	0	○
Display on	1	

Table 8 Display ON/OFF

P2：Setting BIAS voltage

Setting	P2	Initial Value
1/3 BIAS	0	○
1/2 BIAS	1	

Table 9 bias Set

Display OFF：

Does not related to DDRAM contents. After 1FRAME OFF is written in, SEGMENT, COMMON output will stop. Display OFF will interrupt after Display on (DSPON).

Display ON：

SEGMENT, COMMON ouput becomes effective, reading action from DDRAM to LCD is activated.

According to Bias configurations of SEG/COM, for its output waveform pleaser refer to LCD drive waveform.

5.2. Address set (ADSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

Figure 41 Address Set Byte

Configuring address counter based on P[4:0] appointed address data, the configurable address ranges from 00000～10011 (execute Software Reset loading in ICSET command). Users must note not to set other values except the above one (or the address will be set as 0).

ICSET command only configure address MSB (’0’ or ’1’), note the address. ADSET command must be given when setting address.

When write in ICSET [P2]=0b to data, ADSET[P4:P0]=0Fh (SEG15) address, the address will automatically ascend 1 to be ICSET [P2]=0b, ADSET[P4:P0]=10h, making address ascends from 0Fh to 10h.

When write in ICSET [P2]=0b to data, ADSET[P4:P0]=1Fh (SEG31) address, the address will automatically ascend 1 to be ICSET [P2]=1b, ADSET[P4:P0]=00h, making address ascends from 1Fh to 20h.

When write in ICSET [P2]=1b to data, ADSET[P4:P0]=03h (SEG35) address, the addresswill automatically ascend from beginning, to be ICSET [P2]=0b, ADSET[P4:P0]=00h, making address from 23h to 00h.

If the previous address is 2xh (ICSET [P2]=1b), users must reset ICSET [P2] bit as 0 in order to return display address to 0xh when re-display data from 0xh(SEG0~SEG15) address. If the previous display address is 2xh (ICSET [P2]=1b), users must reset ICSET [P2] bit as 0 in order to return display address from 1xh (SEG16~SEG31).

5.3. Display control (DISCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Figure 42 Display Control Byte

P4, P3：Power Save Mode FR Configuration

Power save mode FR	P4	P3	Initial Value
Normal mode	0	0	○
Power save mode1	0	1	
Power save mode2	1	0	
Power save mode3	1	1	

Table 10 Power Save Mode FR

Operation current decreases in the following sequence: Normal mode＞Power save mode1＞Power save mode2＞Power save mode3.

P2：Configuring LCD Drive Waveform

Setting	P2	Initial Value
LINE inversion	0	○
FRAME inversion	1	

Table 11 Configure LCD Drive Waveform

Operation current: LINE Inversion>FRAME. For detailed LINE and FRAME Inversion driving methods, please refer to Chapter*4.3 LCD Driver (Bias Circuit and* Wave*.*

P1, P0：Configuring Power Save Mode

Power save mode SR	P1	P0	Initial Value
Power save mode1	0	0	
Power save mode2	0	1	
Normal mode	1	0	○
High Power mode	1	1	

Table 12 Configure LCD Drive Waveform

Operation current increases in the following sequence: Power save mode 1< Power save mode 2< Normal< High. Under *High Power Mode, please make sure that VDD-VLCD>=3.0V.

Current Consumption Reference Data

Power save mode SR	**Current Consumption**
Power save mode1	*0.5
Power save mode2	0.67
Normal mode	*1.0
High Power mode	*1.8

Table 13 Configure LCD Drive Waveform

Table 13 shows reference value of current consumption, the value changes accoring to PANEL loading.

(Note) Configurations of Power save mode FR, LCD Drive Waveform, Power Save Mode SR, have the following influences on display quality. Please select the best matched value according to LCD panel's current consumption and display quality.

Mode	Panel Tremble	Display Quality /Contrast
Power save mode FR	○	-
LCD Drive Waveform	○	○
Power save mode SR	-	○

Table 14 LCD Display Quality Table

5.4. Set IC Operation (ICSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	*	P1	P0

Figure 43 IC Operation Set Byte

P1：RESET Configuration

Configure	P1
Unexecuted Software Reset	0
Execute Software Reset	1

Table 15 Configure RESET

When executing Software Reset command, set HY2613 RESET as the initial status, please refer to *Chapte 4.9 Reset* Initialization Status

P0：Clock Source Configuration

OSC MODE	P0	Initial Value
Internal Oscillation Circuit	0	○
External Clock Signal Input	1	

Table 16 Configuration of Clock Source

When setting internal oscillation circuit, please short OSCIN pin and VSS level pin.

When setting external clock signal, inputting external signal from OSCIN pin.

Reference time sequence is as follows:

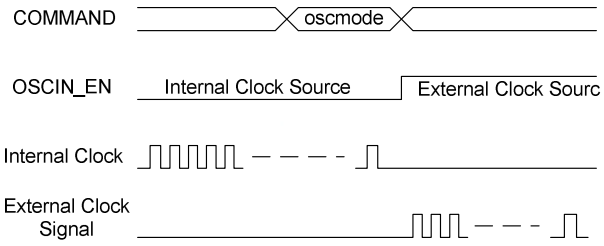


Figure 44 Clock Source Switching Sequence

P2：High bite address counter setup

ICSET [P2] only configures MSB ('0' or '1') bit, not the address. When setting address, users must input ADSET[P4:P0] command.

ICSET [P2]=0b, address setup as 00h~1Fh.

ICSET [P2]=1b, address setup as 20h~23h.

5.5. Blink Control (BLKCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	*	P1	P0

Figure 45 Blink Control Set Byte

P1, P0：Blink Setting

Blink Model (HZ)	P1	P0	Initial Value
OFF	0	0	○
0.5	0	1	
1	1	0	
2	1	1	

Table 17 Blink Configuration

5.6. ALL Pixel Control (APCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

Figure 46 Blink Control Set Byte

P1, P0: LCD Pixels ON and OFF Configuration

APON	P1	P0	Initial Value
Normal	0	0	○
All pixel OFF	0	1	
All pixel ON	1	0	
All pixel OFF	1	1	

Table 18 LCD Pixels ON and OFF Configuration

All pixels ON：Light up all pixels that do not relate to DDRAM contents.

All pixels OFF：Cancel all pixels that do not relate to DDRAM contents.

All pixels ON/OFF command is effective only when Display ON. DDRAM contents will not change under this status.

Note: Configuring P1, P0 as ‘1’, select APOFF first.

5.7. Extend Control (EXCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	0	P2	P1	P0

Figure 47 Extend Control Byte

P2：Setting LED back light function

Setting	P2	Initial Value
LED back light OFF	0	○
LED back light ON	1	

Table 19 LED back light function

Inactivating LED back light function

LED back light ON ：

Activating LED back light function, at this time, SEG32 to SEG35 switches to LED drive circuit automatically.

LED back light OFF：

P1：Reserved

Setting	P1	Initial Value
RTC OFF	0	○
Reserved	1	

Table 20

RTC OFF：

External 32KHz clock input.

System clock source control register, setting system clock source to determin f_{CLK} and TM clock source.

ICSET[P0]	EXCTL[P1]	System Clock Source	Remark
0	0	Using internal 32KHz LPO as clock source	External OSCIN input clock source is prohibited
1	0	Using external OSCIN pin to input 32KHz as clock source	
x	1	Reserved	

Table 21 Clock Source Select List

P0：Configure special register

Setting	P0	Initial Value	Remark
SROFF	0	○	Only POR event is valid
SRON	1		

Please refer Chapter 9

Table 22 Special Register

SROFF：

Inactivating special refsiter function

SRON：

Activating special refsiter function

Configuring P0 of EXCTL command as ”1” to read/write extend control register. Configured P0 as ”0” and the following extend registers is unable to read/write:

"u"：不變更,"-"：未使用,"*"：可讀/寫,"$"：0→1→0

位址	名稱	Bit 3	Bit 2	Bit 1	Bit 0	POR	non-POR	R/W
Extend Control Register								
000h	**VLCD**	VLCD[3]	VLCD[2]	VLCD[1]	VLCD[0]	0000	uuuu	*,*,*,*
001h	**CTVR**	CTVR[3]	CTVR[2]	CTVR[1]	CTVR[0]	0000	uuuu	*,*,*,*
002h	**LCDM**	ENBUF				0000	0000	*,*,*,*
003h	**LCDM**			VLCDEN[1]	VLCDEN[0]	0000	00uu	*,*,*,*
004h	**TM**	IRQM	TMD[2]	TMD[1]	TMD[0]	0000	uuuu	*,*,*,*
005h	**TM**		TMEN[1]	TMEN[0]	TMCR[0]	0000	0uu$	*,*,*,*

Table 23 Extend Control Register

5.7.1. Extend Control Register Description

➢ VLCD[3:0]

Internal Charge pump output control register can configure VLCD output voltage. When power is floating, VLCD output can keep at configured voltage to prevent LCD display from contrast insufficiency. When starting VLCD internal charge pump output, it must conform to voltage operation range, VDD <= VLCD <= 1.5*VDD.

VLCD[3:0]	VLCD Output Voltage	VLCD[3:0]	VLCD Output Voltage	VLCD[3:0]	VLCD Output Voltage	VLCD[3:0]	VLCD Output Voltage
0000	4.5V	0100	4.1V	1000	3.7V	1100	3.3V
0001	4.4V	0101	4.0V	1001	3.6V	1101	3.2V
0010	4.3V	0110	3.9V	1010	3.5V	1110	3.1V
0011	4.2V	0111	3.8V	1011	3.4V	1111	3.0V

Table 24 HY2613A/HY2613C VLCD Output Voltage Controller List

➢ CTVR[3:0]

Internal constrast control register can adjust LCD display contrast for the best display effect.

CTVR[3:0]	LCD Driver Voltage	CTVR[3:0]	LCD Driver Voltage	CTVR[3:0]	LCD Driver Voltage	CTVR[3:0]	LCD Driver Voltage
0000	1*VLCD	0100	0.849*VLCD	1000	0.738*VLCD	1100	0.652*VLCD
0001	0.957*VLCD	0101	0.818*VLCD	1001	0.714*VLCD	1101	0.634*VLCD
0010	0.918*VLCD	0110	0.789*VLCD	1010	0.692*VLCD	1110	0.616*VLCD
0011	0.882*VLCD	0111	0.763*VLCD	1011	0.672*VLCD	1111	0.600*VLCD

Table 25 HY2613A/HY2613C LCD 1/3 Bias Contrast Adjusting Controller List

➢ VLCDEN[1:0]

VLCD power drive controller can select VLCD disposition to satisfy different applications.

VLCDEN[1:0]	VLCD Power Driver control option	Remark
00	VLCD connects to VSS	Adopting Low Side connection way Only applicable to HY2613B product
01	VLCD connects to VDD	Adopting High Side connection way Only applicable to HY2613A/HY2613C product
10	VLCD voltage supplies by internal charge pump circuit	Adopting internal charge pump circuit, High Side connection way Only applicable to HY2613A/HY2613C product
11	VLCD voltage supplies by internal charge pump circuit	Adopting internal charge pump circuit, High Side connection way Only applicable to HY2613A/HY2613C product

Table 26 VLCD Power Drive Control List

➢ ENBUF

VLCD Buffer enable bit, applicable for HY2613A/HY2613C.

When starting CTVR internal contrast control function, VLCD Buffer must be initiated compulsively.

ENBUF=0b, close VLCD Buffer.

ENBUF=1b, start VLCD Buffer.

➢ TMD[2:0]

Counter frequency divider control register, which can configure counter output frequency.

TMD[2:0]	Timer Clock Source	OSC=32.768KHz		TMD[2:0]	Timer Clock Source	OSC=32.768KHz	
000	OSC_CK÷2	32Hz	31.25ms	100	OSC_CK÷32	2Hz	500ms
001	OSC_CK÷4	16Hz	62.5ms	101	OSC_CK÷64	1Hz	1000ms
010	OSC_CK÷8	8Hz	125ms	110	OSC_CK÷128	0.5Hz	2000ms
011	OSC_CK÷16	4Hz	250ms	111	OSC_CK÷256	0.25Hz	4000ms

Table 27 System Clock 32.768KHz Counter Output Frequency List

TMD[2:0]	Timer Clock Source	OSC=32KHz		TMD[2:0]	Timer Clock Source	OSC=32KHz	
000	OSC_CK÷2	31.25Hz	32ms	100	OSC_CK÷32	1.95Hz	512ms
001	OSC_CK÷4	15.62Hz	64ms	101	OSC_CK÷64	0.97Hz	1024ms
010	OSC_CK÷8	7.81Hz	128ms	110	OSC_CK÷128	0.48Hz	2048ms
011	OSC_CK÷16	3.90Hz	256ms	111	OSC_CK÷256	0.24Hz	4096ms

Table 28 System Clock 32KHz Counter Output Frequency List

➢ TMEN[1:0]

Counter enable and mode control register, which can enable counter and select output mode. Users must note that theory graph must be designed well when using HY2613A/HY2613C external pin, IRQ.

TMEN[1:0]	Counter Mode Control	Remark
00	Counter prohibited	IRQ pin is high impedance
01	Enable counter and set as Timer Base output	IRQ pin output as CMOS buffer, Duty Cycle 50%
10	Enable counter and set as NMI pulse high potential output	IRQ pin output as CMOS buffer, Pulse wide as 32us
11	Enable counter and set as NMI pulse low potential output	IRQ pin output as Open-drain buffer, Pulse wide as 32us

Table 29 Counter Output Mode List (HY2613A/HY2613C only)

➢ TMCR[0]

Counter zero control register.

TMCR[0]	Counter Zero Control	Remark
0	Normal counting status	Zero when switch on, entry into normal counting mode

		after switch on.
1	Counter Zero	Write in“1” to clear zero of counter, then set as “0” automatically.

Table 3031 Counter Output Mode List (HY2613A/HY2613C only)

6. DISPLAY DATA EXAMPLE

As shown in Table 27, LCD panel will show as Figure 51 after data written to DDRAM.

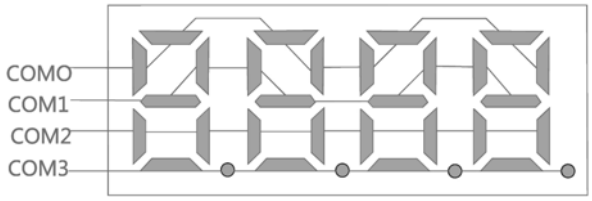


Figure 48 COM End Bitmap

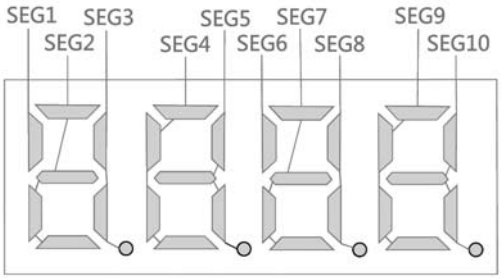


Figure 49 SEG End Bitmap

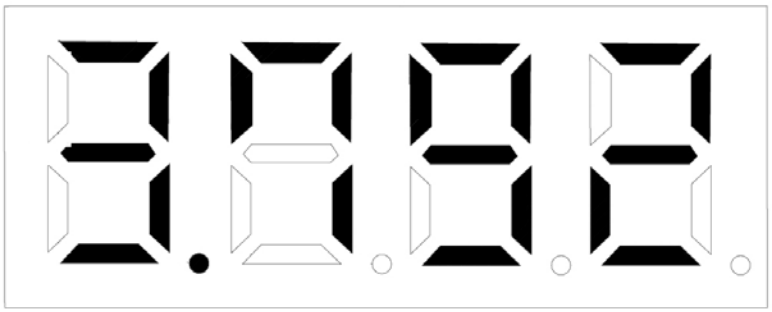


Figure 49 Display Example “3.792”

		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19
COM0	D0	0	0	1	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0
COM1	D1	0	0	1	1	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
COM2	D2	0	0	0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
COM3	D3	0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
Address		00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	10h	11h	12h	13h	14h	15h	16h	17h	18h	19h

Table 32 DDRAM Data Map

7. CHIP OPERATION DESCRIPTION

The operation way is illustrated as the flow chart. Detailed operation of each function is given in the following chapters. The adjusting flow of display also depicted in this chapter.

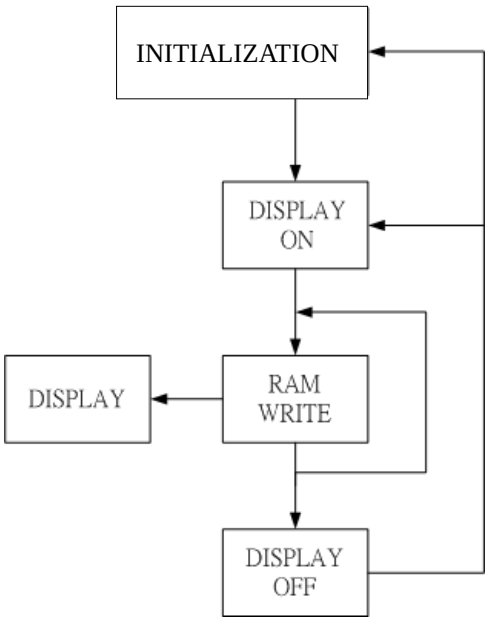


Figure 50 Flow of Chip Operation

NO.	Input	DATA								Decrisption
		D7	D6	D5	D4	D3	D2	D1	D0	
1	POWER ON									VDD=0→5V（Tr=0.1ms）
	↓									
2	wait 100us									Chip initiation
	↓									
3	STOP									Stop condition
	↓									
4	START									Start condition
	↓									
5	Slave address	0	1	1	1	1	1	0	0	Send Slave address
	↓									
6	ICSET	1	1	1	0	1	*	1	0	Software reset
	↓									
7	BLKCTL	1	1	1	1	0	*	0	0	No need initiation
	↓									
8	DISCTL	1	0	1	0	0	0	1	0	No need initiation
	↓									
9	ICSET	1	1	1	0	1	*	0	1	Set MSB of RAM address

	↓									
10	ADSET	0	0	0	0	0	0	0	0	Set RAM address
	↓									
	Display data	*	*	*	*	*	*	*	*	Address 00h~01h
11	……									
	Display data	*	*	*	*	*	*	*	*	Address 22h~23h
	↓									
12	Stop									Stop condition
	↓									
13	Start									Start condition
	↓									
14	Slave address	0	1	1	1	1	1	0	0	Send Slave address
	↓									
15	MODESET	1	1	0	*	1	0	*	*	Display ON
	↓									
16	Stop									Stop condition

Table 33 Operate Flow Chart

7.1. Initiation

Input	**DATA**								**Description**
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
POWER ON									
Wait for 100us									
STOP									
START									
Slave address	0	1	1	1	1	1	0	0	
ICSET	1	1	1	0	1	0	1	0	Software reset
DISCTL	1	0	1	1	1	1	1	1	Set Display Control
ADSET	0	0	0	0	0	0	0	0	Set RAM address
Display data	*	*	*	*	*	*	*	*	Display data
⋮ ⋮									
Stop									

Table 34 Initiation Flow

7.2. Enable Display

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	
DISCTL	1	0	1	1	1	1	1	1	Set Display Control
BLKCTL	1	1	1	1	0	0	0	0	Set BLKCTL
APCTL	1	1	1	1	1	1	0	0	Set APCTL
MODESET	1	1	0	0	1	0	0	0	Enable display
Stop									

Table 35 Flow of Enabling Display

7.3. RAM Write-in Display

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	
DISCTL	1	0	1	1	1	1	1	1	Set Display Control
BLKCTL	1	1	1	1	0	0	0	0	Set BLKCTL
APCTL	1	1	1	1	1	1	0	0	Set APCTL
MODESET	1	1	0	0	1	0	0	0	Enable display
ADSET	0	0	0	0	0	0	0	0	Set RAM address
Display data	*	*	*	*	*	*	*	*	Display write in data
⋮ ⋮									
Stop									

Table 36 RAM Write-in Flow

7.4. Disable Display

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
START									
Slave address	0	1	1	1	1	1	0	0	
MODESET	1	1	0	0	0	0	0	0	Enable display
Stop									

Table 37 Flow of Disabling Display

7.5. Adjust Display

Display quality can be adjusting through DISCTL command. Please refer to the flow in below when adjusting diaply and determining parameter.

Figure 51 Flow of Adjusting Display

8. ELECTRICAL CHARACTERISTICS

Absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Voltage applied at V_{DD} to V_{SS} . . . . . −0.5 V to 7.0 V

Voltage applied to any pin . . . . . −0.5 V to V_{DD} + 0.5 V

Diode current at any device terminal . . . . . ±2 mA

Storage temperature, Tstg: (unprogrammed device) . . . . . −55℃ to 150℃

(programmed device) . . . . . −40℃ to 85℃

Total power dissipation at 25℃ 6mW

8.1. Recommended Operating Conditions

T_A = -40℃～85℃,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{DD}	Supply Voltage		2.4		5.5	V
VLCD	LCD Supply Voltage		2.4		5.5	
V_{SS}	Supply Voltage		0		0	

8.2. Internal LPO Oscillator

T_A = 25℃,V_{DD} = 2.4V ～ 5.5V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
f_{CLK}	Frame Frequency	V_{DD} = 2.2V ～ 5.5V,1/4 duty mode		80		Hz
LPO	Internal RC	V_{DD} =3.3V		33		KHz

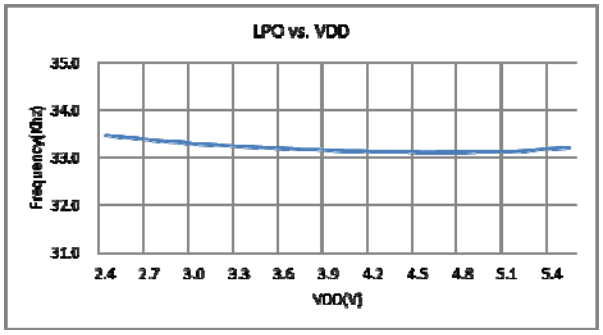


Figure 53 LPO vs. VDD

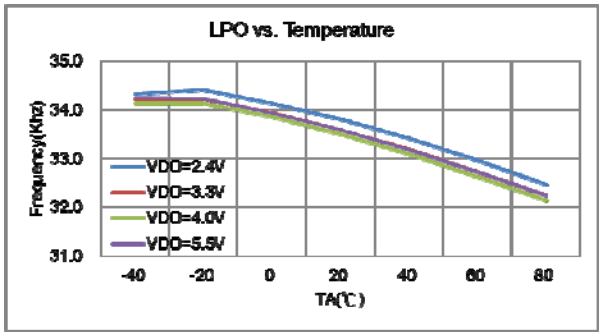


Figure 54 LPO vs. Temperature

8.3. Supply Current into VDD excluding Peripherals Current

T_A = 25℃,V_{DD} = 2.4V ～ 5.5V,OSC_LPO = 33KHz,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
I_{AM1}	Active mode 1	OSC_LPO = 33khz, VDD=3.3V, Ta=25℃, Power save mode SR=Power save mode1, Power save mode FR=Power save mode3 1/3bias,1/4duty, Frame Inversion.		7.5	11.5	uA
I_{AM2}	Active mode 2	OSC_LPO = 33khz, VDD=3.3V, Ta=25℃, Power save mode SR=Power save mode1, Power save mode FR=Normal mode 1/3bias,1/4duty, Frame Inversion.		7.5	11.5	uA
I_{AM3}	Active mode 3	OSC_LPO = 33khz, VDD=3.3V, Ta=25℃, Power save mode SR=Power save mode1, Power save mode FR=Power save mode3 1/3bias,1/4duty, Line Inversion.		11	15	uA
I_{AM4}	Active mode 4	OSC_LPO = 33khz, VDD=3.3V, Ta=25℃, Power save mode SR=Power save mode1, Power save mode FR=Normal mode 1/3bias,1/4duty, Line Inversion.		11	15	uA
I_{LP1}	Low Power 1	Display Off, Standby mode		0.5	1	uA

OSC_LPO：Internal High Accuracy Oscillator frequency.

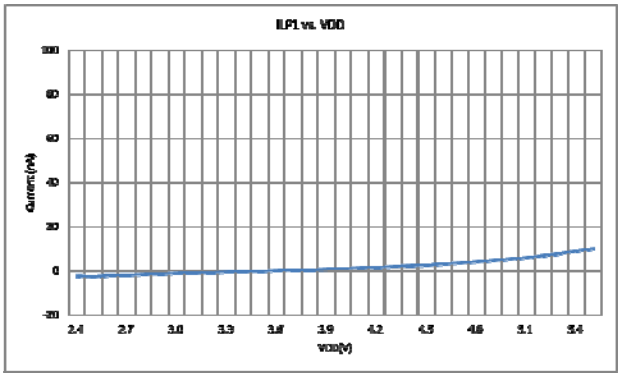


Figure 55 I_{LP1} vs. VDD

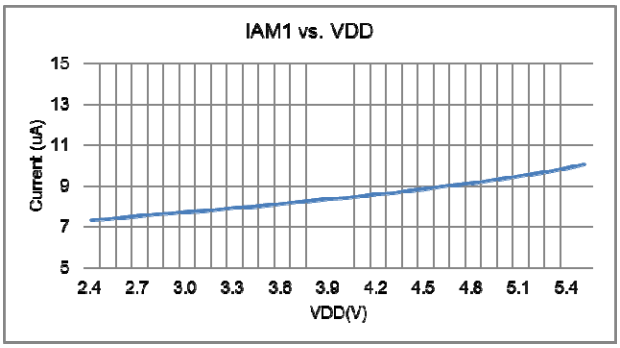


Figure 56 I_{AM1} vs. VDD

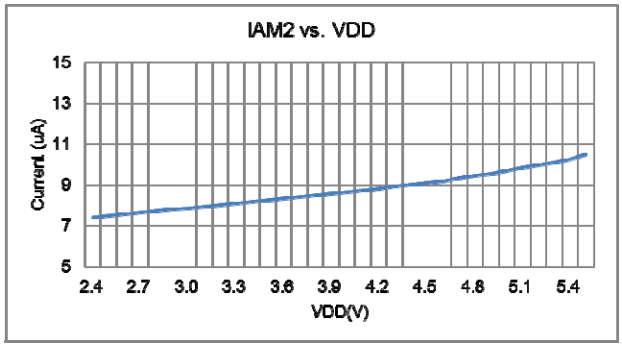


Figure 57 I_{AM2} vs. VDD

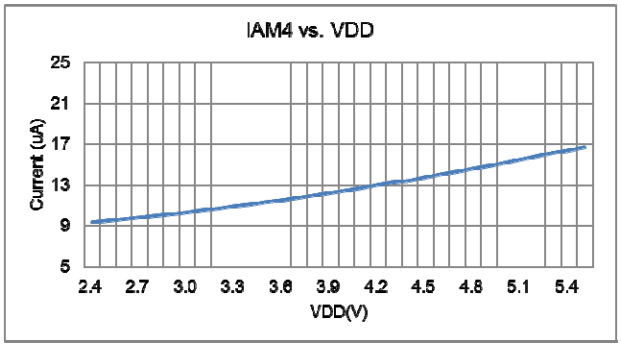


Figure 58 I_{AM4} vs. VDD

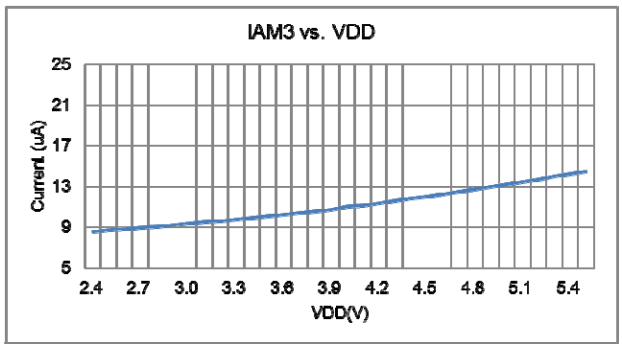


Figure 59 I_{AM3} vs. VDD

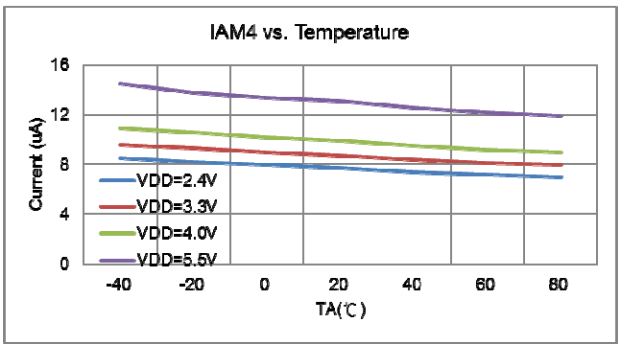


Figure 60 I_{AM4} vs. Temperature

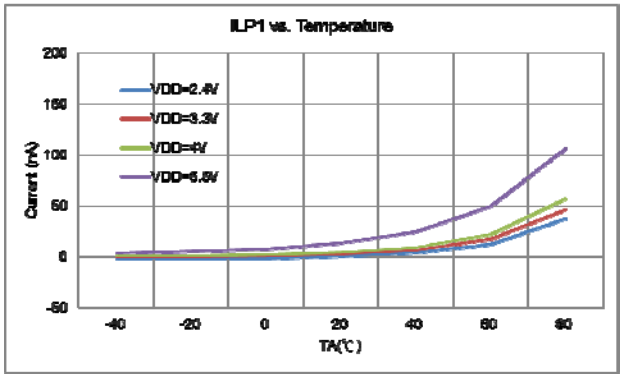


Figure 61 I_{LP1} vs. Temperature

8.4. LED Driver

T_A = 25℃,V_{DD} = 2.4V ～ BLOUT+0.2V, ENLED[0]=1b , -40℃<T_A<85℃, unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
V_{IN}	V_{DD} Supply Voltage		2.4		V_{BL} +0.2	V
V_{BL}	backlight voltage	C_{BL}=10uF,C_{HL}=1uF,V_{DD}=3V, I_{LED}≦15mA		3.3		V
I_{LED}	drive current	RL=13Ω			15	mA
V_{FB}	Feedback Reference Voltage			0.2		V

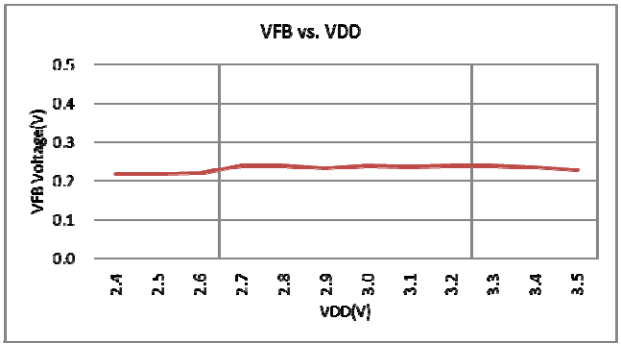


Figure 62 V_{FB} vs. VDD

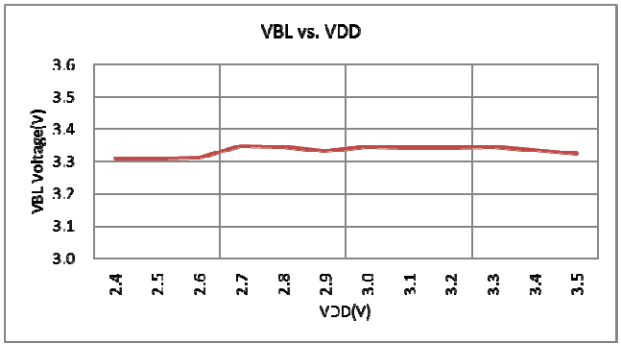


Figure 63 V_{BL} vs. VDD

8.5. LCD

T_A = 25℃,V_{DD} = 2.4V ～ 5.5V,unless otherwise noted

Sym.	Parameter	Test Conditions		Min.	Typ.	Max.	unit
V_{VLCD}	V_{DD} Supply Voltage			2.4		5.5	V
	VLCD Supply Voltage					V_{DD}	V
I_{NORM1}	Operation supply current with chip at VDD=2.4V	Function enable about LPO,POR,VLCD(charge pump), without LCD panel			12		uA
I_{NORM2}	Operation supply current with chip at VDD=3.3V	Function enable about LPO,POR,VLCD(charge pump), without LCD panel			22		uA
VLCD1	Embedded Charge Pump output voltage at VLCD pin	VDD=3.3V, VLCDEN=1xb C_{VLCD}=1.0uF	VLCD[3:0]=1111b		3.0		V
			VLCD[3:0]=1110b		3.1		V
			VLCD[3:0]=1101b		3.2		V
			VLCD[3:0]=1100b		3.3		V
			VLCD[3:0]=1011b		3.4		V
			VLCD[3:0]=1010b		3.5		V
			VLCD[3:0]=1001b		3.6		V
			VLCD[3:0]=1000b		3.7		V
			VLCD[3:0]=0111b		3.8		V
			VLCD[3:0]=0110b		3.9		V
			VLCD[3:0]=0101b		4.0		V
			VLCD[3:0]=0100b		4.1		V
			VLCD[3:0]=0011b		4.2		V
			VLCD[3:0]=0010b		4.3		V
			VLCD[3:0]=0001b		4.4		V
			VLCD[3:0]=0000b		4.5		V
VLCD2	External Supply Voltage at VLCD pin	VLCDEN=01b			V_{DD}	5.5	V
	Built-in contrast to adjust the controller, 1/3bias	VLCD = 5.0V as V3 Voltage.	CTVR[3:0]=1111b		3.000		V
			CTVR [3:0]=1110b		3.080		V
			CTVR [3:0]=1101b		3.170		V
			CTVR [3:0]=1100b		3.260		V
			CTVR [3:0]=1011b		3.360		V
			CTVR [3:0]=1010b		3.460		V
			CTVR [3:0]=1001b		3.570		V
			CTVR [3:0]=1000b		3.690		V

			CTVR [3:0]=0111b	3.815	V
			CTVR [3:0]=0110b	3.945	V
			CTVR [3:0]=0101b	4.090	V
			CTVR [3:0]=0100b	4.245	V
			CTVR [3:0]=0011b	4.410	V
			CTVR [3:0]=0010b	4.590	V
			CTVR [3:0]=0001b	4.785	V
			CTVR [3:0]=0000b	5.000	V
Z_{LCD}	Output impedance with LCD buffer	f_{CLK}=80Hz,VLCD=4.5V		5	kΩ

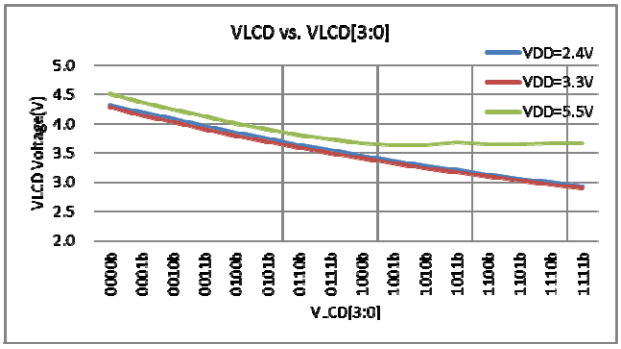


Figure 64 VLCD vs. VDD

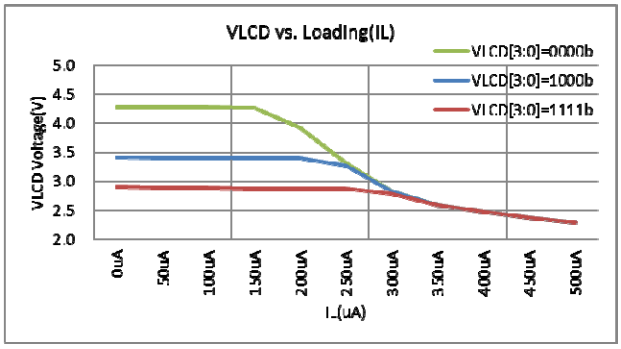


Figure 65 VLCD vs. VLCD Loading

8.6. I^2C

T_A = 25℃,V_{DD} = 3.0V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
f_{SCL}	SCL Clock Frequency(Note 1)		0		400	Khz
t_F	Fall Time of Both SDA and SCL Signals				0.3	us
$t_{HD;STA}$	Hold Time (Repeated) START Condition		0.6			us
t_{LOW}	Low Period of SCL Clock		1.3			us
t_{HIGH}	High Period of SCL Clock		0.6			us
t_R	Rise Time of Both SDA and SCL Signals				0.3	us
$t_{HD:DAT}$	Data Hold Time(Note 2, Note 3)		100			us
$t_{SU:DAT}$	Data Setup Time		100			us
$t_{SU;STA}$	Setup Time for a Repeated START Condition		0.6			us
t_{SP}	Spike Pulse Widths Suppressed by Input Filter (Note 4)		0		50	ns
$t_{SU:STO}$	Setup Time for STOP Condition		0.6			us
t_{BUF}	Bus Free Time Between a STOP and START Condition		1.3			us
C_B	Capacitive Load for Each Bus Line(Note 5)				400	pF
C_{BIN}	SCL, SDA Input Capacitance				60	pF

Note 1: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

Note 2: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

Note 3: This device internally provides a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 4: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

Note 5: C_b – total capacitance of one bus line in pF.

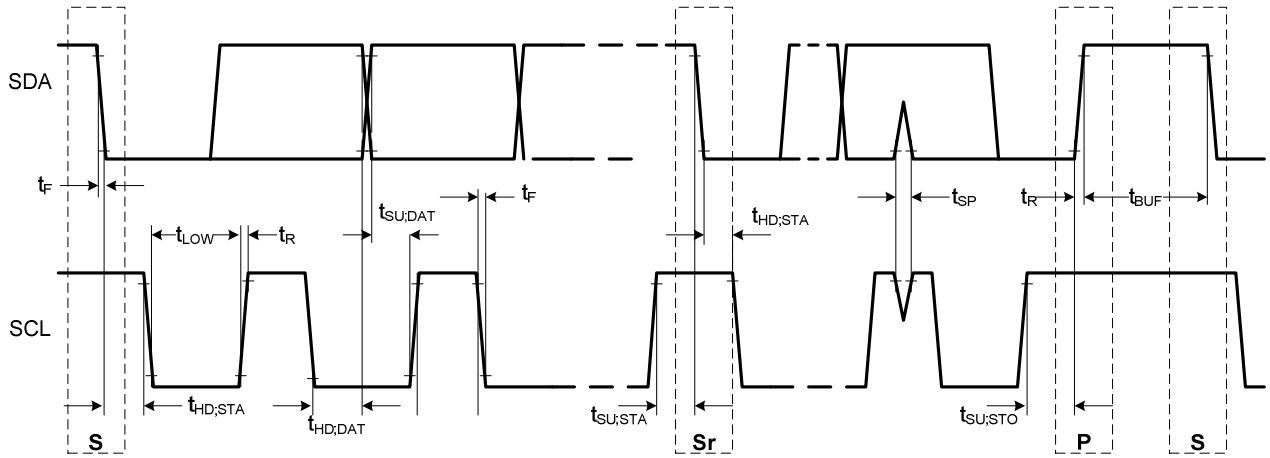


Figure 6652 I^2C Bus Timing Diagram

8.7. Reset (Brownout)

T_A = 25℃,V_{DD} = 3.3V,unless otherwise noted

Sym.	Parameter	Test Conditions	Min.	Typ.	Max.	unit
POR	Power voltage increase delay time (TR)				1	msec
	Power voltage decrease delay time (TF)				1	msec
	Chip Reset time (TOFF)		100			msec
	Chip power on stable delay time (Tdelay)				5	msec
	Chip Reset voltage (VBOT)				0.1	V

POR: Power on Reset

8.7.1. Power on Protection Description

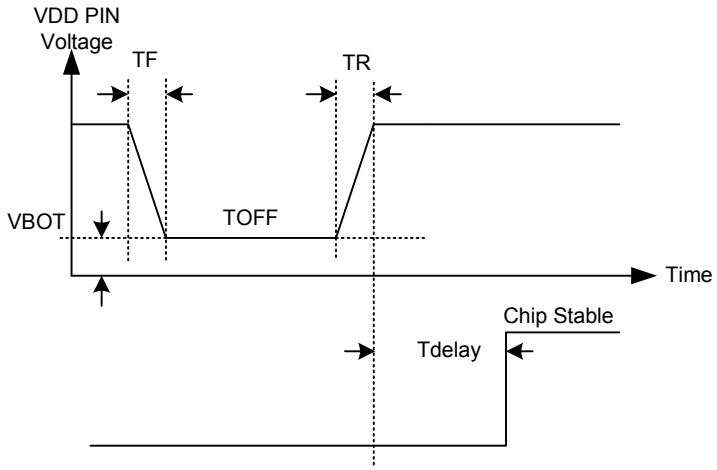
During power voltage increasing process, internal circuit and RESET circuit will stay in unstable low voltage area for certain of time, which may result in incomplete internal RESET of the chip. To strengthen hardware POR (Power-on-reset) circuit and to have effective software RESET control function, help to prevent the above mentioned situation. It is suggested to satisfy the following conditions when powering on:

1. For POR circuit to operate normally, please control the following conditions when powering on:

   Matching TR<1msec, TF<1msec, TOFF>100msec, VBOT<0.1V conditions.

   From power on to stable POR, TPOR>5msec.

   Note: When POR circuit is effective, POR pin must be placed in low potential.



2. If the above power on conditions were dissatisfied, the following countermeasures must be taken:

   In order to have ineffective POR circuit, POR pin must be placed in high potential.

9. Ordering Information

Device No.[1]	Package Type	Pins	Package Drawing		Shipment Packing Type	Unit Q'ty	Material Composition	MSL[2]
HY2613A-T048	TSSOP	48	T	048	Tube	38	Green	MSL-3
HY2613A-T048	TSSOP	48	T	048	Tape & Reel	2500	Green	MSL-3
HY2613A-L048	LQFP	48	L	048	Tray	250	Green	MSL-3
HY2613B-T048	TSSOP	48	T	048	Tube	38	Green	MSL-3
HY2613B-T048	TSSOP	48	T	048	Tape & Reel	2500	Green	MSL-3
HY2613B-L048	LQFP	48	L	048	Tray	250	Green	MSL-3
HY2613C-T048	TSSOP	48	T	048	Tube	38	Green	MSL-3
HY2613C-T048	TSSOP	48	T	048	Tape & Reel	2500	Green	MSL-3
HY2613C-L048	LQFP	48	L	048	Tray	250	Green	MSL-3

[1] **Device No.: Model No. – Package Type Description – Code** (Blank Code/ Standard/ Customized Programming Code)

Ex: You request HY2613A in TSSOP48 package and shipment packing type is Tube. The device number will be HY2613A-T048. And please clearly indicate the shipment packing type (Tube) when placing orders.

Ex: You request HY2613B in LQFP48 package and shipment packing type is Tray. The device number will be HY2613B-L048. And please clearly indicate the shipment packing type (Tray) when placing orders.

[2] **MSL:**

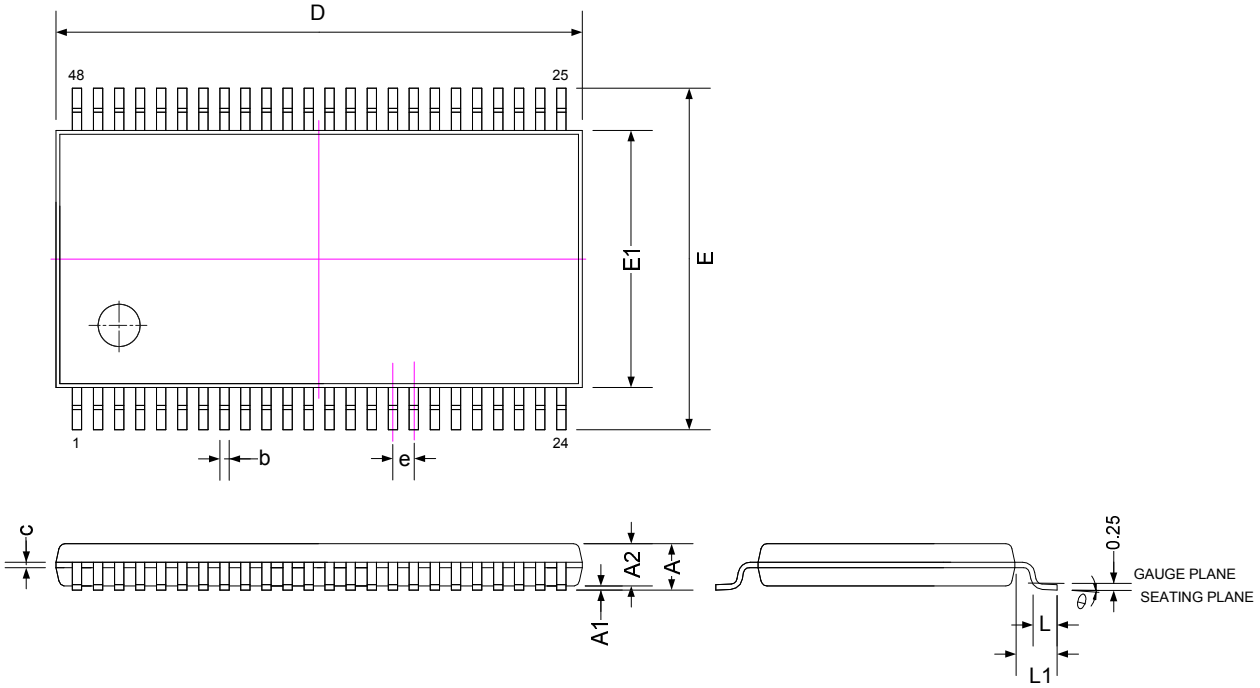
The Moisture Sensitivity Level ranking conforms to IPC/JEDEC J-STD-020 industry standard categorization. The products are processed, packed, transported and used with reference to IPC/JEDEC J-STD-033.

[3] **Green (RoHS & no Cl/Br):**

HYCON products are Green products that compliant with RoHS directive and are Halogen free (Br/Cl<0.1%).

10. Package Information

10.1. TSSOP48 (T048)

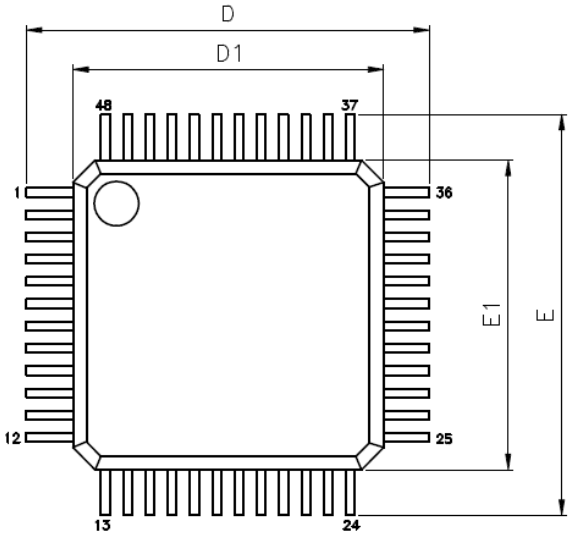


SYMBOLS	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.17	-	0.27
c	0.09	-	0.20
D	12.40	12.50	12.60
E1	6.00	6.10	6.20
E	8.10 BSC.		
L	0.45	0.60	0.75
L1	1.0 REF.		
e	0.50 BSC.		
θ°	0	-	8

Note:

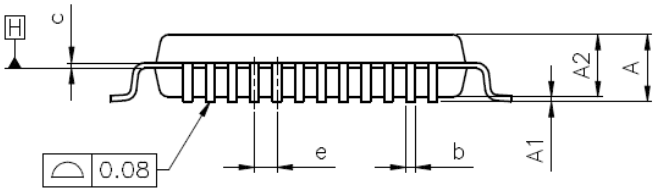
1. All dimensions refer to JEDEC OUTLINE MO-153.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm

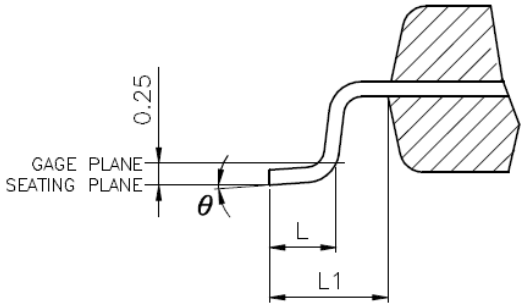
10.2. LQFP48 (L048)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°





Note:

1. All dimensions refer to JEDEC OUTLINE MS-026.
2. Do not include Mold Flash or Protrusions.
3. Unit: mm

11. Revision Record

Major differences are stated thereinafter:

Version	Page	Revision Summary
V05	All	First edition
V06	All	Circuit amendment
		Address description
		IRQ/NMI description