HYUNDAI

HY5117100A Series

16M x 1-bit CMOS DRAM

DESCRIPTION

The HY5117100A is the new generation and fast dynamic RAM organized 16,777,216 x 1-bit. The HY5117100A utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5117100A to be packaged in standard 24/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.
The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5 V±10% tolerence and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**
  Max. battery back-up 2.75mW (SL-part)
  Max. CMOS standby 2.2mW (SL-part)
  5.5mW
  Max. TTL standby 11.0mW
  Max. operating

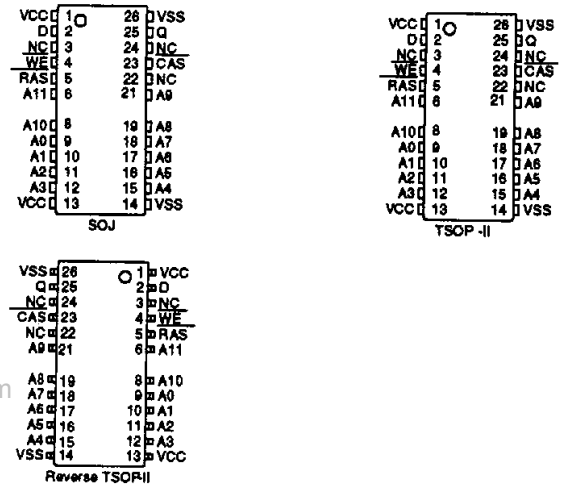
Speed	Power
50	798mW
60	660mW
70	550mW

- **Single power supply of 5V±10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

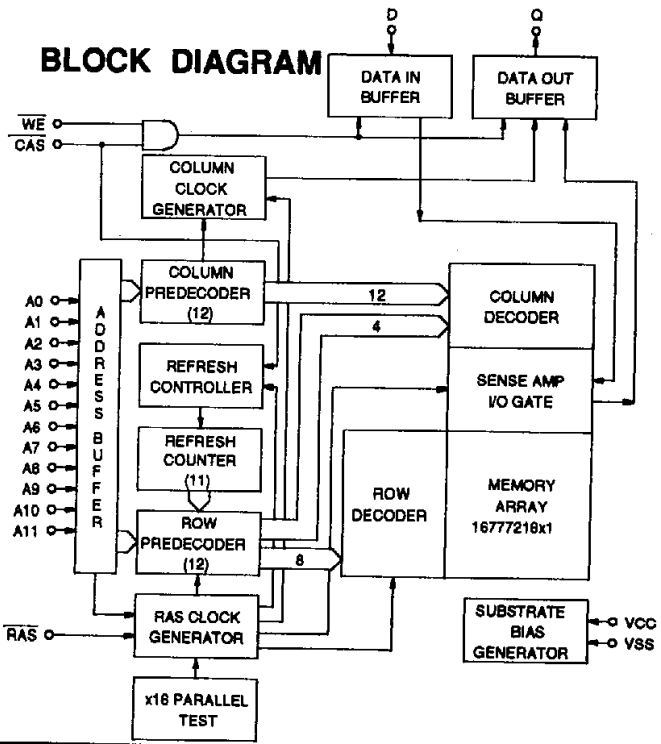
Speed	tRAC	tCAC	tPC
50	50ns	13ns	35ns
60	60ns	15ns	40ns
70	70ns	18ns	45ns

- **Fast page mode operation**
- **Multi-bit test capability**
- **Read-Modify-Write capability**
- **CAS-before-RAS, RAS-only, Hidden refresh and Self Refresh**
- **2048 refresh cycles / 256ms (SL-part)**
- **2048 refresh cycles / 32ms**

PIN CONNECTION



BLOCK DIAGRAM



PIN DESCRIPTION

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0-A11	Address Input
D	Data Input
Q	Data Output
Vcc	Power (+5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.02	W
T_{SOLDER}	Soldering Temperature• Time	260• 10	°C• sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+ 1.0	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS} \le V_{IN} \le V_{CC}+1.0$, All other pins not under test=V_{SS}		-10	10	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	V_{CC} Supply Current, Operating	$t_{RC}=t_{RC}$ (min.)	50 60 70	- - -	145 120 100	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}(min.), other inputs ≥ V_{SS}		-	2	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	$t_{RC}=t_{RC}$ (min.),	50 60 70	- - -	145 120 100	mA	1,3
I_{CC4}	V_{CC} Supply Current, Fast Page mode	$t_{PC}=t_{PC}$ (min.),	50 60 70	- - -	90 80 70	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ V_{CC} - 0.2V	 SL-part	- -	1 0.4	mA	 5
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$t_{RC}=t_{RC}$ (min.),	50 60 70	- - -	145 120 100	mA	1,3
I_{CC7}	V_{CC} Supply Current, Battery Back Up (SL-part only)	t_{RC}=125µs, $\overline{CAS}$=CBR cycling or 0.2V, $\overline{WE}$=V_{CC}-0.2V, A0-A11=V_{CC}-0.2V or 0.2V, D=V_{CC} - 0.2V, 0.2V or open, Q=open	t_{RAS}≤ 300ns	-	300	µA	1,4,5
			t_{RAS}≤ 1µs	-	500		
I_{CC8}	V_{CC} Supply Current Self Refresh (SL-part only)	$\overline{RAS}$ & $\overline{CAS}$ ≤0.2V $\overline{WE}$ & A0-A11=V_{CC}-0.2V or 0.2V, D=V_{CC} - 0.2V, 0.2V or open, Q=open			300	µA	5
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=-5mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while $\overline{RAS}$=V_{IL} and $\overline{CAS}$=V_{IH}.
4. t_{RAS}(max.)=1µs is only applied to refresh of battery backup but t_{RAS}(max.)=10µs is applied to normal functional operating.
5. I_{CC5}(max.)=0.4mA and I_{CC7} and I_{CC8} are applied to SL-part only (HY5117100ASLJ, HY5117100ASLT and HY5117100ASLR).

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HY5117100AJC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	110	-	130	-	155	-	ns	
3	tPC	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	55	-	60	-	70	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	50	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	13	-	15	-	18	ns	4,9
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	30	-	35	-	40	ns	4
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	10	0	13	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	13	-	15	-	18	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	50	-	60	-	70	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	13	10K	15	10K	18	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	13	37	20	45	20	52	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	13	25	15	30	15	35	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	10	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	45	-	50	-	55	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	8	-	10	-	10	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	50	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	8	-	10	-	10	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	13	-	15	-	18	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	13	-	15	-	18	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	12
		SL-part	-	256	-	256	-	256		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY5117100AJC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	13	-	15	-	18	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	50	-	60	-	70	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	25	-	30	-	35	-	ns	8
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	15	-	15	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	15	-	20	-	25	-	ns	
48	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	30	-	35	-	40	-	ns	8
49	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	-	35	-	40	-	ns	
50	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
51	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
52	tWTS	Write Command Set-up Time (Test Mode In)	10	-	10	-	10	-	ns	
53	tWTH	Write Command Hold Time (Test Mode In)	10	-	10	-	10	-	ns	
54	tRASS	$\overline{RAS}$ Pulse Width (Self Refresh)	100	-	100	-	100	-	µs	
55	tRPS	$\overline{RAS}$ Pre charge Time (Self Refresh)	120	-	130	-	150	-	ns	
56	tCHS	$\overline{CAS}$ Hold Time from $\overline{RAS}$ (Self Refresh)	-50	-	-50	-	-50	-	ns	

AC CHARACTERISTICS IN TEST MODE NOTE 13

#	SYMBOL	PARAMETER	HY5117100AJ/T/R/SLJ/SLT/SLR/						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	95	-	115	-	135	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	115	-	135	-	160	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	60	-	65	-	75	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	55	-	65	-	75	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	18	-	20	-	23	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	4
13	tRAS	$\overline{RAS}$ Pulse Width	55	10K	65	10K	75	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	55	200K	65	200K	75	200K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	18	-	20	-	23	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	55	-	65	-	75	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	18	10K	20	10K	23	10K	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	18	-	20	-	23	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	55	-	65	-	75	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	30	-	35	-	40	-	ns	8

NOTE :

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operation is achieved.
2. If $\overline{RAS}$=Vss during power-up, the HY5117100A could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min.) and V_{IL}(max.), and are assumed to be 5ns for all inputs.
4. Measured at V_{OH}=2.4V and V_{OL}=0.4V with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) and t_{OEZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS}≥t_{WCS}(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If t_{RWD}≥t_{RWD}(min.), t_{CWD}≥t_{CWD}(min.), t_{AWD}≥t_{AWD}(min.), and t_{CPWD}≥t_{CPWD}(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. t_{REF}(max.)=256ms is applied to SL-Parts (HY5117100ASLJ, HY5117100ASLT and HY5117100ASLR).
12. A burst of 2048 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 32ms(256ms for SL-part) after exiting self refresh.
13. These specifications are applied to the test Mode.

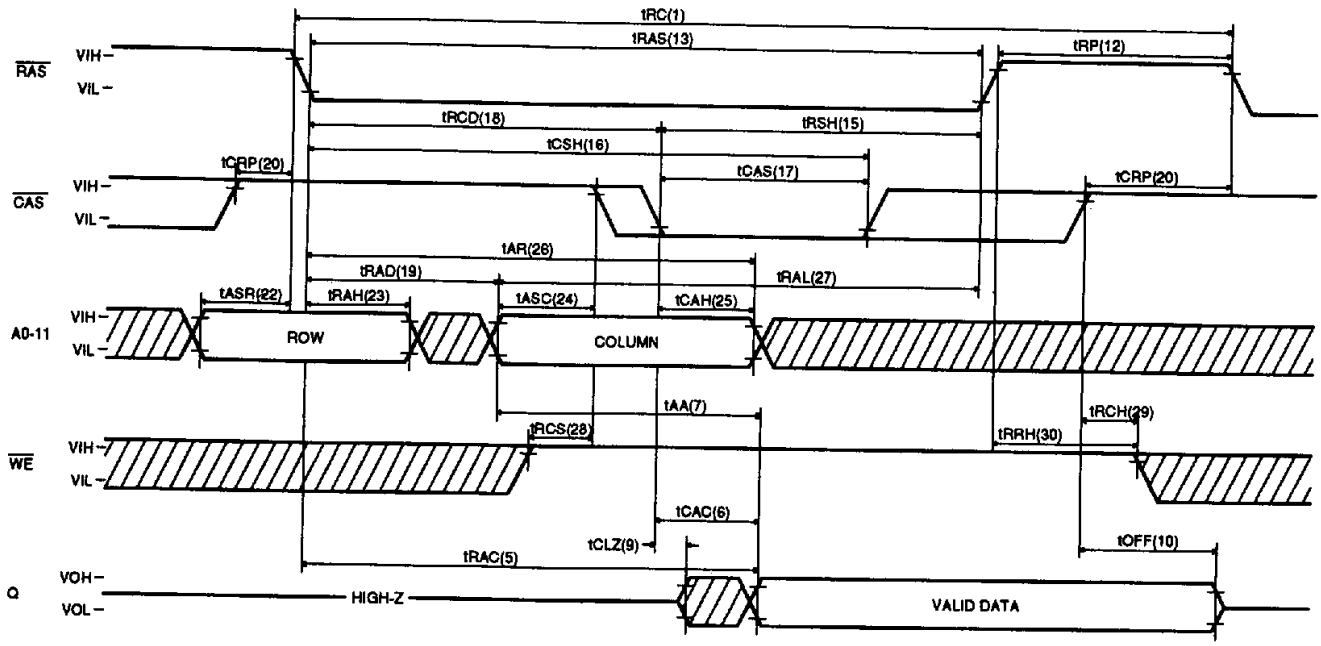
CAPACITANCE

(T_A=25°C, V_{CC}=5V 10%, V_{SS}=0V, f=1MHz, unless otherwise noted.)

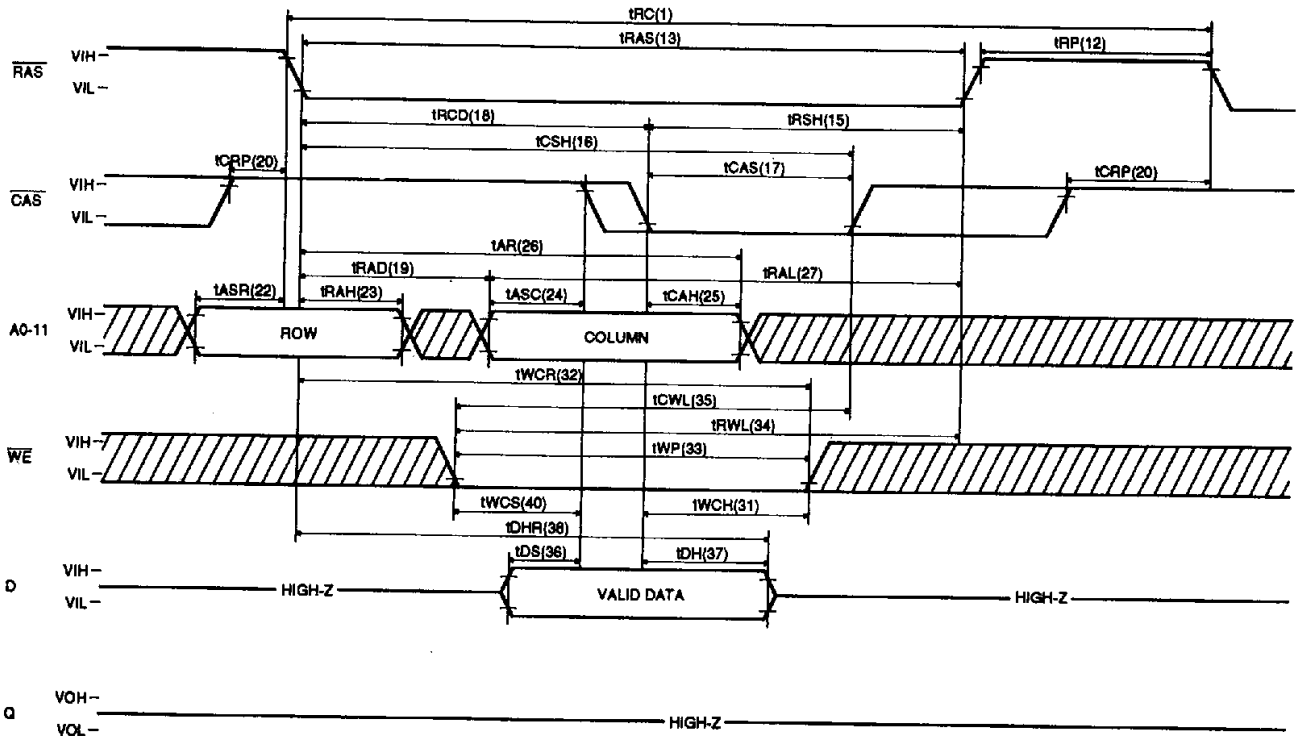
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10)	-	5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	-	7	pF
C_{OUT}	Output Capacitance (Q)	-	7	pF

TIMING DIAGRAM

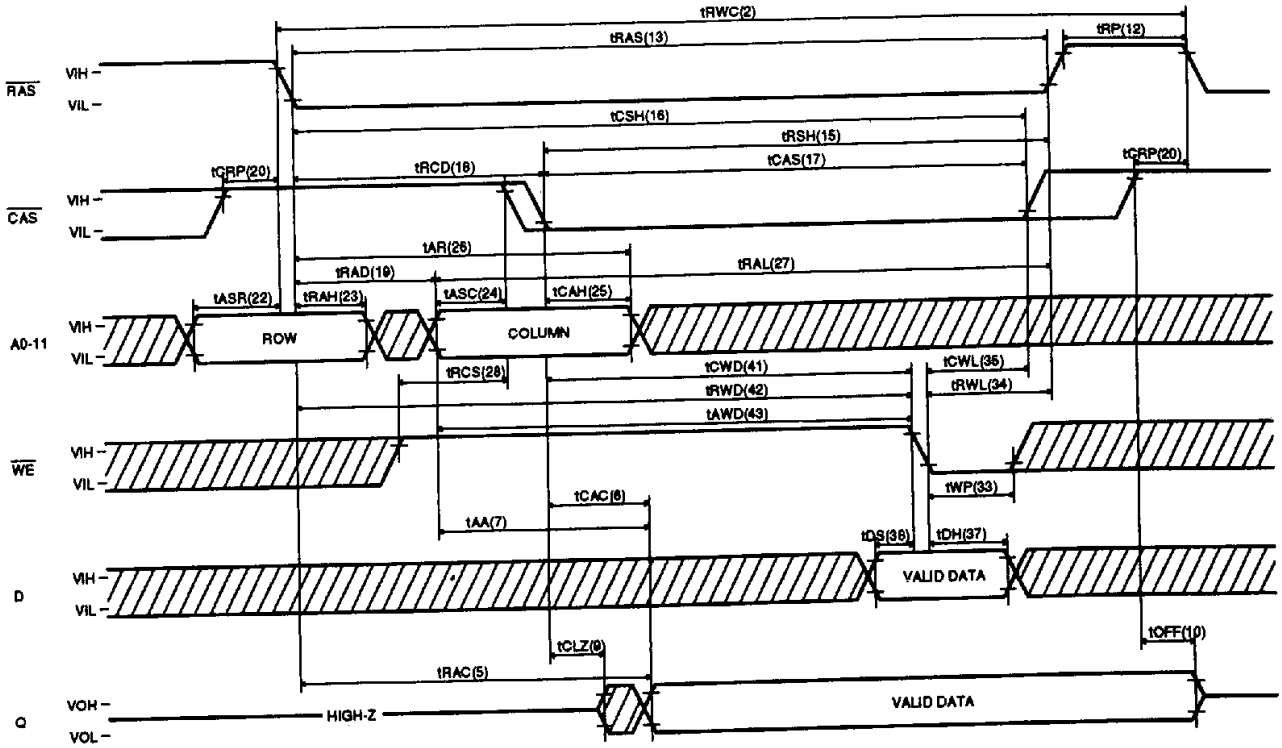
READ CYCLE



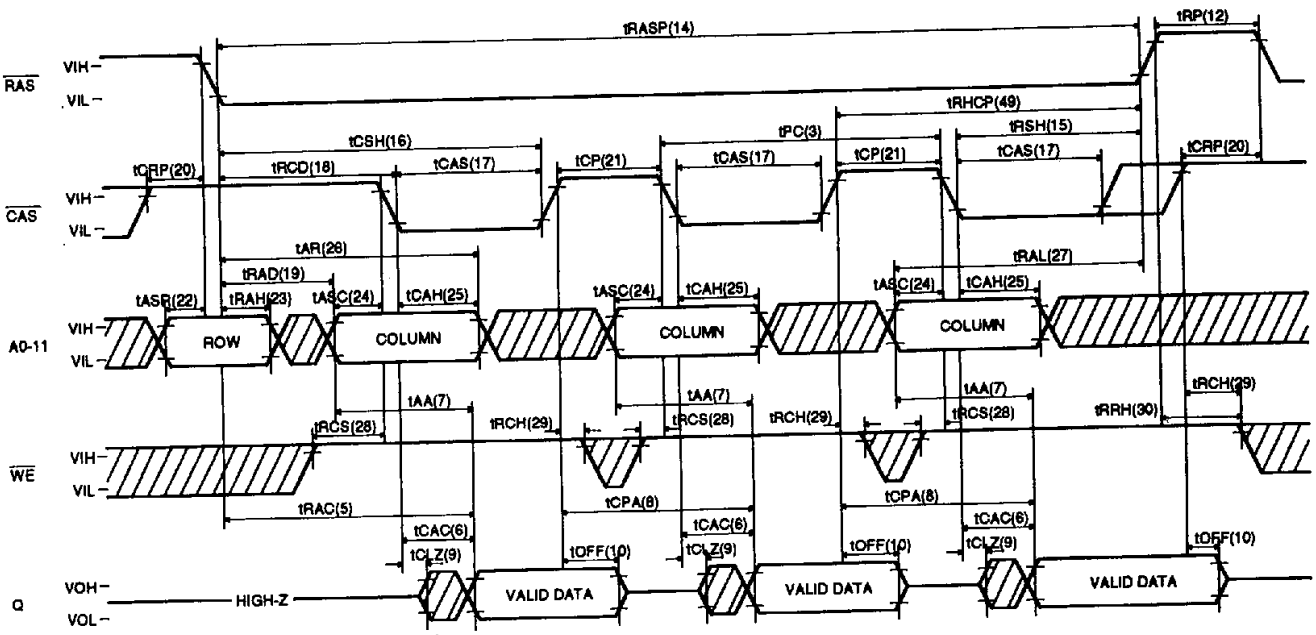
EARLY WRITE CYCLE



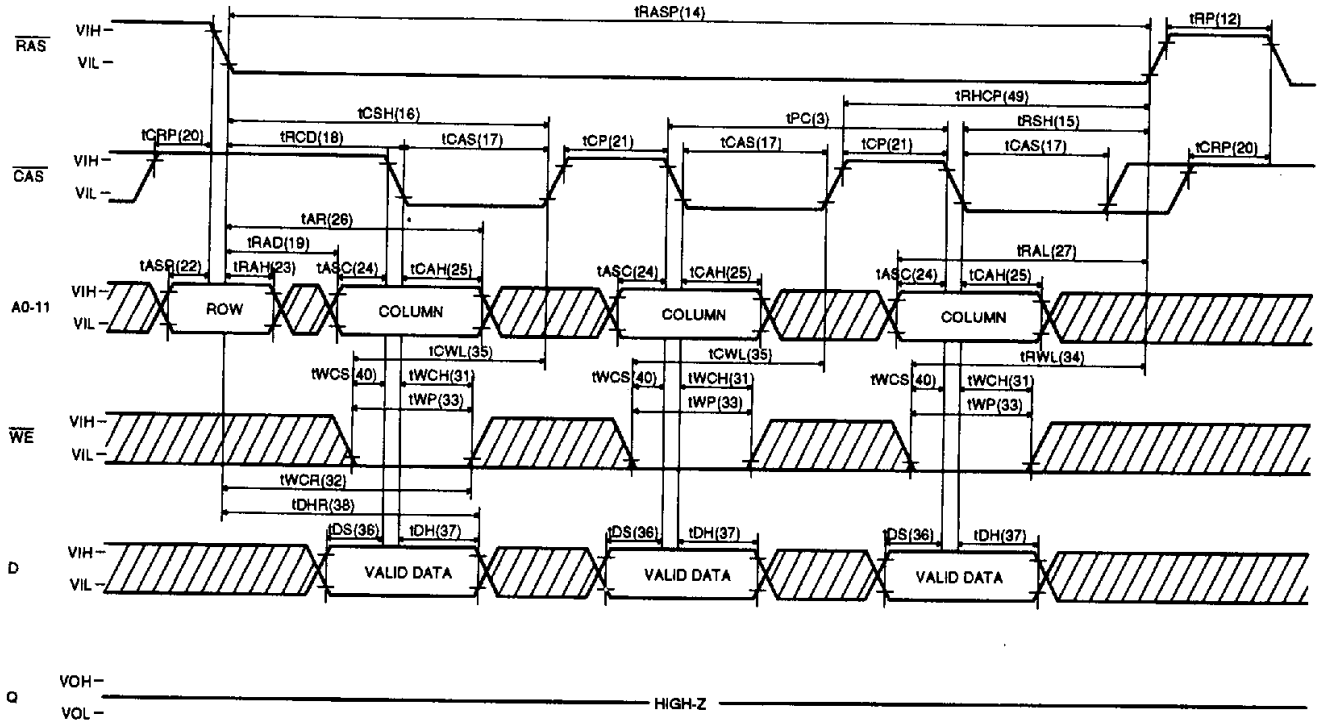
READ-MODIFY-WRITE CYCLE



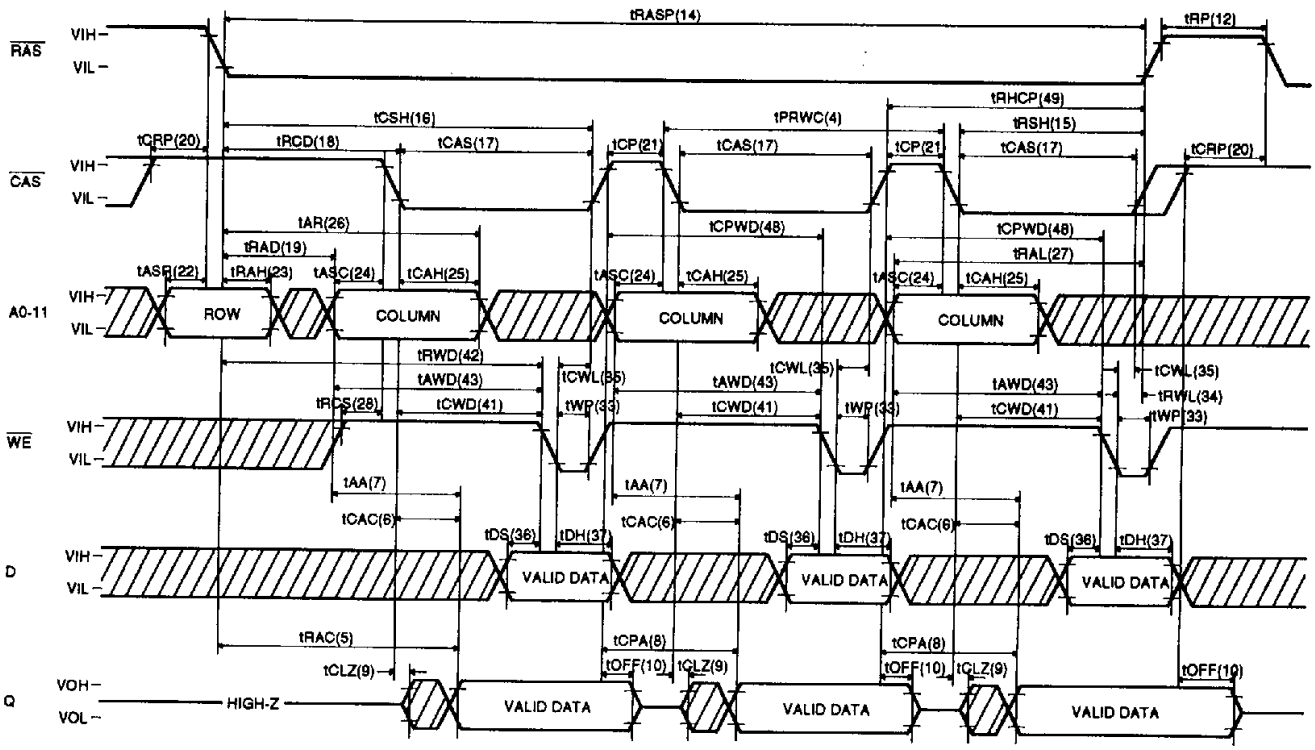
FAST PAGE MODE READ CYCLE



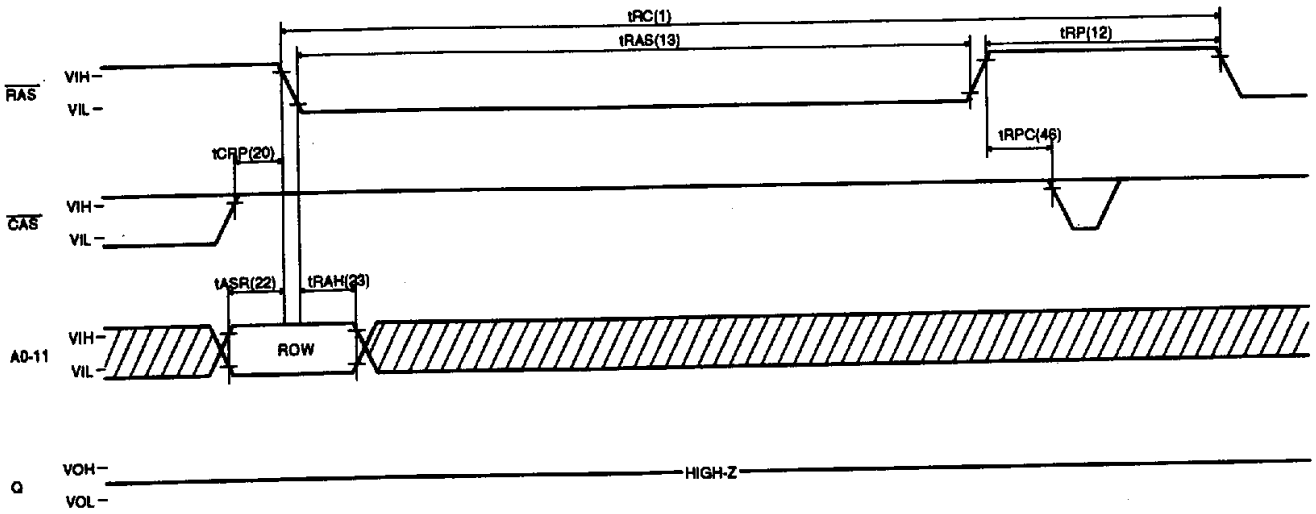
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

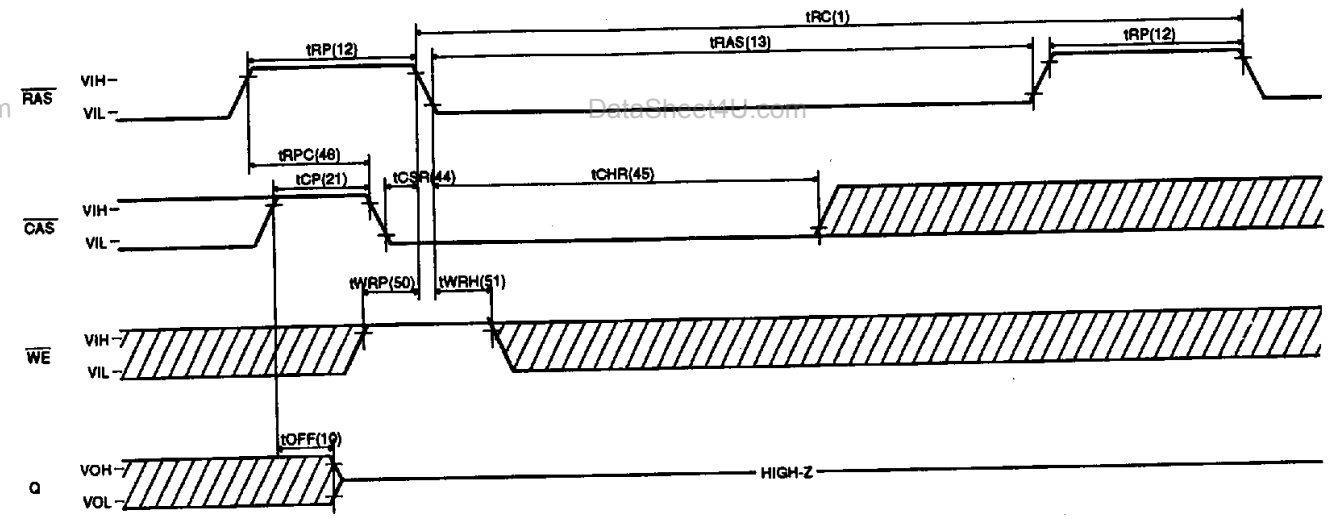


RAS-ONLY REFRESH CYCLE



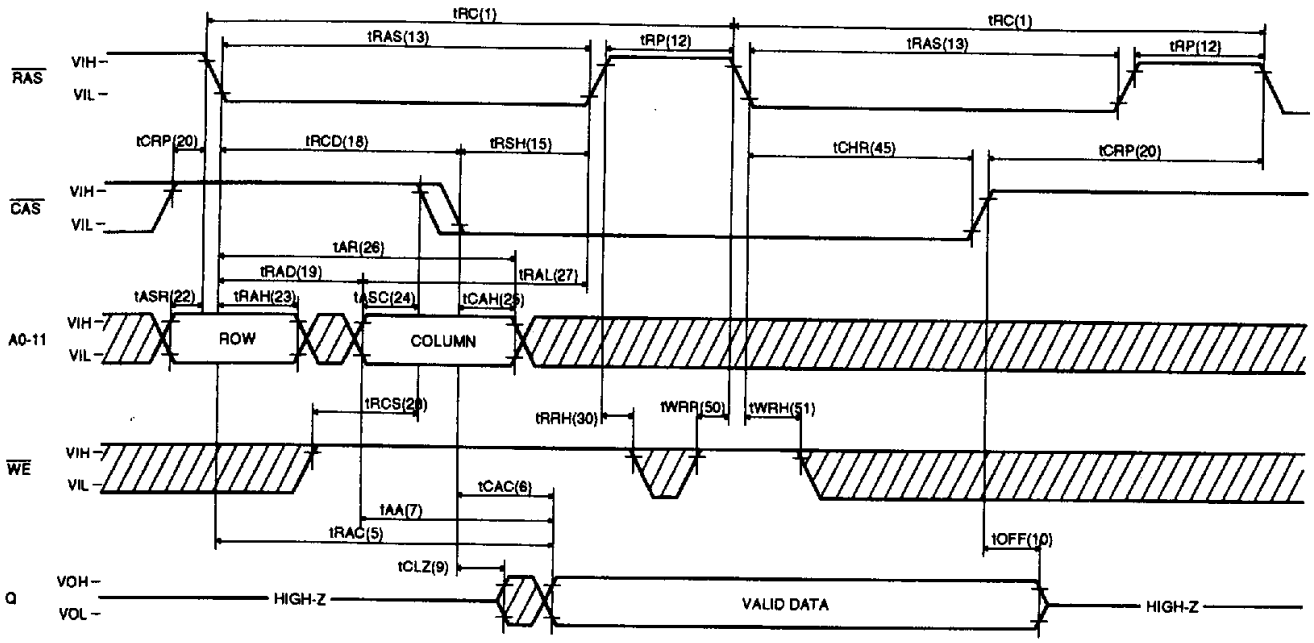
NOTE : $\overline{WE}$ = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

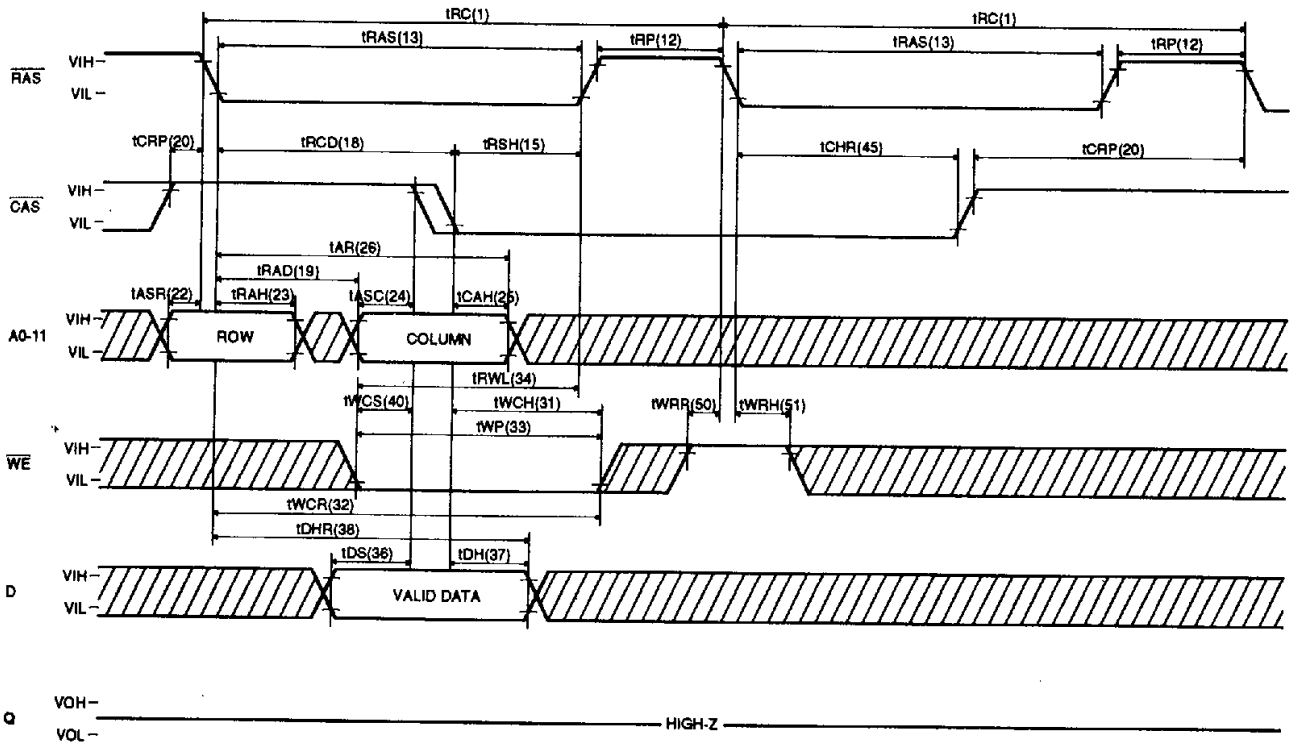


NOTE : A0 - A11 = "H" or "L"

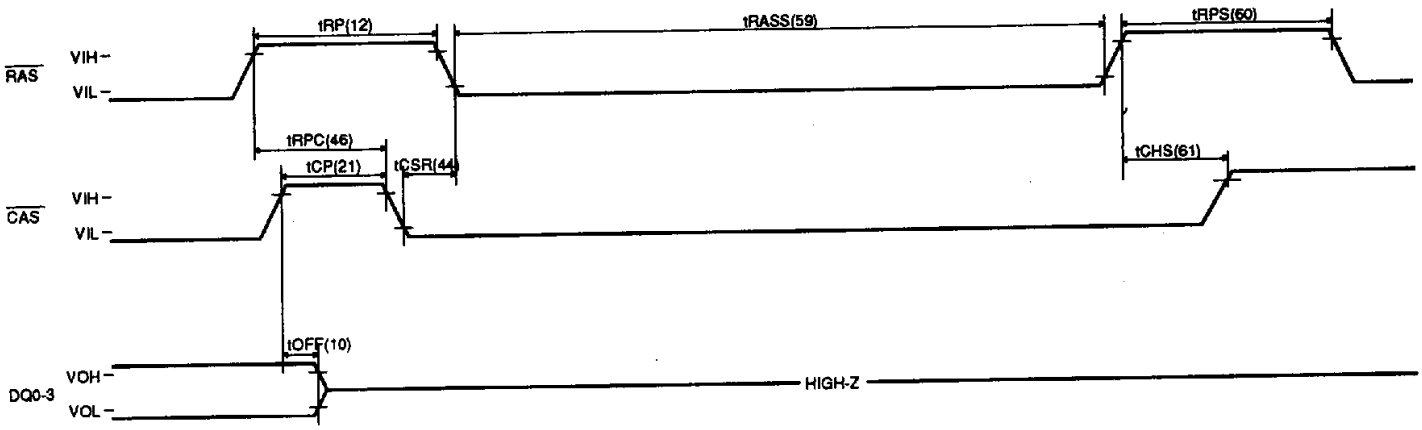
HIDDEN REFRESH CYCLE (READ)



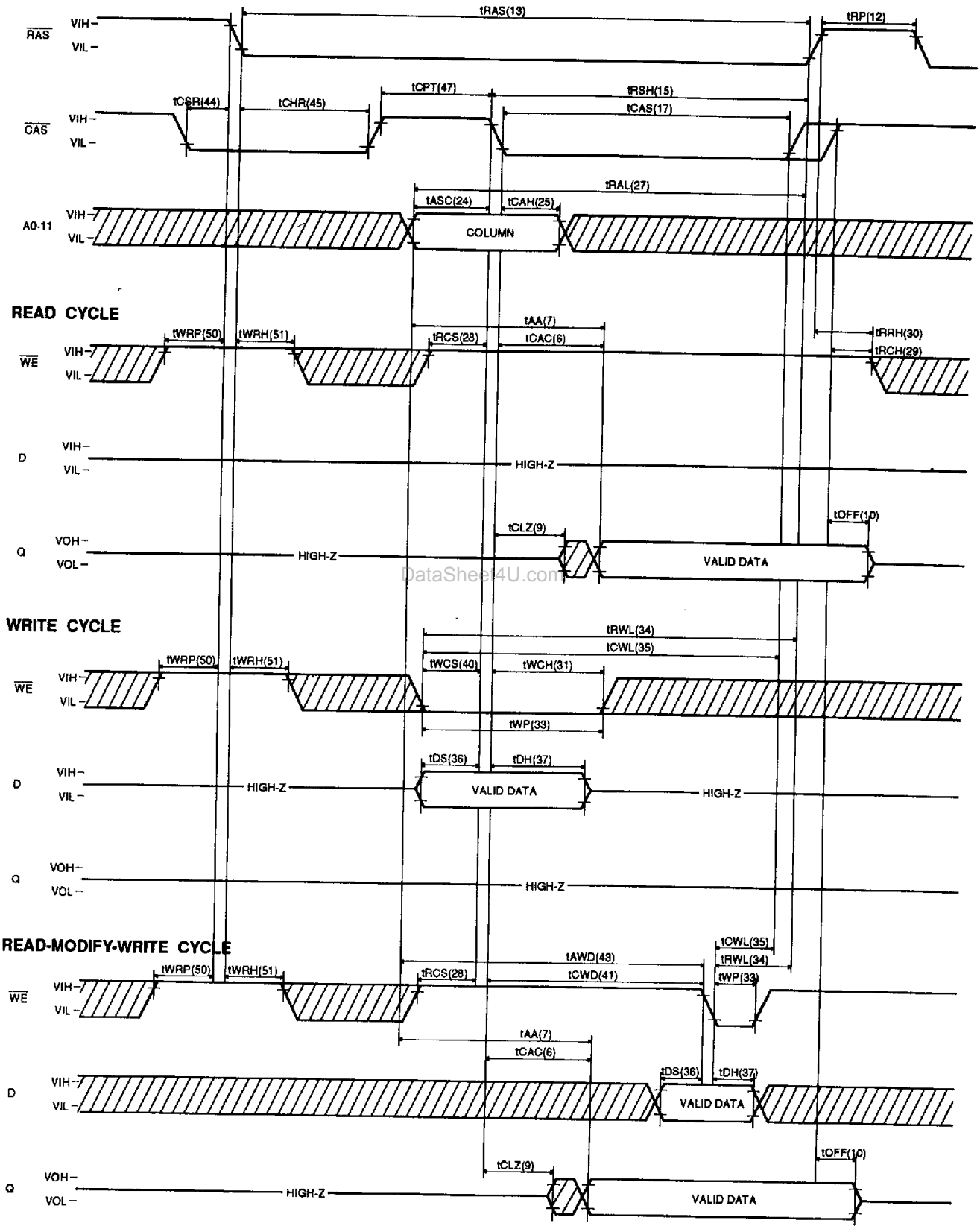
HIDDEN REFRESH CYCLE (WRITE)



CAS-BEFORE-RAS SELF REFRESH



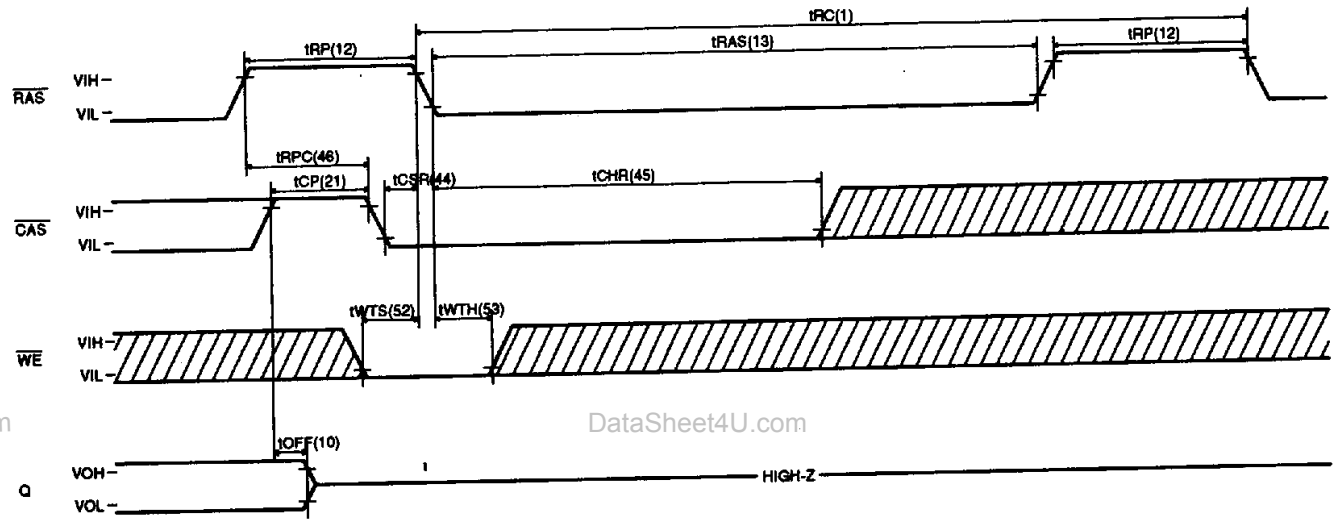
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



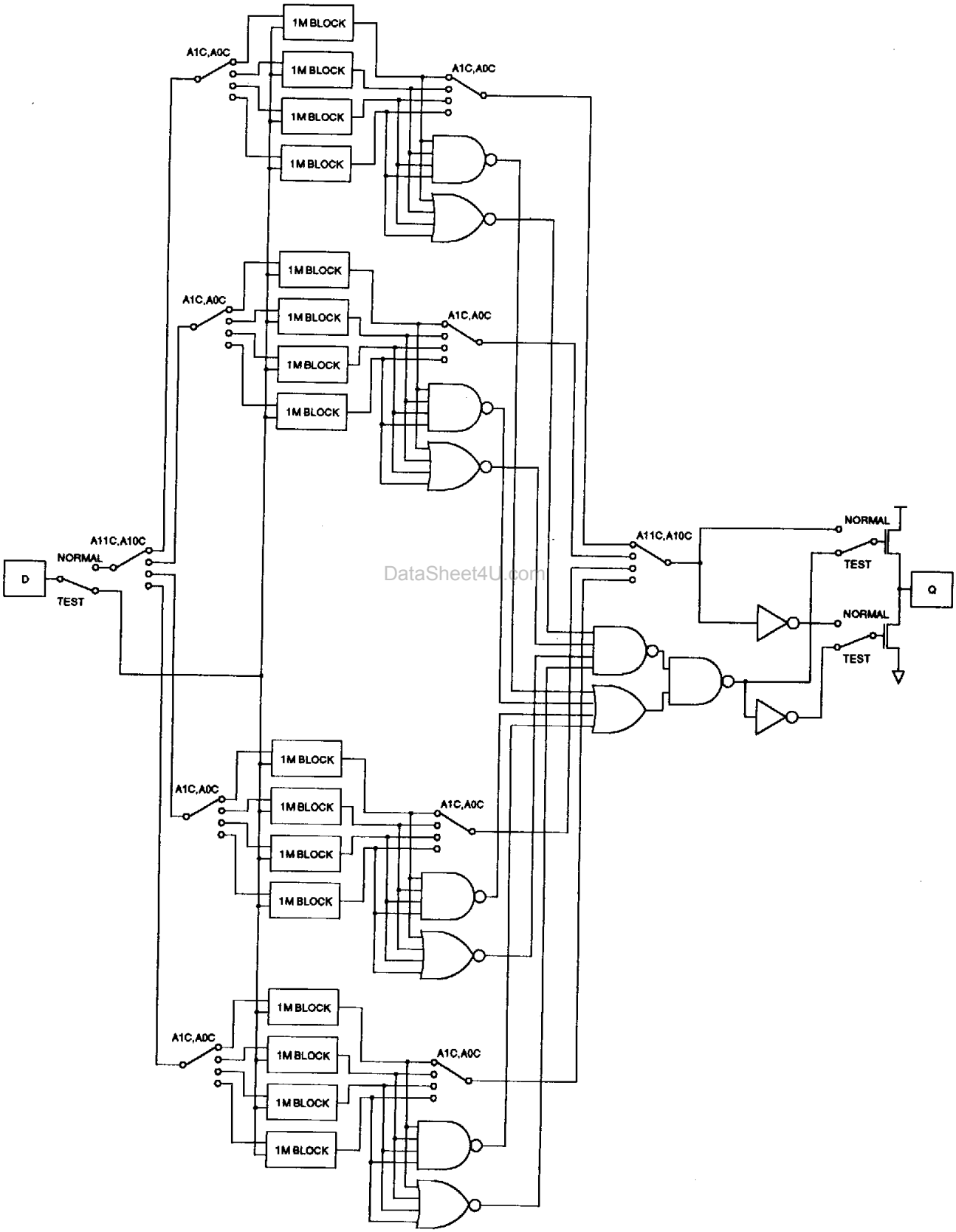
TEST MODE

The HY5117100A is a DRAM organized 16,777,216 x 1-bit. It is internally organized 1,048,576 x 16-bit. In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0, A1, A10 and A11 are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the Q pin indicates a "1". If they are not equal, the Q pin indicates a "0". Belowing shows the timing diagram of the HY5117100A to enter Test Mode. In Test Mode, the 16Mx1 DRAM can be tested as if it were a 1Mx1 DRAM. $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle (Test Mode In Cycle) puts the HY5117100A into Test Mode and $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycle puts it back into Normal Mode. In Test Mode, $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle shall be used for the refresh operation. The Test Mode function reduces test time (1/16 in case of N test pattern)

TEST MODE IN CYCLE



BLOCK DIAGRAM IN TEST MODE



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY5117100AJ	50/60/70		SOJ
HY5117100ASLJ	50/60/70	SL-part	SOJ
HY5117100AT	50/60/70		TSOP-II
HY5117100ASLT	50/60/70	SL-part	TSOP-II
HY5117100AR	50/60/70		TSOP-II(R)
HY5117100ASLR	50/60/70	SL-part	TSOP-II(R)