PRELIMINARY

HYUNDAI SEMICONDUCTOR HY514400

1M×4-Bit CMOS DRAM

M1A1200A-MAY91

T-46-23-17

DESCRIPTION

The HY514400 is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The HY514400 utilizes HYUNDAI's CMOS process technology as well as advanced circuit techniques to provide wide operating margins. Multiplexed address inputs permit the HY514400 to be packaged in a standard 20/26 pin plastic SOJ and TSOP.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented feature include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**
  - **Operating Current, 100ns : 85mA(max.)**
  - **TTL Standby Current : 2mA(max.)**
  - **CMOS Standby Current : 1mA(max.)**
- **Read-Modify-Write Capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Capability**
- **Common I/O capability**
- **Fast Page mode and Test mode capability**
- **1024 refresh cycles/16 ms**
- **High reliability 300 mil 20/26 pin SOJ and 20/26 pin TSOP**
- **Fast access time and cycle time (ns)**

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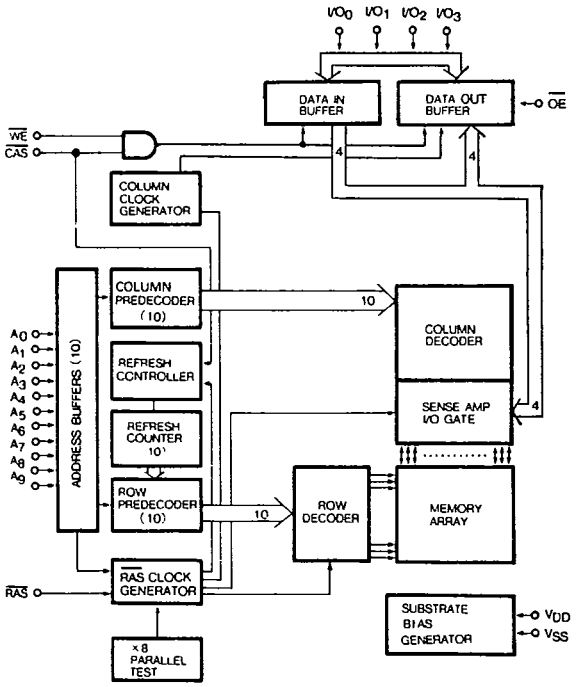
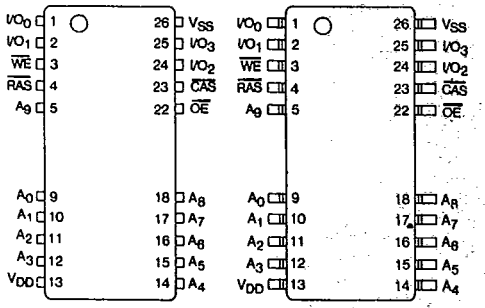
	HY514400-80	HY514400-10
Max $\overline{RAS}$ Access Time, t_{RAC}	80	100
Max $\overline{CAS}$ Access Time, t_{CAC}	25	25
Min Fast Page Mode Cycle Time, t_{PC}	55	60
Min Cycle Time, t_{RC}	150	180

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_9	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	−55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	0.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input Hight Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	STEED	HY514400		UNIT	NOTE
				MIN.	MAX.		
$\lvert I_{LI} \rvert$	Input Leakage Current(any input pin)	0V ≤V_{IN} ≤ 6.5V, All other pin not under test=V_{SS}			10	μA	
$\lvert I_{LO} \rvert$	Output Leakage Current for High Impedance State	D_{OUT} is disable, 0V ≤ V_{OUT} ≤ 5.5V			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$\overline{RAS}$, $\overline{CAS}$, Address cycling, t_{RC}=t_{RC}(min.)	−80		95	mA	1, 2
			−10		85		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$=$\overline{CAS}$=V_{IH}			2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, t_{RC}=t_{RC}(min.)	−80		95	mA	2
			−10		85		
I_{DD4}	V_{DD} Supply Current, Fast page mode	$\overline{RAS}$=V_{IL}, Address cycling, t_{PC}=t_{PC}(min.)	−80		55	mA	1, 2
			−10		45		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$=$\overline{CAS}$=V_{DD}−0.2V			1	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{RC}(min.)	−80		95	mA	2
			−10		85		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :
1. I_{DD} and I_{DD4} depend on output loading, specified values are obtained with the output open.
2. I_{DD1}, I_{DD3}, I_{DD4} and I_{DD6} depend on cycle rate.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1, 2, 3

#	SYMBOL	PARAMETER	HY514400				UNIT	NOTES
			80		10			
			MIN.	MAX.	MIN.	MAX.		
1	t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
2	t_{RWC}	Read-Modify-Write Cycle Time	210	–	245	–	ns	
3	t_{PC}	Fast Page Mode Cycle Time	55	–	60	–	ns	
4	t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	120	–	125	–	ns	
5	t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	4,9
6	t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	ns	4,9
7	t_{AA}	Access Time from Column Address	–	40	–	45	ns	4,9
8	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	50	–	55	ns	4
9	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	4
10	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	5
11	t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	3
12	t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
13	t_{RAS}	$\overline{RAS}$ Pulse Width	80	10K	100	10K	ns	
14	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	80	200K	100	200K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	ns	
16	t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
17	t_{CAS}	$\overline{CAS}$ Pulse Width	25	10K	25	10K	ns	
18	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	55	25	75	ns	9
19	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	55	ns	10
20	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
21	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	ns	
22	t_{ASR}	Row Address Set-up Time	0	–	0	–	ns	
23	t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
24	t_{ASC}	Column Address Set-up Time	0	–	0	–	ns	
25	t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
26	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	80	–	ns	
27	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	45	–	ns	
28	t_{RCS}	Read Command Set-up Time	0	–	0	–	ns	
29	t_{RCH}	Read Command Hold Time	0	–	0	–	ns	
30	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	
31	t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
32	t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	80	–	ns	
33	t_{WP}	Write Command Pulse Width	15	–	20	–	ns	
34	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	–	25	–	ns	
35	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	–	25	–	ns	
36	t_{DS}	Data Set-up Time	0	–	0	–	ns	7
37	t_{DH}	Data Hold Time	15	–	20	–	ns	7
38	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	–	80	–	ns	
39	t_{REF}	Refresh Period	–	16	–	16	ms	
40	t_{WCS}	Write Command Set-up Time	0	–	0	–	ns	8
41	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	55	–	60	–	ns	8
42	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	110	–	135	–	ns	8
43	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	70	–	80	–	ns	8

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#	SYMBOL	PARAMETER	HY514400				UNIT	NOTES
			80		10			
			MIN.	MAX.	MIN.	MAX.		
44	t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	30	–	30	–	ns	
46	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
47	t_{CPT}	$\overline{CAS}$ Precharge Time($\overline{CAS}$ Before $\overline{RAS}$ Counter Test Cycle)	40	–	50	–	ns	
48	t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	20	–	ns	
49	t_{OEA}	$\overline{OE}$ Access Time	–	20	–	25	ns	
50	t_{OED}	$\overline{OE}$ to Data Delay	20	–	25	–	ns	
51	t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	0	20	0	20	ns	
52	t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	25	–	ns	
53	t_{WTS}	Write Command Set-up Time(Test Mode In)	10	–	10	–	ns	
54	t_{WTH}	Write Command Hold Time(Test Mode In)	10	–	10	–	ns	
55	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
56	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	ns	

AC CHARACTERISTICS IN THE TEST MODE NOTE11

#	SYMBOL	PARAMETER	HY514400				UNIT	NOTES
			80		10			
			MIN.	MAX.	MIN.	MAX.		
57	t_{RC}	Random Read or Write Cycle Time	155	–	185	–	ns	
58	t_{RWC}	Read-Modify-Write Cycle Time	215	–	250	–	ns	
59	t_{PC}	Fast Page Mode Cycle Time	60	–	65	–	ns	
60	t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	120	–	130	–	ns	
61	t_{RAC}	Access Time from $\overline{RAS}$	–	85	–	105	ns	4,9
62	t_{CAC}	Access Time from $\overline{CAS}$	–	30	–	30	ns	4,9
63	t_{AA}	Access Time from Column Address	–	45	–	50	ns	4,9
64	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	55	–	60	ns	4
65	t_{RAS}	$\overline{RAS}$ Pulse Width	85	10K	105	10K	ns	
66	t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	200K	105	200K	ns	
67	t_{RSH}	$\overline{RAS}$ Hold Time	30	–	30	–	ns	
68	t_{CSH}	$\overline{CAS}$ Hold Time	85	–	105	–	ns	
69	t_{CAS}	$\overline{CAS}$ Pulse Width	30	10K	30	10K	ns	
70	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	50	–	ns	
71	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	60	–	65	–	ns	8
72	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	115	–	140	–	ns	8
73	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	75	–	85	–	ns	8
74	t_{OEA}	$\overline{OE}$ Access Time	–	25	–	30	ns	
75	t_{OED}	$\overline{OE}$ to Data Delay	25	–	30	–	ns	
76	t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	30	–	ns	

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) and t_{OEZ} defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle : If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.) the cycle is a read-modify-write cycle and data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. These specifications are applied to the test mode.

CAPACITANCE

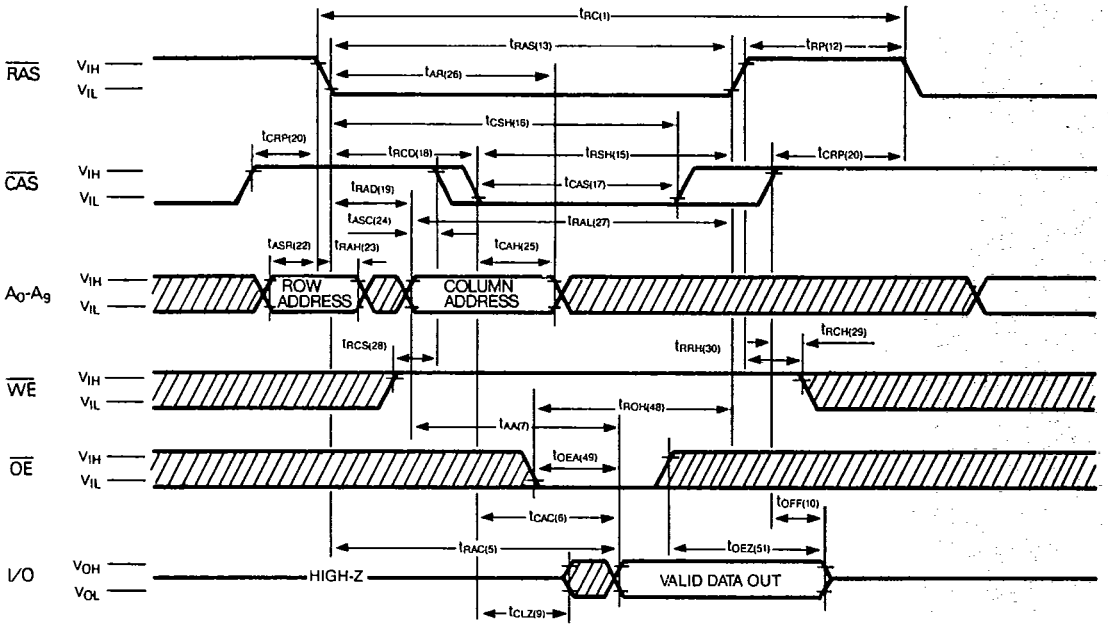
(T_A=0°C to 70°C, V_{DD}=5V± 10%, f=1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Input Capacitance (A_0~A_9, Data In)	–	5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_{OUT}	Output Capacitance (Data Out)	–	7	pF

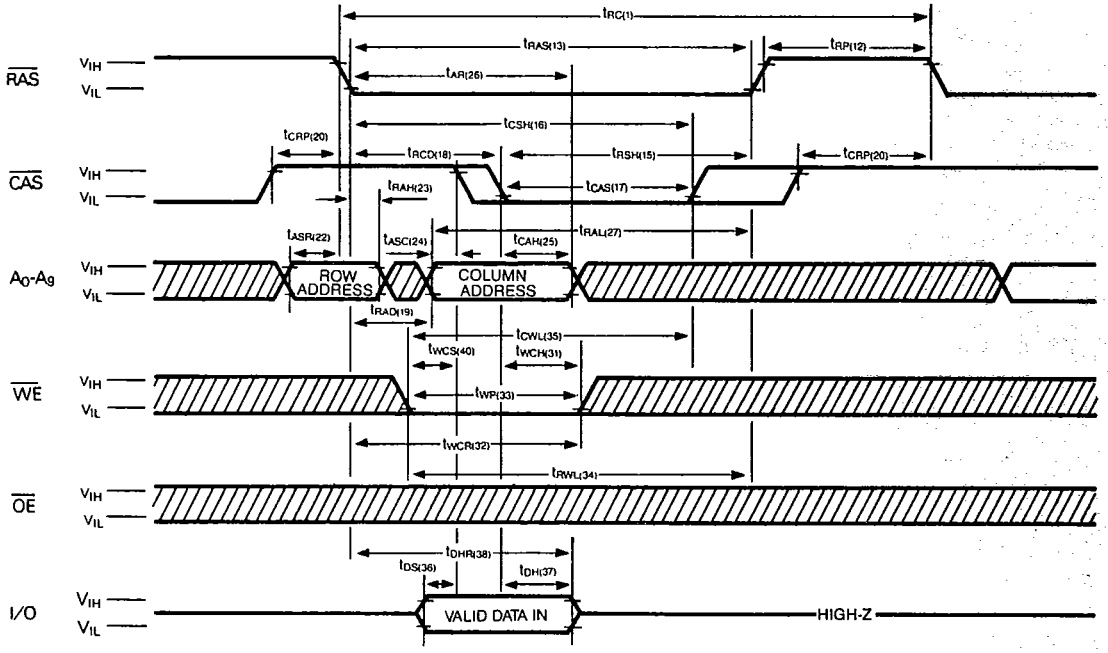
4

TIMING DIAGRAM

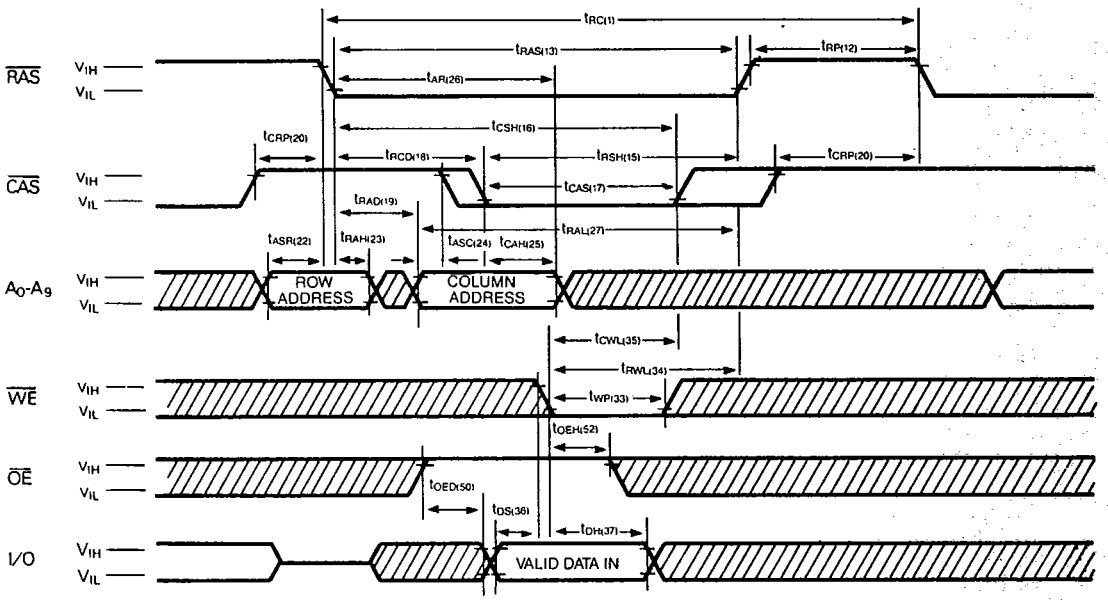
READ CYCLE



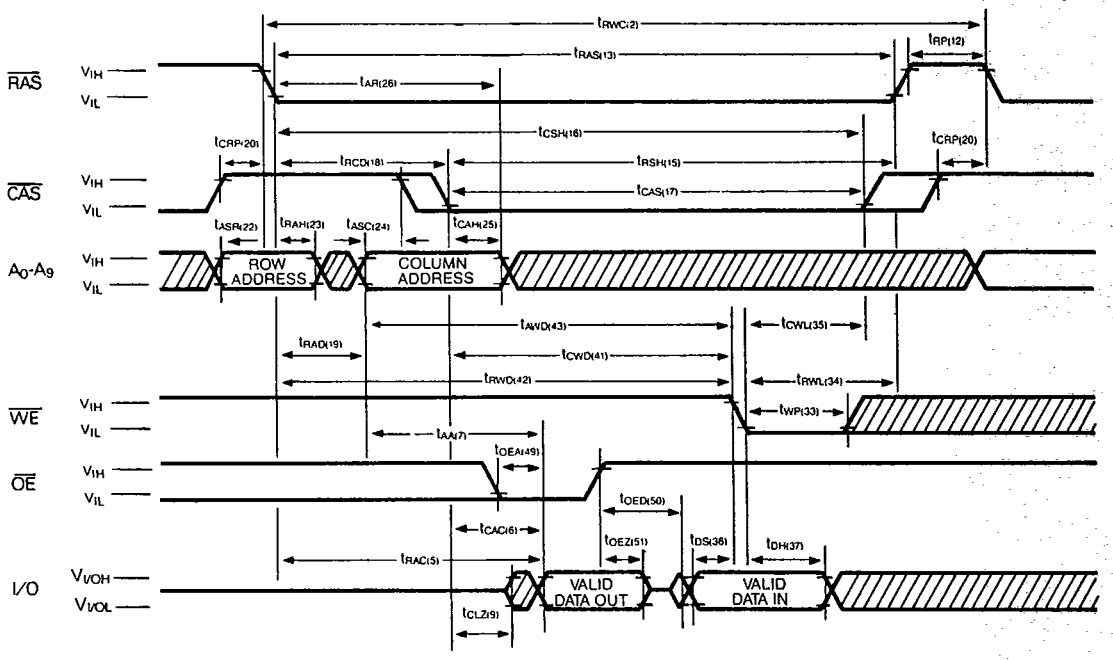
WRITE CYCLE



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



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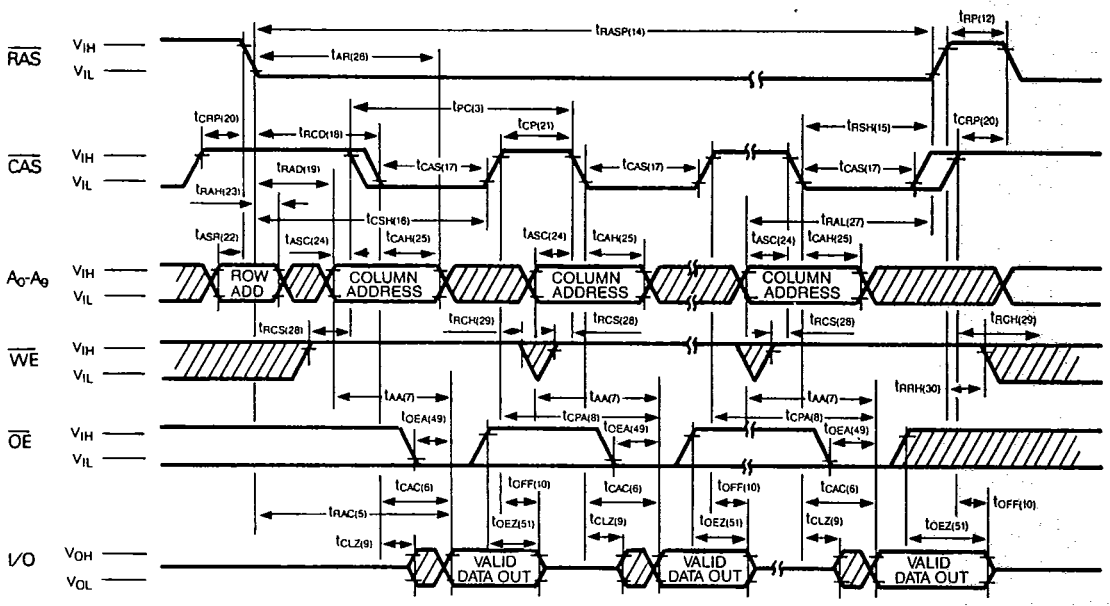
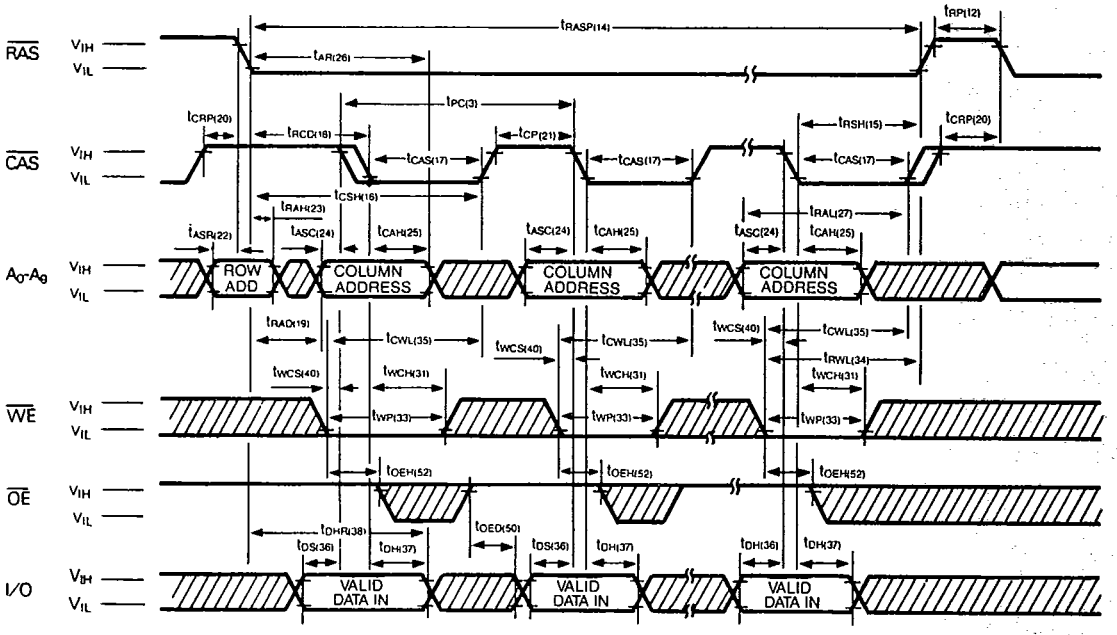
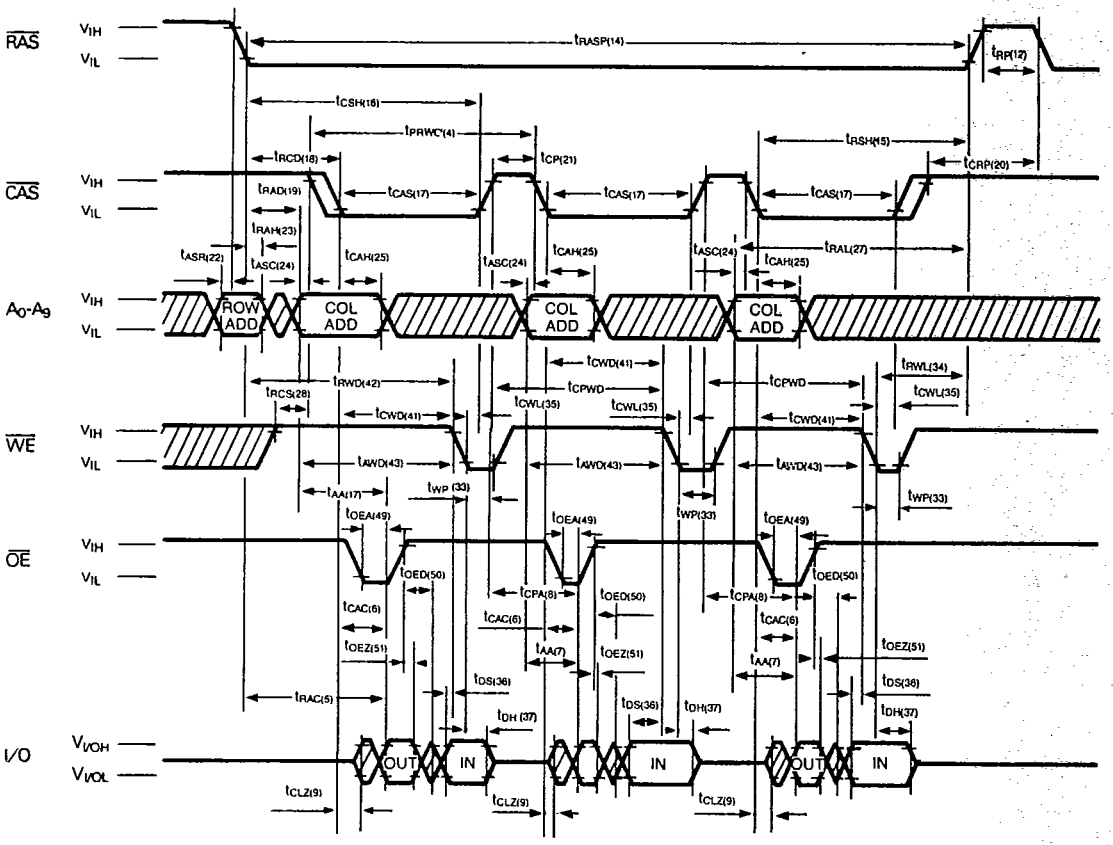
FAST PAGE MODE READ CYCLE



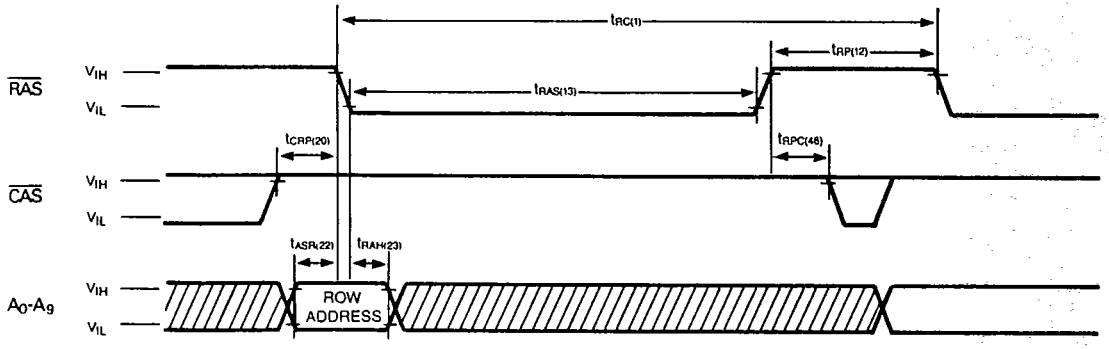
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

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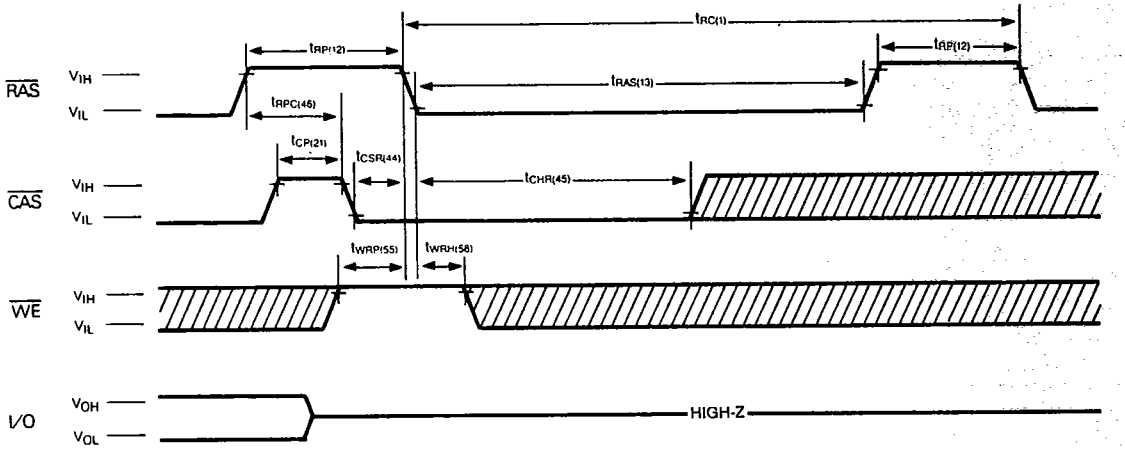
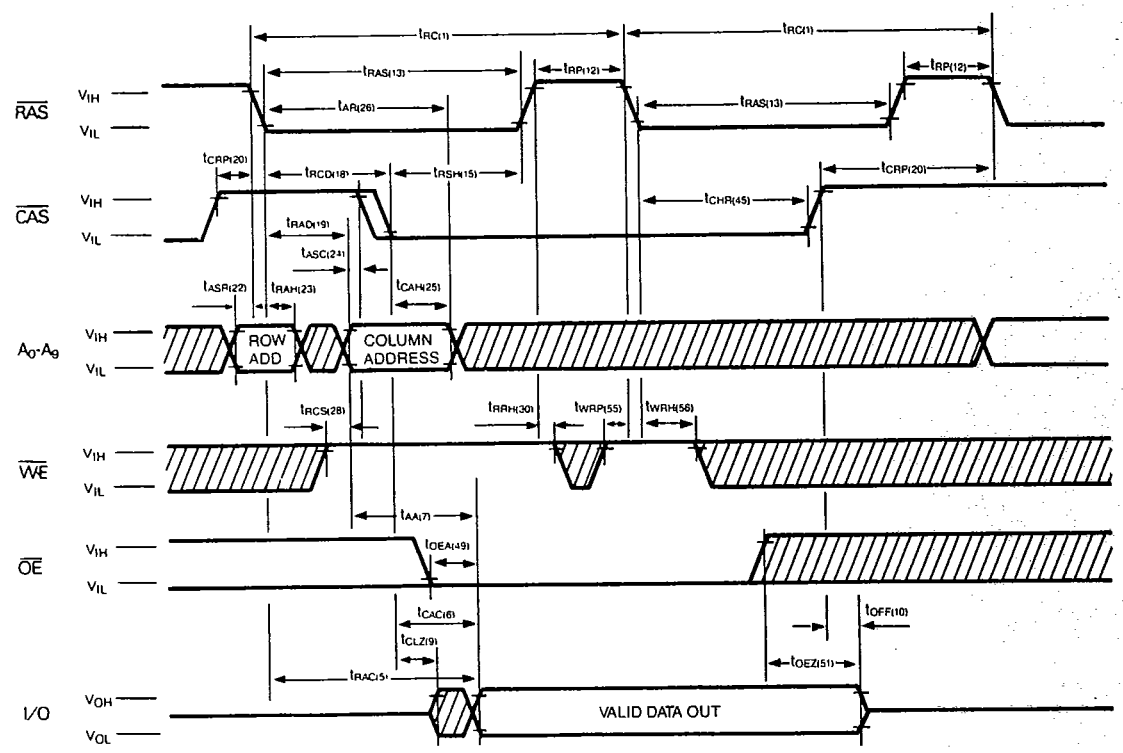
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

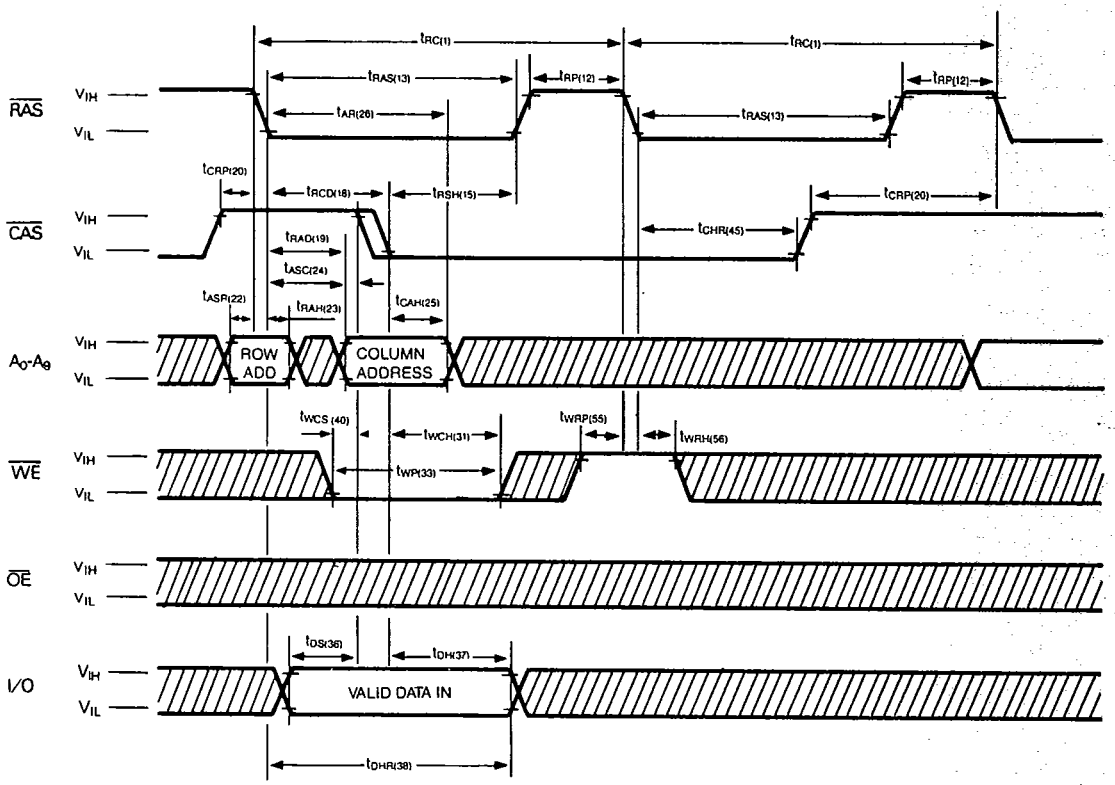


NOTE : $\overline{OE}$ and A_0-A_9 : "H" or "L"

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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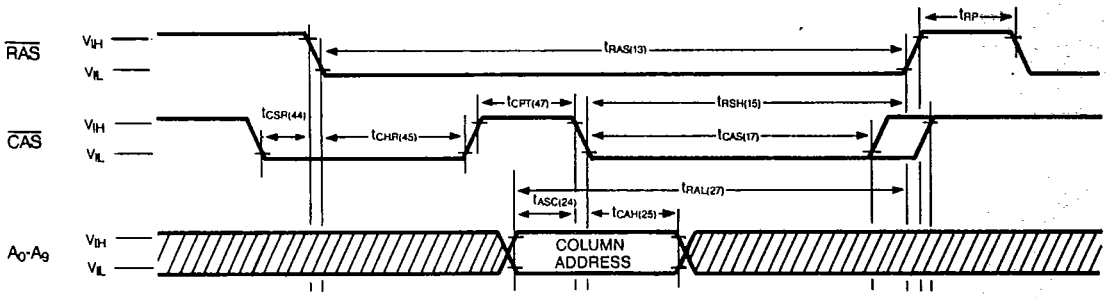
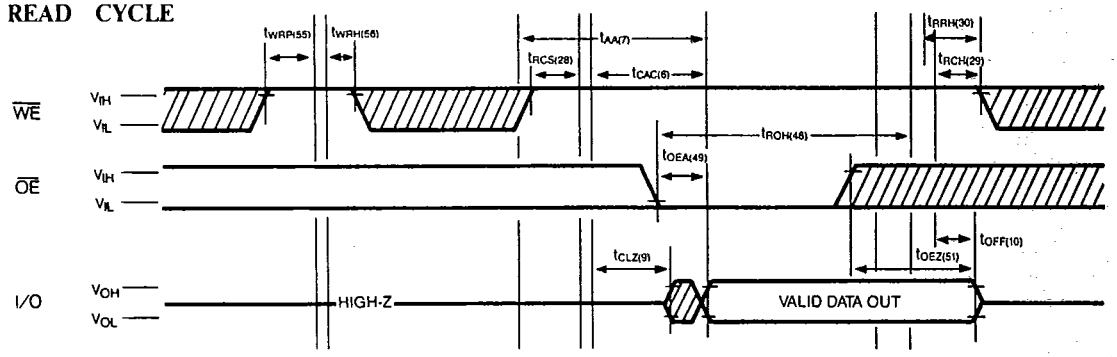
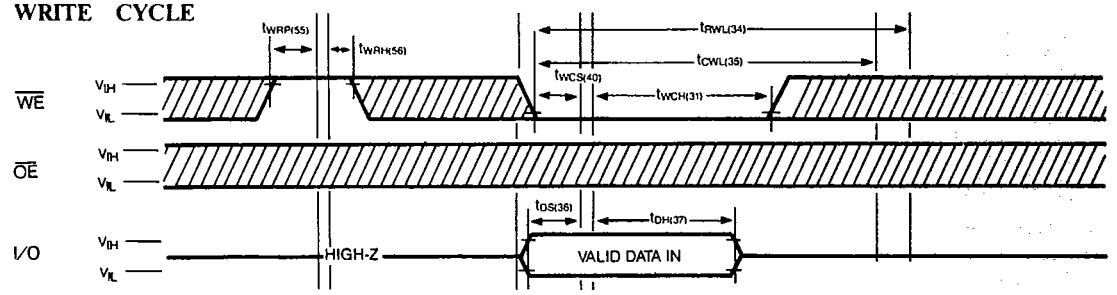
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



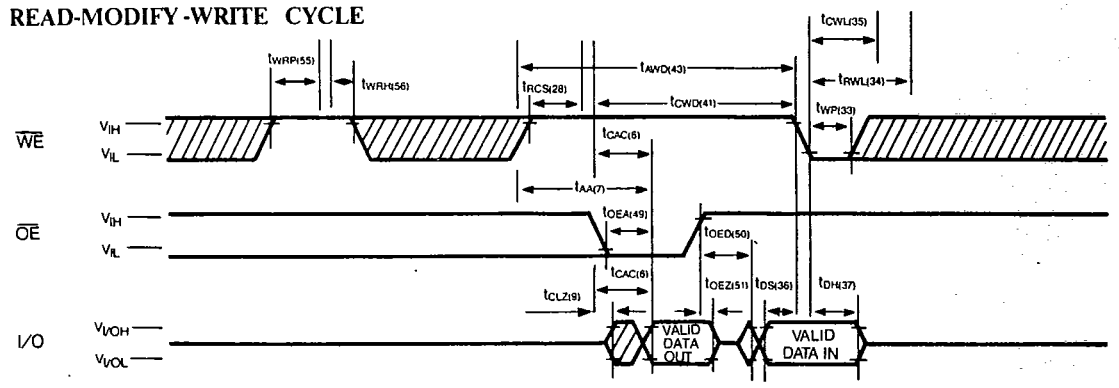
READ CYCLE



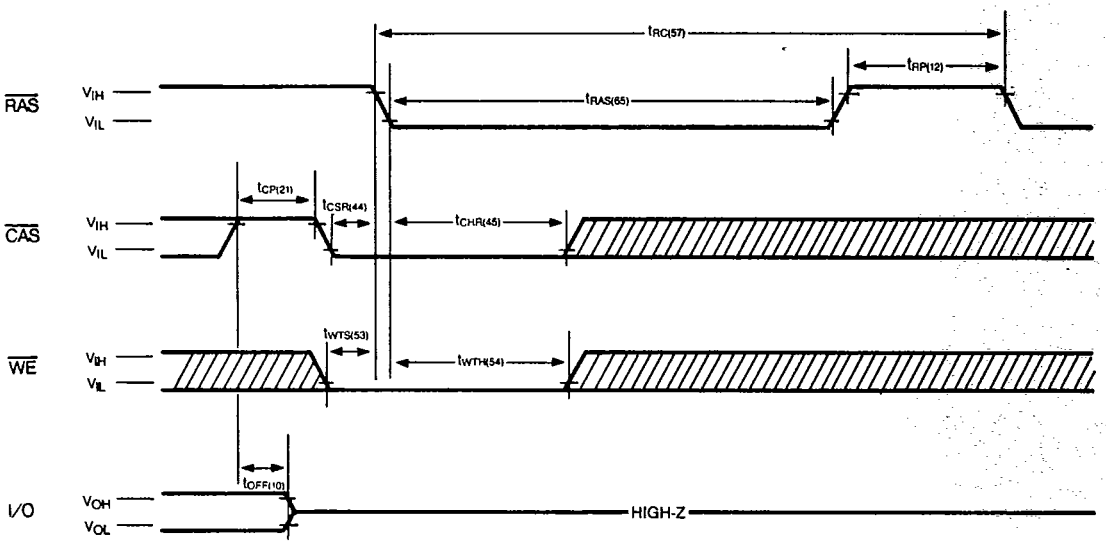
WRITE CYCLE



READ-MODIFY-WRITE CYCLE



TEST MODE IN CYCLE



NOTE : $\overline{OE}$ and A_0-A_9 : "H" or "L"

4

TEST MODE

The HY514400 is a DRAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In Test Mode, data are written into 8 sectors in parallel and recieved the same way. A_{oc} is not used. If, upon reading, two bits on one I/O are equal(all 1's or 0's), the I/O pin indicates 1.

If they were not equal, the I/O pin would indicate 0. Fig. 1 shows the block diagram of HY514400. In Test Mode, the 1M×4 DRAM can be tested as if it were a 512K×8 DRAM.

$\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle(Test Mode in Cycle) puts it back into Normal Mode. The Test Mode function reduces test times(1/2 in case of N test pattern).

FIG. 1 BLOCK DIAGRAM IN TEST MODE