DESCRIPTION

This family is a 1M bit dynamic RAM organized 1,048,576 x 1-bit configuration with Fast Page mode CMOS DRAMs. Fast Page mode offers high speed of random access memory within the same row. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(60, 70 or 80ns) and power consumption (Normal or Low power). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

FEATURES

- Fast Page Mode operation
- Read-modify-write Capability
- TTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- Max. Active power dissipation

Speed	Power
60	467mW
70	412mW
80	357mW

- JEDEC standard pinout
- 20/26-pin SOJ (300mil)
- Single power supply of 5V ± 10%
- Early Write or output enable controlled write
- Fast access time and cycle time

Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	20ns	40ns
80	80ns	20ns	45ns

- Refresh cycle

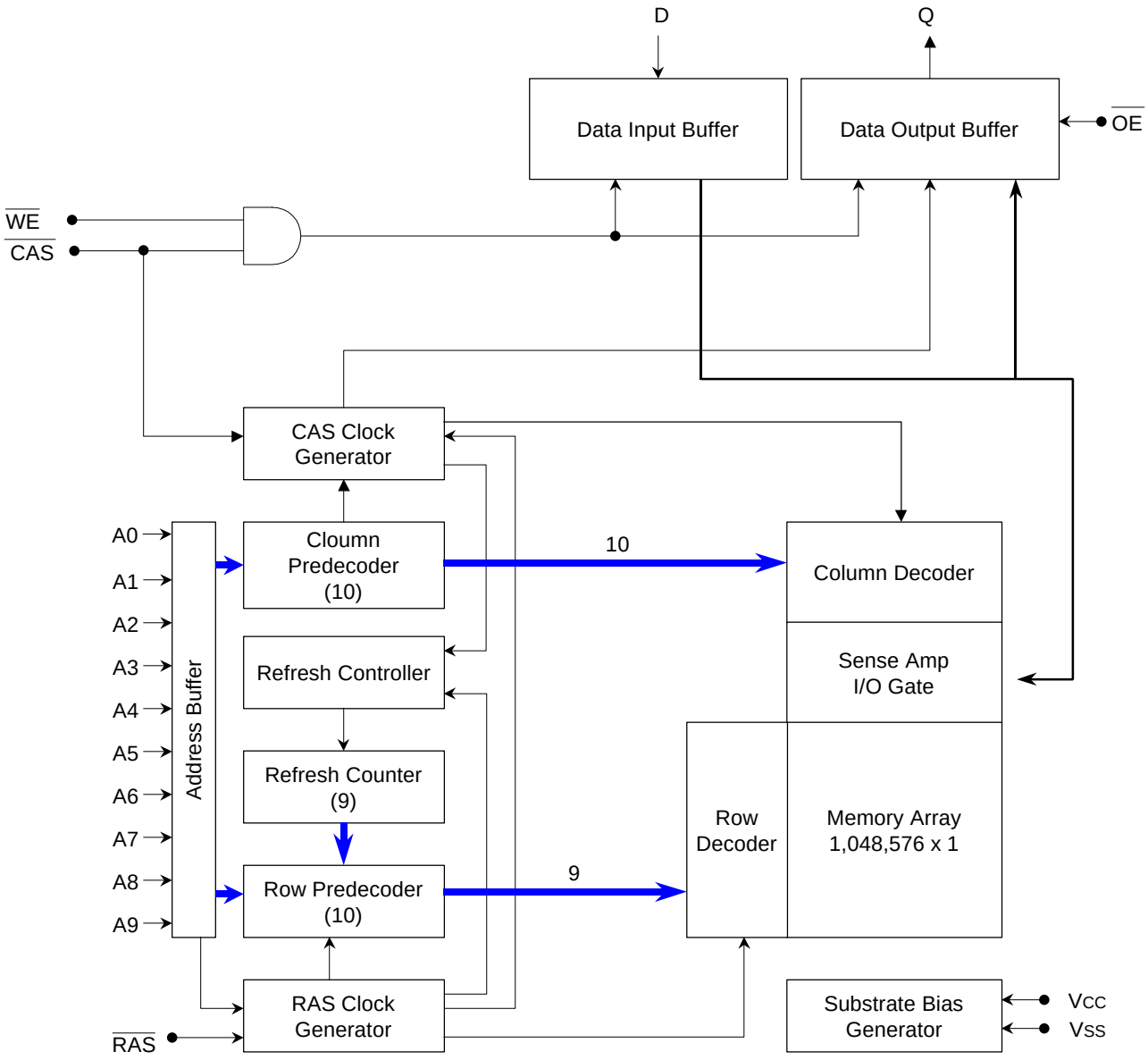
Part number	Refresh	Normal	L-part
HY531000A	512	8ms	64ms

ORDERING INFORMATION

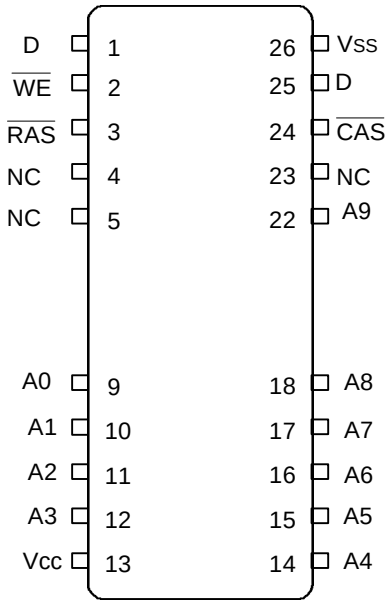
Part Name	Refresh	Power	Package
HY531000AJ	512		20/26Pin SOJ
HY531000ALJ	512	L-part	20/26Pin SOJ

*L : Low power

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Marking Side)



20/26 Pin Plastic SOJ (300mil)

PIN DESCRIPTION

Pin Name	Parameter
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0~A9	Address Input
D	Data Input
Q	Data Output
Vcc	Power (5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	0.9	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

Note : All voltages are referenced to V_{SS}.

DC OPERATING CHARACTERISTICS

Symbol	Parameter	Test condition	Min	Max	Unit
I_{LI}	Input Leakage Current (Any input)	$V_{SS} \le V_{IN} \le V_{CC}$ All other pins not under test = V_{SS}	-10	10	µA
I_{LO}	Output Leakage Current (Any input)	$V_{SS} \le V_{OUT} \le V_{CC}$ /RAS & /CAS at V_{IH}	-10	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -5.0mA	2.4	-	V

DC CHARACTERISTICS

(T_A = 0°C to 70°C , V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	Test condition	Speed	Max.	Unit
I_{CC1}	Operating Current	/RAS, /CAS Cycling t_{RC} = $t_{RC(min)}$	60 70 80	85 75 65	mA
I_{CC2}	TTL Standby Current	/RAS, /CAS ≥ $V_{IH(min)}$ Other inputs ≥ V_{SS}		2	mA
I_{CC3}	/RAS-only Refresh Current	/RAS Cycling,/CAS = V_{IH} t_{RC} = $t_{RC(min)}$	60 70 80	85 75 65	mA
I_{CC4}	Fast Page mode Current	/CAS Cycling, /RAS = V_{IL} t_{PC} = $t_{PC(min)}$	60 70 80	70 55 45	mA
I_{CC5}	CMOS Standby Current	/RAS = /CAS ≥ V_{CC} - 0.2V	L-part	1 200	mA µA
I_{CC6}	/CAS-before-/RAS Refresh Current	/RAS & /CAS = 0.2V t_{RC} = $t_{RC(min.)}$	60 70 80	85 75 65	mA
I_{CC7}	Battery Back-up Current (L-part)	tRC=125µs /CAS = CBR cycling or 0.2V /OE & /WE = V_{CC} - 0.2V Address = Vcc-0.2V or 0.2V D = Vcc-0.2, 0.2V or Open Q = open	tRAS ≤ 300ns	300	µA
			tRAS ≤ 1us	400	

Note

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on output loading and cycle rates.
2. Specified values are obtained with output unloaded.
3. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, address can be changed only once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once while /CAS=V_{IH} within one cycle time t_{PC}.
4. Only tRAS(max) = 1µs is applied to refresh of battery backup but tRAS(max) = 10µs is to applied to normal functional operation.
5. Icc5(max.), Icc7 are applied to L-part only.

AC CHARACTERISTICS

(T_A = 0 °C to 70 °C, V_{CC} = 5V ± 10% , V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	60ns		70ns		80ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
tRC	Random read or write cycle time	110	-	130	-	150	-	ns	
tRWC	Read-modify-write cycle time	130	-	155	-	175	-	ns	
tPC	Fast Page mode cycle time	40	-	40	-	45	-	ns	
tPRWC	Fast Page mode read-modify-write cycle time	60	-	65	-	70	-	ns	
tRAC	Access time from /RAS	-	60	-	70	-	80	ns	4,9,10
tCAC	Access time from /CAS	-	15	-	20	-	20	ns	4,9
tAA	Access time from column address	-	30	-	35	-	40	ns	4,10
tCPA	Access time from /CAS precharge	-	35	-	35	-	40	ns	4,
tCLZ	/CAS to output low impedance	0	-	0	-	0	-	ns	4
tOFF	Output Buffer Turn-off Dealy Time	0	20	0	20	0	20	ns	4
tT	Transition time(rise and fall)	3	50	3	50	3	50	ns	3
tRP	/RAS precharge time	40	-	50	-	60	-	ns	
tRAS	/RAS pulse width	60	10K	70	10K	80	10K	ns	
tRASP	/RAS pulse width(Fast Page Mode)	60	100K	70	100K	80	100K	ns	
tRSH	/RAS hold time	15	-	20	-	20	-	ns	
tCSH	/CAS hold time	60	-	70	-	80	-	ns	
tCAS	/CAS pulse width	15	10K	15	10K	20	10K	ns	
tRCD	/RAS to /CAS delay time	20	45	20	50	20	60	ns	9
tRAD	/RAS to column address delay time	15	30	15	35	15	40	ns	10
tCRP	/CAS to /RAS precharge time	5	-	5	-	5	-	ns	15
tCP	/CAS precharge time	10	-	10	-	10	-	ns	17
tASR	Row address set-up time	0	-	0	-	0	-	ns	
tRAH	Row address hold time	10	-	10	-	10	-	ns	
tASC	Column address set-up time	0	-	0	-	0	-	ns	13
tCAH	Column address hold time	15	-	15	-	15	-	ns	
tAR	Column address hold time from /CAS	45	-	50	-	55	-	ns	
tRAL	Column address to /RAS lead time	25	-	30	-	35	-	ns	
tRCS	Read command set-up time	0	-	0	-	0	-	ns	
tRCH	Read command hold time referenced to /CAS	0	-	0	-	0	-	ns	6
tRRH	Read command hold time referenced to /RAS	0	-	0	-	0	-	ns	6
tWCH	Write command hold time	15	-	15	-	15	-	ns	
tWCR	Write command hold time from /RAS	45	-	50	-	55	-	ns	
tWP	Write command pulse width	10	-	15	-	15	-	ns	
tRWL	Write command to /RAS lead time	15	-	20	-	20	-	ns	

AC CHARACTERISTICS

Continued

Symbol	Parameter	60ns		70ns		80ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
tCWL	Write command to /CAS lead time	15	-	20	-	20	-	ns	
tDS	Data-in set-up time	0	-	0	-	0	-	ns	7
tDH	Data-in hold time	15	-	15	-	15	-	ns	7
tREF	Refresh period(512 cycles)	8	-	8	-	8	-	ms	11
	Refresh period(L-part)	64	-	64	-	64	-	ms	11
tWCS	Write command set-up time	0	-	0	-	0	-	ns	8
tCWD	/CAS to /WE delay time	15	-	20	-	20	-	ns	8
tRWD	/RAS to /WE delay time	60	-	70	-	80	-	ns	8
tAWD	Column address to /WE delay time	30	-	35	-	40	-	ns	8
tCSR	/CAS set-up time(CBR cycle)	5	-	5	-	5	-	ns	
tCHR	/CAS hold time(CBR cycle)	15	-	15	-	15	-	ns	
tRPC	/RAS to /CAS precharge time	0	-	0	-	0	-	ns	
tCPT	/CAS precharge time(CBR counter test)	40	-	40	-	40	-	ns	
tCPWD	/WE delay time from /CAS precharge	30	-	35	-	40	-	ns	8
tRHCP	/RAS hold time from /CAS precharge	30	-	35	-	35	-	ns	

NOTE

1. An initial pause of 200μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS-only refresh cycles are required.
2. AC measurements assume tT=5ns
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.).
4. Measured at V_{OH}=2.0V and V_{OL}=0.8V with a load equivalent to 2TTL loads and 100pF.
5. tOFF(max.) defines the time at which the output achieves in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in read-modify-write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD(min.)}$, $t_{CWD} \geq t_{CWD(min.)}$, $t_{AWD} \geq t_{AWD(min)}$, and $t_{CPWD} \geq t_{CPWD(min.)}$, the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.)=64ms is applied to L-parts only.(HY531000ALS and HY531000ALJ)

CAPACITANCE

(T_A = 25°C, V_{CC} = 5V ± 10%, V_{SS} = 0V and f=1MHz, unless otherwise noted.)

Symbol	Parameter	Typ.	Max	Unit
C_{IN1}	Input Capacitance (A0~A9)	-	5	pF
C_{IN2}	Input Capacitance (/RAS, /CAS, /WE)	-	7	pF
C_{OUT}	Data Output Capacitance (Q)	-	7	pF