HYUNDAI

16Mbit Synchronous DRAM Series

HY57V164010- 4Mx4bit Synchronous DRAM
HY57V168010- 2Mx8bit Synchronous DRAM
HY57V161610- 1Mx16bit Synchronous DRAM

DESCRIPTION

The HY57V164010, HY57V168010, HY57V161610 are high speed 3.3 Volt synchronous dynamic RAMs organized as 2Mbit x 2bank x 4 I/O, 1Mbit x 2bank x 8 I/O, 512Kbit x 2bank x 16 I/O, respectively and fabricated with the Hyundai CMOS process. This dual bank circuit share the same chip inputs and outputs but otherwise can be independently operated. These devices are compatible with the JEDEC functional description and pinout, offering fully synchronous operation. All address, data and control inputs are latched on the rising edge of the master clock input. The data paths are internally pipelined to achieve very high bandwidth.

Programmable options include the length of pipeline(Read latency of 1,2, or 3), the number of consecutive read or write cycles initiated by a single control command(Burst length of 1,2,4,8, or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle.(This pipelined design is not restricted by a `2N` rule.)

The synchronous DRAM also allows both Auto refresh and self refresh. All input and output voltage levels are LVTTL compatible.

FEATURES

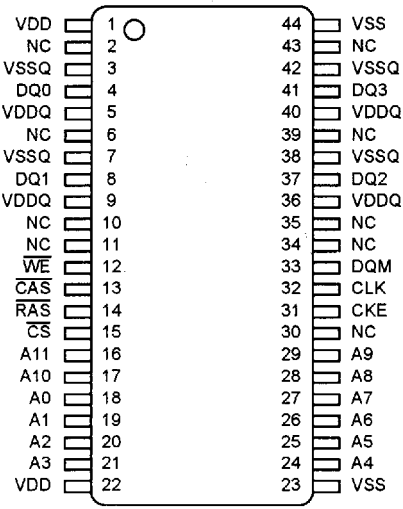
- Fully synchronous ; all inputs referenced to positive edge of system clock
- Dual internal banks with single pulsed $\overline{RAS}$
- Auto precharge/precharge all banks by A10 flag
- Single 3.3V±0.3V power supply
- All device pins are LVTTL compatible
- 400mil 44pin/ 50pin TSOP(II) with 0.8mm of lead pitch (Lead-On-Chip)
- 4096 refresh cycles every 64ms
- Possible to assert random column address every clock cycle
- Interleaved auto refresh mode
- Programmable burst lengths and sequences
  - 1,2,4,8,full page for Sequential type
  - 1,2,4,8 for Interleave type
- Programmable $\overline{CAS}$ latency ; 1,2,3 clocks
- Support clock suspend/power down mode by CKE
- Data mask function by DQM or UDQM/LDQM
- Mode register set programming
- Burst termination command
- Meets all the other JEDEC specifications
- Self refresh provides minimum power, full internal refresh control

ORDERING INFORMATION

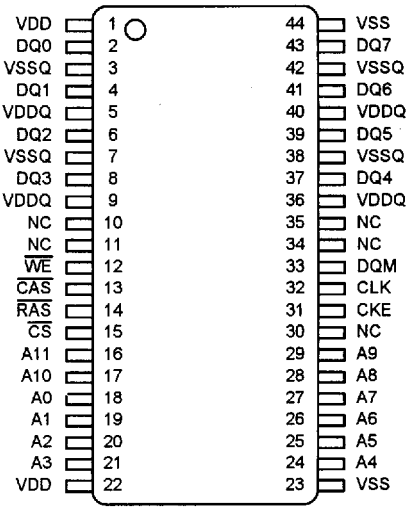
Part No.	Max. Frequency	Package	Remark
HY57V164010ATC -10/12/15	100/83/67MHz	400mil TSOP-II	x4, 4K Ref., LVTTL
HY57V164010ALTC -10/12/15	100/83/67MHz	400mil TSOP-II	x4, 4K Ref., L-part, LVTTL
HY57V168010ATC -10/12/15	100/83/67MHz	400mil TSOP-II	x8, 4K Ref. , LVTTL
HY57V168010ALTC -10/12/15	100/83/67MHz	400mil TSOP-II	x8, 4K Ref., L-part, LVTTL
HY57V161610ATC -10/12/15	100/83/67MHz	400mil TSOP-II	x16, 4K Ref. , LVTTL
HY57V161610ALTC -10/12/15	100/83/67MHz	400mil TSOP-II	x16, 4K Ref., L-part, LVTTL

PIN CONTENTION

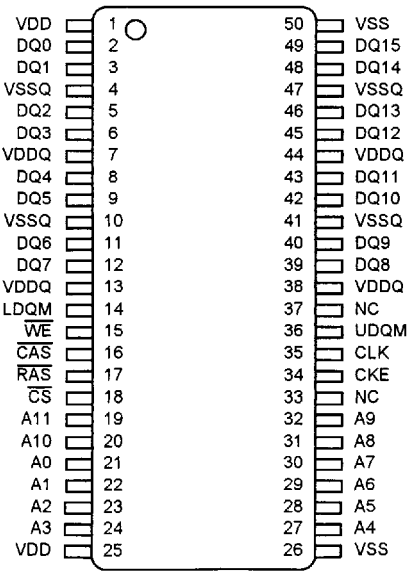
4Mx4 Synchronous DRAM
400mil x 725mil
44pin TSOP-II



2Mx8 Synchronous DRAM
400mil x 725mil
44pin TSOP-II



1Mx16 Synchronous DRAM
400mil x 825mil
50pin TSOP-II



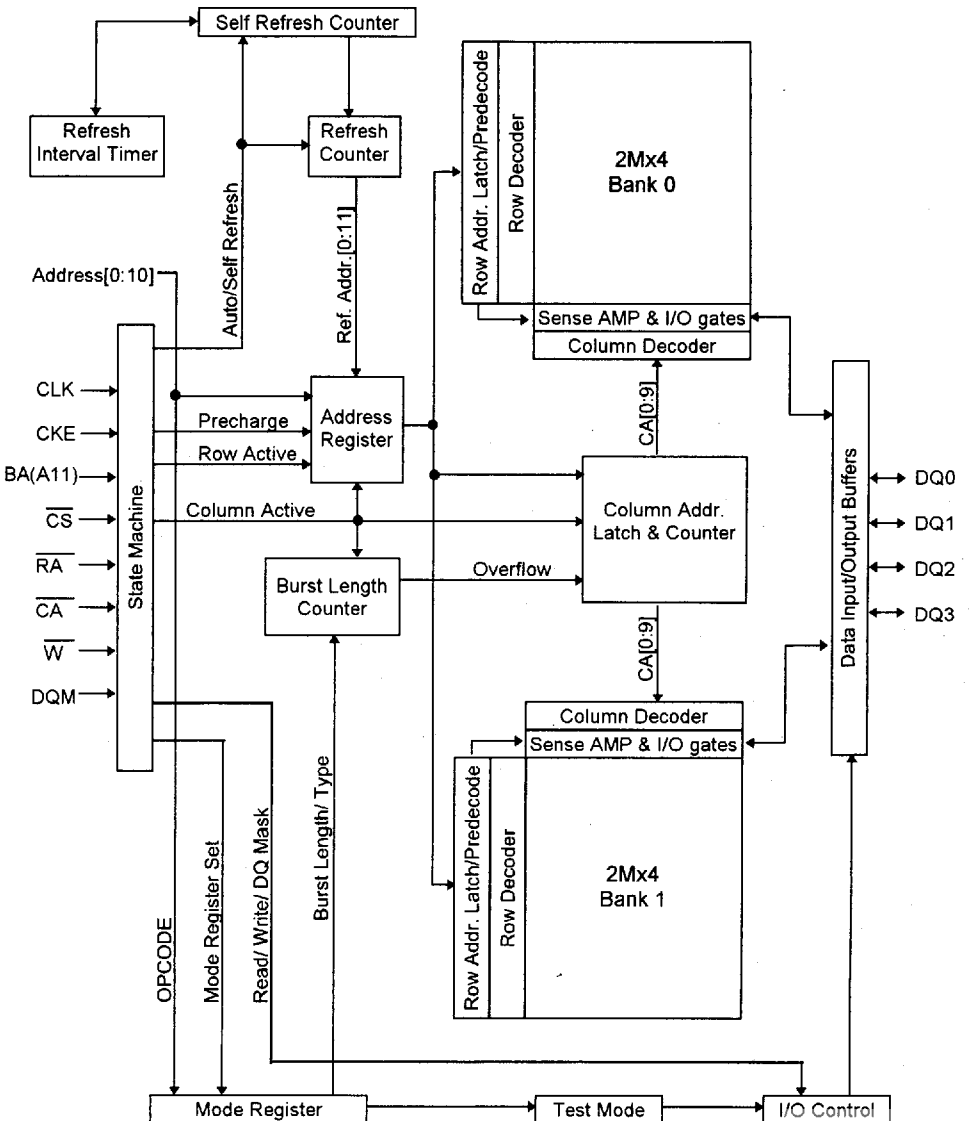
PIN DESCRIPTION

Pin Number		Pin Name	Pin Type	Description
x4/x8	x16			
32	35	CLK	Input	System clock Input; All other inputs except CKE are registered to the SDRAM on the rising edge of CLK.
31	34	CKE	Input	Clock enable; Controls internal clock signal and when deactivated, the SDRAM will be either one of the states among power down, suspend, or self refresh.
16	19	A11	Input	Bank select address(BA) ; Select either one of dual banks during both $\overline{RAS}$ and $\overline{CAS}$ activity.
17-21 24-29	20-24 27-32	A0-A10	Input	Address Inputs; Row&Column address : x4[A0-A9], x8[A0-A8], x16[A0-A7] Row address only : x4[A10], x8[A9-A10], x16[A8-A10] Precharge flag : A10 Opcode for mode register set : A0-A11
15	18	$\overline{CS}$	Input	Chip select; Functions command mask(NOP).
14	17	$\overline{RAS}$	Input	Row address strobe; See functional truth table for details.
13	16	$\overline{CAS}$	Input	Column address strobe; See functional truth table for details.
12	15	$\overline{W}$	Input	Write Enable; See functional truth table for details.
33	14,36	DQM LDQM,UDQM	Input	Data Input / Output Mask
Note 1	Note 1	DQ0-DQ3 DQ0-DQ7 DQ0-DQ15	Input/ Output	Data Input / Output; Include inputs, outputs, or Hi-z state.
5,9,36,40 3,7,38,42	7,13,28,44 4,10,41,47	V_{DDQ} V_{SSQ}	Supply for DQ	DQ Power Supplies
1,22	1,25	V_{DD}	Supply	Power Supplies; 3.3V$\pm$0.3V
23,44	26,50	V_{SS}	Supply	Ground

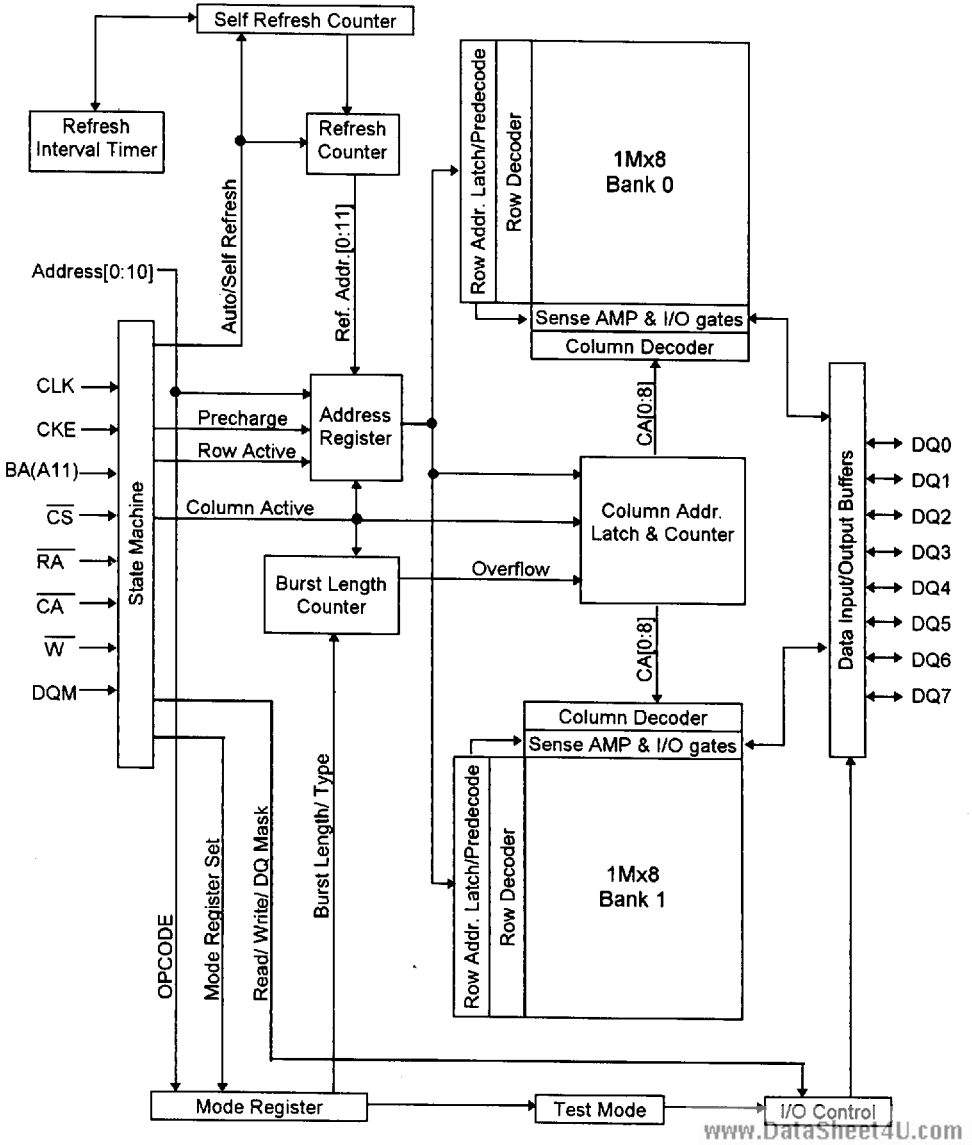
Note 1. DQ pin Number ;
x4 : 4,8,37,41
x8 : 2,4,6,8,37,39,41,43
x16 : 2,3,5,6,8,9,11,12,39,40,42,43,45,46,48,49

FUNCTIONAL BLOCK DIAGRAM

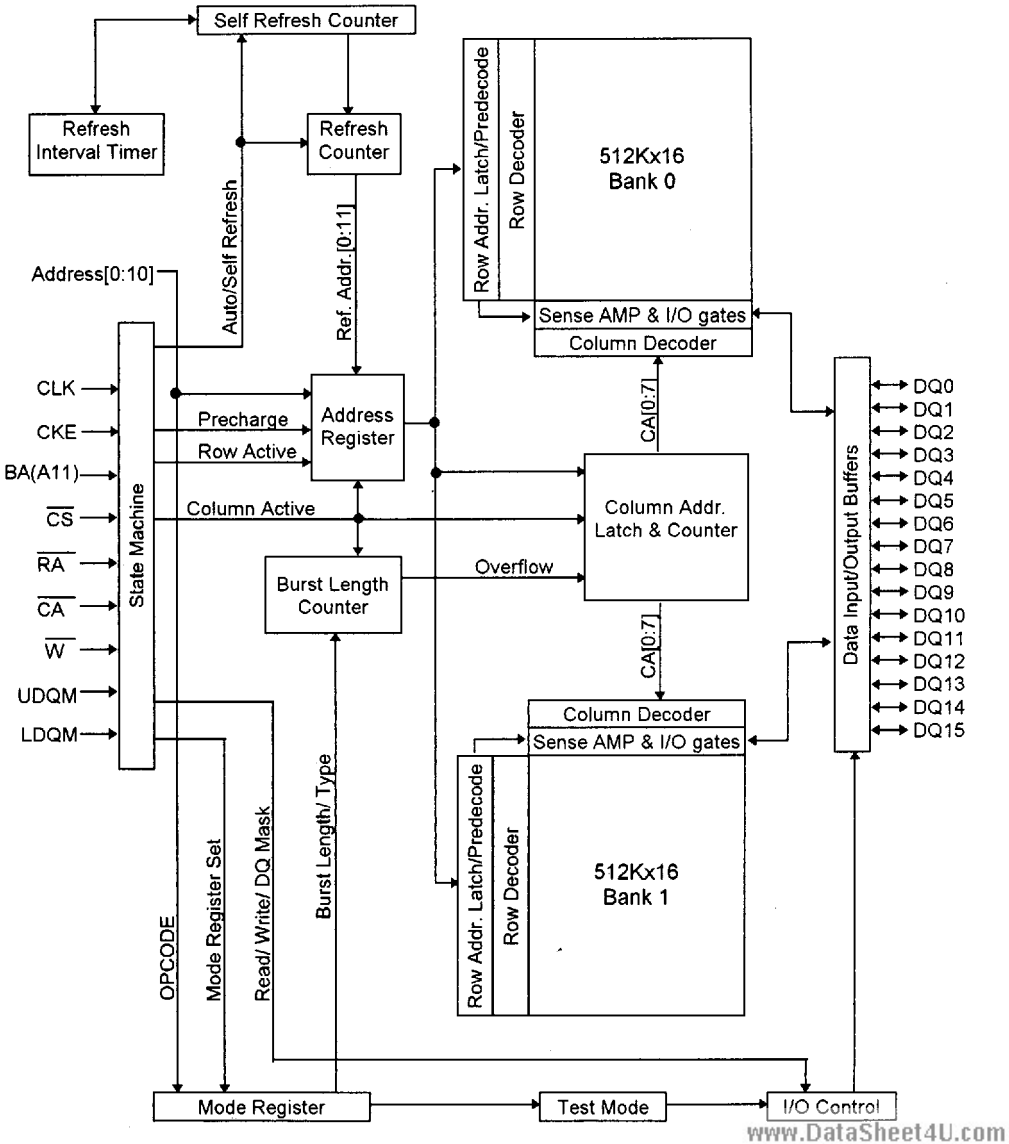
4Mx4 Synchronous DRAM



2Mx8 Synchronous DRAM



1Mx16 Synchronous DRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	-55 to 125	℃
V_{IN}, V_{OUT}	Voltage on Any Pin relative to Vss	-0.5 to 4.6	V
V_{DD}	Voltage on V_{DD} relative to Vss	-1.0 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	℃ · sec

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED AC OPERATING CONDITIONS*

(T_A=0℃ to 70℃, V_{DD}=3.3V±10%, Vss=0V)

Symbol	Parameter	Value	Unit
V_{IH} / V_{IL}	AC Input High/Low Level Voltage	2.4 / 0.4	V
Vtrip	Input Timing Measurement Reference Level Voltage	1.4	V
tr / tf	Input Rise/Fall Time	1 / 1	ns
Voutref	Output Reference Voltage	1.4	V
C_L	Output Load Capacitance for Access Time Measurement	Note1	pF

Notes: 1. Output load to measure access times(t_{AC}, t_{OH}, etc.) varies to clock frequency. A load is equivalent to one TTL gate and one capacitance.

RECOMMENDED DC OPERATING CONDITIONS*

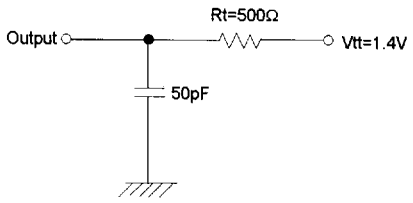
(T_A=0℃ to 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}, V_{DDQ}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.5	-	0.8	V

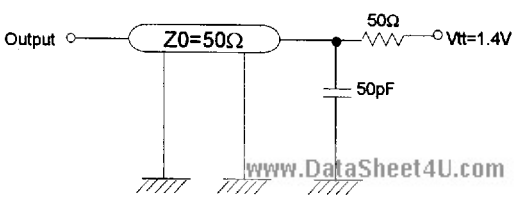
Notes: 1. All voltages are referenced to Vss.

Note: *

DC Output Load Circuit



AC Output Load Circuit



DC CHARACTERISTICS(I)

(T_A=0℃ to 70℃, V_{DD}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS}<V_{IN}<V_{DD}$+1.0 All other pins not under test=Vss	-5	5	μA
I_{LO}	Output Leakage Current (High impedance State)	$V_{SS}<V_{OUT}<V_{DD}$ Both Banks in idle state	-5	5	μA
V_{OL}	Output Low Voltage	I_{OL}=2.0mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=-2.0mA	2.4	-	V

DC CHARACTERISTICS(II)

(T_A=0℃ to 70℃, V_{DD}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter/Condition	t_{CLK}	Speed/Power-Max.			Unit	Note
			-10	-12	-15		
I_{DD1}	$\overline{RAS}$ Operating Current per bank No $\overline{CAS}$ activity, t_{RC}=t_{RC}(min)	min	100	80	75	mA	1,2
I_{DD2PD}	Precharge Stand-by Current in Power-Down Mode, CKE<V_{IL}(max)	min ∞	3 2	3 2	3 2	mA	
I_{DD2NP}	Precharge Stand-by Current in Non Power-Down Mode, CKE>V_{IH}(min)	min ∞	20 15	20 15	20 15	mA	3
I_{DD3PD}	Active Stand-by Current in Power-Down Mode, CKE<V_{IL}(max)	min ∞	30 30	30 30	30 30	mA	4
I_{DD3NP}	Active Stand-by Current in Non Power-Down Mode, CKE>V_{IH}(min)	min ∞	50 30	50 30	50 30	mA	3,4
I_{DD4}	Burst Mode Operating Current($\overline{CAS}$ Lat.=3)	min	100	80	75	mA	2,5,6
I_{DD5}	Auto Refresh Operating Current, t_{RC}=t_{RC}(min)	min	100	80	75	mA	2
I_{DD6}	Self Refresh Operating Current, CKE<0.2V	- -	2 400	2 400	2 400	mA μA	 L-part

Notes :

1. `No $\overline{CAS}$ activity` means that the operating cycle activates row circuits only while it does not command any read or write cycle, what could be called, $\overline{CAS}$ activity.
2. All I_{DD} currents except I_{DDS} depend on cycle rate.
3. All input signals are toggled every other clock cycle.
4. Assuming that one bank is active.
5. These I_{DD} Parameters are dependent on output loading. Specified values are obtained with the outputs open.
6. Specified values are obtained with the timing that a burst cycle is completed upto its registered burst length without any interrupt cycle. Interrupted burst cycle may consume more power.

CAPACITANCE

(T_A=25℃, V_{DD}=3.3V, f=1MHz)

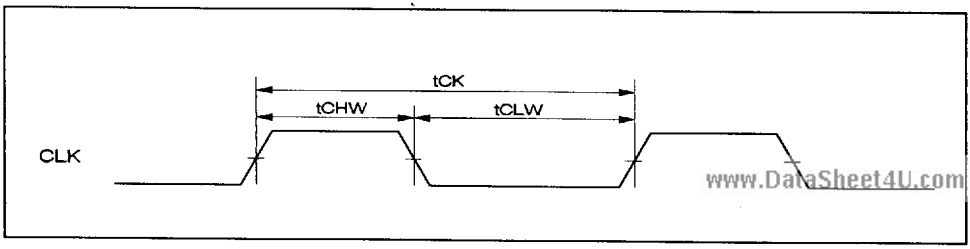
Symbol	Parameter	Pin	Typ.	Max.	Unit
C_{I1}	Input Capacitance	A0-A11	-	5	pF
C_{I2}	Input Capacitance	CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM(LDQM,UDQM)	-	5	pF
C_{OUT}	Output Capacitance	DQ0-DQ3, DQ0-DQ7, DQ0-DQ15	-	7	pF

AC CHARACTERISTICS

Synchronous Characteristics(I)[1,2,3,4]

#	Symbol	Parameter		-10		-12		-15		Unit	Note
				Min.	Max.	Min.	Max.	Min.	Max.		
1	tCK	System Clock Cycle Time	CAS Lat.= 3	10	-	12	-	15	-	ns	5
			CAS Lat.= 2	15	-	18	-	22.5	-	ns	5
2	tCHW	CLK High Level Width		3	-	4	-	5	-	ns	5
3	tCLW	CLK Low Level Width		3	-	4	-	5	-	ns	5
4	tAC	Access Time from Clock	CAS Lat.= 3	-	8	-	8.5	-	9	ns	50pF
			CAS Lat.= 2	-	9	-	9.5	-	10	ns	50pF
5	tAA	Read command to DQ access		-	20	-	25	-	30	ns	50pF
6	tAS	Address Set-up Time		3	-	3	-	3	-	ns	
7	tAH	Address Hold Time		1	-	1.5	-	1.5	-	ns	
8	tCKS	CKE set-up Time		3	-	3	-	3	-	ns	
9	tCKH	CKE Hold Time		1	-	1.5	-	1.5	-	ns	
10	tCS	Command Set-up Time		3	-	3	-	3	-	ns	
11	tCH	Command Hold Time		1	-	1.5	-	1.5	-	ns	
12	tDS	Data-in Set-up Time		3	-	3	-	3	-	ns	
13	tDH	Data-in Hold Time		1	-	1.5	-	1.5	-	ns	
14	tOH	Data-out Hold Time		3	-	3	-	3	-	ns	
15	tOLZ	Data-out Low-Z Time		2	-	2	-	2	-	ns	
16	tOHZ	Data-out High-Z Time	CAS Lat.= 3	-	8	-	8.5	-	9	ns	
			CAS Lat.= 2	-	9	-	9.5	-	10	ns	

Notes:
1. An initial pause of 200 μS is required after power-up by `Power On Sequence`(JEDEC Standard.) and Auto Refresh before proper device operation is achieved.
2. AC measurements assume tT=1ns
3. (VIH+VIL)/2 is a reference level for measuring of timing of input signals. Also transition time is measured between VIH and VIL.
4. Voutref is a reference level for measuring of timing of output signals.
5.



Synchronous Characteristics[1,2,3,4]

#	Symbol	Parameter	-10		-12		-15		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
1	tRC	Normal/Refresh cycle Time	100	-	108	-	120	-	ns	
2	tRCD	$\overline{RAS}$-to-$\overline{CAS}$delay Time	30	-	36	-	45	-	ns	3Clk
3	tRAS	Bank Active Time	60	10K	70	10K	80	10K	ns	
4	tRASP	Bank Active Time(full page)	60	400K	70	400K	80	400K	ns	
5	tRP	Bank Precharge Time	30	-	36	-	45	-	ns	
6	tRRD	Bank Active-to-Active Time	20	-	24	-	30	-	ns	
7	tWR	Write Recovery Time	10	-	12	-	15	-	ns	
8	tSRE	Self-Refresh Exit Time	10	-	12	-	15	-	ns	1Clk
9	tT	Transition Time	1	5	1	5	1	5	ns	
10	tPDE	Power Down Exit Time	3	-	4	-	5	-	ns	
11	tREF	Refresh Period	-	64	-	64	-	64	ms	

Notes:
1. An initial pause of 200 μS is required after power-up by `Power On Sequence`(JEDEC Standard.) and Auto Refresh before proper device operation is achieved.
2. AC measurements assume tT=1ns
3. (VIH+VIL)/2 is a reference level for measuring of timing of input signals. Also transition time is measured between VIH and VIL.
4. Voutref is a reference level for measuring of timing of output signals.

Latency - Fixed Parameters[1]

#	Symbol	Parameter		-10	-12	-15	Unit	Note
				Lat.	Lat.	Lat.		
1	tCKED	CKE to CLK Suspend or Power Down Mode Entry		1	1	1	Clk(s)	
2	tDQMOZ	DQM to Data Output in Hi-Z		2	2	2	Clk(s)	
3	tDQMIM	DQM to Data Input Mask		0	0	0	Clk(s)	
4	tWTL	Write command to Data Input Valid		0	0	0	Clk(s)	2
5	tPROZ	Precharge to Data Output in Hi-Z delay	$\overline{CAS}$ Lat.=1	1	1	1	Clk(s)	
			$\overline{CAS}$ Lat.=2	2	2	2	Clk(s)	
			$\overline{CAS}$ Lat.=3	3	3	3	Clk(s)	
6	tMRD	Mode Register Set to Bank Active		2	2	2	Clk(s)	
7	tCCD	$\overline{CAS}$-to-$\overline{CAS}$ command delay		1	1	1	Clk(s)	3

Notes :
1. The latency values in the above table are fixed regardless of clock cycle time.
2. `Write Latency` as JEDEC standard says.
3. Superset of `2N-rule .

STATE AND FUNCTIONAL TRUTH TABLE, OPERATIONS INVOLVING BOTH BANKS

Current State	CLK ↑									Action
	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11 (BA)	A10	A9-A0	
	Prev.	Curr.								
Power Down	L	L	X	X	X	X	X	X	X	Maintain Power Down
	L	H	L	H	H	H	X	X	X	Exit Power Down → BBI
	L	H	H	X	X	X	X	X	X	Exit Power Down → BBI
Self Refresh[1]	L	L	X	X	X	X	X	X	X	Maintain Self Refresh
	L	H	L	H	H	H	X	X	X	Exit Self Refresh → BBI
	L	H	H	X	X	X	X	X	X	
All Banks Idle (BBI)	H	L	L	H	H	H	X	X	X	Enter Power Down
	H	L	H	X	X	X	X	X	X	Enter Power Down
	H	L	L	L	L	H	X	X	X	Enter Self Refresh
	H	H	L	H	H	H	X	X	X	NOP
	H	H	H	X	X	X	X	X	X	Deselect
	H	H	L	L	L	L	OPCODE			Mode Register Access
	H	H	L	L	L	H	X	X	X	Auto Refresh
CLK Suspend	L	L	X	X	X	X	X	X	X	Maintain CLK Suspend
	L	H	X	X	X	X	X	X	X	Exit CLK Suspend
Auto Refresh	H	H	L	H	H	H	X	X	X	NOP→All Banks Idle After t_{RC}
	H	H	H	X	X	X	X	X	X	Deselect
Any state other than above	H	L	X	X	X	X	X	X	X	Suspend Clock, next Cycle → Clock Suspend
DQM	H	X	X	X	X	X	X	X	X	Write DQM Latency is 0, Read DQM Latency is 2.

Note: 1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high.

STATE AND FUNCTIONAL TRUTH TABLE, SELECTED BANK[1]

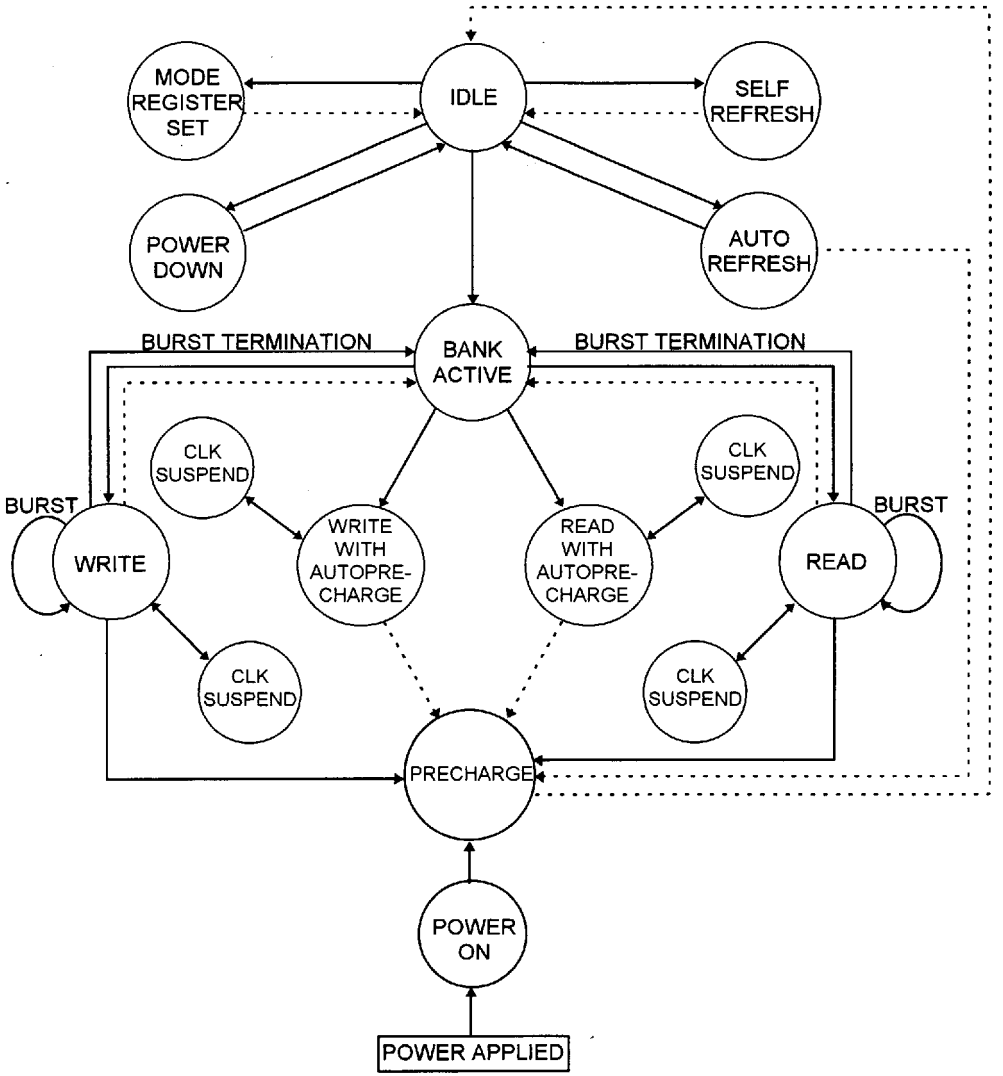
Current State of Selected Bank	CLK↑							Action to Selected Bank (Unless otherwise noted)
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11(BA)	A10	A0-A9	
Idle	L	L	L	L	OPCODE			Mode Register Access
	L	H	H	H	X	X	X	NOP
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	X	X	NOP
	L	L	L	H	X	X	X	Auto or Self Refresh
	L	L	H	H	BA	RA	RA	Activate Row
Row Active	L	L	L	X	X	X	X	ILLEGAL
	L	H	H	H	X	X	X	NOP
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	Precharge Selected Bank
	L	L	H	L	X	H	X	Precharge All Banks
	L	H	L	L	BA	L	CA	Begin Write
	L	H	L	L	BA	H	CA	Begin Write/Auto Precharge
	L	H	L	H	BA	L	CA	Begin Read
	L	H	L	H	BA	H	CA	Begin Read/Auto Precharge
Read	L	H	H	H	X	X	X	NOP(Continue burst to end → Row Active)
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	Precharge Selected Bank
	L	L	H	L	X	H	X	Precharge All banks
	L	L	L	X	X	X	X	ILLEGAL
	L	H	L	L	BA	L	CA	Begin Write[2]
	L	H	L	L	BA	H	CA	Begin Write/Auto Precharge[2]
	L	H	L	H	BA	L	CA	Begin New Read
	L	H	L	H	BA	H	CA	Begin New Read/Auto Precharge
	L	H	H	L	X	X	X	Term Burst → Row Active
Write	L	H	H	H	X	X	X	NOP(Continue burst to end → Row Active)
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	Precharge Selected Bank
	L	L	H	L	X	H	X	Precharge All banks
	L	L	L	X	X	X	X	ILLEGAL
	L	H	L	L	BA	L	CA	Begin New Write
	L	H	L	L	BA	H	CA	Begin New Write / Auto Precharge
	L	H	L	H	BA	L	CA	Begin New Read
	L	H	L	H	BA	H	CA	Begin New Read / Auto Precharge
	L	H	H	L	X	X	X	Term Burst → Row Active
Read with Auto Precharging	L	H	H	H	X	X	X	NOP, Continue burst to end → Precharge[3]
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	ILLEGAL
	L	L	H	L	X	H	X	ILLEGAL
	L	H	L	L	BA	L	CA	ILLEGAL
	L	H	L	L	BA	H	CA	ILLEGAL
	L	H	L	H	BA	L	CA	ILLEGAL
	L	H	L	H	BA	H	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL

Current State of Selected Bank	CLK↑							Action to Selected Bank (Unless otherwise noted)
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11(BA)	A10	A0-A9	
Write with Auto Precharging	L	H	H	H	X	X	X	NOP, Continue burst to end → Precharge[3]
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	ILLEGAL
	L	L	H	L	X	H	X	ILLEGAL
	L	H	L	L	BA	L	CA	ILLEGAL
	L	H	L	L	BA	H	CA	ILLEGAL
	L	H	L	H	BA	L	CA	ILLEGAL
	L	H	L	H	BA	H	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL
Precharging	L	H	H	H	X	X	X	NOP → Idle after t_{RP}
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	NOP
	L	L	H	L	X	H	X	NOP
	L	H	L	L	BA	L	CA	ILLEGAL
	L	H	L	L	BA	H	CA	ILLEGAL
	L	H	L	H	BA	L	CA	ILLEGAL
	L	H	L	H	BA	H	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
Row Activating	L	H	H	H	X	X	X	NOP→ Row active after t_{RCD}
	H	X	X	X	X	X	X	Deselect
	L	L	H	L	BA	L	X	ILLEGAL
	L	L	H	L	X	H	X	ILLEGAL
	L	H	L	L	BA	X	CA	ILLEGAL
	L	H	L	H	BA	X	CA	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL
	L	L	L	X	X	X	X	ILLEGAL
Mode Register Accessing	L	H	H	H	X	X	X	NOP
	H	X	X	X	X	X	X	Deselect
	L	L	H	H	X	X	X	ILLEGAL
	L	H	L	H	X	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	H	H	L	X	X	X	ILLEGAL

Notes:

1. Assume CKE high on the previous and current clock cycles.
2. Read burst must terminate one cycle before the start of a write sequence. This can be accomplished in one of two ways.
   First, if the last bit of the burst is output two cycles before the start of the write sequence, the burst will terminate. And the output will tristate, the internal read pipeline will be flushed during the cycle before the write command is issued.
   Second, the burst can be terminated by bringing DQM high and issuing a terminate burst command two cycles before the write command. This will also guarantee that the output will tristate and the read pipeline will be flushed during the cycle before the write command is issued.
3. While either bank is executing a Read or Write burst sequence with Auto Precharge selected, no Read or Write commands are allowed to the opposite bank.
4. X=Don`t care, L=Low, H=High, BA=Bank Address, RA= Row Address, CA=Column Address, Opcode=Operand Code, NOP=No Operation

STATE DIAGRAM(SIMPLIFIED)



Notes: ——→ By command Input
·····→ Automatic sequence after finishing the command

PROGRAMMABLE MODE REGISTER

MODE REGISTER SET

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	$\overline{CAS}$ Latency			BT	Burst Length		

A3	Burst Type
0	Sequential
1	Interleaved

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	Burst Length	Remark
0	0	0	1	Used
0	0	1	2	Used
0	1	0	4	Used
0	1	1	8	Used
1	0	0	16	Reserved
1	0	1	32	Reserved
1	1	0	64	Reserved
1	1	1	Full Page	Used[1]

Note : 1. Full page burst supports only sequential type.

TEST MODE

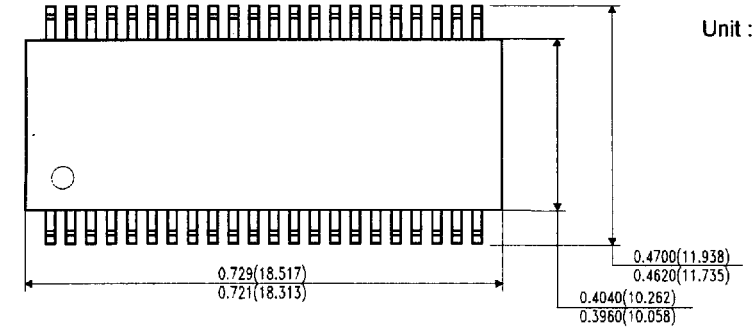
A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
X	X	X	X	1	X	X	X	X	X	X	X	Refresh Counter Test

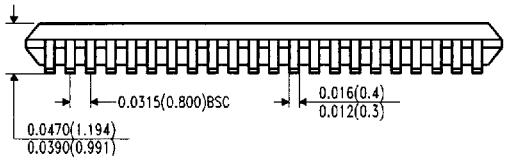
Note: Test Mode - Used to test the counter of Auto Refresh.
- Exit test mode using `Precharge All bank`.

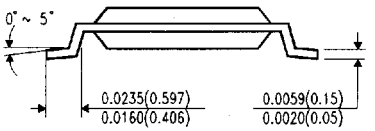
PACKAGE INFORMATION

400mil 44pin Thin Small Outline Package (TC)

4Mx4 Synchronous DRAM/ 2Mx8 Synchronous DRAM

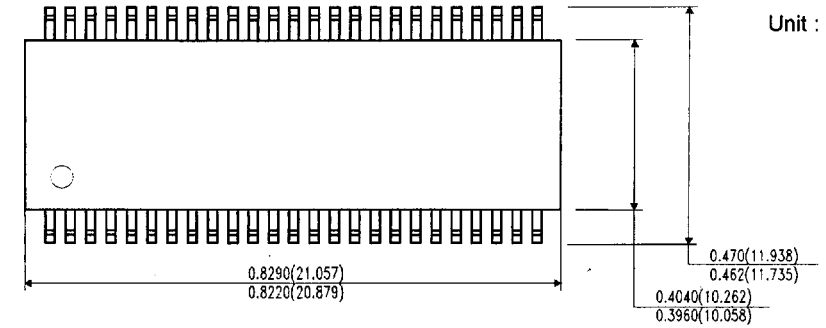


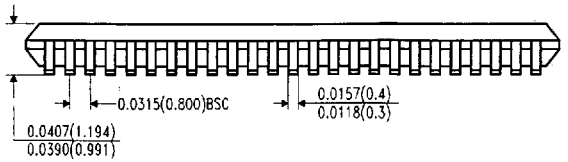


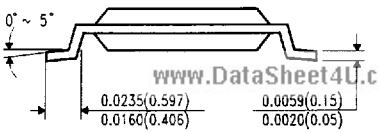


400mil 50pin Thin Small Outline Package (TC)

1Mx16 Synchronous DRAM







OPERATION(Cycle Description, Timing Overview)

1. Mode Register Access

1.1. Description of Register Functions

The SDRAM has an on-chip mode register which is programmed by the user to select the read latency, burst length, and burst type to be used during read/write operations to the DRAM.

To achieve very high data rates, the SDRAM is equipped with a read pipeline which can be programmed by the user to operate with one, two, or three cycles of clock latency. Read latency is defined as the number of the first positive clock edge following the initial read invocation cycle (which we arbitrarily define as cycle 0) at which the first piece of data is guaranteed to be valid. Figure 1 illustrates read latencies of one, two, and three. The higher the latency, the higher the clock frequency the SDRAM can run at, and the higher the peak data rate.

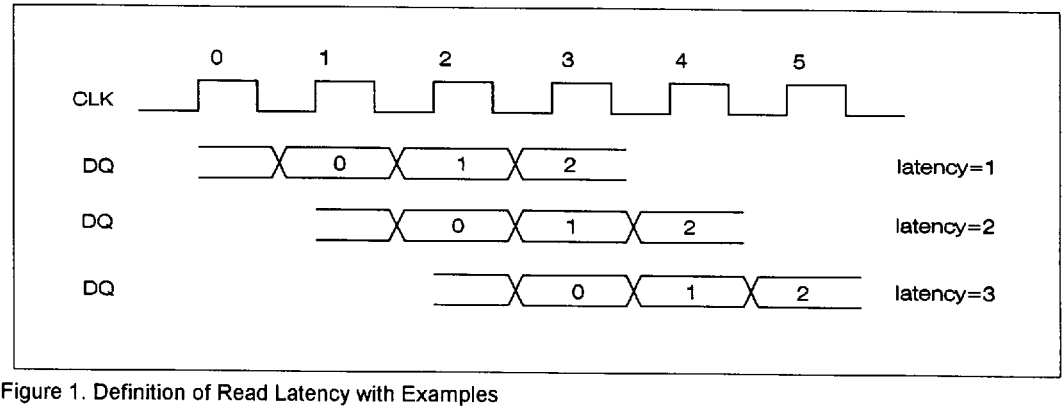


Figure 1. Definition of Read Latency with Examples

Whenever a read(or write) command is invoked, the SDRAM initiates a read(or write) to the appropriate column address selected by An^{1}-A0. This is defined as the beginning of the read(or write) burst. Subsequent clock cycles can be used to perform high speed read bursts (or write bursts) to column addresses adjacent to the column address supplied on An^{1}-A0 when the read or write was invoked. The number of column addresses which can be read or written, including the original address supplied on An^{1}-A0 is defined as the burst length. The SDRAM supports burst lengths of one, two, four, eight, or a full page of column addresses.

The SDRAM supports both sequential and interleaved mode address bursting. In burst mode, read or write is done to the address selected by An^{1}-A0 at the beginning of the burst. On successive burst cycles, the column address is internally incremented and a read(or write) is performed to the incremented address. Table 1 shows the sequence of burst addressing for burst lengths of two, four, eight, and full page.

Note : 1. Number of column address depends on data I/O width(Data I/O organization).
4Mx4: An=A9, 2Mx8: An=A8, 1Mx16: An=A7

Burst Length	Initial Address	Burst Type	
	A2 A1 A0	Sequential	Interleave
2	X X 0	0,1	0,1
	X X 1	1,0	1,0
4	X 0 0	0,1,2,3	0,1,2,3
	X 0 1	1,2,3,0	1,0,3,2
	X 1 0	2,3,0,1	2,3,0,1
	X 1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
	0 1 0	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
	0 1 1	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
	1 1 0	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
	1 1 1	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0
Full page	Note	0,1,2,3,4,~~~,m 1,2,3,4,5,~~~,0 : : m,0,1,2,3,~~~,m-1	Not supported

Table 1. Address sequence for different burst lengths

Note : 4Mx4 - Initial address: A9-A0, Page length: 1024, m=1023
2Mx8 - Initial address: A8-A0, Page length: 512, m= 511
1Mx16 - Initial address: A7-A0, Page length: 256, m= 255

1.2. Mode Register Set

Figure 2 shows the general timing and control for loading the mode register.

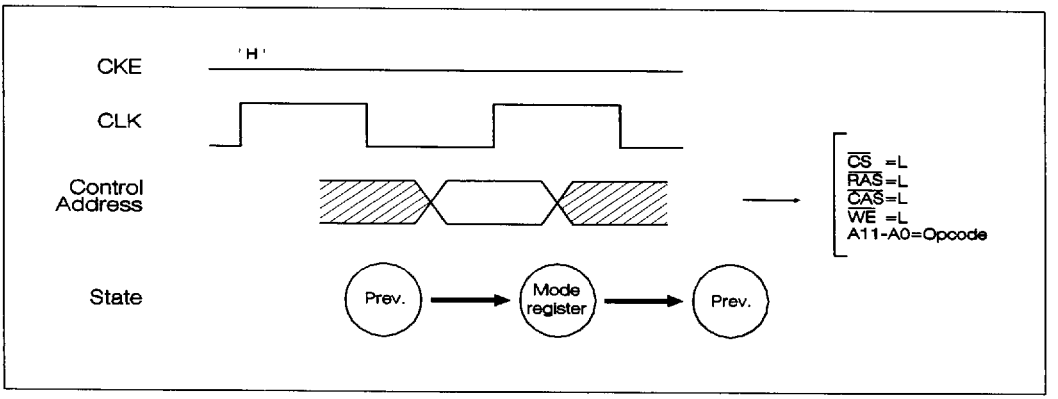


Figure 2. Timing of mode register set (program latency and burst).

2. Row Activate

A single row in either bank of DRAM can be activated using a row active command. A bank can be activated even when the opposite bank is active. A row active command cannot be given to a bank if that bank is already active. Also, a row active command cannot be given to either bank if the SDRAM is currently in the power down, self refresh, auto refresh (for the period specified by t_{RC}), or clock suspend states. Once a row active command has been issued to the bank selected by the bank address (supplied by A11(BA)), the selected bank leaves its idle state and goes into its row activating state. Accordingly, the row address is latched and the appropriate row in the bank selected. Data from that row of memory is sensed and latched by the bank`s sense amplifiers, to be used for later read(or write) operations. During the row activating period, defined by timing parameter t_{RCD}, only NOP cycles can be executed on the selected bank. After the period t_{RCD}, selected bank is in the row active state. Figure 4 shows a row activation cycle. Once in the row active state, the user can initiate a read or write burst, or can precharge the bank back to its idle state.

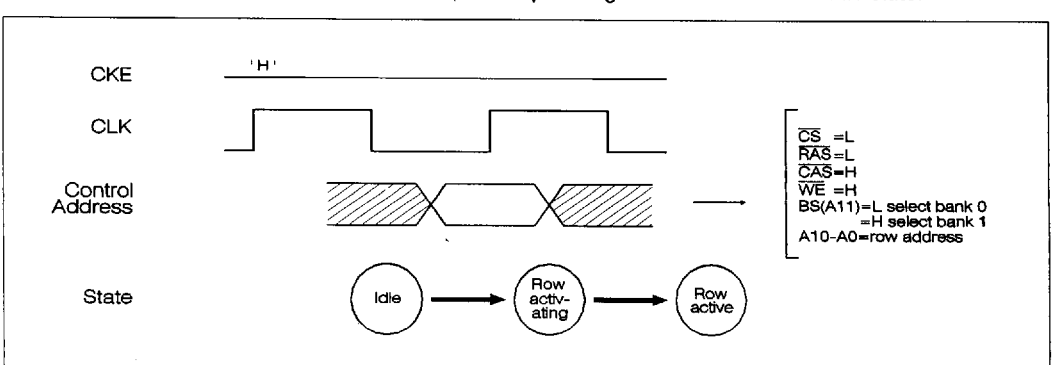


Figure 4. Row Active command to idle bank.

3. Read Operation with Programmable Pipeline

3.1. Normal Read Bursts(Auto Precharge Deselected)

Figure 5 shows the basic timing and control for initiating a burst read operation without Auto Precharge selected. Output of data depends on the read latency, burst length, and burst type selected(See Section 1., Mode Register Access, for details). The higher the latency, the higher the operating frequency the SDRAM can run at, and the higher the peak data rate. See Table 2 and Figures 17 through 19 for details. Figures 17 through 19 illustrate burst writes following burst read on the same page. The examples assume a burst length of four but burst lengths of 1, 2, 4, 8, or full page can also be used. By issuing NOPs after the initial read command, the SDRAM will continue reading data starting from the starting column address to the end of the read burst. Data will be read to the DQ outputs(assuming DQM remains disabled low) until the last address in the burst, defined by the burst length and type has been read out. On the next clock cycle, the DQ outputs will go to Hi-Z and the bank will re-enter the row active state .

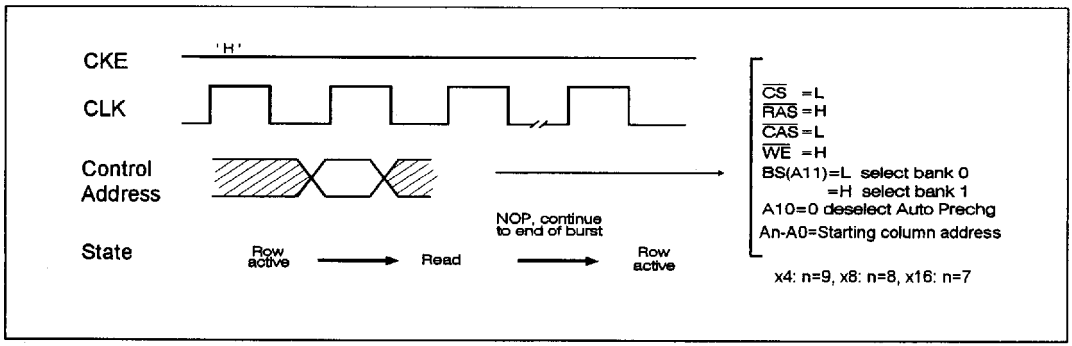


Figure 5. Burst read sequence, Auto Precharge Deselected.

While in a read burst with Auto Precharge deselected, the user can issue the following command sequences:

1. Issue NOPs, continue reading data starting from the starting column address to the end of the read burst. Data will be read to the DQ outputs(assuming DQM remains disabled low) until the last address in the burst, defined by the burst length and type, has been read out. On the next clock cycle, the DQ outputs will go to Hi-Z and the bank will re-enter the row active state.
2. Initiate another read command (with or without Auto Precharge selected) before the end of the burst and begin a new read burst starting from another column address. The burst in progress is terminated and the first address of the new burst is read to the output after a number of clock cycles defined by the $\overline{CAS}$ latency. See Figure 6 for details.
3. Initiate a write command with or without Auto Precharge selected before the end of the burst and begin a write burst starting from another column address. The burst in progress is terminated and the first address of the new burst is initiated. Figure 7 illustrates the timing and control for this sequence. The appropriate DQMi read/write byte enable signals must be asserted two clock cycles before the write command is issued (JEDEC specifies DQM latency is always two regardless of the $\overline{CAS}$ latency.This needs further clarification from users.)
4. Issue a terminate burst command and return to the row active state. The timing and control for this sequence is shown in Figure 8 for the case where $\overline{CAS}$ latency is three and burst length is greater than four. Note that in this example the terminate burst command occurs on the third clock cycle after the initial read command. Currently, the SDRAM is defined such that the terminate burst command initiates the burst terminate such that the data associated with the burst counter address at the beginning of the burst terminate cycle (M3 in Figure 8) is output to DQ after the number of clock cycles defined by the clock latency. On the next clock cycle, DQ goes to Hi-Z and the bank goes to the row active state. This last bit read out upon a terminate burst cycle is the subject of some controversy and needs clarification from customers whether or not the data stream should end one cycle earlier.

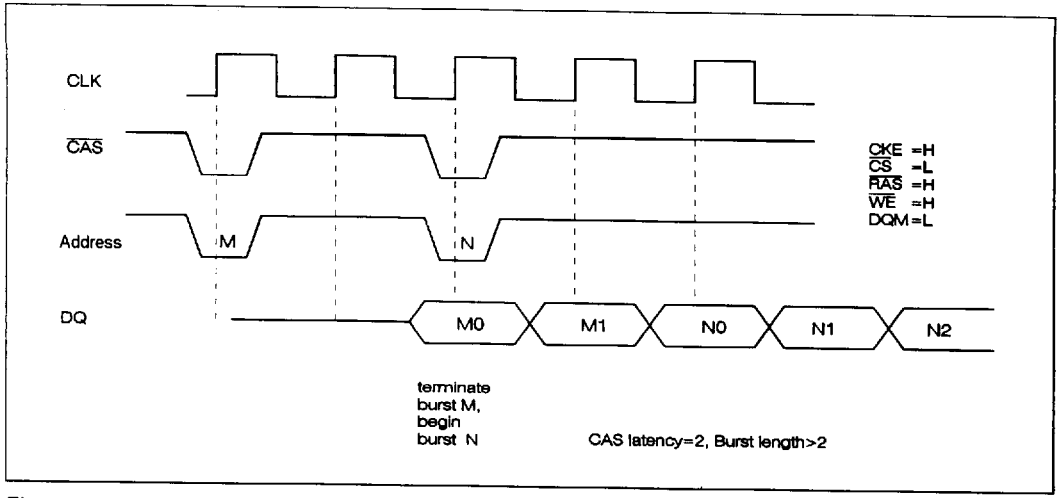


Figure 6. Timing of read initiation with read burst in progress.

5. Issue a precharge command(for only the selected bank or for both banks, depending on the logic level of A10), terminate the burst, and return to the idle state after the precharge interval. Like the terminate burst command, the last data read out is that associated with burst address during the precharge command cycle. The major difference between a precharge command and a burst terminate command is that the burst terminate command returns the bank to its row active state while the precharge command returns the bank to its idle state after the designated precharge interval. The timing and control for the precharge cycle is shown in Figure 9 for the case where $\overline{CAS}$ latency is two and burst length is greater than four. Like the burst terminate the last data read out is the subject of controversy and needs clarification from customers whether or not the data stream should end one cycle earlier.

6. Suspend the clock. While in the clock suspended state, the state of both banks will remain unchanged.

Maximum Frequency	50MHz	66MHz	83MHz	100MHz
CLK cycle time	20ns	15ns	12ns	10ns
$\overline{CAS}$ Latency (20ns)	2 cycles	2 cycles	2 cycles	3 cycles
tRCD Min. (30ns)	2 cycles	2 cycles	3 cycles	3 cycles
$\overline{RAS}$ to precharge (70ns)	4 cycles	5 cycles	6 cycles	7 cycles
$\overline{RAS}$ precharge (30ns)	2 cycles	2 cycles	3 cycles	3 cycles
$\overline{RAS}$ cycle time (100ns)	6 cycles	7 cycles	9 cycles	10 cycles

Table 2. Performance Parameters and Frequency vs. Clock Latency(-10part)

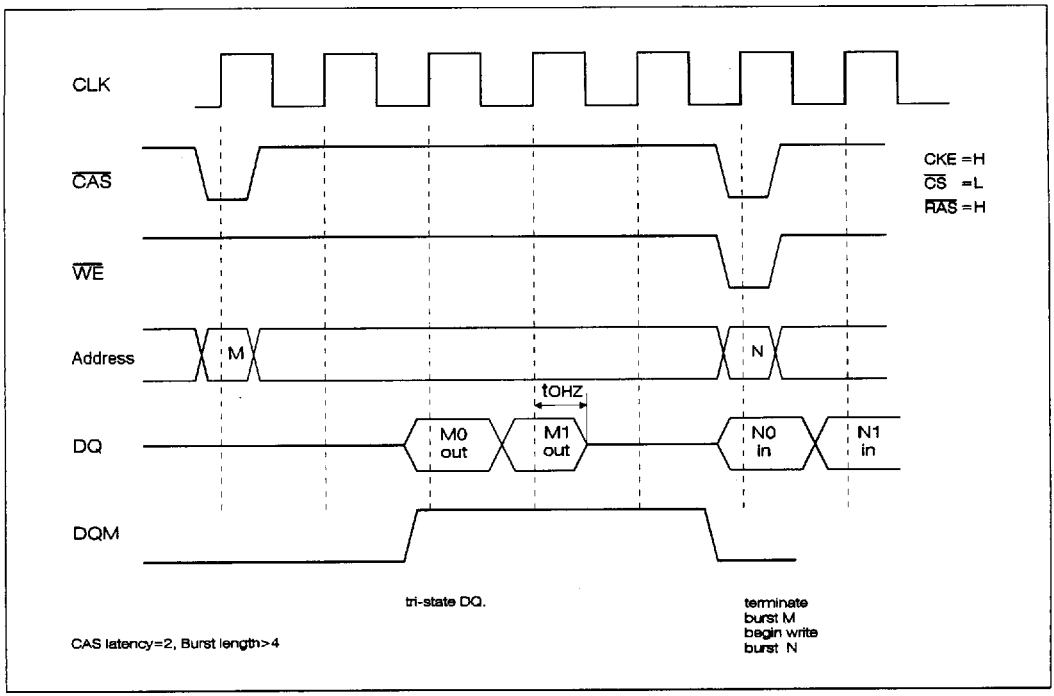


Figure 7. Timing of write initiation with read burst in progress.

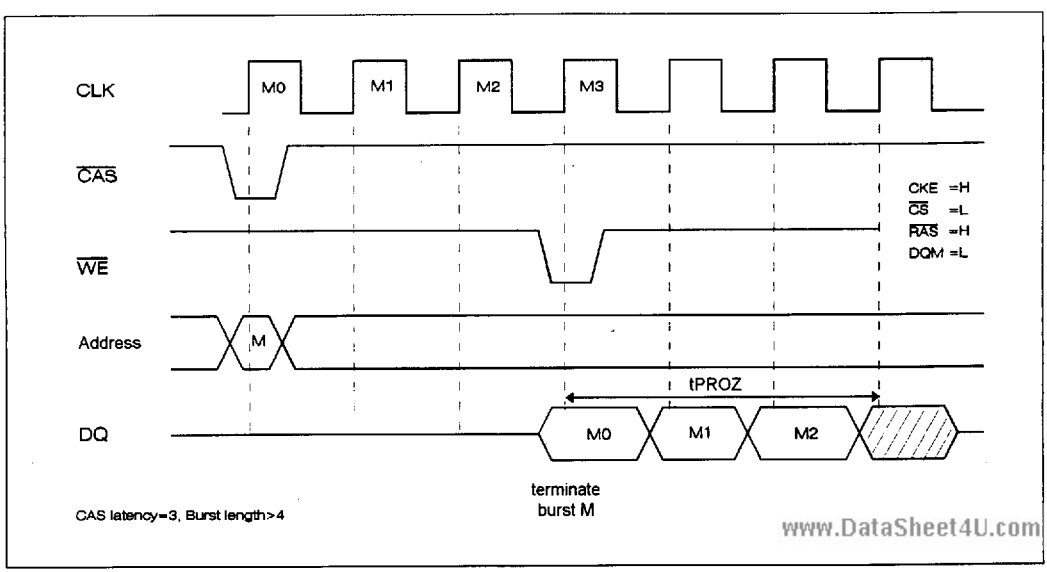


Figure 8. Timing of burst terminate command with read burst in progress.

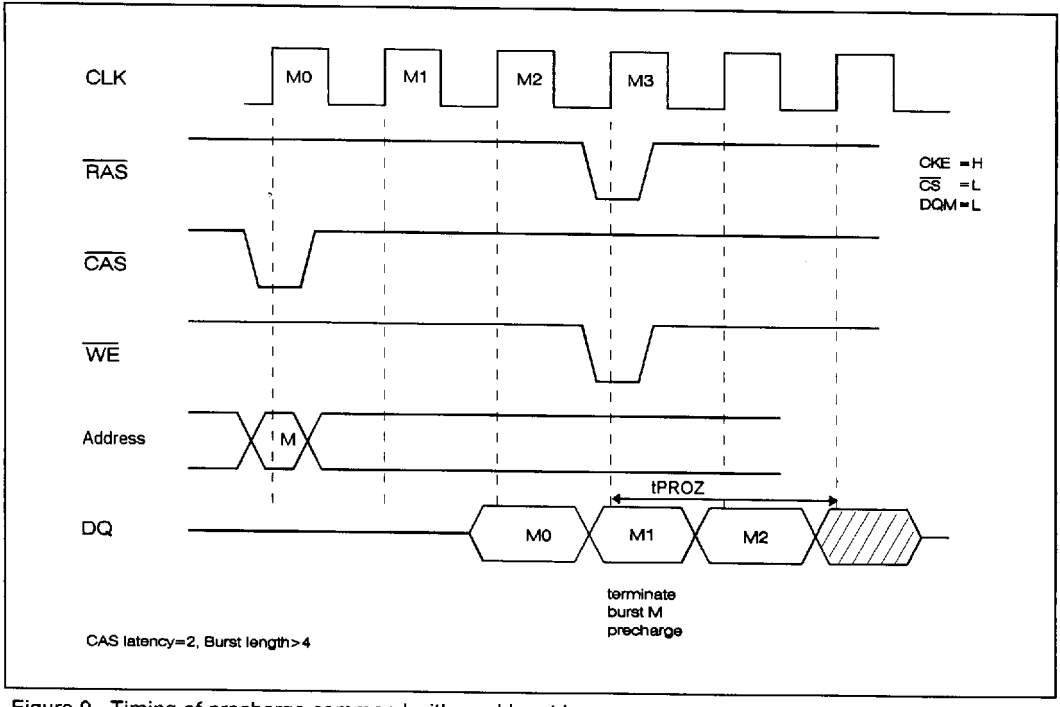


Figure 9 . Timing of precharge command with read burst in progress.

3.2. Read Bursts with Auto Precharge Selected.

Read with Auto Precharge operation is similar to normal read(Auto Precharge deselected) operation except that the read burst cannot be terminated by issuing another command. Once the read with Auto Precharge command is invoked in a bank, only NOP commands can be issued to that bank. After the data from the last address in the burst sequence has been read out according to the selected $\overline{CAS}$ latency, burst length, and burst type, the bank will enter precharge and return to the idle state after the t_{RP} period has expired. Figure 10 illustrates a burst read sequence with Auto Precharge selected for the case where $\overline{CAS}$ latency is two and burst length is two .

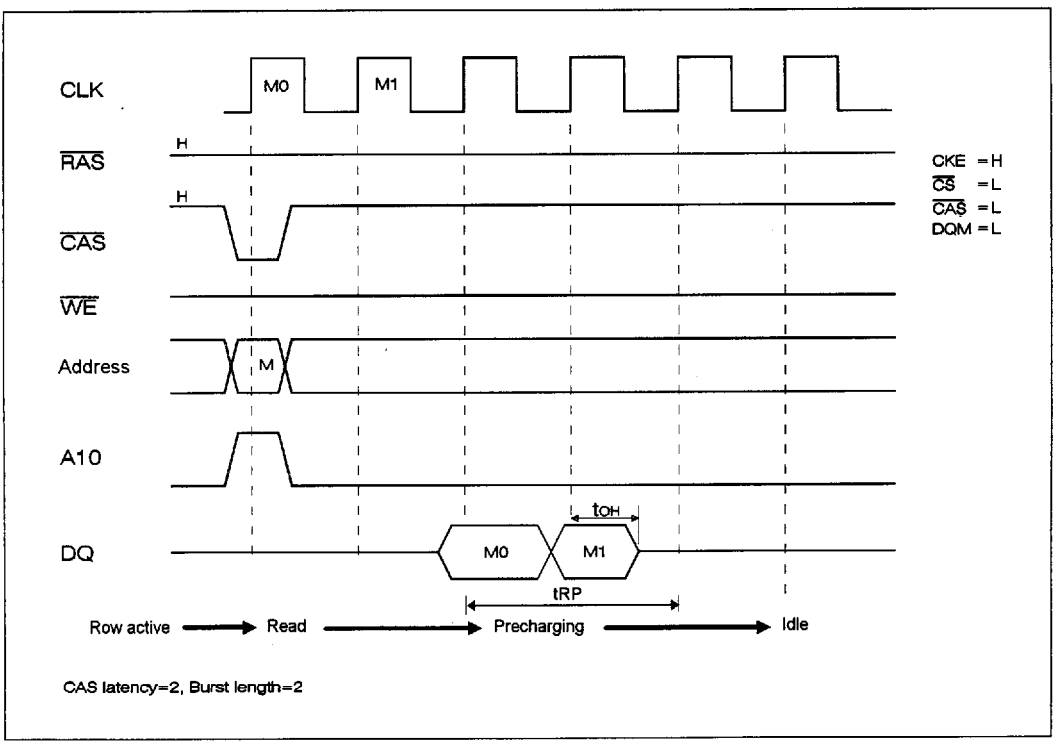


Figure 10. Read burst with Auto Precharge selected

4. Write Operation

There are several variations of write operation to the two banks of DRAM. Write bursts can be initiated to either bank with and without Auto Precharge selected. The basic write operation showing the relationship to the programmed burst length, and burst mode will be described first, and the variations for Auto Precharge will be described subsequently.

4.1. Writ e Operation with Auto Precharge Deselected

The latency for write operation is defined as the clock cycle difference between the clock where write command and column address are asserted and the clock cycle where the first data to be written is presented and is always equal to zero. That is the data for a write operation presented on the same clock cycle as its corresponding address, regardless of what value of $\overline{CAS}$ latency is programmed into the mode register. Figure 11 shows this relationship.

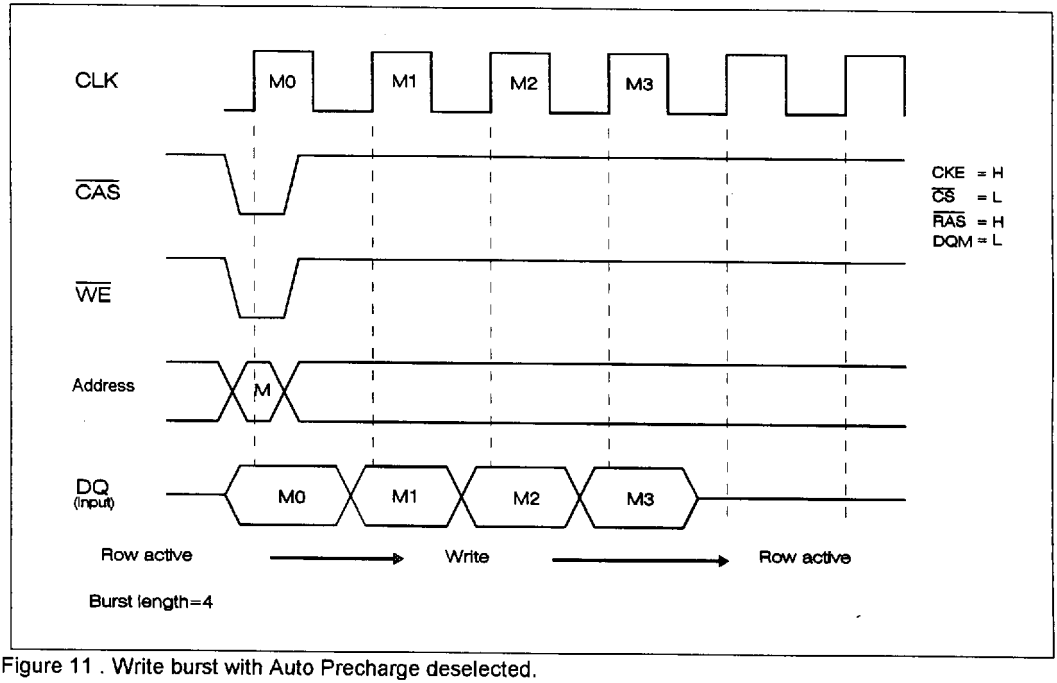


Figure 11 . Write burst with Auto Precharge deselected.

4.2. Write Operation with Auto Precharge

Write operation with Auto Precharge is similar to write operation without Auto Precharge except that once initiated the write burst cannot be terminated by another command. To complete the burst, NOPs must be executed and data input supplied for each address in the burst until the end of the burst has been reached. On the clock cycle following the last address in the burst, the bank will begin precharging and will re-enter the idle state after the precharge period, t_{RP}. Figure 12 illustrates the sequence.

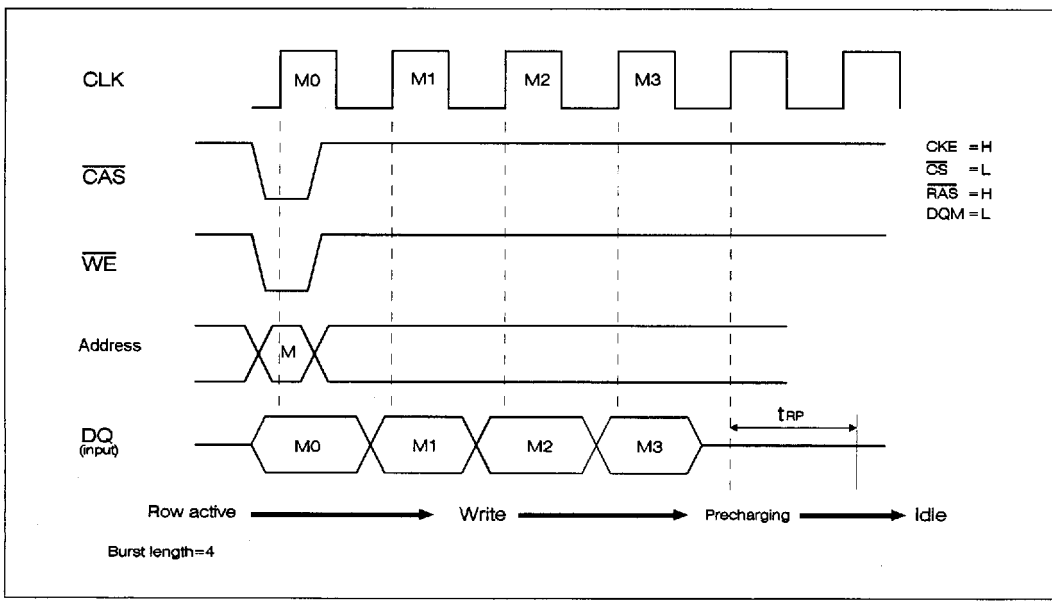


Figure 12. Write burst with Auto Precharge selected.

5. Refresh Operation

Since the SDRAM is a dynamic memory device, the stored data must be refreshed periodically or will be lost. To avoid data loss, all rows in both banks must be accessed during the maximum refresh interval specified by tREF. A row of data in either bank of RAM is refreshed whenever that row is activated. For example, activating a row for the purpose of reading or writing addresses along that row causes the data in that row to be refreshed. In addition to normal read and write operation, the SDRAM has two modes of refreshing the banks of memory: Auto Refresh and Self Refresh.

5.1. Auto Refresh

Auto Refresh is similar to $\overline{CAS}$ before $\overline{RAS}$ refresh found on previous generation asynchronous DRAMs. One Auto Refresh cycle refreshes one row of memory using 12 bits for 4K refresh parts(11 bits for 2K parts) on-chip refresh counter as the row address and bank select. The refresh counter is incremented during each Auto Refresh cycle. The upper 11 bits of the counter supply the address of one of the 2048 rows in each bank to be refreshed and the least significant bit selects the bank in which the refresh will occur. Thus, successive Auto Refresh cycles alternate between the two banks. Because Auto Refresh operation alternate between banks, both banks must be idle when Auto Refresh commands are invoked. Figure 13 shows two successive Auto Refresh cycles. Once an Auto Refresh cycle has been invoked, it is controlled internally until its duration. NOP cycles must be inserted during the entire Auto Refresh cycle time defined by tRC.

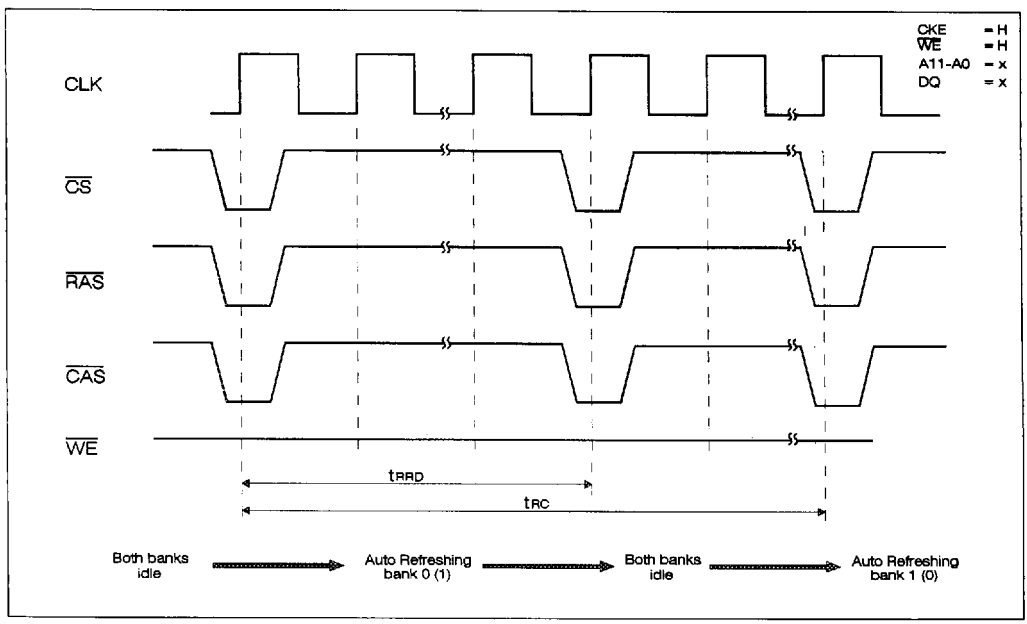


Figure 13. Timing and control for Auto Refresh Operation

5.2. Self Refresh

The SDRAM features an on-chip refresh cycle timing generator which can be used in conjunction with the row refresh counter(described in Section 5.1.) to completely refresh the two banks of DRAM entirely under internal control. Self Refresh can be invoked only when both banks are idle. While the device is in Self Refresh mode, CKE is the only enabled input to the device. All other inputs, including the clock are disabled and any input is ignored. Self Refresh mode is entered by invoking an Auto Refresh command with CKE low transition. Once this command is invoked, the cycle timing generator performs a burst refresh sequencing through all 4096 rows (2048 rows in each bank) with a per row refresh cycle time of approximately 1 microsecond. To conserve power, once the burst refresh has been completed to all 4096 rows the cycle timing generator automatically slows down to a per row refresh period of approximately 32 microseconds and refresh operation continues until Self Refresh mode is exited.(Important : The internal per row refresh cycle times are not guaranteed.) Upon exiting Self Refresh mode, the time elapsed since the least recently refreshed row was refreshed can vary from a few milliseconds to 32 milliseconds. Consequently, to be sure that all DRAM rows remain refreshed it is recommended that a burst of 4096 Auto Refresh commands be performed immediately after exiting Self Refresh mode. Self refresh mode is exited by starting the clock (if the clock had stopped) and then asserting CKE after the clock wave form has stabilized. The low-to-high transition of CKE will re-enable the clock and other inputs asynchronously. A minimum time, specified by tSRE, must be satisfied before any command other than Exit Self Refresh is invoked. Figure 14 shows how Self Refresh mode is entered and exited.

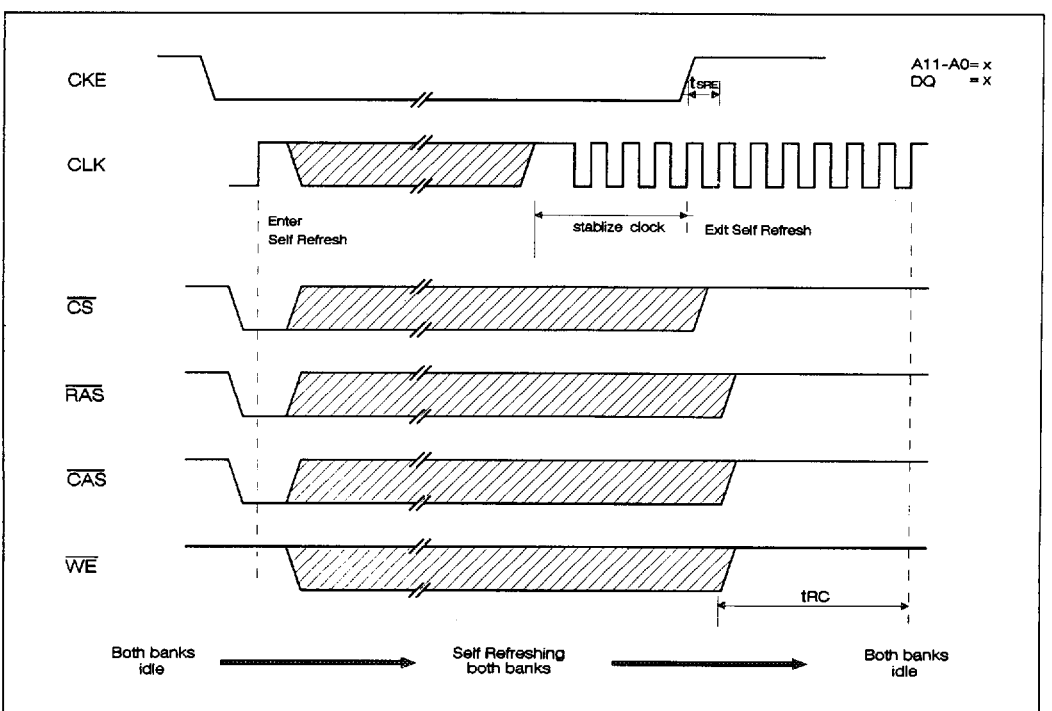


Figure 14. Timing and control for Self Refresh Operation

6. Power Down

The SDRAM has two internal clock buffers. A low current capacity clock buffer feeds the CKE input buffer while a high current clock buffer feeds the state machine and all DRAM circuits. During the Power Down state, the large clock buffer is disabled but the small clock buffer is not. In contrast to the Self Refresh state, entering and exiting Power Down is completely synchronous with respect to CKE. That is, CKE is sampled on every clock cycle, rather than asynchronously changing the state of the SDRAM Power Down is the lowest power state available. During Power Down, the SDRAM is not refreshed. Therefore, the minimum refresh specification still applies during power down. Figure 15 shows an example of the timing and control for entering and exiting Power Down. Exiting Power Down requires one clock cycle, as shown in the figure. Other commands can be issued on the clock cycle following the Exit Power Down command cycle.

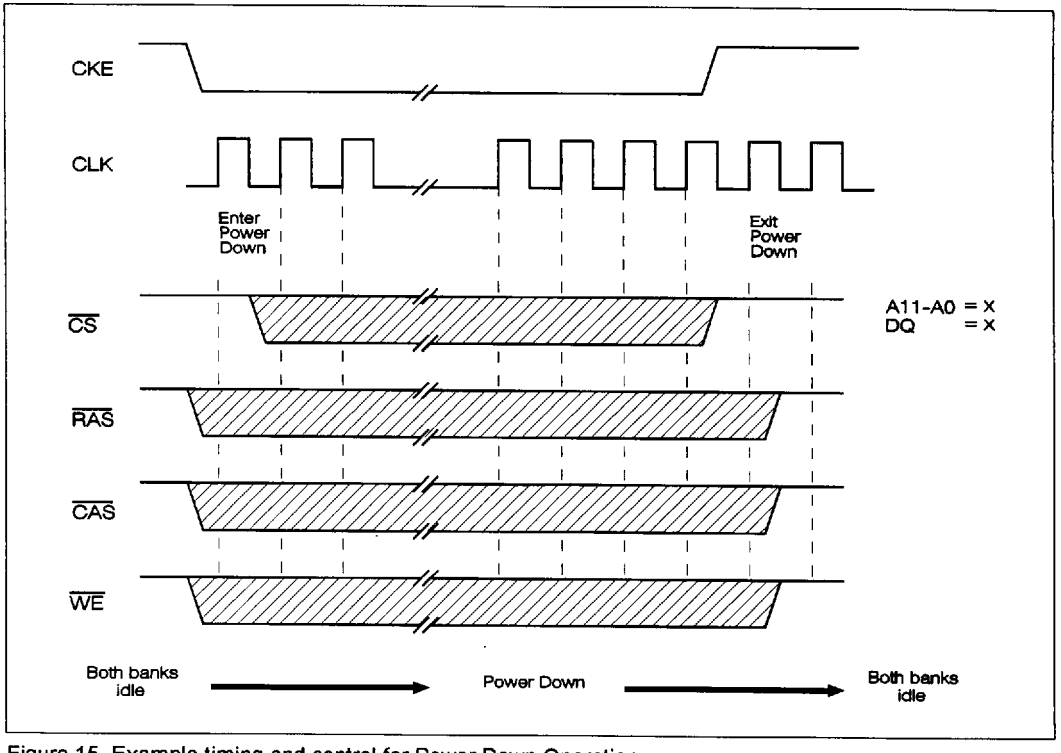


Figure 15. Example timing and control for Power Down Operation

7. Clock Suspend

Clock Suspend is very similar to Power Down, except that the Clock Suspend command is invoked by sampling the CKE signal low while one or both banks are not idle. While the clock is suspended, only the CLK and CKE inputs are enabled, and the state of CKE is sampled on every clock cycle. Internally, the banks remain in the state they were in when the clock was suspended. For example, if bank 0 was in the middle of a read burst when the clock was suspended, the read state will be maintained after exiting Clock Suspend. On the next clock cycle, the burst can be resumed from the next memory location designated by the burst length and burst type programmed in the Mode Register, or other legal commands can be issued to the active or both banks. While the clock is suspended, the SDRAM is not refreshed. Therefore, the minimum refresh specification still applies during the period when the clock is suspended. Figure 16 illustrates how Clock Suspend is entered and exited.

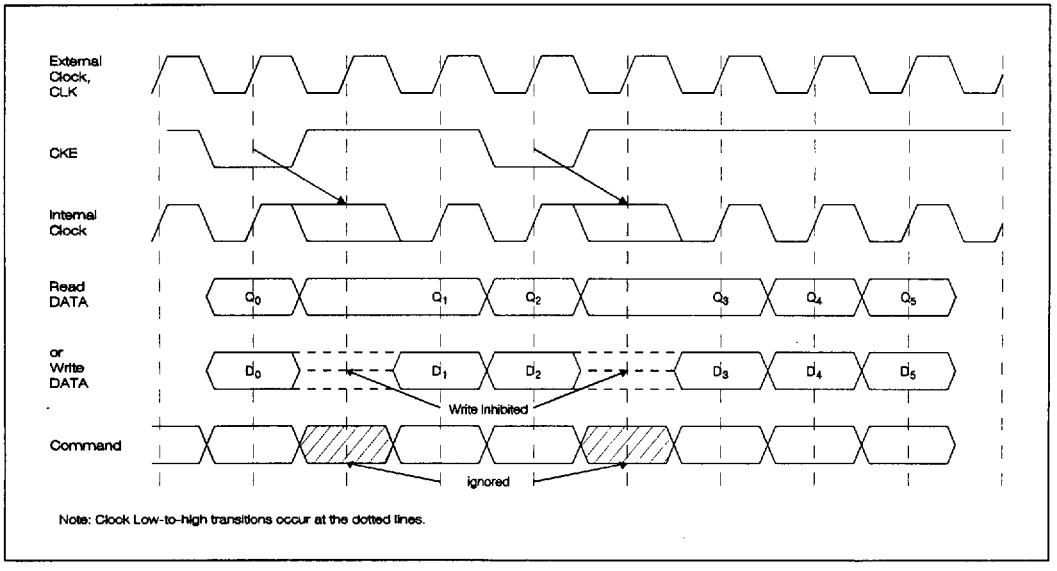


Figure 16. Example timing and control for Clock Suspend Operation

8. Test Mode

Test mode is used to check the functionality of refresh address counter in this SDRAM. For more details, refer to attached timing diagram 29 and 30.

9. Power Sequence

Once power has been applied, Synchronous DRAM must be initialized with proper power on sequence. (JEDEC standard)

step 1) Pause a time of 200 μS with NOPs, keeping CKE and DQM be high.
step 2) Assert `Precharge command(s)` to ensure both banks are precharged.
step 3) Wait t_{RP}, then assert `Mode register set command` to program the mode register.
step 4) Stay NOP for 2 clocks, then 8 or more `Auto refresh commands` should be performed.

For more details, refer to attached timing diagram 4.

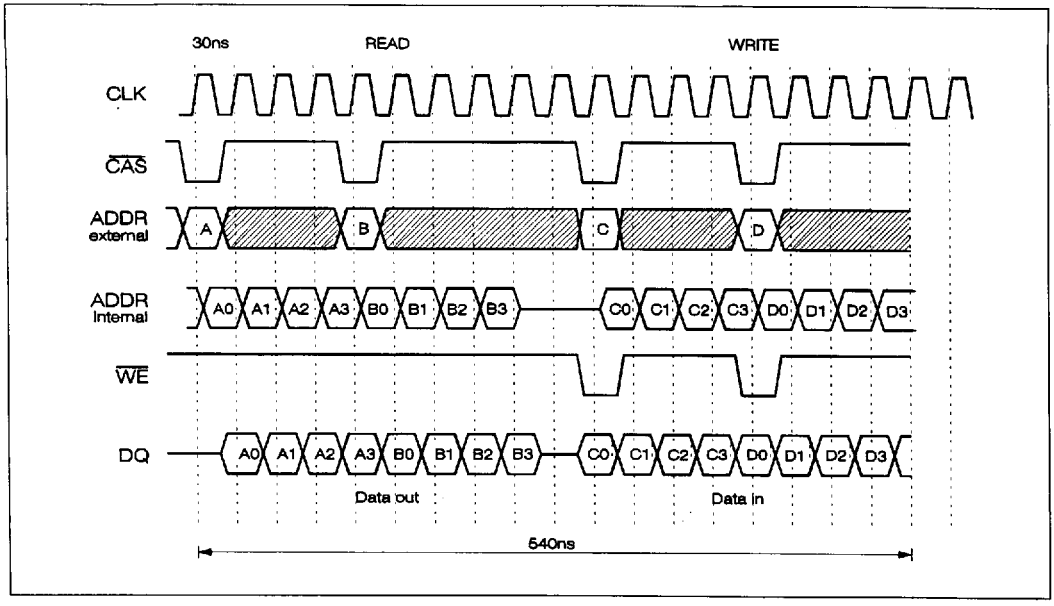


Figure 17. Timing of pipeline operation, Latency=1, Burst length=4.

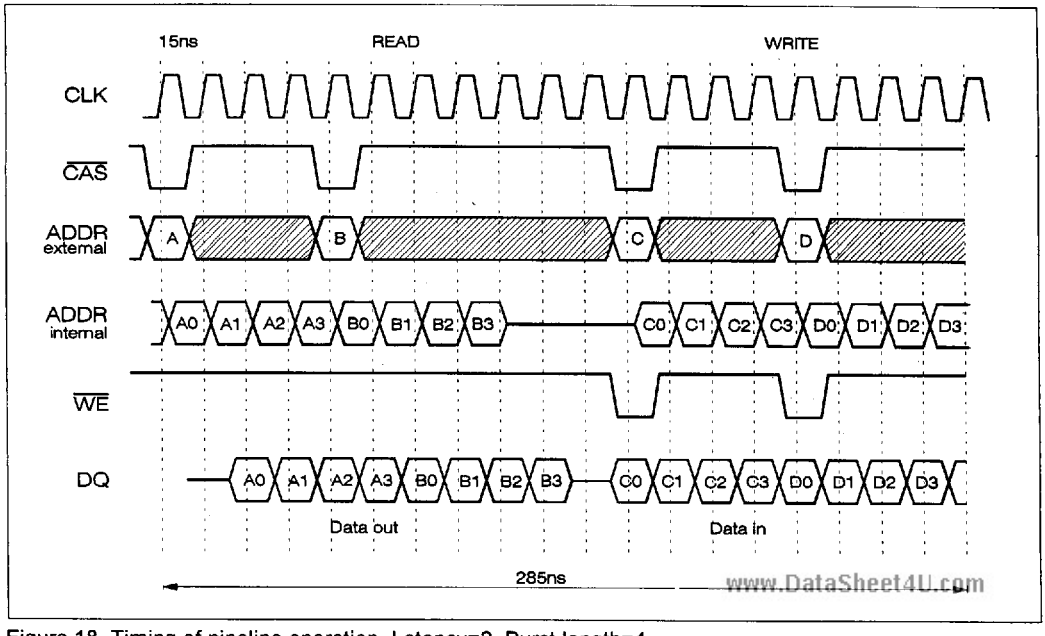


Figure 18. Timing of pipeline operation, Latency=2, Burst length=4.

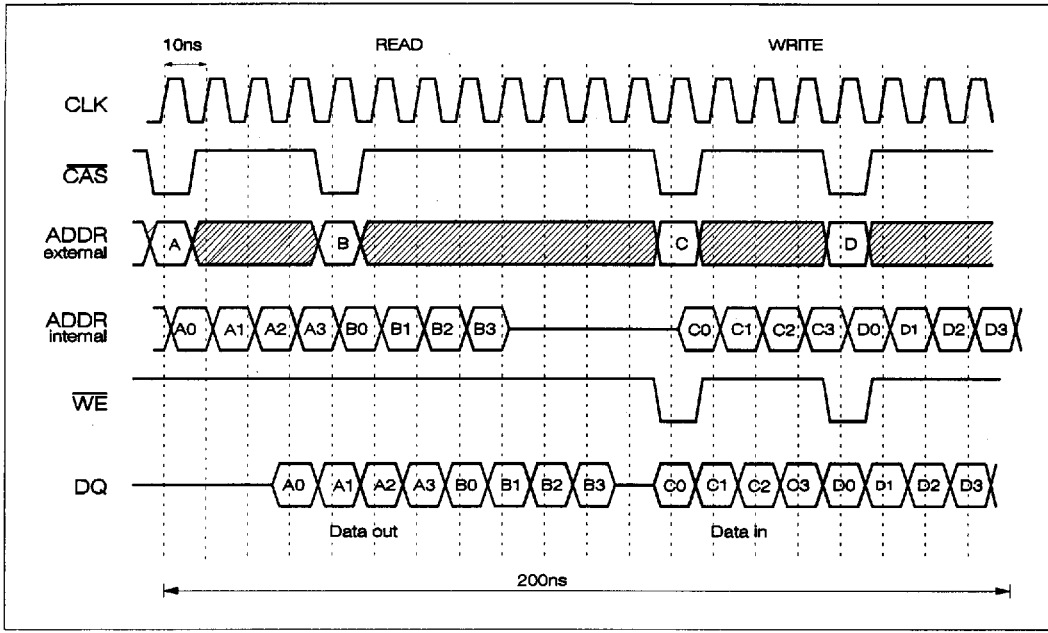


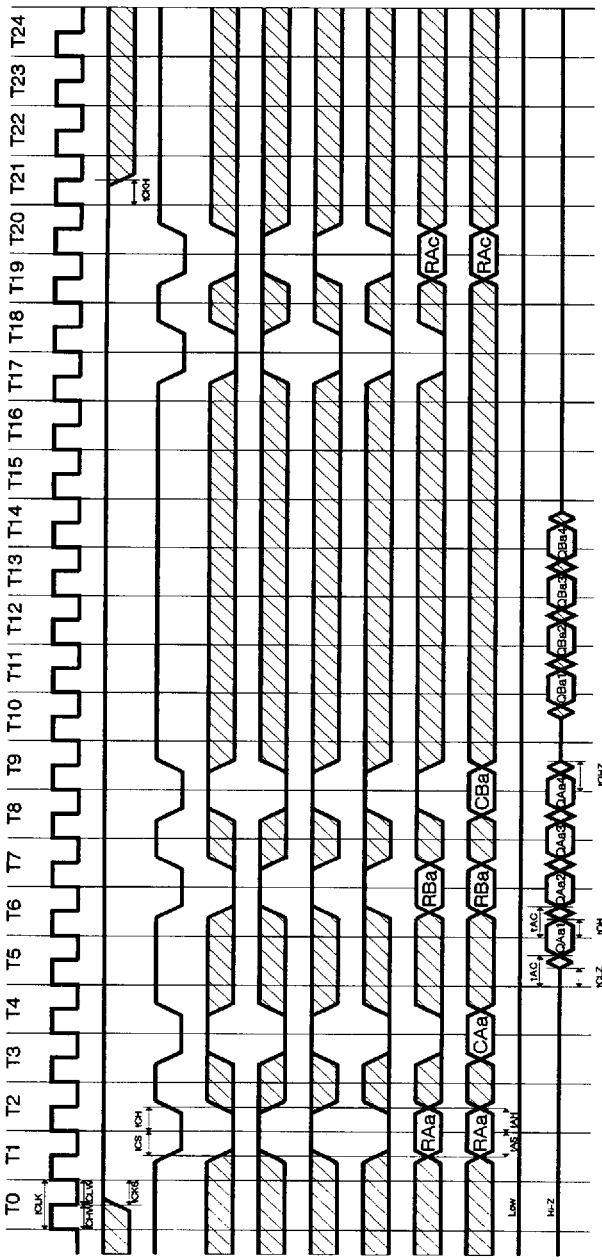
Figure 19. Timing of pipeline operation, Latency=3, Burst length=4.

Timing Diagram

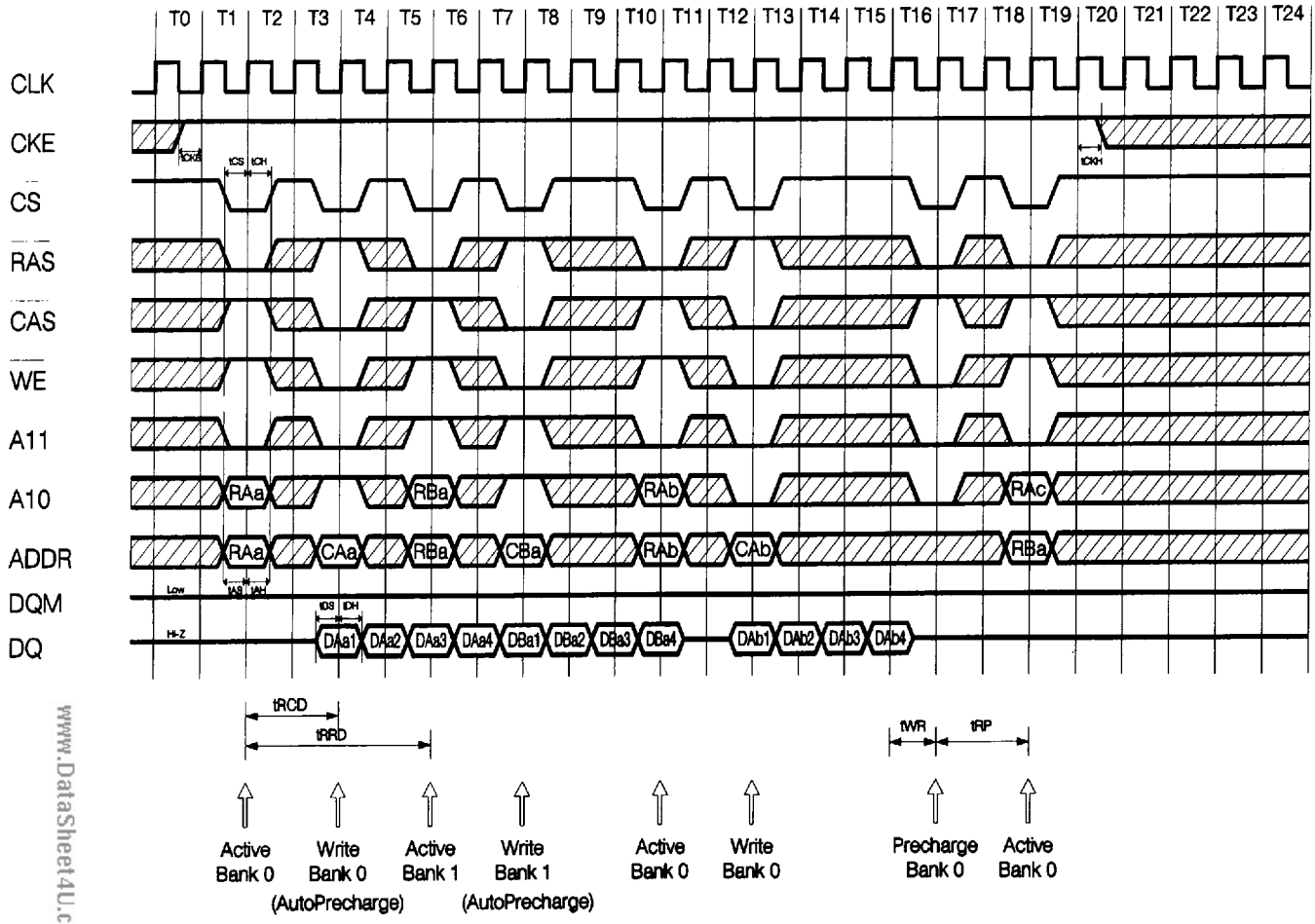
1. AC Parameters for READ Timing
2. AC Parameters for WRITE Timing
3. Mode Register Set Cycle
4. Power on Sequence and Auto Refresh
5. $\overline{C}$ Function (Only $\overline{C}$ Signal needs to be asserted at minimum rate)
6. CKE Timing the Power Down Mode
7. Self-Refresh Entry and Exit
8. CKE Timing for Clock Suspend during Burst READ (BL=4, CL=2)
9. CKE Timing for Clock Suspend during Burst READ (BL=4, CL=3)
10. CKE Timing for Clock Suspend during Burst WRITE (BL=4)
11. Random Column Read (Page with same bank, BL=4, CL=2)
12. Random Column Read (Page with same bank, BL=4, CL=3)
13. Random Column Write (Page with same bank, BL=4, CL=2)
14. Random Column Write (Page with same bank, BL=4, CL=3)
15. Random Row Read (Pingpong banks, BL=8, CL=2)
16. Random Row Read (Pingpong banks, BL=8, CL=3)
17. Random Row Write (Pingpong banks, BL=8, CL=2)
18. Random Row Write (Pingpong banks, BL=8, CL=3)
19. Read and Write DQM Function (BL=4, CL=2)
20. Read and Write DQM Function (BL=4, CL=3)
21. Interleaved Column Read Cycle (BL=4, CL=2)
22. Interleaved Column Read Cycle (BL=4, CL=3)
23. Interleaved Column Write Cycle (BL=4, CL=2)
24. Interleaved Column Write Cycle (BL=4, CL=3)
25. Full Page Read Cycle (CL=2)
26. Full Page Write Cycle (CL=2)
27. Auto Precharge after READ Burst (BL=4, CL=2)
28. Auto Precharge after WRITE Burst (BL=4, CL=2)
29. Test Mode for Read Cycle (BL=4, CL=2)
30. Test Mode for Write Cycle (BL=4, CL=2)

Notes:
1. BL=Burst Length, CL=$\overline{CAS}$ Latency

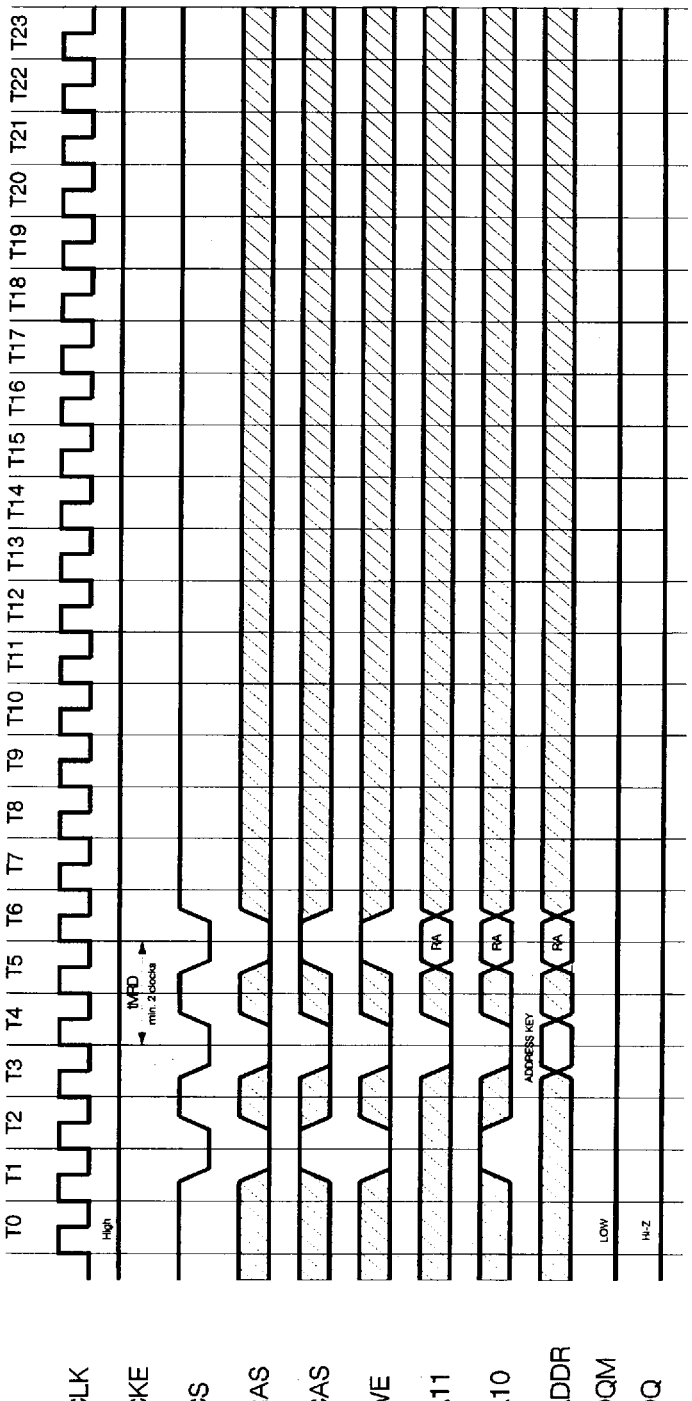
1. AC Parameters for READ Timing : BL=4, CL=2



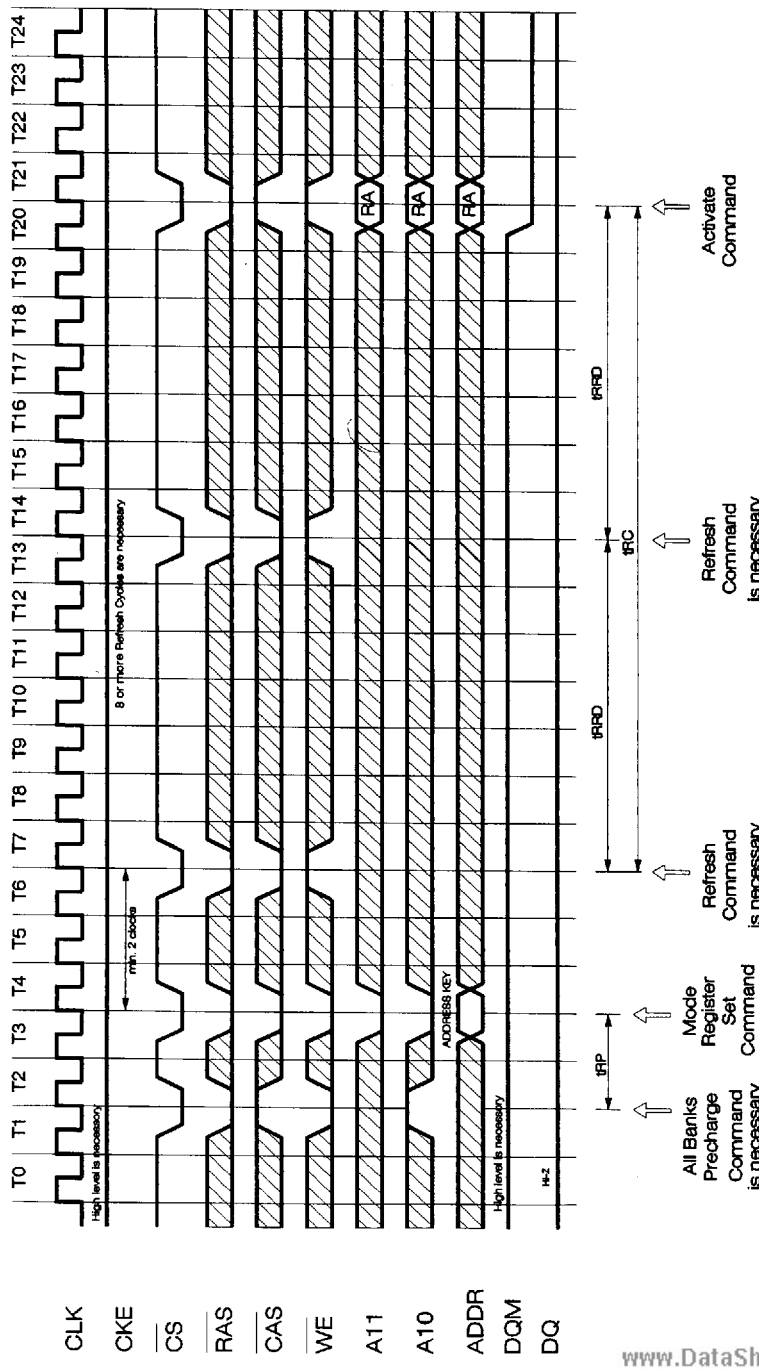
2. AC Parameters for WRITE Timing : BL=4, CL=2



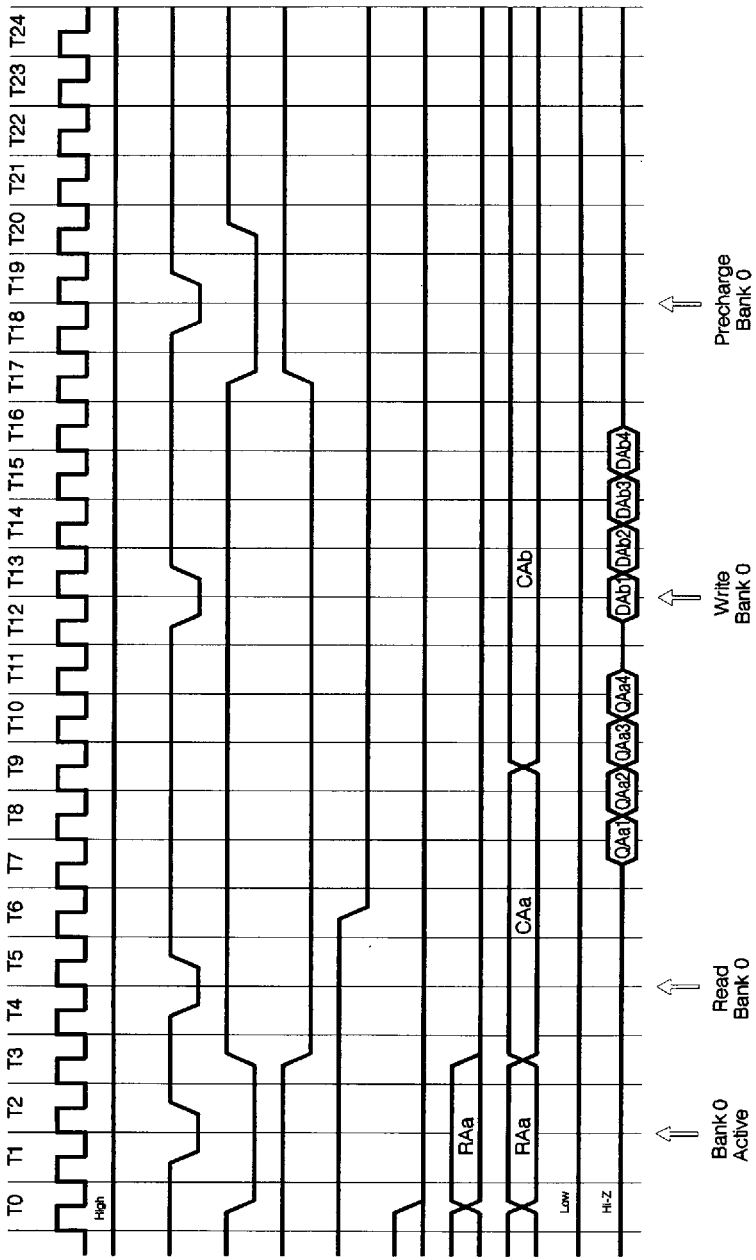
3. Mode Register Set Cycle



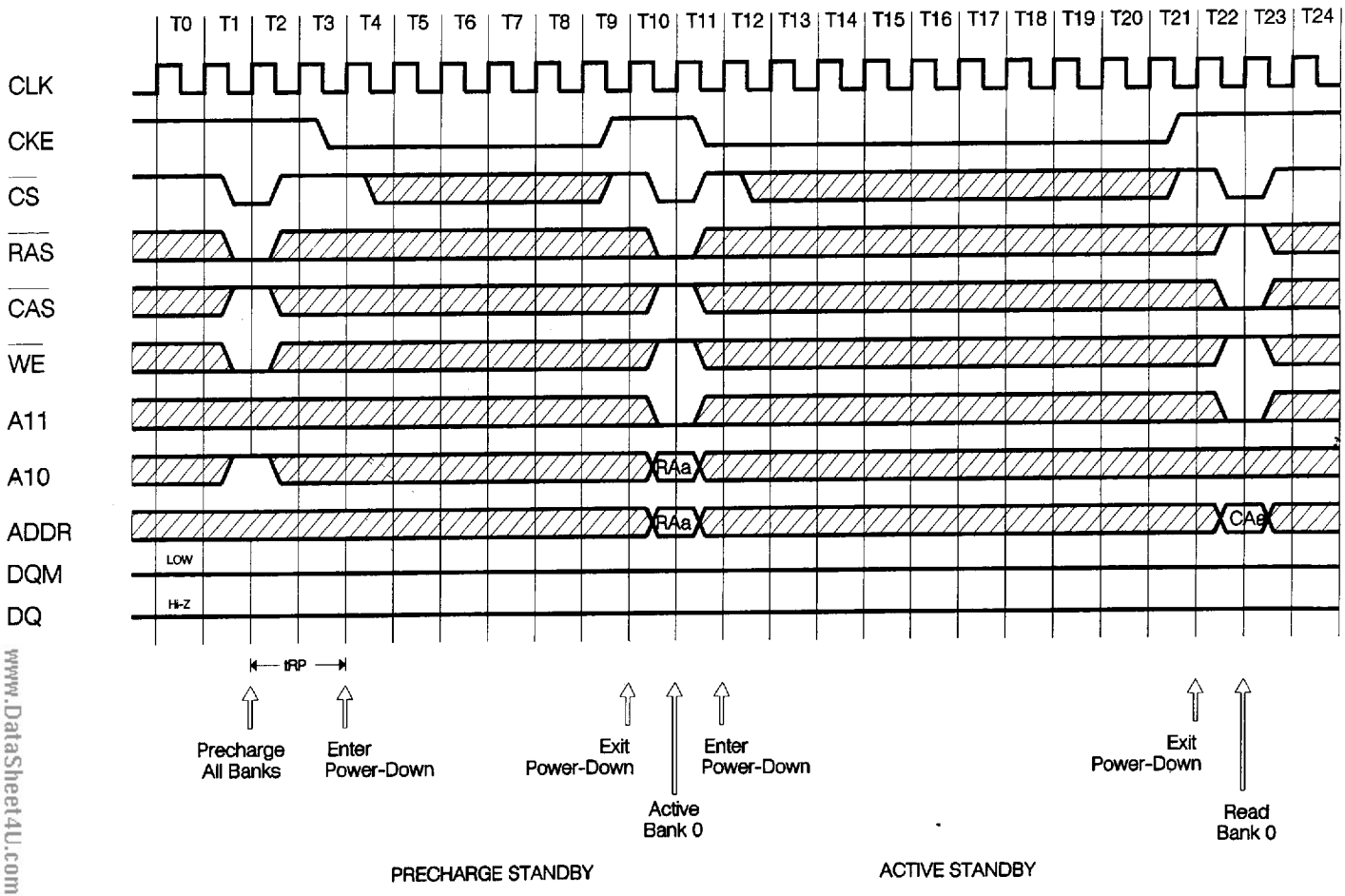
4. Power on Sequence and Auto Refresh



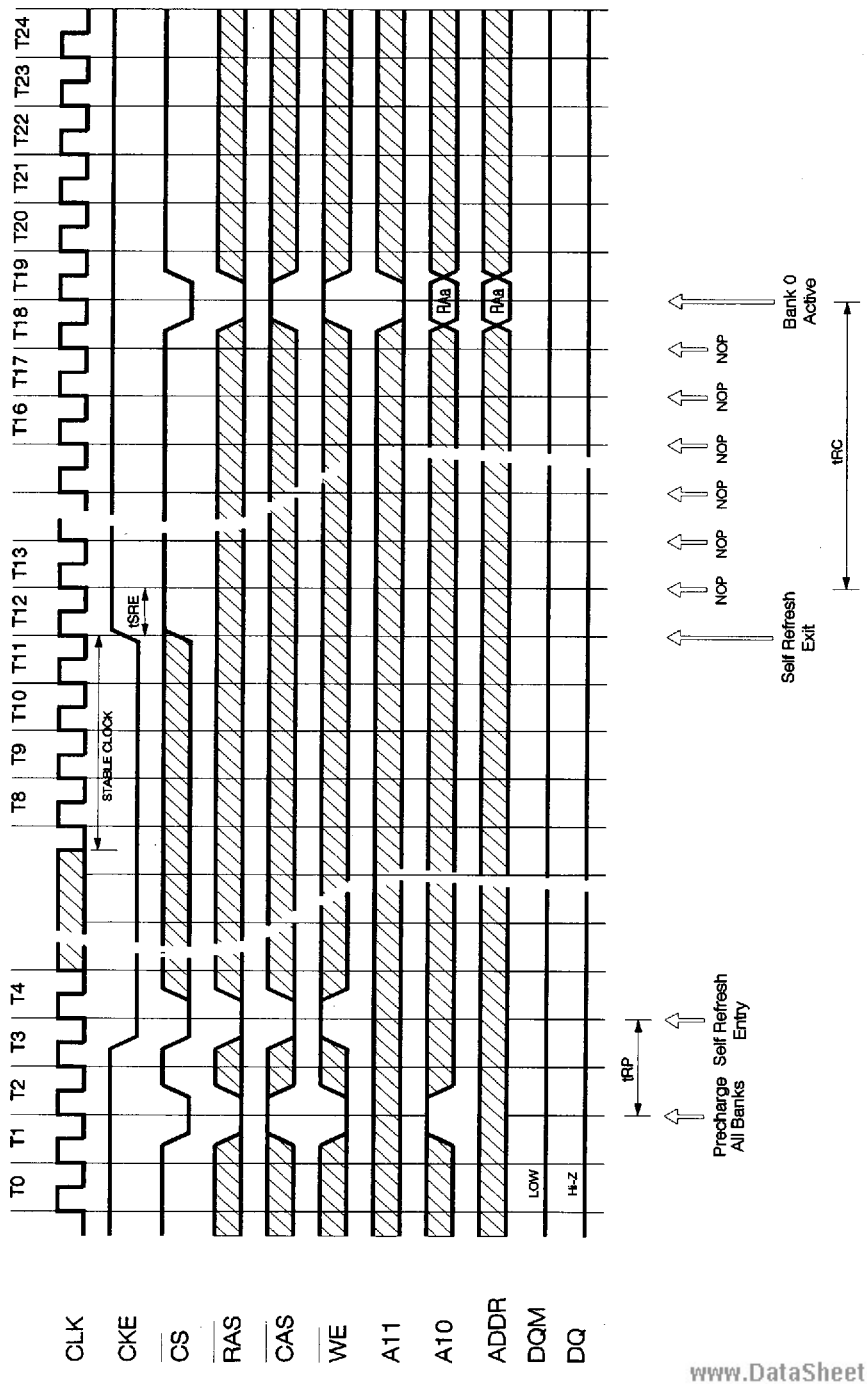
5. $\overline{CS}$ Function (Only $\overline{CS}$ signal needs to be asserted at min. rate) : BL=4, CL=3



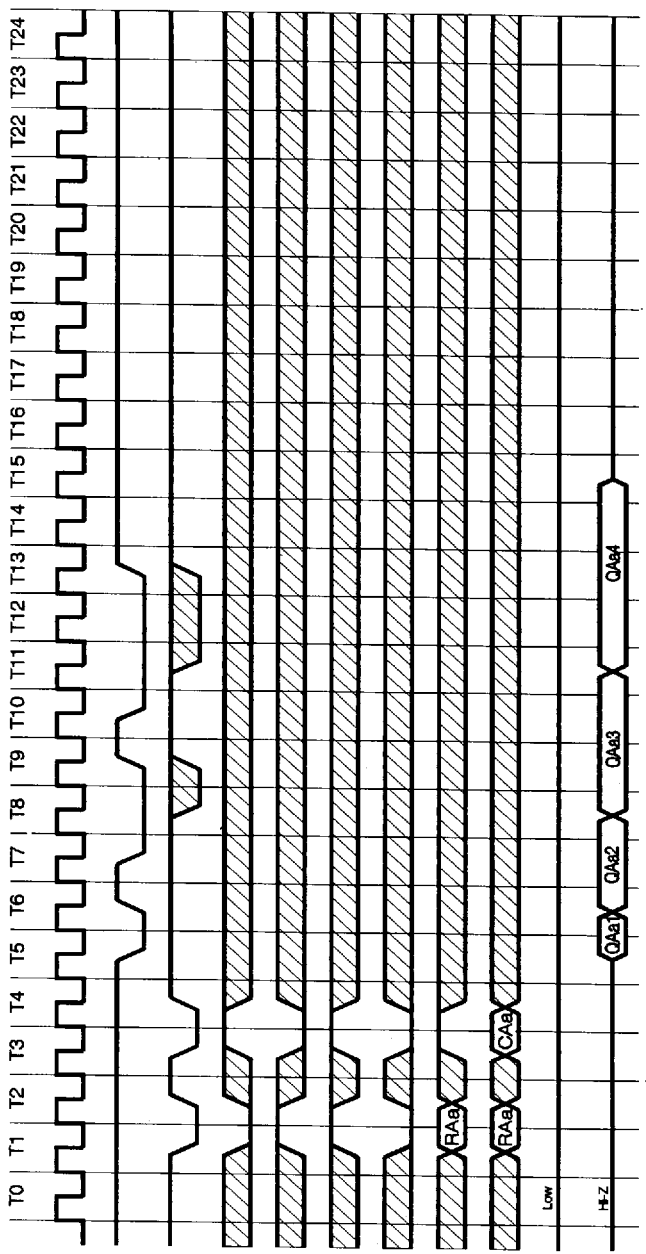
6. CKE Timing for Power Down Mode



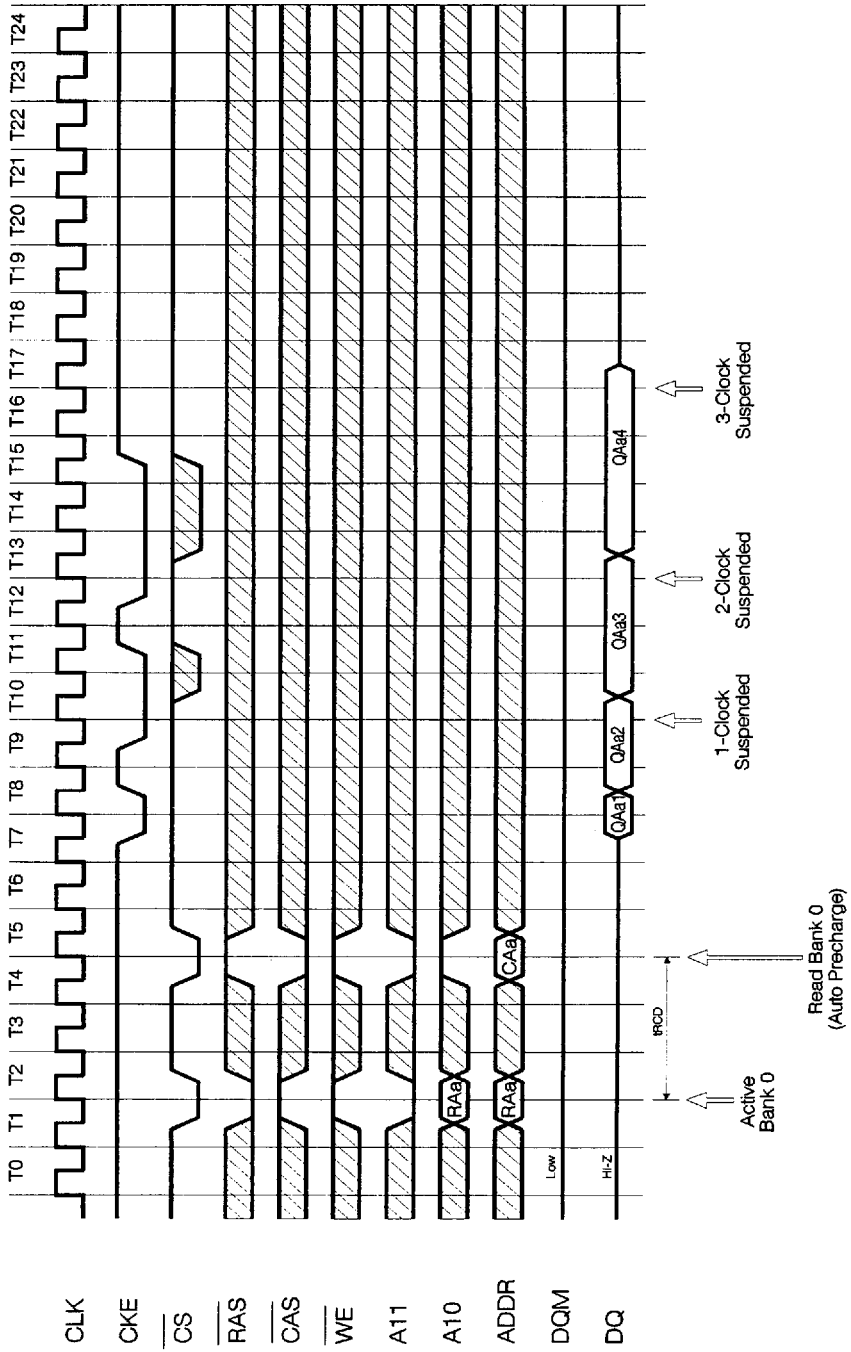
7. Self Refresh Entry and Exit



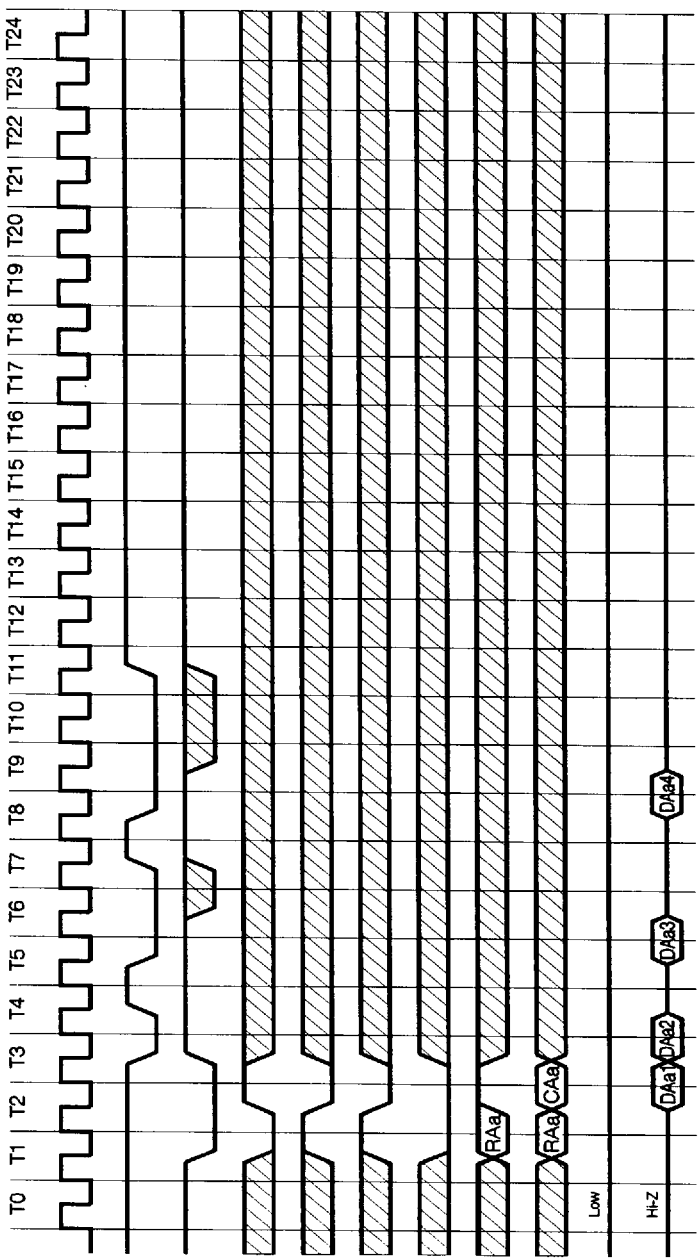
8. CKE Timing for Clock Suspend during Burst READ : BL=4, CL=2



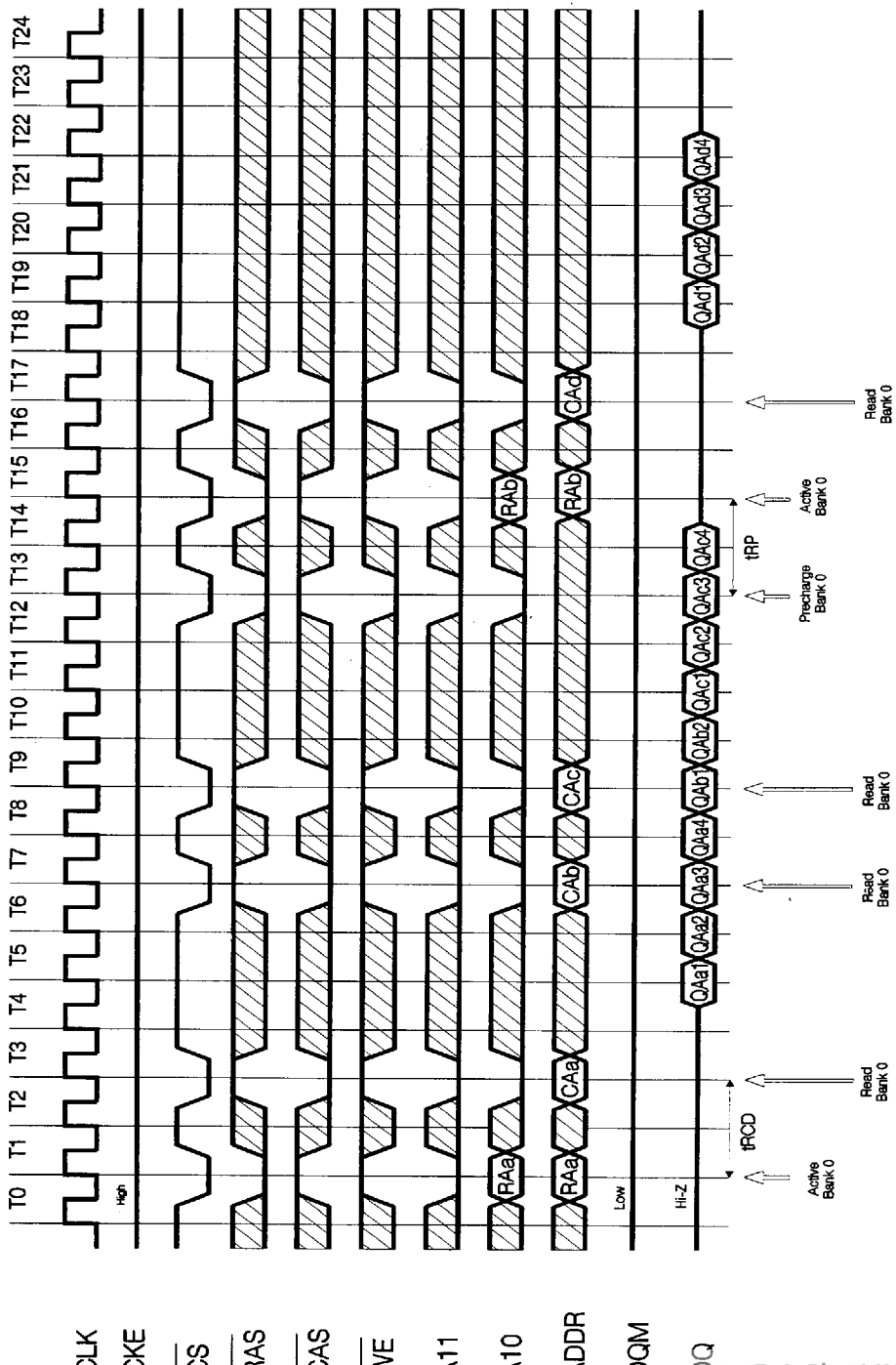
9. CKE Timing for Clock Suspend during Burst READ : BL=4, CL=3



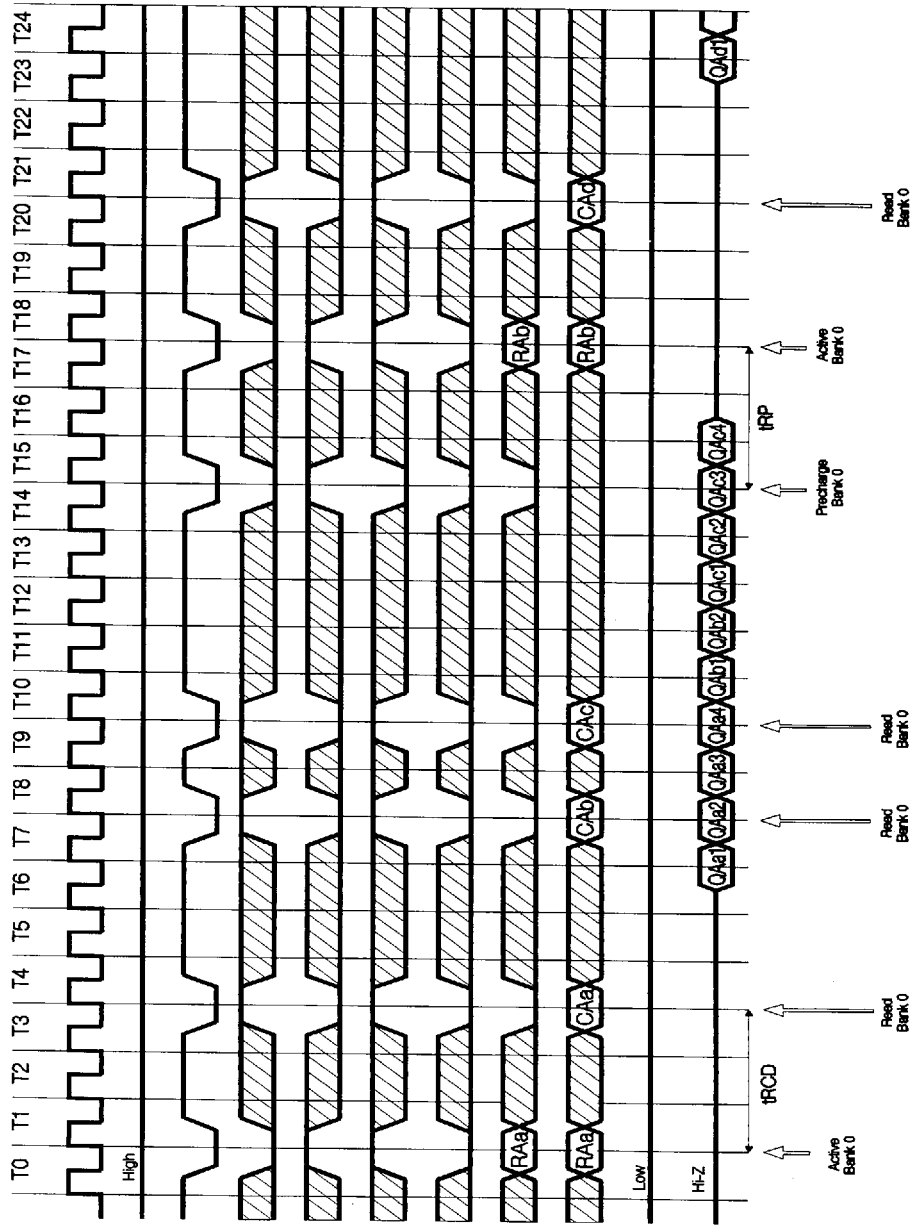
10. CKE Timing for Clock Suspend during Burst WRITE : BL=4



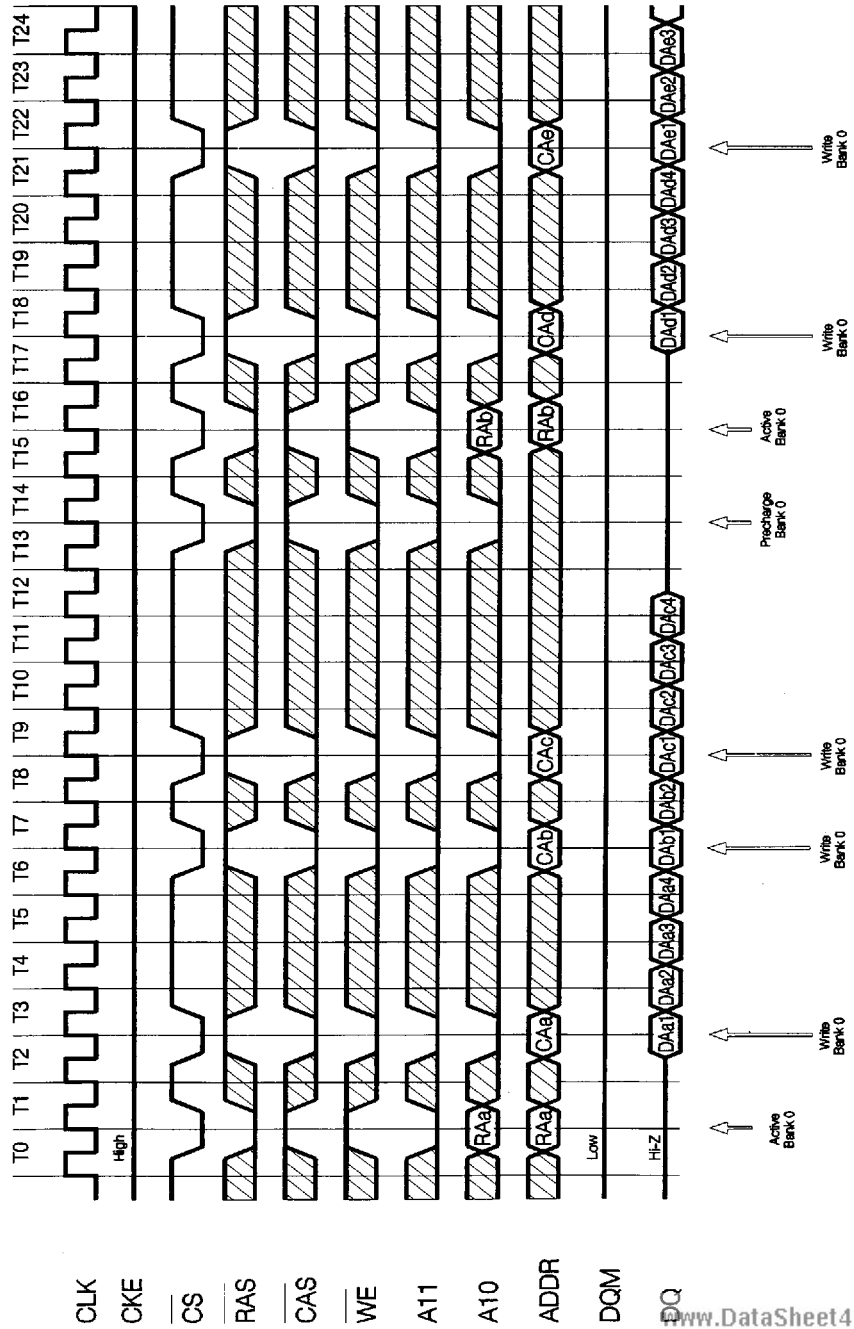
11. Random Column Read (Page with same bank) : BL=4, CL=2



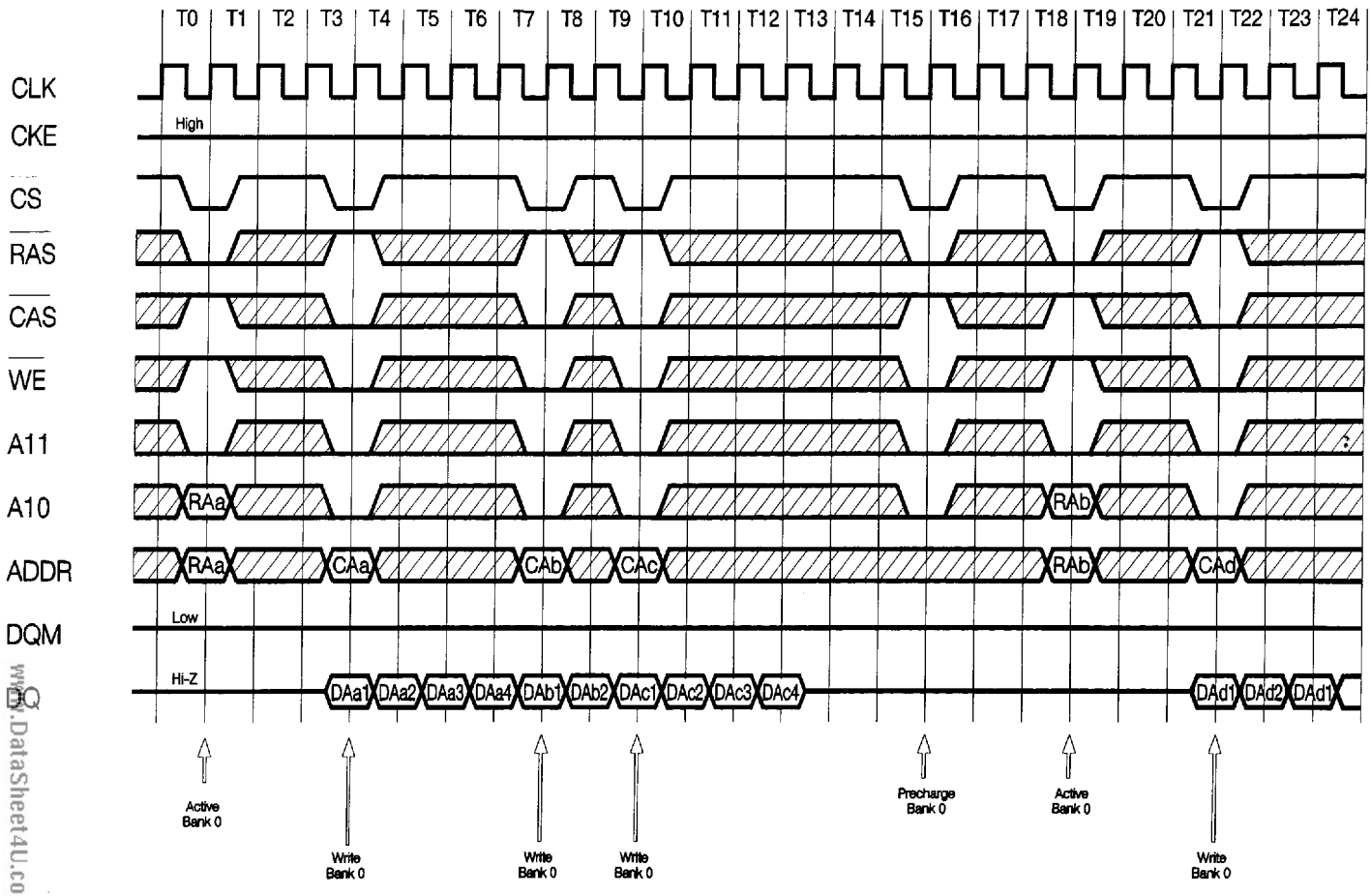
12. Random Column Read (Page with same bank) : BL=4, CL=3



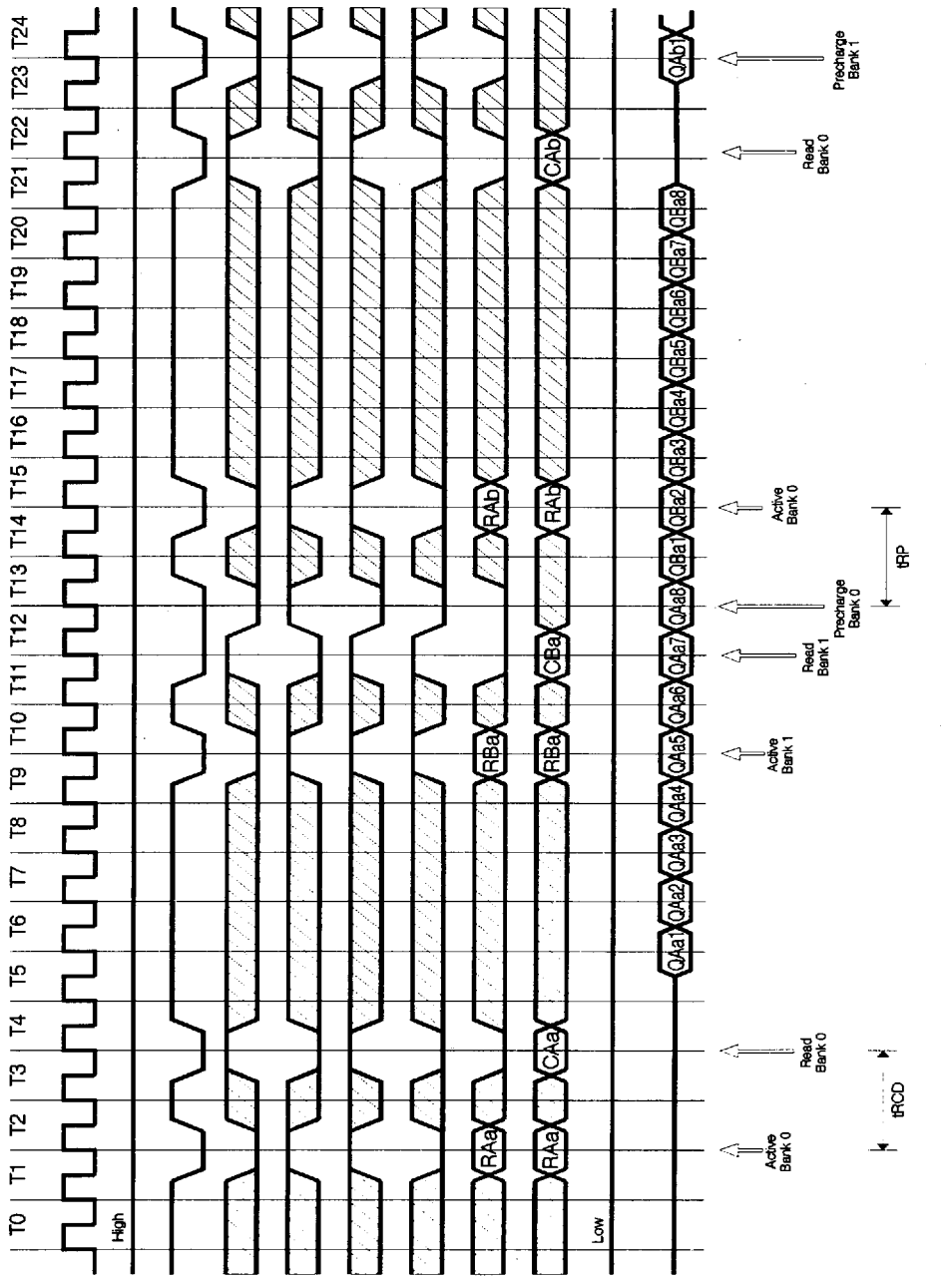
13. Random Column Write (Page with same bank) : BL=4, CL=2



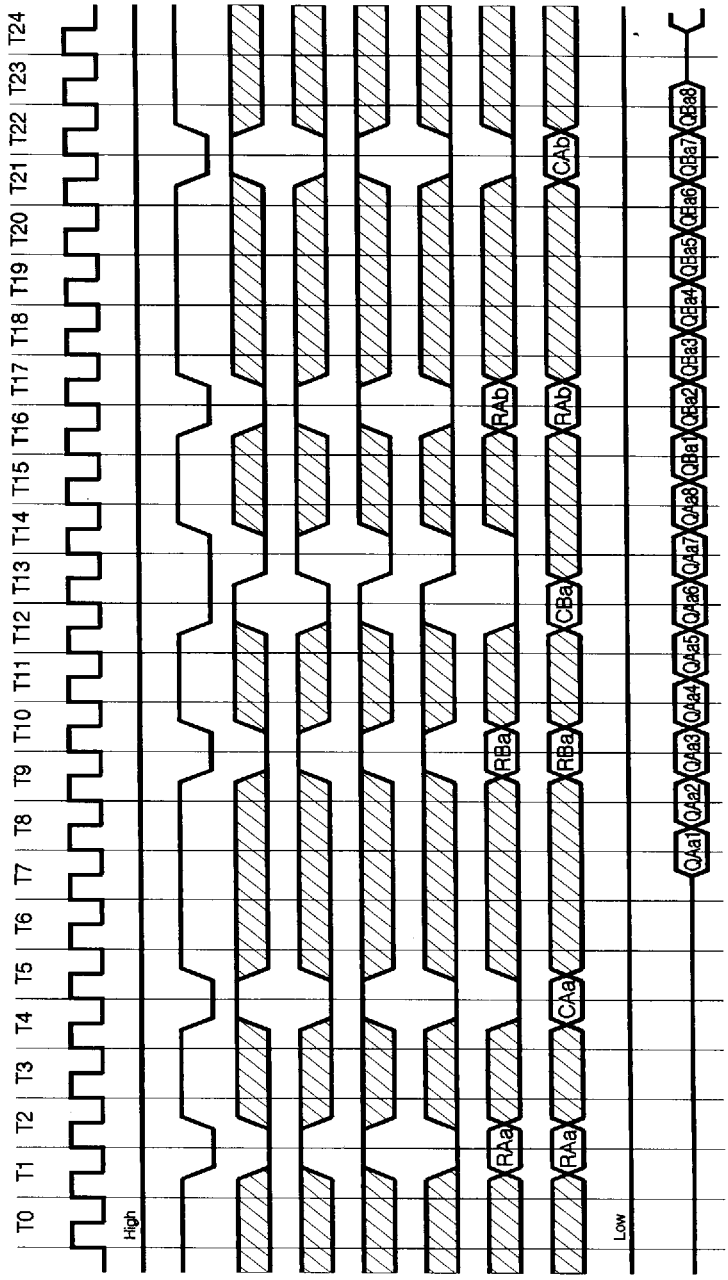
14. Random Column Write (Page with same bank) : BL=4, CL=3



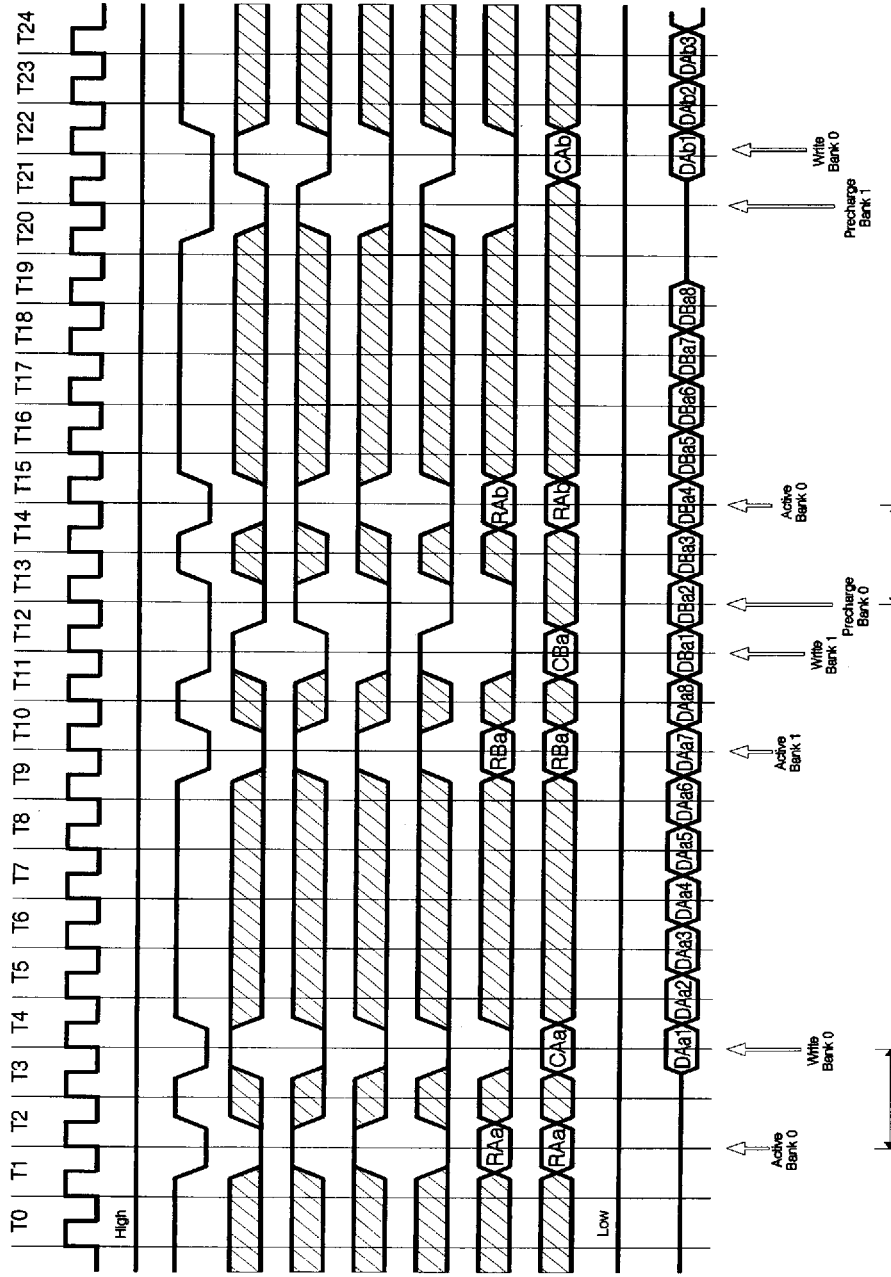
15. Random Row Read (Pingpong banks) : BL=8, CL=2



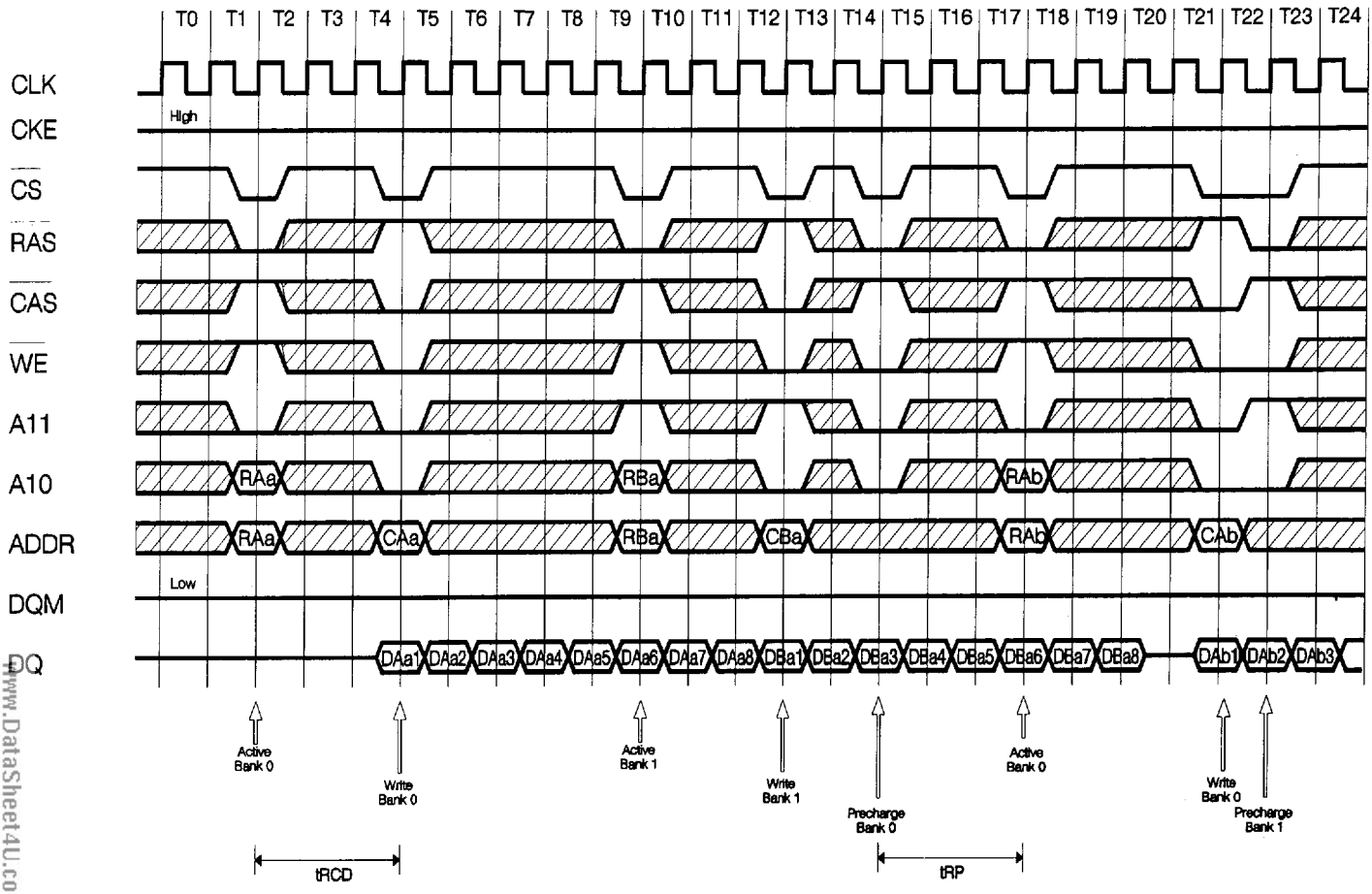
16. Random Row Read (Pingpong banks) : BL=8, CL=3



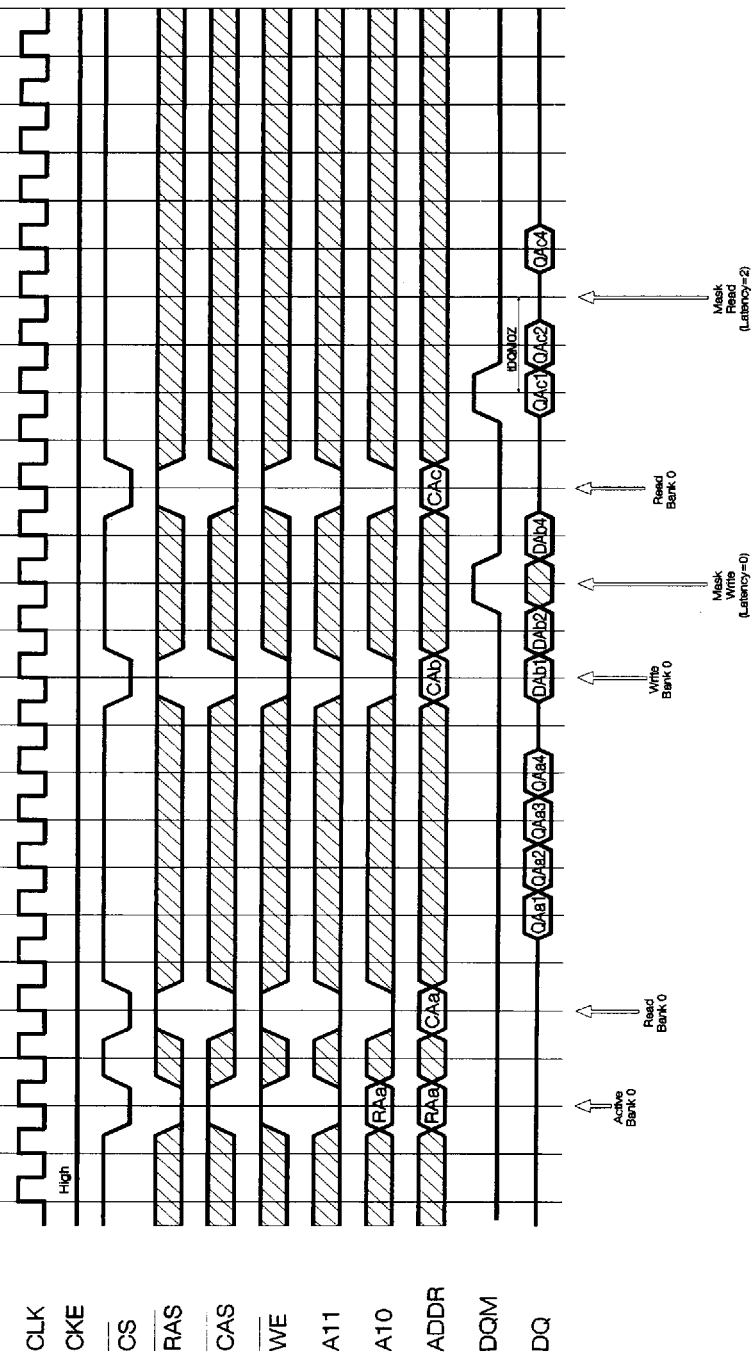
17. Random Row Write (Pingpong banks) : BL=8, CL=2



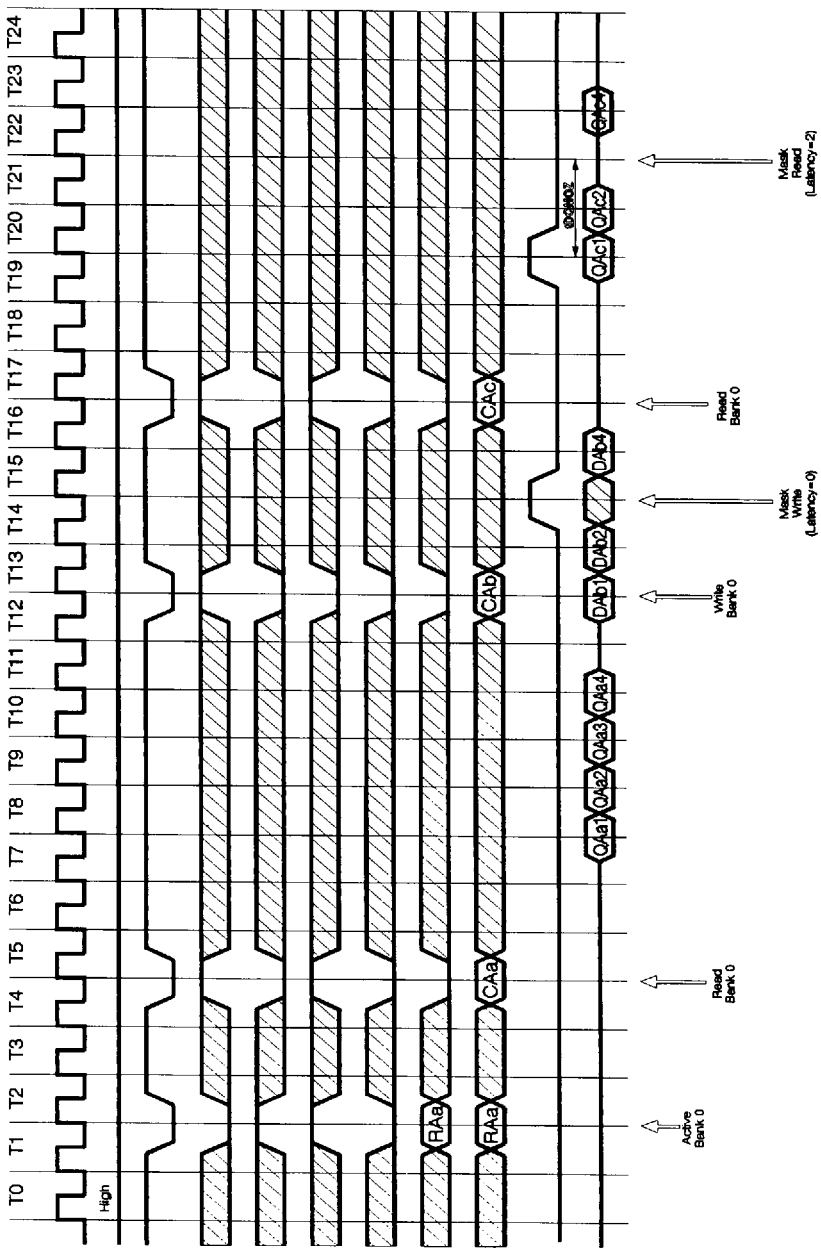
18. Random Row Write (Pingpong banks) : BL=8, CL=3



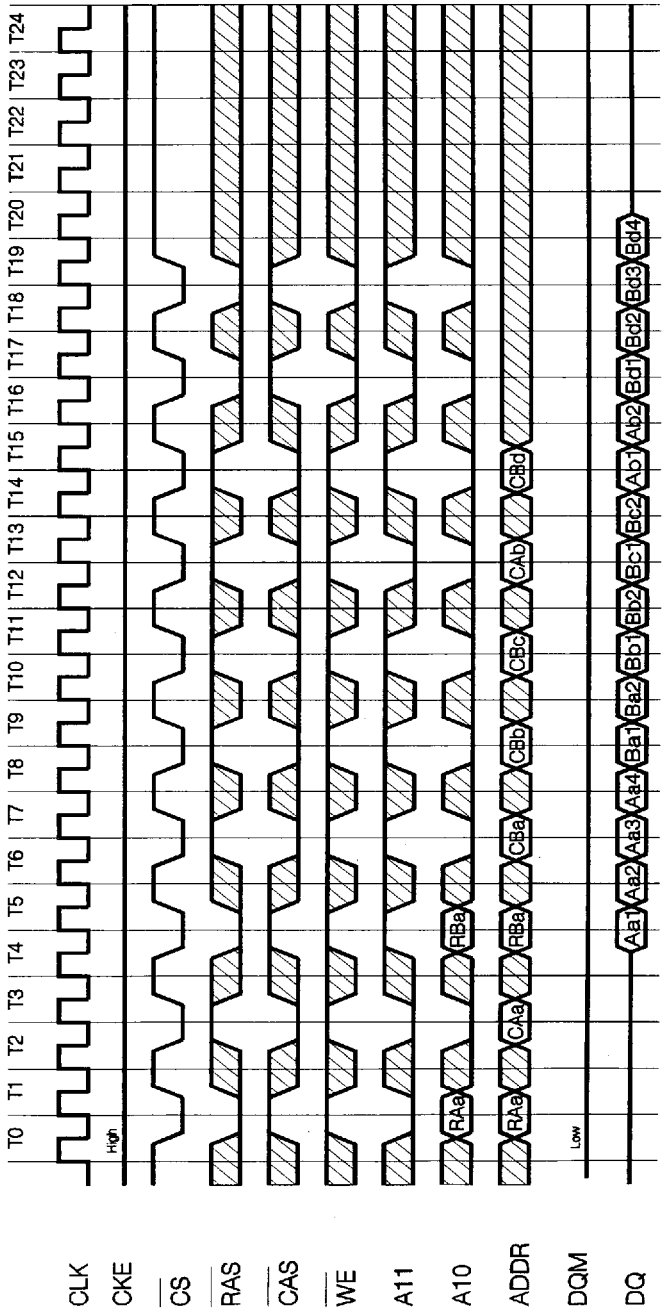
19. Read and Write with DQM Function : BL=4, CL=2



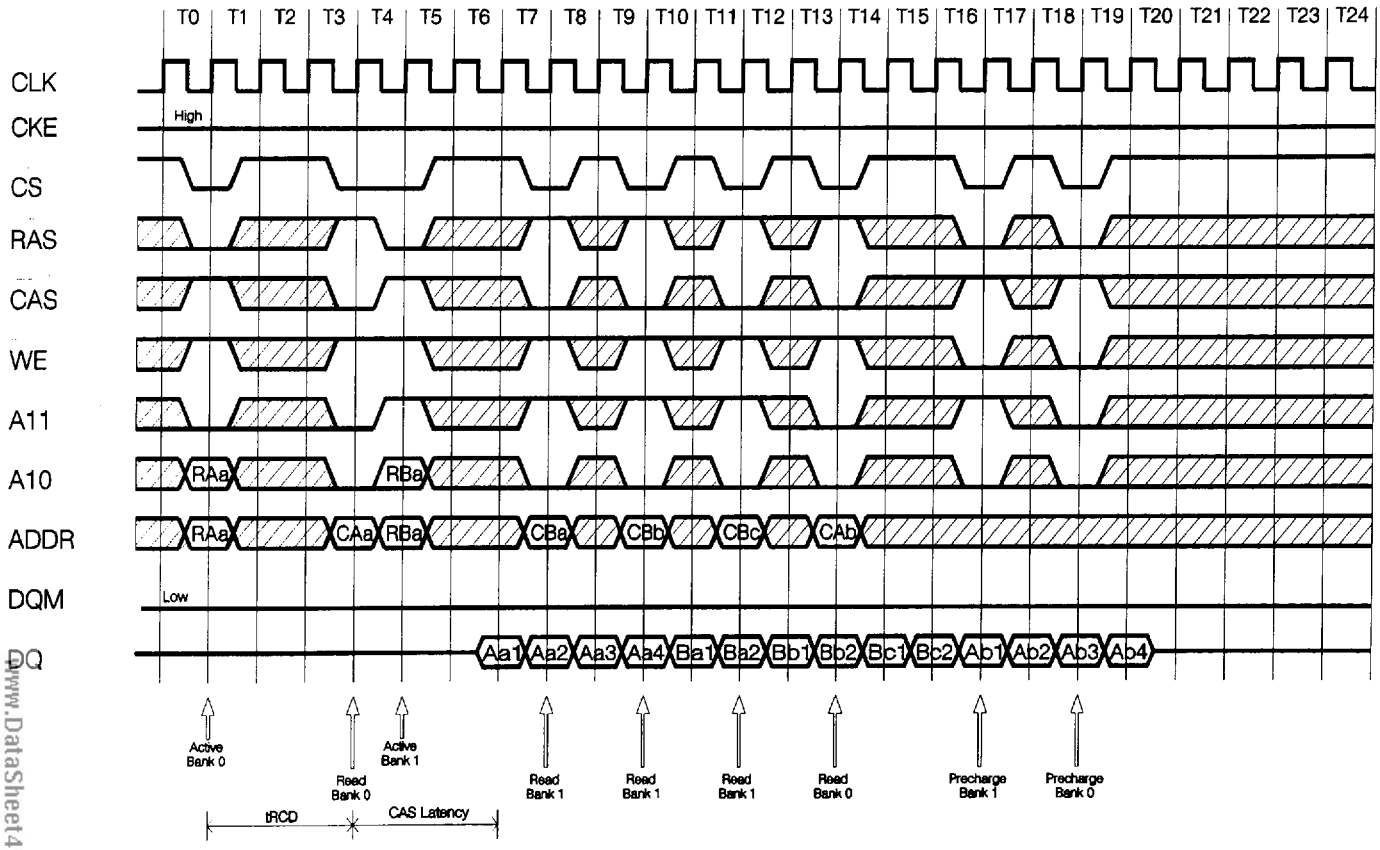
20. Read and Write with DQM Function : BL=4, CL=3



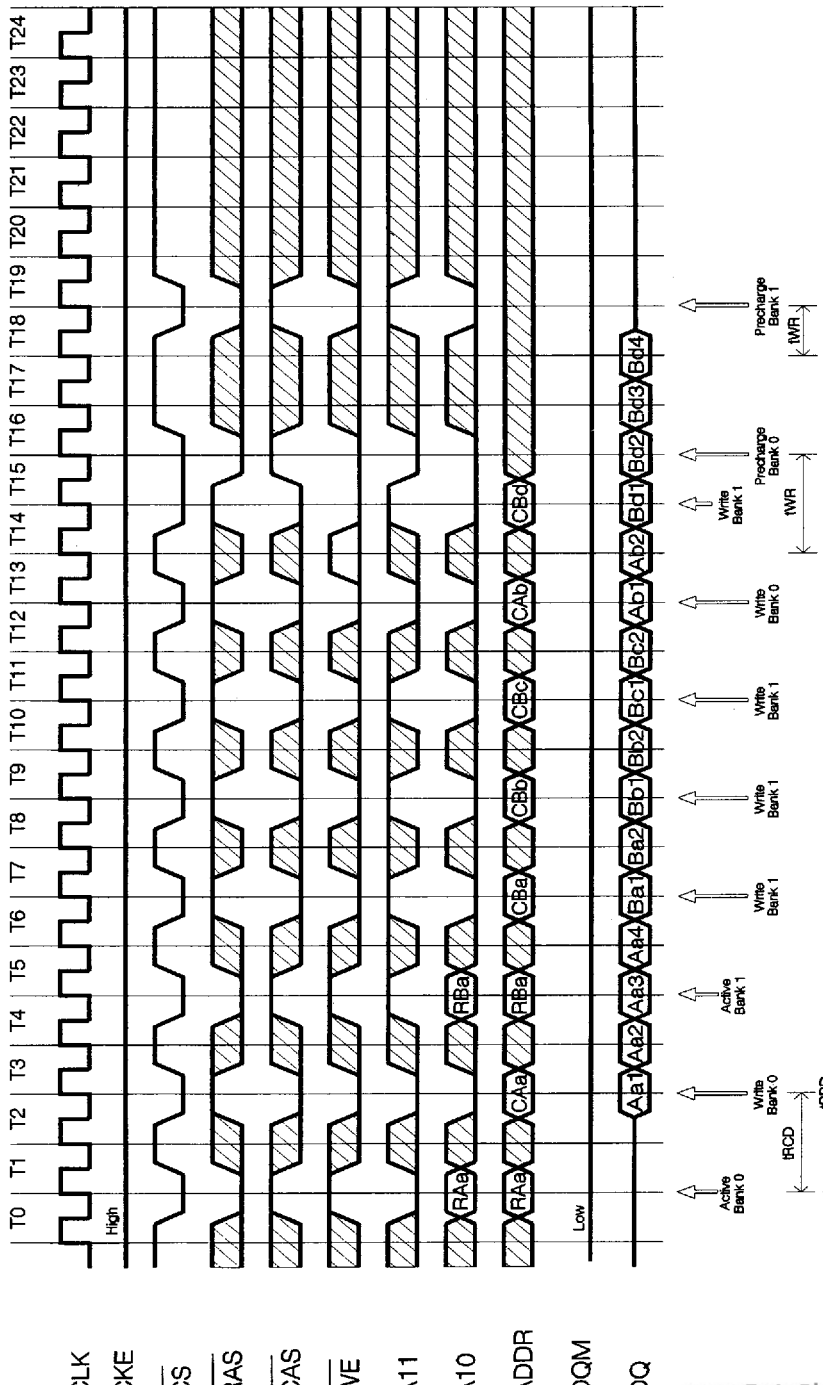
21. Interleaved Column Read Cycle : BL=4, CL=2



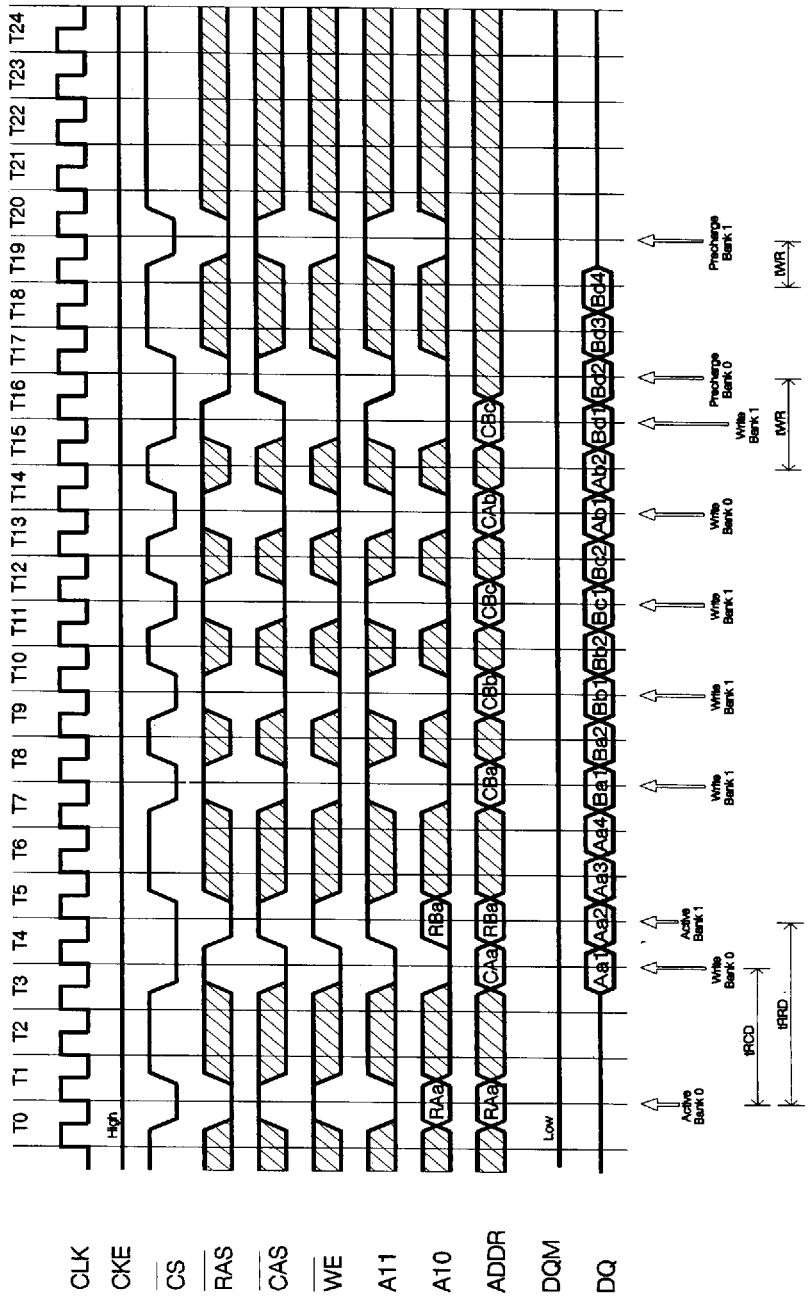
22. Interleaved Column Read Cycle : BL=4, CL=3



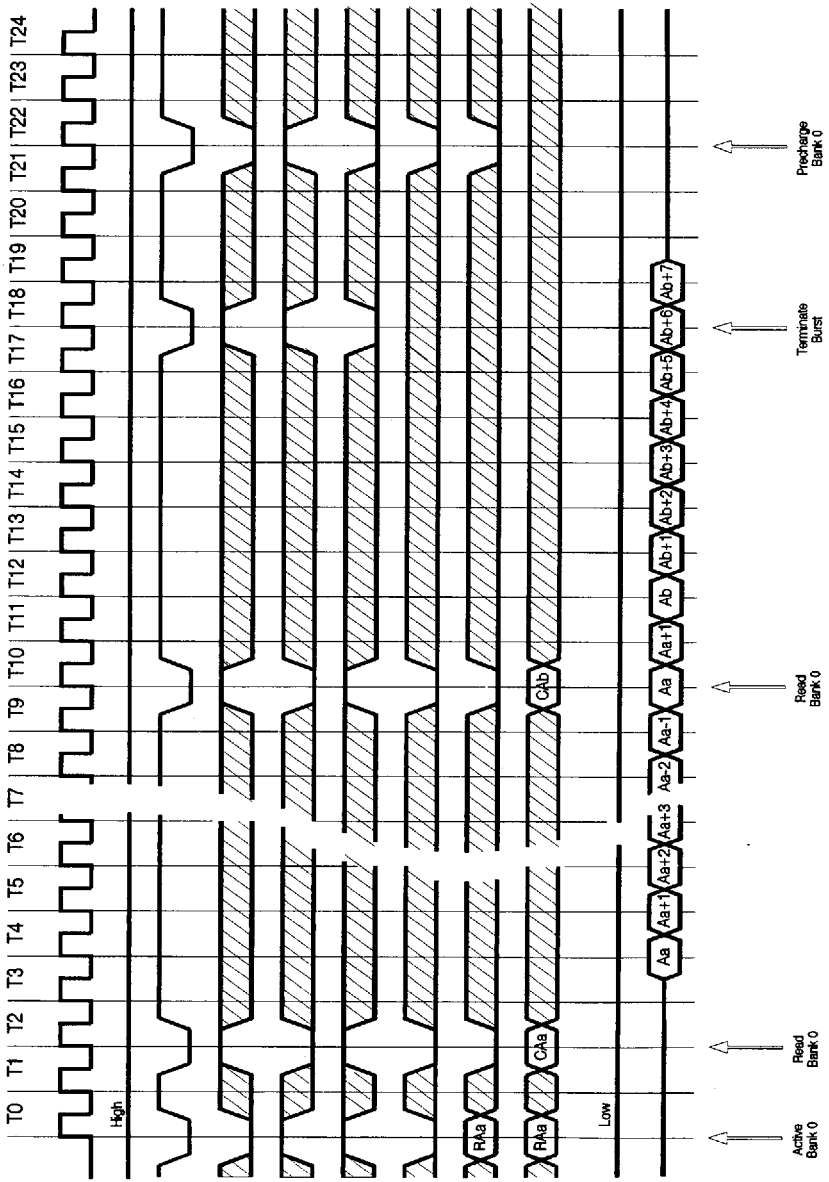
23. Interleaved Column Write Cycle : BL=4, CL=2



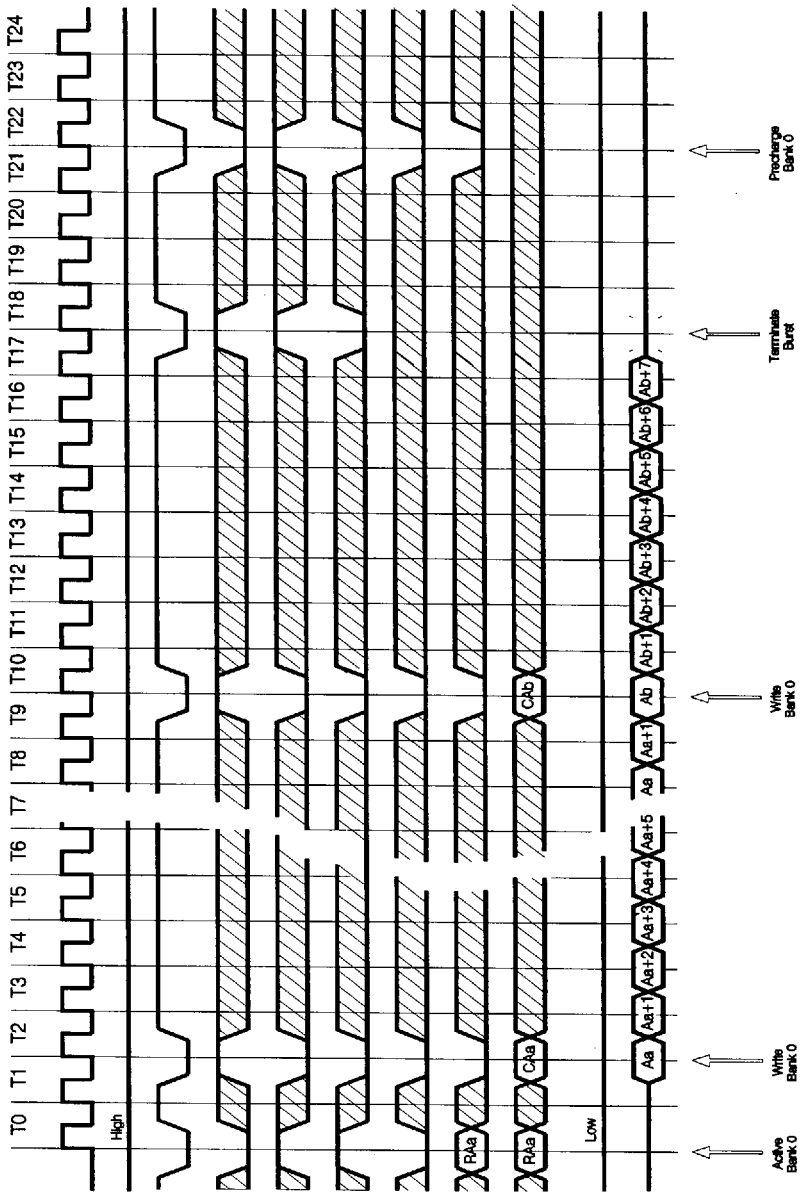
24. Interleaved Column Write Cycle : BL=4, CL=3



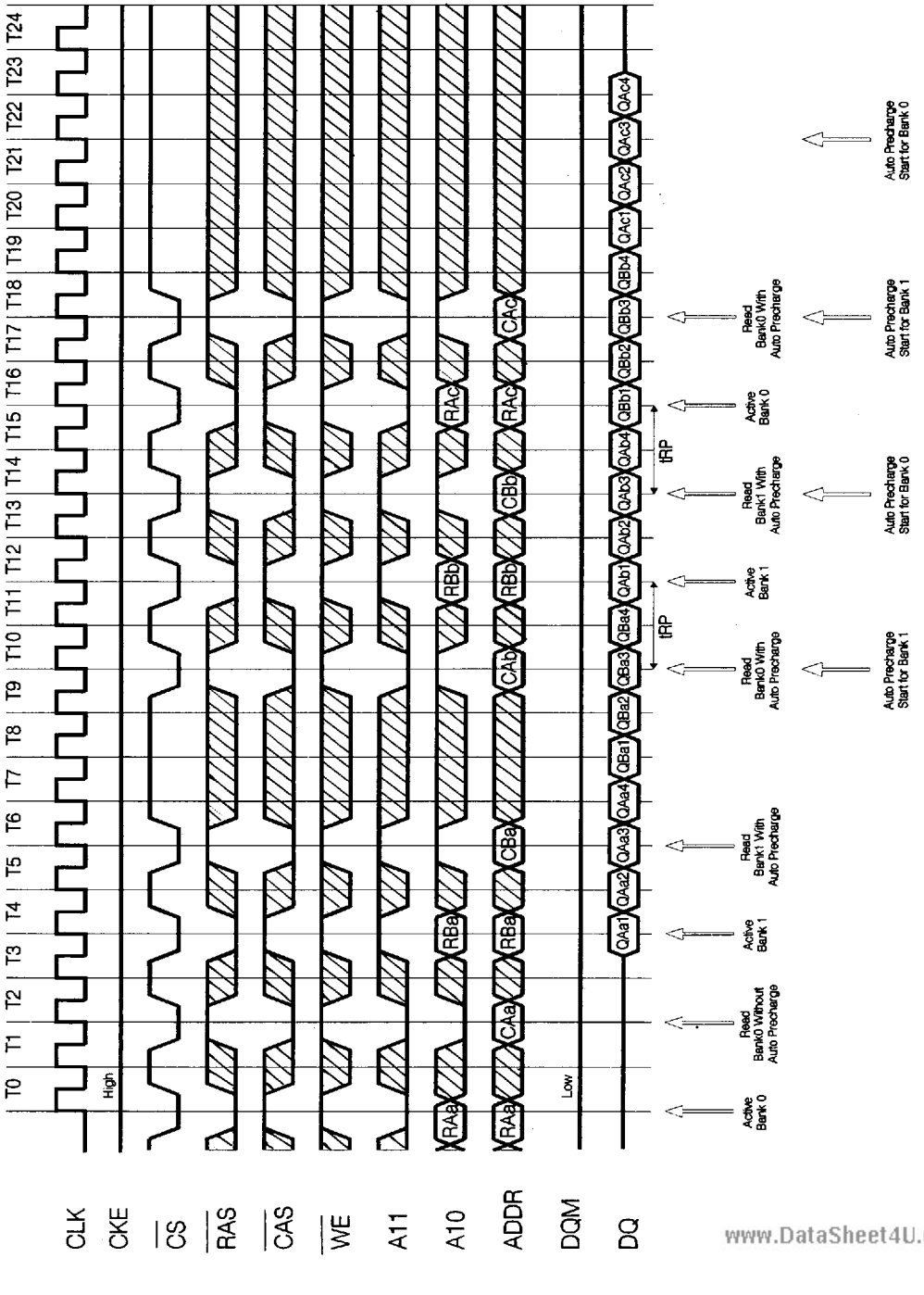
25. Full Page Read Cycle : CL=2



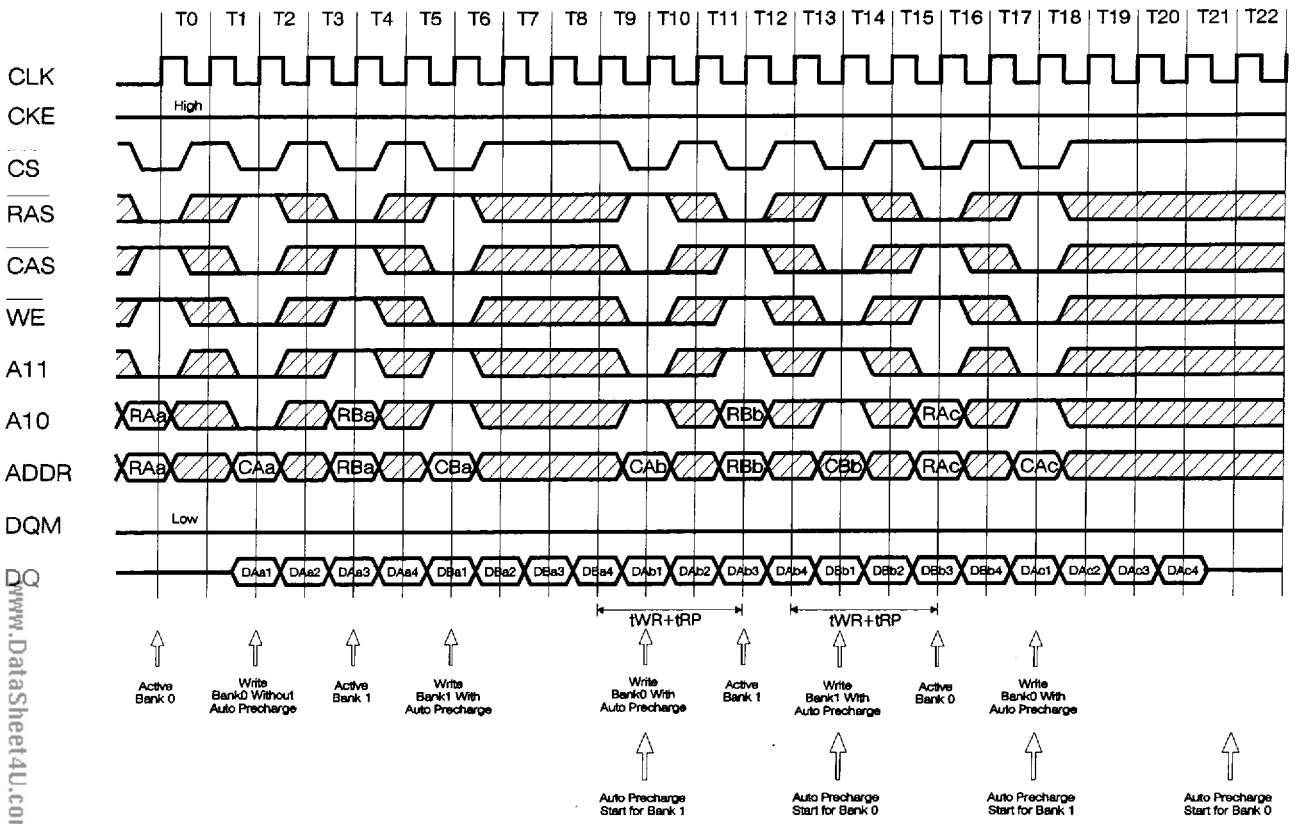
26. Full Page Write Cycle : CL=2



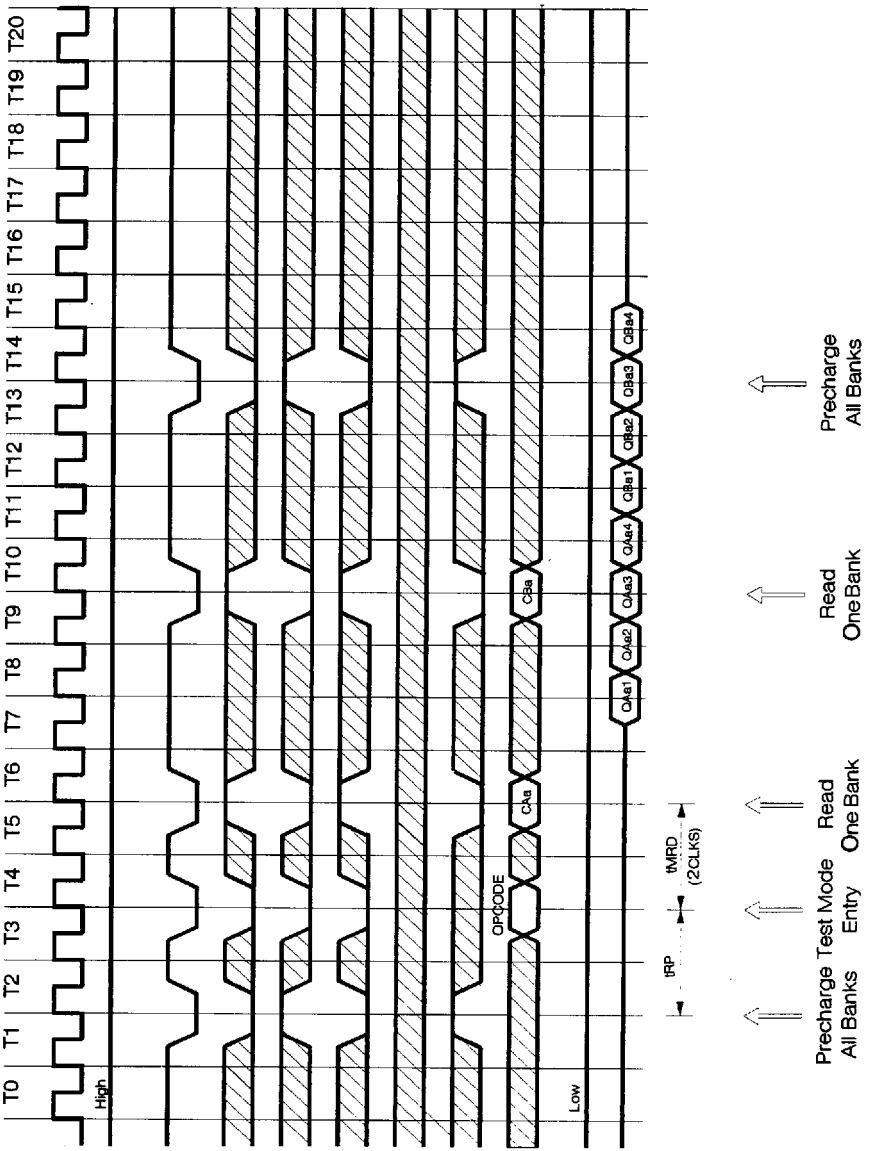
27. Auto Precharge after Read Burst : BL=4, CL=2



28. Auto Precharge after Write Burst : BL=4, CL=2



29. Test Mode for Read Cycle : BL=4, CL=2



30. Test Mode for Write Cycle : BL=4, CL=2