## DESCRIPTION

The Hynix HY57V281620A is a 134,217,728bit CMOS Synchronous DRAM, ideally suited for the Mobile applications which require low power consumption and extended temperature range . HY57V281620A is organized as 4banks of 2,097,152x16

HY57V281620A is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8, or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

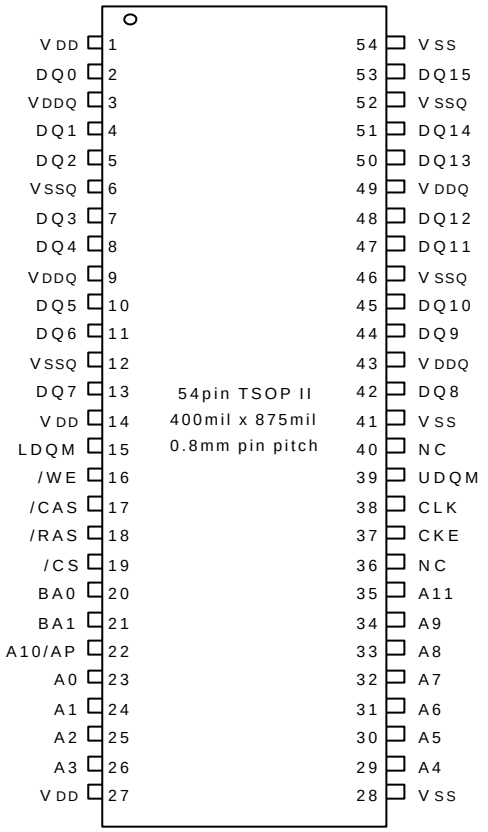
## FEATURES

- Single 3.3±0.3V power supply
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 54pin TSOP-II with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM or LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or Full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 2, 3 Clocks

## ORDERING INFORMATION

| Part No. | Clock Frequency | Power | Organization | Interface | Package |
|---|---|---|---|---|---|
| HY57V281620AT-KI | 133MHz | Normal | 4Banks x 2Mbits x16 | LVTTL | 400mil 54pin TSOP II |
| HY57V281620AT-HI | 133MHz | | | | |
| HY57V281620AT-PI | 100MHz | | | | |
| HY57V281620AT-SI | 100MHz | | | | |
| HY57V281620ALT-KI | 133MHz | Low Power | | | |
| HY57V281620ALT-HI | 133MHz | | | | |
| HY57V281620ALT-PI | 100MHz | | | | |
| HY57V281620ALT-SI | 100MHz | | | | |

## PIN CONFIGURATION

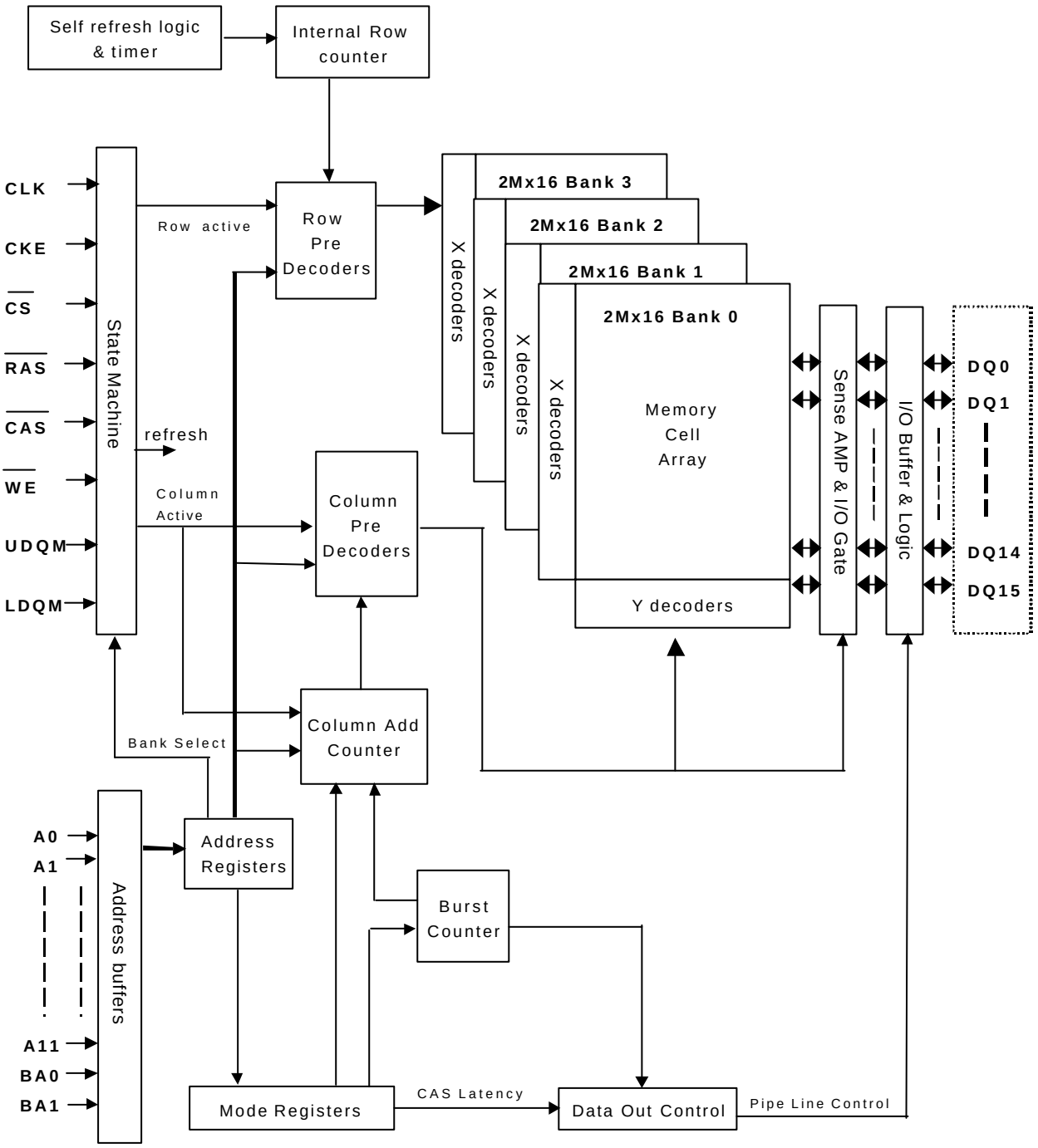



## PIN DESCRIPTION

| PIN | PIN NAME | DESCRIPTION |
|---|---|---|
| CLK | Clock | The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK |
| CKE | Clock Enable | Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh |
| $\overline{CS}$ | Chip Select | Enables or disables all inputs except CLK, CKE, UDQM and LDQM |
| BA0, BA1 | Bank Address | Selects bank to be activated during $\overline{RAS}$ activity<br>Selects bank to be read/written during $\overline{CAS}$ activity |
| A0 ~ A11 | Address | Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA8<br>Auto-precharge flag : A10 |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Row Address Strobe, Column Address Strobe, Write Enable | $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation<br>Refer function truth table for details |
| UDQM, LDQM | Data Input/Output Mask | Controls output buffers in read mode and masks input data in write mode |
| DQ0 ~ DQ15 | Data Input/Output | Multiplexed data input / output pin |
| VDD/VSS | Power Supply/Ground | Power supply for internal circuits and input buffers |
| VDDQ/VSSQ | Data Output Power/Ground | Power supply for output buffers |
| NC | No Connection | No connection |

## FUNCTIONAL BLOCK DIAGRAM

2Mbit x 4banks x 16 I/O Synchronous DRAM



## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Ambient Temperature | $T_A$ | -40 ~ 85 | °C |
| Storage Temperature | $T_{STG}$ | -55 ~ 125 | °C |
| Voltage on Any Pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -1.0 ~ 4.6 | V |
| Voltage on $V_{DD}$ relative to $V_{SS}$ | $V_{DD}$, $V_{DDQ}$ | -1.0 ~ 4.6 | V |
| Short Circuit Output Current | $I_{OS}$ | 50 | mA |
| Power Dissipation | $P_D$ | 1 | W |
| Soldering Temperature · Time | $T_{SOLDER}$ | 260 · 10 | °C · Sec |

**Note :** Operation at above absolute maximum rating can adversely affect device reliability.

## DC OPERATING CONDITION ($T_A$= -40 to 85°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{DD}$, $V_{DDQ}$ | 3.0 | 3.3 | 3.6 | V | 1 |
| Input High voltage | $V_{IH}$ | 2.0 | 3.0 | $V_{DDQ}$ + 0.3 | V | 1,2 |
| Input Low voltage | $V_{IL}$ | -0.3 | 0 | 0.8 | V | 1,3 |

**Note :**
1.All voltages are referenced to $V_{SS}$ = 0V
2.$V_{IH}$(max) is acceptable 5.6V AC pulse width with <=3ns of duration.
3.$V_{IL}$(min) is acceptable -2.0V AC pulse width with <=3ns of duration.

## AC OPERATING TEST CONDITION ($T_A$= -40 to 85°C, $V_{DD}$=3.3±0.3V, $V_{SS}$=0V)

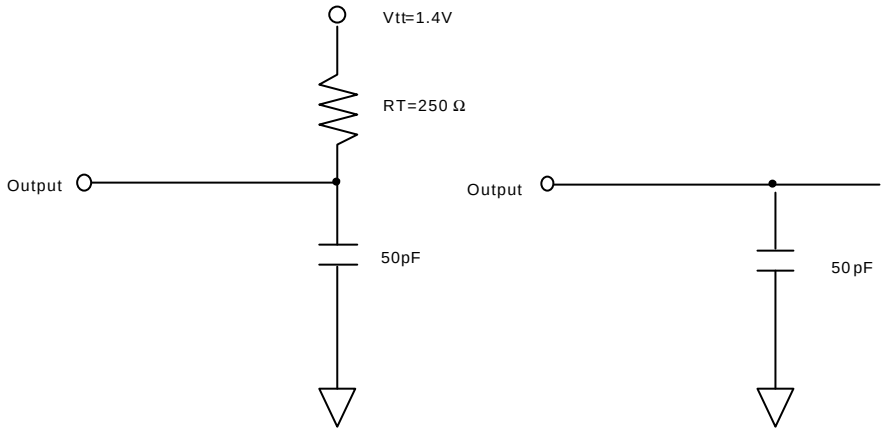
| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| AC Input High / Low Level Voltage | $V_{IH}$ / $V_{IL}$ | 2.4/0.4 | V | |
| Input Timing Measurement Reference Level Voltage | Vtrip | 1.4 | V | |
| Input Rise / Fall Time | tR / tF | 1 | ns | |
| Output Timing Measurement Reference Level Voltage | Voutref | 1.4 | V | |
| Output Load Capacitance for Access Time Measurement | $C_L$ | 50 | pF | 1 |

**Note :**
1.Output load to measure access times is equivalent to two TTL gates and one capacitor (50pF). For details, refer to AC/DC output load circuit

## CAPACITANCE (TA=25°C, f=1MHz)

| Parameter | Pin | Symbol | -HI | | -SI | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Input capacitance | CLK | $C_{I1}$ | 2.5 | 3.5 | 2.5 | 4.0 | pF |
| | A0 ~ A11, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, UDQM, LDQM | $C_{I2}$ | 2.5 | 3.8 | 2.5 | 5.0 | pF |
| Data input / output capacitance | DQ0 ~ DQ15 | $C_{I/O}$ | 4.0 | 6.5 | 4.0 | 6.5 | pF |

## OUTPUT LOAD CIRCUIT




DC Output Load Circuit

AC Output Load Circuit

## DC CHARACTERISTICS I (TA= -40 to 85°C, $V_{DD}$=3.3±0.3V)

| Parameter | Symbol | Min. | Max | Unit | Note |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | -1 | 1 | uA | 1 |
| Output Leakage Current | $I_{LO}$ | -1 | 1 | uA | 2 |
| Output High Voltage | $V_{OH}$ | 2.4 | - | V | $I_{OH}$ = -4mA |
| Output Low Voltage | $V_{OL}$ | - | 0.4 | V | $I_{OL}$ = +4mA |

**Note :**

1. $V_{IN}$ = 0 to 3.6V, All other pins are not tested under $V_{IN}$ =0V
2. $D_{OUT}$ is disabled, $V_{OUT}$=0 to 3.6

## DC CHARACTERISTICS II (TA= -40 to 85°C, VDD=3.3±0.3V, VSS=0V)

| Parameter | Symbol | Test Condition | | Speed | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | -KI | -HI | -PI | -SI | | |
| Operating Current | IDD1 | Burst length=1, One bank active<br>tRC ≥ tRC(min), IOL=0mA | | 120 | 110 | 100 | 100 | mA | 1 |
| Precharge Standby Current in Power Down Mode | IDD2P | CKE ≤ VIL(max), tCK = 15ns | | 2 | | | | mA | |
| | IDD2PS | CKE ≤ VIL(max), tCK = ∞ | | 2 | | | | | |
| Precharge Standby Current in Non Power Down Mode | IDD2N | CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns<br>Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V | | 20 | | | | mA | |
| | IDD2NS | CKE ≥ VIH(min), tCK = ∞<br>Input signals are stable. | | 10 | | | | | |
| Active Standby Current in Power Down Mode | IDD3P | CKE ≤ VIL(max), tCK = 15ns | | 7 | | | | mA | |
| | IDD3PS | CKE ≤ VIL(max), tCK = ∞ | | 7 | | | | | |
| Active Standby Current in Non Power Down Mode | IDD3N | CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns<br>Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V | | 40 | | | | mA | |
| | IDD3NS | CKE ≥ VIH(min), tCK = ∞<br>Input signals are stable. | | 40 | | | | | |
| Burst Mode Operating Current | IDD4 | tCK ≥ tCK(min), IOL=0mA<br>All banks active | CL=3 | 120 | 120 | 100 | 100 | mA | 1 |
| | | | CL=2 | 120 | 100 | 100 | 90 | | |
| Auto Refresh Current | IDD5 | tRRC ≥ tRRC(min), All banks active | | 240 | 220 | 200 | 200 | mA | 2 |
| Self Refresh Current | IDD6 | CKE ≤ 0.2V | | 2 | | | | mA | 3 |
| | | | | 800 | | | | uA | 4 |

Note:

1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
2. Min. of tRRC (Refresh $\overline{RAS}$ cycle time) is shown at AC CHARACTERISTICS II
3. HY57V281620AT-KI/HI/PI/SI
4. HY57V281620ALT-KI/HI/PI/SI

## AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

| Parameter | | Symbol | -KI | | -HI | | -PI | | -SI | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| System Clock Cycle Time | CAS Latency = 3 | tCK3 | 7.5 | 1000 | 7.5 | 1000 | 10 | 1000 | 10 | 1000 | ns | |
| | CAS Latency = 2 | tCK2 | 7.5 | | 10 | | 10 | | 12 | | ns | |
| Clock High Pulse Width | | tCHW | 2.5 | - | 2.5 | - | 3 | - | 3 | - | ns | 1 |
| Clock Low Pulse Width | | tCLW | 2.5 | - | 2.5 | - | 3 | - | 3 | - | ns | 1 |
| Access Time From Clock | CAS Latency = 3 | tAC3 | - | 5.4 | - | 5.4 | - | 6 | - | 6 | ns | 2 |
| | CAS Latency = 2 | tAC2 | - | 5.4 | - | 6 | - | 6 | - | 6 | ns | |
| Data-Out Hold Time | | tOH | 2.5 | - | 2.5 | - | 2.5 | - | 2.5 | - | ns | |
| Data-Input Setup Time | | tDS | 1.5 | - | 1.5 | - | 2 | - | 2 | - | ns | 1 |
| Data-Input Hold Time | | tDH | 0.8 | - | 0.8 | - | 1 | - | 1 | - | ns | 1 |
| Address Setup Time | | tAS | 1.5 | - | 1.5 | - | 2 | - | 2 | - | ns | 1 |
| Address Hold Time | | tAH | 0.8 | - | 0.8 | - | 1 | - | 1 | - | ns | 1 |
| CKE Setup Time | | tCKS | 1.5 | - | 1.5 | - | 2 | - | 2 | - | ns | 1 |
| CKE Hold Time | | tCKH | 0.8 | - | 0.8 | - | 1 | - | 1 | - | ns | 1 |
| Command Setup Time | | tCS | 1.5 | - | 1.5 | - | 2 | - | 2 | - | ns | 1 |
| Command Hold Time | | tCH | 0.8 | - | 0.8 | - | 1 | - | 1 | - | ns | 1 |
| CLK to Data Output in Low-Z Time | | tOLZ | 1 | - | 1 | - | 1 | - | 1 | - | ns | |
| CLK to Data Output in High-Z Time | CAS Latency = 3 | tOHZ3 | 2.7 | 5.4 | 2.7 | 5.4 | 3 | 6 | 3 | 6 | ns | |
| | CAS Latency = 2 | tOHZ2 | 2.7 | 5.4 | 3 | 6 | 3 | 6 | 3 | 6 | ns | |

**Note :**

1. Assume tR / tF (input rise and fall time ) is 1ns
   If tR & tF > 1ns, then [(tR+tF)/2-1]ns should be added to the parameter
2. Access times to be measured with input signals of 1v/ns edge rate, from 0.8v to 2.0v
   If tR > 1ns, then (tR/2-0.5)ns should be added to the parameter

## AC CHARACTERISTICS II

| Parameter | | Symbol | -KI | | -HI | | -PI | | -SI | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| $\overline{RAS}$ Cycle Time | Operation | tRC | 60 | - | 65 | - | 70 | - | 70 | - | ns | |
| | Auto Refresh | tRRC | 60 | - | 65 | - | 70 | - | 70 | - | ns | |
| $\overline{RAS}$ to$\overline{CAS}$ Delay | | tRCD | 15 | - | 20 | - | 20 | - | 20 | - | ns | |
| $\overline{RAS}$ Active Time | | tRAS | 45 | 100K | 45 | 100K | 50 | 100K | 50 | 100K | ns | |
| $\overline{RAS}$ Precharge Time | | tRP | 15 | - | 20 | - | 20 | - | 20 | - | ns | |
| $\overline{RAS}$ to$\overline{RAS}$ Bank Active Delay | | tRRD | 15 | - | 15 | - | 20 | - | 20 | - | ns | |
| $\overline{CAS}$ to$\overline{CAS}$ Delay | | tCCD | 1 | - | 1 | - | 1 | - | 1 | - | CLK | |
| Write Command to Data-In Delay | | tWTL | 0 | - | 0 | - | 0 | - | 0 | - | CLK | |
| Data-In to Precharge Command | | tDPL | 2 | - | 2 | - | 2 | - | 2 | - | CLK | |
| Data-In to Active Command | | tDAL | 4 | - | 5 | - | 3 | - | 4 | - | CLK | |
| DQM to Data-Out Hi-Z | | tDQZ | 2 | - | 2 | - | 2 | - | 2 | - | CLK | |
| DQM to Data-In Mask | | tDQM | 0 | - | 0 | - | 0 | - | 0 | - | CLK | |
| MRS to New Command | | tMRD | 2 | - | 2 | - | 2 | - | 2 | - | CLK | |
| Precharge to Data Output Hi-Z | $\overline{CAS}$ Latency = 3 | tPROZ3 | 3 | - | 3 | - | 3 | - | 3 | - | CLK | |
| | $\overline{CAS}$ Latency = 2 | tPROZ2 | 2 | - | 2 | - | 2 | - | 2 | - | CLK | |
| Power Down Exit Time | | tPDE | 1 | - | 1 | - | 1 | - | 1 | - | CLK | |
| Self Refresh Exit Time | | tSRE | 1 | - | 1 | - | 1 | - | 1 | - | CLK | 1 |
| Refresh Time | | tREF | - | 64 | - | 64 | - | 64 | - | 64 | ms | |

**Note :**

1. A new command can be given tRRC after self refresh exit

## DEVICE OPERATING OPTION TABLE

### HY57V281620A(L)T-KI

| | $\overline{CAS}$ Latency | tRCD | tRAS | tRC | tRP | tAC | tOH |
|---|---|---|---|---|---|---|---|
| 133MHz(7.5ns) | 2CLKs | 2CLKs | 6CLKs | 8CLKs | 2CLKs | 5.4ns | 2.5ns |
| 100MHz(10ns) | 2CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 2.5ns |

### HY57V281620A(L)T-HI

| | $\overline{CAS}$ Latency | tRCD | tRAS | tRC | tRP | tAC | tOH |
|---|---|---|---|---|---|---|---|
| 133MHz(7.5ns) | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 5.4ns | 2.5ns |
| 100MHz(10ns) | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 6ns | 2.5ns |

### HY57V281620A(L)T-PI

| | $\overline{CAS}$ Latency | tRCD | tRAS | tRC | tRP | tAC | tOH |
|---|---|---|---|---|---|---|---|
| 100MHz(10ns) | 2CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 2.5ns |
| 83MHz(12ns) | 2CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 2.5ns |

### HY57V281620A(L)T-SI

| | $\overline{CAS}$ Latency | tRCD | tRAS | tRC | tRP | tAC | tOH |
|---|---|---|---|---|---|---|---|
| 100MHz(10ns) | 3CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 2.5ns |
| 83MHz(12ns) | 2CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 3ns |

## COMMAND TRUTH TABLE

| Command | | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | ADDR | A10/AP | BA | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode Register Set | | H | X | L | L | L | L | X | OP code | | | |
| No Operation | | H | X | H | X | X | X | X | X | | | |
| | | | | L | H | H | H | | | | | |
| Bank Active | | H | X | L | L | H | H | X | RA | | V | |
| Read | | H | X | L | H | L | H | X | CA | L | V | |
| Read with Autoprecharge | | | | | | | | | | H | | |
| Write | | H | X | L | H | L | L | X | CA | L | V | |
| Write with Autoprecharge | | | | | | | | | | H | | |
| Precharge All Banks | | H | X | L | L | H | L | X | X | H | X | |
| Precharge selected Bank | | | | | | | | | | L | V | |
| Burst Stop | | H | X | L | H | H | L | X | X | | | |
| DQM | | H | X | | | | | V | X | | | |
| Auto Refresh | | H | H | L | L | L | H | X | X | | | |
| Self Refresh[1] | Entry | H | L | L | L | L | H | X | X | | | |
| | Exit | L | H | H | X | X | X | X | | | | |
| | | | | L | H | H | H | | | | | |
| Precharge power down | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | L | H | H | H | | | | | |
| | Exit | L | H | H | X | X | X | X | | | | |
| | | | | L | H | H | H | | | | | |
| Clock Suspend | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | L | V | V | V | | | | | |
| | Exit | L | H | X | | | | X | | | | |

**Note :**

1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA =Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation

## PACKAGE INFORMATION

**400mil 54pin Thin Small Outline Package**