256Mb DDR SDRAM

HY5DU56422D(L)T

HY5DU56822D(L)T

HY5DU561622D(L)T

Revision History

Revision No.	History	Draft Date	Remark
1.0	First Version Release- Merged HY5DU564(8,16)22D(L)T and HY5DU564(8,16)22D(L)T-D into HY5DU564(8,16)22D(L)T.	Oct. 2004	

DESCRIPTION

The HY5DU56422D(L)T, HY5DU56822D(L)T and HY5DU561622D(L)T are a 268,435,456-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth.

This Hynix 256Mb DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

FEATURES

- VDD, VDDQ = 2.5V +/- 0.2V for DDR200, 266, 333
  VDD, VDDQ = 2.6V +/- 0.1V for DDR400
- All inputs and outputs are compatible with SSTL_2 interface
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
- x16 device has two bytewide data strobes (UDQS, LDQS) per each x8 I/O
- Data outputs on DQS edges when read (edged DQ)
  Data inputs on DQS centers when write (centered DQ)
- On chip DLL align DQ and DQS transition with CK transition
- DM mask write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 2/2.5 (DDR200, 266, 333) and 3 (DDR400) supported
- Programmable burst length 2/4/8 with both sequential and interleave mode
- Internal four bank operations with single pulsed /RAS
- Auto refresh and self refresh supported
- tRAS lock out function supported
- 8192 refresh cycles / 64ms
- JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
- Full and Half strength driver option controlled by EMRS

ORDERING INFORMATION

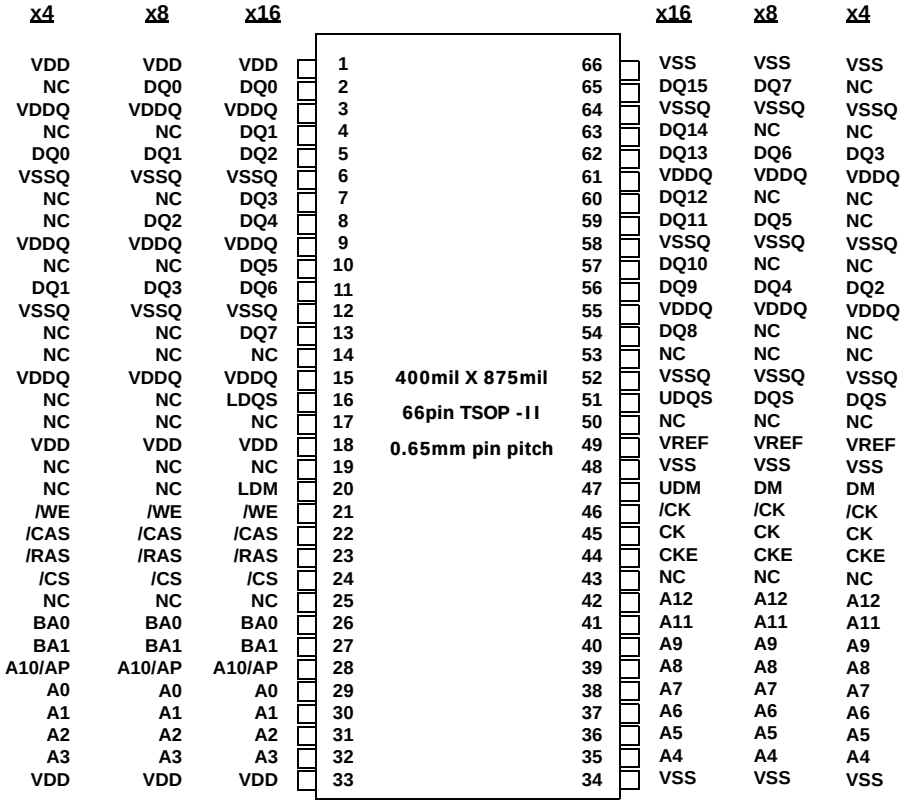
Part No.	Configuration	Package
HY5DU56422D(L)T-X*	64M x 4	400mil 66pin TSOP-II
HY5DU56822D(L)T-X*	32M x 8	
HY5DU561622D(L)T-X*	16M x 16	

* X means speed grade

OPERATING FREQUENCY

Grade	Clock Rate		Remark (CL-tRCD-tRP)
-D43	200MHz@CL3		DDR400B (3-3-3)
- J	133MHz@CL2	166MHz@CL2.5	DDR333 (2.5-3-3)
- K	133MHz@CL2	133MHz@CL2.5	DDR266A (2-3-3)
- H	100MHz@CL2	133MHz@CL2.5	DDR266B (2.5-3-3)
- L	100MHz@CL2		DDR200 (2-2-2)

PIN CONFIGURATION



ROW AND COLUMN ADDRESS TABLE

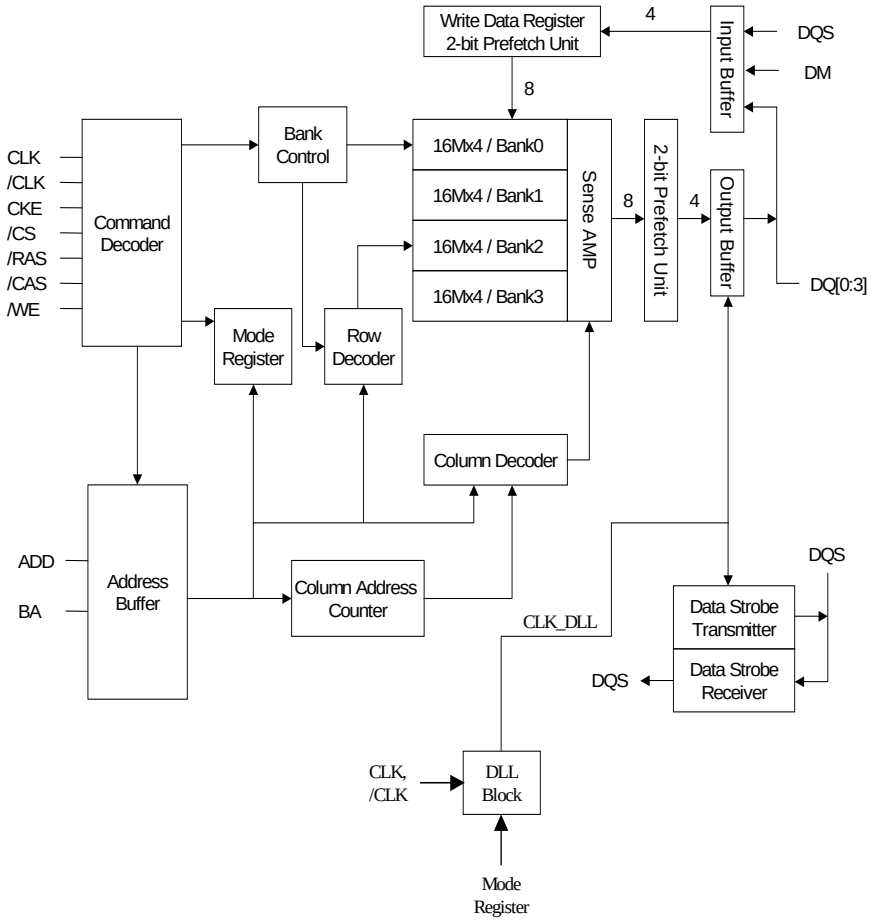
ITEMS	64Mx4	32Mx8	16Mx16
Organization	16M x 4 x 4banks	8M x 8 x 4banks	4M x 16 x 4banks
Row Address	A0 - A12	A0 - A12	A0 - A12
Column Address	A0-A9, A11	A0-A9	A0-A8
Bank Address	BA0, BA1	BA0, BA1	BA0, BA1
Auto Precharge Flag	A10	A10	A10
Refresh	8K	8K	8K

PIN DESCRIPTION

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied.
/CS	Input	Chip Select: Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when CS is registered high. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
DM (LDM,UDM)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For the x16, LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15.
DQS (LDQS,UDQS)	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. For the x16, LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15.
DQ	I/O	Data input / output pin: Data bus
VDD/VSS	Supply	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Supply	Power supply for output buffers for noise immunity.
VREF	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

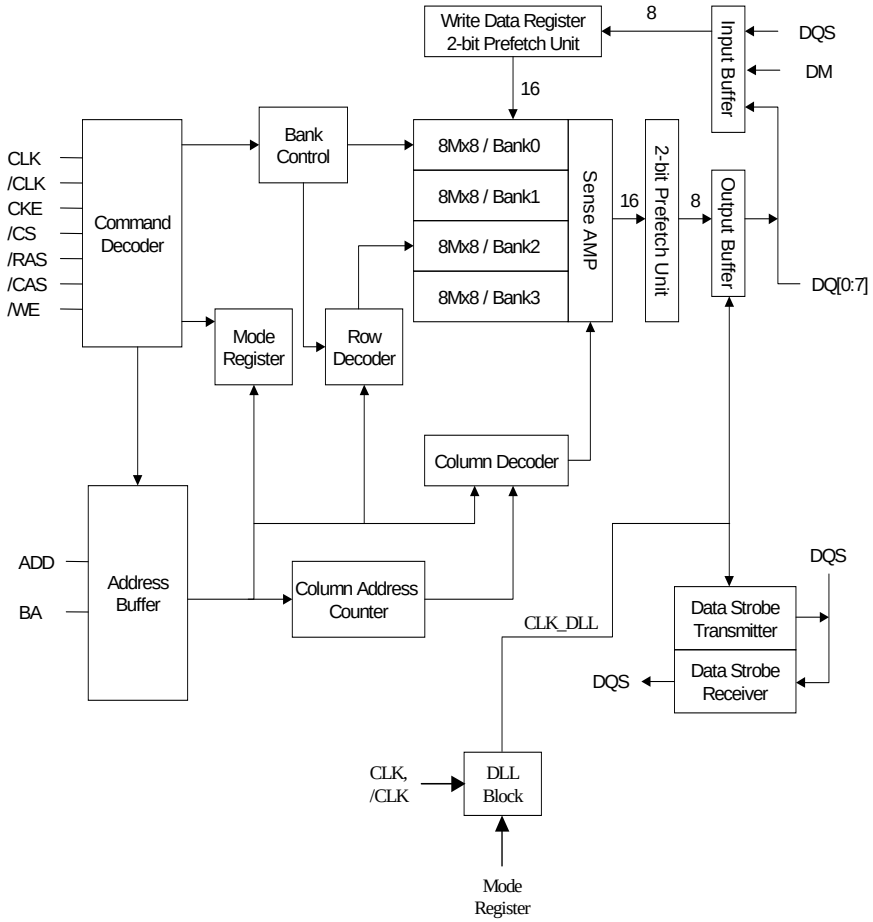
FUNCTIONAL BLOCK DIAGRAM (64Mx4)

4Banks x 16Mbit x 4 I/O Double Data Rate Synchronous DRAM



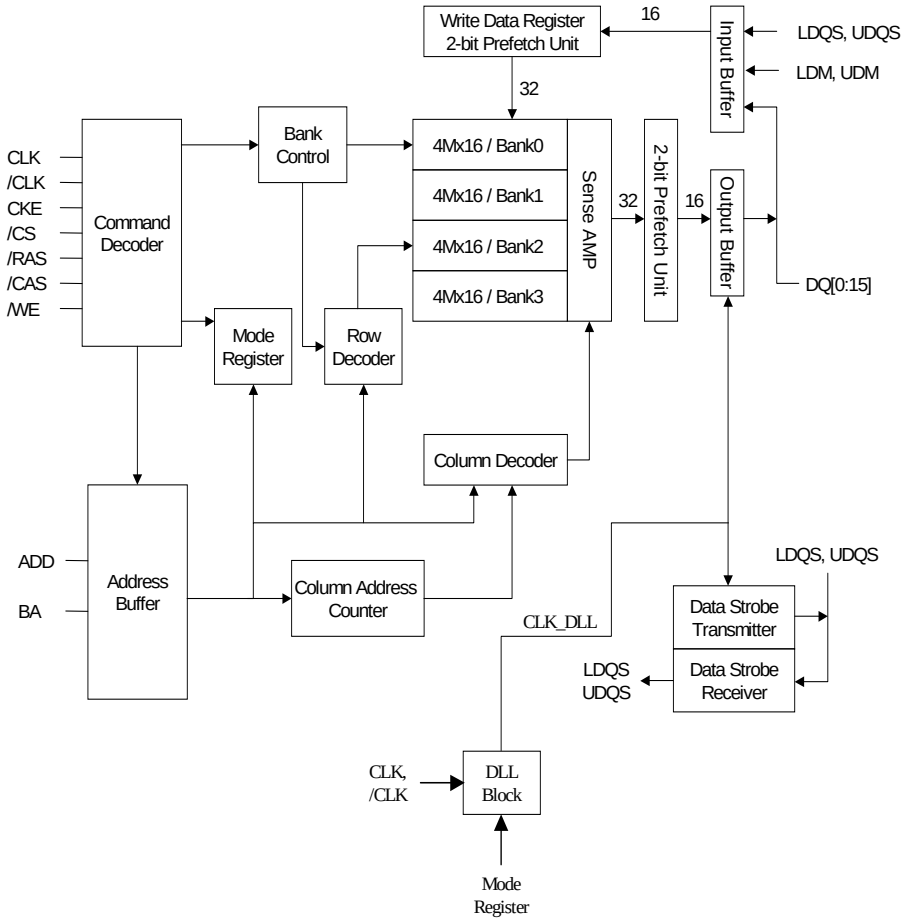
FUNCTIONAL BLOCK DIAGRAM (32Mx8)

4Banks x 8Mbit x 8 I/O Double Data Rate Synchronous DRAM



FUNCTIONAL BLOCK DIAGRAM (16Mx16)

4Banks x 4Mbit x 16 I/O Double Data Rate Synchronous DRAM



SIMPLIFIED COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	CS	RAS	CAS	WE	ADDR	A10/AP	BA
Extended Mode Register Set[1,2]		H	X	L	L	L	L	OP code		
Mode Register Set[1,2]		H	X	L	L	L	L	OP code		
Device Deselect[1]		H	X	H	X	X	X	X		
No Operation[1]				L	H	H	H			
Bank Active[1]		H	X	L	L	H	H	RA		V
Read[1]		H	X	L	H	L	H	CA	L	V
Read with Autoprecharge[1,3]									H	
Write[1]		H	X	L	H	L	L	CA	L	V
Write with Autoprecharge[1,4]									H	
Precharge All Banks[1,5]		H	X	L	L	H	L	X	H	X
Precharge selected Bank[1]									L	V
Read Burst Stop[1]		H	X	L	H	H	L	X		
Auto Refresh[1]		H	H	L	L	L	H	X		
Self Refresh[1]	Entry	H	L	L	L	L	H	X		
	Exit	L	H	H	X	X	X			
				L	H	H	H			
Precharge Power Down Mode[1]	Entry	H	L	H	X	X	X	X		
				L	H	H	H			
	Exit	L	H	H	X	X	X			
				L	H	H	H			
Active Power Down Mode[1]	Entry	H	L	H	X	X	X	X		
				L	V	V	V			
	Exit	L	H	X						

(H=Logic High Level, L=Logic Low Level, X=Don't Care, V=Valid Data Input, OP Code=Operand Code, NOP=No)

Note:

1. LDM/UDM states are Don't Care. Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of A0~A12 and BA0~BA1 used for Mode Register setting during Extended MRS or MRS. Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Precharge command.
3. If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
4. If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tWR+tRP). Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
5. If A10/AP is High when Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.

*For more information about Truth Table, refer to "Device Operation" section in Hynix website.

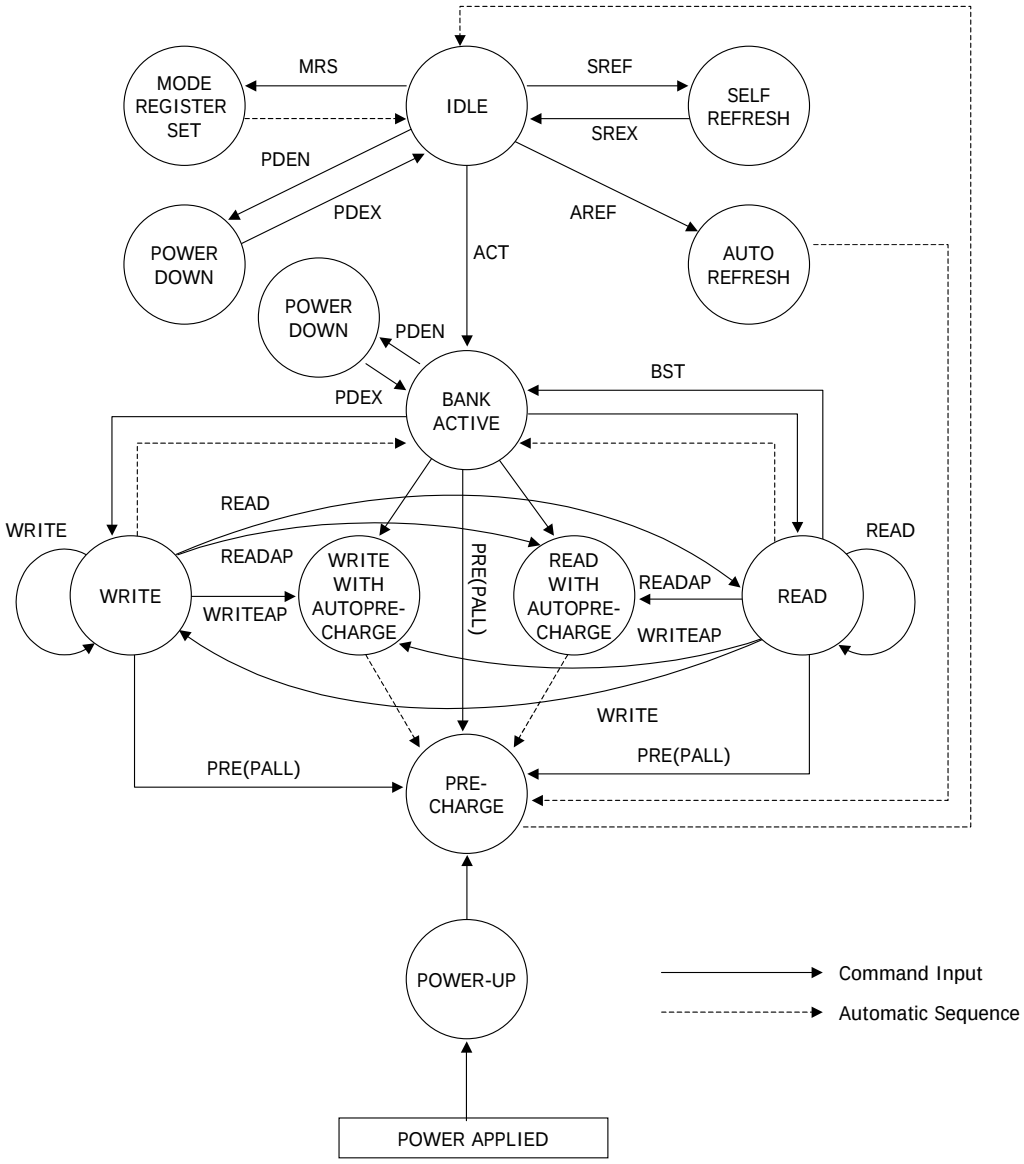
WRITE MASK TRUTH TABLE

Function	CKEn-1	CKEn	/CS, /RAS, /CAS, /WE	DM	ADDR	A10/AP	BA
Data Write[1]	H	X	X	L	X		
Data-In Mask[1]	H	X	X	H	X		

Note:

1. Write Mask command masks burst write data with reference to LDQS/UDQS(Data Strobes) and it is not related with read data. In case of x16 data I/O, LDM and UDM control lower byte(DQ0~7) and Upper byte(DQ8~15) respectively.

SIMPLIFIED STATE DIAGRAM



POWER-UP SEQUENCE AND DEVICE INITIALIZATION

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD, then to VDDQ, and finally to VREF (and to the system VTT). VTT must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied anytime after VDDQ, but is expected to be nominally coincident with VTT. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after VDD is applied. Maintaining an LVCMOS LOW level on CKE during power-up is required to guarantee that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200us delay prior to applying an executable command.

Once the 200us delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRECHARGE ALL command should be applied. Next a EXTENDED MODE REGISTER SET command should be issued for the Extended Mode Register, to enable the DLL, then a MODE REGISTER SET command should be issued for the Mode Register, to reset the DLL, and to program the operating parameters. After the DLL reset, tXSRD(DLL locking time) should be satisfied for read command. After the Mode Register set command, a PRECHARGE ALL command should be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. Additionally, a MODE REGISTER SET command for the Mode Register, with the reset DLL bit deactivated low (i.e. to program operating parameters without resetting the DLL) must be performed. Following these cycles, the DDR SDRAM is ready for normal operation.

1. Apply power - VDD, VDDQ, VTT, VREF in the following power up sequencing and attempt to maintain CKE at LVCMOS low state. (All the other input pins may be undefined.)

   - VDD and VDDQ are driven from a single power converter output.
   - VTT is limited to 1.44V (reflecting VDDQ(max)/2 + 50mV VREF variation + 40mV VTT variation.
   - VREF tracks VDDQ/2.
   - A minimum resistance of 42 Ohms (22 ohm series resistor + 22 ohm parallel resistor - 5% tolerance) limits the input current from the VTT supply into any pin.
   - If the above criteria cannot be met by the system design, then the following sequencing and voltage relationship must be adhered to during power up.

Voltage description	Sequencing	Voltage relationship to avoid latch-up
VDDQ	After or with VDD	< VDD + 0.3V
VTT	After or with VDDQ	< VDDQ + 0.3V
VREF	After or with VDDQ	< VDDQ + 0.3V

2. Start clock and maintain stable clock for a minimum of 200usec.

3. After stable power and clock, apply NOP condition and take CKE high.

4. Issue Extended Mode Register Set (EMRS) to enable DLL.

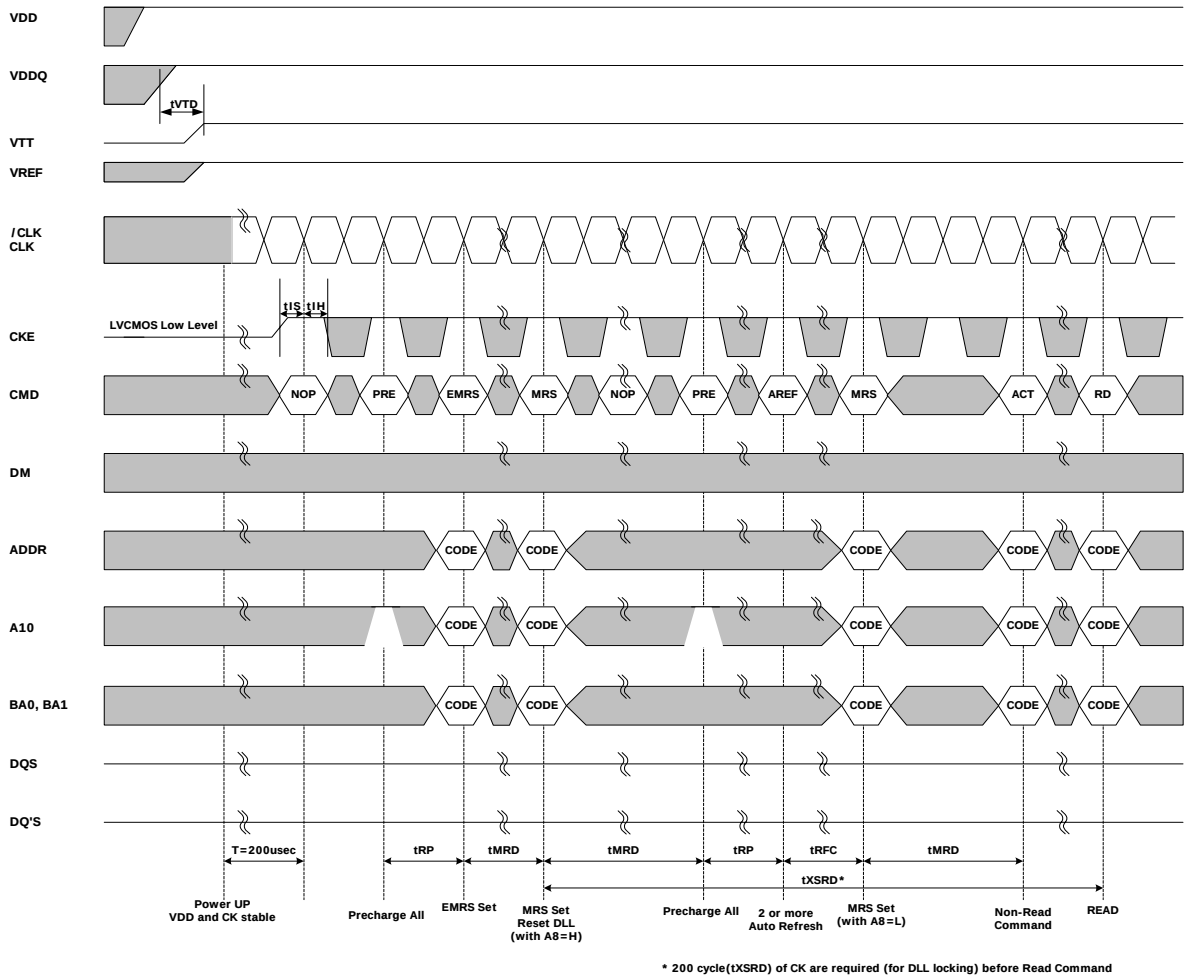
5. Issue Mode Register Set (MRS) to reset DLL and set device to idle state with bit A8=high. (An additional 200 cycles(tXSRD) of clock are required for locking DLL)

6. Issue Precharge commands for all banks of the device.

7. Issue 2 or more Auto Refresh commands.

8. Issue a Mode Register Set command to initialize the mode register with bit A8 = Low

Power-Up Sequence



MODE REGISTER SET (MRS)

The mode register is used to store the various operating modes such as /CAS latency, addressing mode, burst length, burst type, test mode, DLL reset. The mode register is programed via MRS command. This command is issued by the low signals of /RAS, /CAS, /CS, /WE and BA0. This command can be issued only when all banks are in idle state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. Two cycles are required to write the data in mode register. During the MRS cycle, any command cannot be issued. Once mode register field is determined, the information will be held until reset by another MRS command.

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	Operating Mode						CAS Latency			BT	Burst Length		

BA0	MRS Type
0	MRS
1	EMRS

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	1.5
1	1	0	2.5
1	1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleave

A12~A9	A8	A7	A6~A0	Operating Mode
0	0	0	Valid	Normal Operation
0	1	0	Valid	Normal Operation/ Reset DLL
0	0	1	VS	Vendor specific Test Mode
-	-	-	-	All other states reserved

A2	A1	A0	Burst Length	
			Sequential	Interleave
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

BURST DEFINITION

Burst Length	Starting Address (A2,A1,A0)	Sequential	Interleave
2	XX0	0, 1	0, 1
	XX1	1, 0	1, 0
4	X00	0, 1, 2, 3	0, 1, 2, 3
	X01	1, 2, 3, 0	1, 0, 3, 2
	X10	2, 3, 0, 1	2, 3, 0, 1
	X11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

BURST LENGTH & TYPE

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable. The burst length determines the maximum number of column locations that can be accessed for a given Read or Write command. Burst lengths of 2, 4 or 8 locations are available for both the sequential and the interleaved burst types. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a Read or Write command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block if a boundary is reached. The block is uniquely selected by A1-Ai when the burst length is set to two, by A2 -Ai when the burst length is set to four and by A3 -Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both Read and Write bursts.

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Burst Definition Table

CAS LATENCY

The Read latency or CAS latency is the delay in clock cycles between the registration of a Read command and the availability of the first burst of output data. The latency can be programmed 2 or 2.5 clocks for DDR200/266/333 and 3 clocks for DDR400.

If a Read command is registered at clock edge n, and the latency is m clocks, the data is available nominally coincident with clock edge n + m.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DLL RESET

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled, 200 clock cycles must occur to allow time for the internal clock to lock to the externally applied clock before an any command can be issued.

OUTPUT DRIVER IMPEDANCE CONTROL

The normal drive strength for all outputs is specified to be SSTL_2, Class II. Hynix also supports a half strength driver option, intended for lighter load and/or point-to-point environments. Selection of the half strength driver option will reduce the output drive strength by 50% of that of the full strength driver. I-V curves for both the full strength driver and the half strength driver are included in this document.

EXTENDED MODE REGISTER SET (EMRS)

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable, output driver strength selection(optional). These functions are controlled via the bits shown below. The Extended Mode Register is programmed via the Mode Register Set command (BA0=1 and BA1=0) and will retain the stored information until it is programmed again or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements wil result in unspecified operation.

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	Operating Mode										0*	DS	DLL

BA0	MRS Type
0	MRS
1	EMRS

A0	DLL enable
0	Enable
1	Disable

A1	Output Driver Impedance Control
0	Full Strength Driver
1	Half Strength Driver

An~A3	A2~A0	Operating Mode
0	Valid	Normal Operation
_	_	All other states reserved

* This part do not support/QFC function, A2 must be programmed to Zero.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Operating Temperature (Ambient)	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 150	°C
Voltage on VDD relative to VSS	VDD	-1.0 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-1.0 ~ 3.6	V
Voltage on inputs relative to VSS	VINPUT	-1.0 ~ 3.6	V
Voltage on I/O pins relative to VSS	VIO	-0.5 ~3.6	V
Output Short Circuit Current	IOS	50	mA
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note: Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter		Symbol	Min	Typ.	Max	Unit
Power Supply Voltage (DDR200, 266, 333)		VDD	2.3	2.5	2.7	V
Power Supply Voltage (DDR200, 266, 333)[1]		VDDQ	2.3	2.5	2.7	V
Power Supply Voltage (DDR400)		VDD	2.5	2.6	2.7	V
Power Supply Voltage (DDR400)[1]		VDDQ	2.5	2.6	2.7	V
Input High Voltage		VIH	VREF + 0.15	-	VDDQ + 0.3	V
Input Low Voltage[2]		VIL	-0.3	-	VREF - 0.15	V
Termination Voltage		VTT	VREF - 0.04	VREF	VREF + 0.04	V
Reference Voltage[3]		VREF	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V
Input Voltage Level, CK and $\overline{CK}$ inputs		VIN(DC)	-0.3	-	VDDQ+0.3	V
Input Differential Voltage, CK and $\overline{CK}$ inputs[4]		VID(DC)	0.36	-	VDDQ+0.6	V
V-I Matching: Pullup to Pulldown Current Ratio[5]		VI(RATIO)	0.71	-	1.4	-
Input Leakage Current[6]		ILI	-2	-	2	uA
Output Leakage Current[7]		ILO	-5	-	5	uA
Normal Strength Output Driver (VOUT=VTT±0.84)	Output High Current (min VDDQ, min VREF, min VTT)	IOH	-16.8	-	-	mA
	Output Low Current (min VDDQ, max VREF, max VTT)	IOL	16.8	-	-	mA
Half Strength Output Driver (VOUT=VTT±0.68)	Output High Current (min VDDQ, min VREF, min VTT)	IOH	-13.6	-	-	mA
	Output Low Current (min VDDQ, max VREF, max VTT)	IOL	13.6	-	-	mA

Note:

1. VDDQ must not exceed the level of VDD.
2. VIL (min) is acceptable -1.5V AC pulse width with ≤ 5ns of duration.
3. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of the same. Peak to peak noise on VREF may not exceed +/- 2% of the DC value.
4. VID is the magnitude of the difference between the input level on CK and the input level on /CK.
5. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1/7 for device drain to source voltages from 0.1 to 1.0.
6. VIN=0 to VDD, All other pins are not tested under VIN =0V.
7. DQs are disabled, VOUT=0 to VDDQ

IDD SPECIFICATION AND CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Test Conditions

Test Condition	Symbol
Operating Current: One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	IDD0
Operating Current: One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	IDD1
Precharge Power Down Standby Current: All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	IDD2P
Idle Standby Current: /CS=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	IDD2F
Idle Quiet Standby Current: /CS>=Vih(min); All banks idle; CKE>=Vih(min); Addresses and other control inputs stable, Vin=Vref for DQ, DQS and DM	IDD2Q
Active Power Down Standby Current: One bank active; Power down mode; CKE=Low, tCK=tCK(min)	IDD3P
Active Standby Current: /CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N
Operating Current: Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	IDD4R
Operating Current: Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	IDD4W
Auto Refresh Current: tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh tRC=tRFC(min) - 14*tCK for DDR400 at 200Mhz	IDD5
Self Refresh Current: CKE =< 0.2V; External clock on; tCK=tCK(min)	IDD6
Operating Current - Four Bank Operation: Four bank interleaving with BL=4, Refer to the following page for detailed test condition	IDD7

DETAILED TEST CONDITIONS FOR DDR SDRAM IDD1 & IDD7

IDD1: Operating current: One bank operation

1. Typical Case: VDD = 2.5V, T=25 °C for DDR200, 266, 333; VDD = 2.6V, T=25 °C for DDR400
2. Worst Case: VDD = 2.7V, T= 0 °C
3. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA
4. Timing patterns
   - DDR200(100Mhz, CL=2): tCK = 10ns, CL2, BL=2, tRCD = 2*tCK, tRC = 10*tCK, tRAS = 5*tCK
     Read: A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR266B(133Mhz, CL=2.5): tCK = 7.5ns, CL=2.5, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read: A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR266A (133Mhz, CL=2): tCK = 7.5ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read: A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR333(166Mhz, CL=2.5): tCK = 6ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 10*tCK, tRAS = 7*tCK
     Read: A0 N N R0 N N N P0 N N A0 N - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR400(200Mhz, CL=3): tCK = 5ns, CL=3, BL=4, tRCD = 3*tCK, tRC = 11*tCK, tRAS = 8*tCK
     Read: A0 N N R0 N N N N P0 N N - repeat the same timing with random address changing
     50% of data changing at every burst

     Legend: A=Activate, R=Read, W=Write, P=Precharge, N=NOP

IDD7: Operating current: Four bank operation

1. Typical Case: VDD = 2.5V, T=25 °C for DDR200, 266, 333; VDD = 2.6V, T=25 °C for DDR400
2. Worst Case: VDD = 2.7V, T= 0 °C
3. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout = 0mA
4. Timing patterns
   - DDR200(100Mhz, CL=2): tCK = 10ns, CL2, BL=4, tRRD = 2*tCK, tRCD= 3*tCK, Read with Autoprecharge
     Read: A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR266B(133Mhz, CL=2.5): tCK = 7.5ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK Read with autoprecharge
     Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR266A (133Mhz, CL=2): tCK = 7.5ns, CL2=2, BL=4, tRRD = 2*tCK, tRCD = 3*tCK
     Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR333(166Mhz, CL=2.5): tCK = 6ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK, Read with autoprecharge
     Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst
   - DDR400(200Mhz, CL=3): tCK = 5ns, CL = 2, BL = 4, tRRD = 2*tCK, tRCD = 3*tCK, Read with autoprecharge
     Read: A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     50% of data changing at every burst

     Legend: A=Activate, R=Read, W=Write, P=Precharge, N=NOP

IDD Specification

64Mx4

Parameter		Symbol	Speed					Unit
			DDR400B	DDR333	DDR266A	DDR266B	DDR200	
Operating Current		IDD0	90	80	70		65	mA
Operating Current		IDD1	100		90		80	mA
Precharge Power Down Standby Current		IDD2P	10					mA
Idle Standby Current		IDD2F	60	50	40		30	mA
Active Power Down Standby Current		IDD3P	15					mA
Active Standby Current		IDD3N	50	45	40		35	mA
Operating Current		IDD4R	160	150	140		120	mA
Operating Current		IDD4W	160	150	140		120	
Auto Refresh Current		IDD5	150		140		130	
Self Refresh Current	Normal	IDD6	3					mA
	Low Power		1.5					mA
Operating Current - Four Bank Operation		IDD7	250	240	220		200	mA

32Mx8

Parameter		Symbol	Speed					Unit
			DDR400B	DDR333	DDR266A	DDR266B	DDR200	
Operating Current		IDD0	90	80	70		65	mA
Operating Current		IDD1	100		90		80	mA
Precharge Power Down Standby Current		IDD2P	10					mA
Idle Standby Current		IDD2F	60	50	40		30	mA
Active Power Down Standby Current		IDD3P	15					mA
Active Standby Current		IDD3N	50	45	40		35	mA
Operating Current		IDD4R	180	160	150		130	mA
Operating Current		IDD4W	180	160	150		130	
Auto Refresh Current		IDD5	150		140		130	
Self Refresh Current	Normal	IDD6	3					mA
	Low Power		1.5					mA
Operating Current - Four Bank Operation		IDD7	230	220	200		180	mA

16Mx16

Parameter		Symbol	Speed					Unit
			DDR400B	DDR333	DDR266A	DDR266B	DDR200	
Operating Current		IDD0	90	80	70		65	mA
Operating Current		IDD1	100		90		80	mA
Precharge Power Down Standby Current		IDD2P	10					mA
Idle Standby Current		IDD2F	60	50	40		30	mA
Active Power Down Standby Current		IDD3P	15					mA
Active Standby Current		IDD3N	50	45	40		35	mA
Operating Current		IDD4R	200	190	170		150	mA
Operating Current		IDD4W	200	190	170		150	
Auto Refresh Current		IDD5	150		140		130	
Self Refresh Current	Normal	IDD6	3					mA
	Low Power		1.5					mA
Operating Current - Four Bank Operation		IDD7	250	240	220		200	mA

AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS = 0V)

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31	-	V
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)	-	VREF - 0.31	V
Input Differential Voltage, CK and /CK inputs[1]	VID(AC)	0.7	VDDQ + 0.6	V
Input Crossing Point Voltage, CK and /CK inputs[2]	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V

Note:
1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

*For more information about AC Overshoot/Undershoot Specifications, refer to “Device Operation” section in hynix website.

AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS = 0V)

Parameter	Value	Unit
Reference Voltage	VDDQ x 0.5	V
Termination Voltage	VDDQ x 0.5	V
AC Input High Level Voltage (VIH, min)	VREF + 0.31	V
AC Input Low Level Voltage (VIL, max)	VREF - 0.31	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ω
Series Resistor (RS)	25	W
Output Load Capacitance for Access Time Measurement (CL)	30	pF

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	DDR400B		DDR333		DDR266A		DDR266B		DDR200		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Row Cycle Time		tRC	55	-	60	-	65	-	65	-	70	-	ns
Auto Refresh Row Cycle Time		tRFC	70	-	72	-	75	-	75	-	80	-	ns
Row Active Time		tRAS	40	70K	42	70K	45	120K	45	120K	50	120K	ns
Active to Read with Auto Precharge Delay[16]		tRAP	tRCD or tRASmin	-	tRCD or tRASmin	-	tRCD or tRASmin	-	tRCD or tRASmin	-	tRCD or tRASmin	-	ns
Row Address to Column Address Delay		tRCD	15	-	18	-	20	-	20	-	20	-	ns
Row Active to Row Active Delay		tRRD	10	-	12	-	15	-	15	-	15	-	ns
Column Address to Column Address Delay		tCCD	1	-	1	-	1	-	1	-	1	-	tCK
Row Precharge Time		tRP	15	-	18	-	20	-	20	-	20	-	ns
Write Recovery Time		tWR	15	-	15	-	15	-	15	-	15	-	ns
Internal Write to Read Command Delay		tWTR	2	-	1	-	1	-	1	-	1	-	tCK
Auto Precharge Write Recovery + Precharge Time[15]		tDAL	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	(tWR/tCK) + (tRP/tCK)	-	tCK
System Clock Cycle Time	CL = 3	tCK	5	10	-	-	-	-	-	-	-	-	
	CL = 2.5		-	-	6	12	7.5	12	7.5	12	8.0	12	ns
	CL = 2		-	-	7.5	12	7.5	12	10	12	10	12	ns
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Data-Out edge to Clock edge Skew		tAC	-0.7	0.7	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.75	0.75	ns
DQS-Out edge to Clock edge Skew		tDQSCK	-0.55	0.55	-0.6	0.6	-0.75	0.75	-0.75	0.75	-0.75	0.75	ns
DQS-Out edge to Data-Out edge Skew		tDQSQ	-	0.4	-	0.45	-	0.5	-	0.5	-	0.6	ns
Data-Out hold time from DQS[1,10]		tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns
Clock Half Period[1,9]		tHP	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	min (tCL,tCH)	-	ns
Data Hold Skew Factor[10]		tQHS	-	0.5	-	0.55	-	0.75	-	0.75	-	0.75	ns
Valid Data Output Window		tDV	tQH-tDQSQ		tQH-tDQSQ		tQH-tDQSQ		tQH-tDQSQ		tQH-tDQSQ		ns

- Continue

Parameter	Symbol	DDR400B		DDR333		DDR266A		DDR266B		DDR200		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Data-out high-impedance window from CK,/CK[17]	tHZ	-0.7	0.7	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns
Data-out low-impedance window from CK, /CK[17]	tLZ	-0.7	0.7	-0.7	0.7	-0.75	0.75	-0.75	0.75	-0.8	0.8	ns
Input Setup Time (fast slew rate)[2,3,5,6]	tIS	0.6	-	0.75	-	0.9	-	0.9	-	1.1	-	ns
Input Hold Time (fast slew rate)[2,3,5,6]	tIH	0.6	-	0.75	-	0.9	-	0.9	-	1.1	-	ns
Input Setup Time (slow slew rate)[2,4,5,6]	tIS	0.7	-	0.8	-	1.0	-	1.0	-	1.1	-	ns
Input Hold Time (slow slew rate)[2,4,5,6]	tIH	0.7	-	0.8	-	1.0	-	1.0	-	1.1	-	ns
Input Pulse Width[6]	tIPW	2.2	-	2.2	-	2.2	-	2.2	-	2.5	-	ns
Write DQS High Level Width	tDQSH	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	tCK
Write DQS Low Level Width	tDQSL	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	tCK
Clock to First Rising edge of DQS-In	tDQSS	0.72	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK
Data-in Setup Time to DQS-In (DQ & DM)[6,7,11,12,13]	tDS	0.4	-	0.45	-	0.5	-	0.5	-	0.6	-	ns
Data-in Hold Time to DQS-In (DQ & DM)[6,7,11,12,13]	tDH	0.4	-	0.45	-	0.5	-	0.5	-	0.6	-	ns
DQ & DM Input Pulse Width	tDIPW	1.75	-	1.75	-	1.75	-	1.75	-	2	-	ns
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Write DQS Preamble Setup Time	tWPRES	0	-	0	-	0	-	0	-	0	-	tCK
Write DQS Preamble Hold Time	tWPREH	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	tCK
Write DQS Postamble Time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Mode Register Set Delay	tMRD	2	-	2	-	2	-	2	-	2	-	tCK
Exit Self Refresh to non-Read command	tXSNR	75	-	75	-	75	-	75	-	80	-	ns
Exit Self Refresh to Read command[8]	tXSRD	200	-	200	-	200	-	200	-	200	-	tCK
Average Periodic Refresh Interval	tREFI	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	us

Note:

1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock: A0~A12, BA0~BA1, CKE, /CS, /RAS, /CAS, /WE.
3. For command/address input slew rate >=1.0V/ns
4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
   This Derating Table is used to increase tIS/tIH in case where the input slew-rate is below 0.5V/ns.
   Input Setup / Hold Slew-rate Derating Table.

Input Setup / Hold Slew-rate	Delta tIS	Delta tIH
V/ns	ps	ps
0.5	0	0
0.4	+50	0
0.3	+100	0

5. CK, /CK slew rates are >=1.0V/ns
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes(LDQS/UDQS): DQ, LDM/UDM.
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM.
9. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
10. tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS consists of tDQSQ-max, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects and p-channel to n-channel variation of the output drivers.
11. This Derating Table is used to increase tDS/tDH in case where the input slew-rate is below 0.5V/ns.
    Input Setup / Hold Slew-rate Derating Table.

Input Setup / Hold Slew-rate	Delta tDS	Delta tDH
V/ns	ps	ps
0.5	0	0
0.4	+75	+75
0.3	+150	+150

12. I/O Setup/Hold Plateau Derating. This Derating Table is used to increase tDS/tDH in case where the input level is flat below VREF +/-310mV for a duration of up to 2ns.

I/O Input Level	Delta tDS	Delta tDH
mV	ps	ps
+280	+50	+50

13. I/O Setup/Hold Delta Inverse Slew Rate Derating. This Derating Table is used to increase tDS/tDH in case where the DQ and DQS slew rates differ. The Delta Inverse Slew Rate is calculated as (1/SlewRate1)-(1/SlewRate2). For example, if slew rate 1 = 0.5V/ns and Slew Rate2 = 0.4V/n then the Delta Inverse Slew Rate = -0.5ns/V.

(1/SlewRate1)-(1/SlewRate2)	Delta tDS	Delta tDH
ns/V	ps	ps
0	0	0
+/-0.25	+50	+50
+/- 0.5	+100	+100

14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

15. tDAL = (tWR/tCK) + (tRP / tCK). For each of the terms above, if not already an integer, round to the next highest integer.
tCK is equal to the actual system clock cycle time.
Example: For DDR266B at CL=2.5 and tCK = 7.5 ns,
tDAL = (15 ns / 7.5 ns) + (20 ns / 7.5 ns) = (2.00) + (2.67)
Round up each non-integer to the next highest integer: = (2) + (3), tDAL = 5 clocks

16. For the parts which do not has internal RAS lockout circuit, Active to Read with Auto precharge delay should be tRAS - BL/2 x tCK.

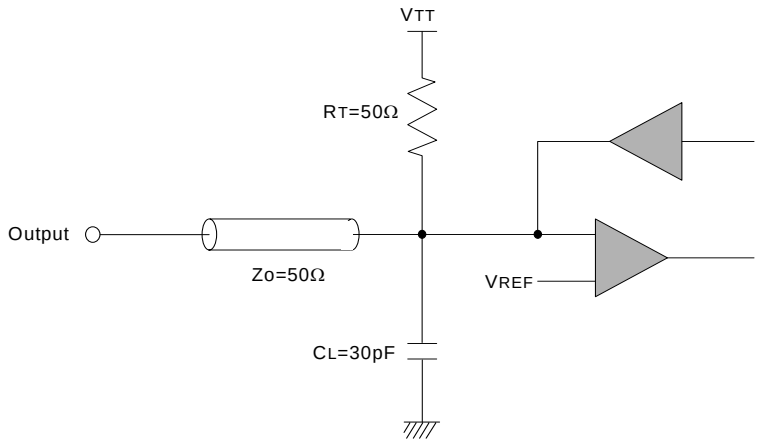
17. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).

CAPACITANCE (T_A=25°C, f=100MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Clock Capacitance	CK, /CK	C_{I1}	2.0	3.0	pF
Delta Input Clock Capacitance	CK, /CK	Delta C_{I1}	-	0.25	pF
Input Capacitance	All other input-only pins	C_{I1}	2.0	3.0	pF
Delta Input Capacitance	All other input-only pins	Delta C_{I2}	-	0.5	pF
Input / Output Capacitance	DQ, DQS, DM	C_{IO}	4.0	5.0	pF
Delta Input / Output Capacitance	DQ, DQS, DM	Delta C_{IO}	-	0.5	pF

Note:
1. VDD = min. to max., VDDQ = 2.3V to 2.7V, V_{ODC} = VDDQ/2, $V_{Opeak-to-peak}$ = 0.2V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

OUTPUT LOAD CIRCUIT



PACKAGE INFORMATION

400mil 66pin Thin Small Outline Package