Document Title
4Bank x 1M x 16bits Synchronous DRAM

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft	Sep. 2003	Preliminary
0.2	Append Super-Low Power Group to the Data-sheet	Oct. 2003	Preliminary
0.3	Changed DC Characteristics	Nov. 2003	
	Changed Package Information	July 2004	

DESCRIPTION

The Hynix Low Power SDRAM is suited for non-PC application which use the batteries such as PDAs, 2.5G and 3G cellular phones with internet access and multimedia capabilities, mini-notebook, handheld PCs.
The Hynix HY5S6B6D(L/S)F(P) is a 67,108,864bit CMOS Synchronous Dynamic Random Access Memory. It is organized as 4banks of 1,048,576x16.
The Low Power SDRAM provides for programmable options including CAS latency of 1, 2, or 3, READ or WRITE burst length of 1, 2, 4, 8, or full page, and the burst count sequence(sequential or interleave). And the Low Power SDRAM also provides for special programmable options including Partial Array Self Refresh of a quarter bank, a half bank, 1bank, 2banks, or all banks.
The Hynix HY5S6B6D(L/S)F(P) has the special Low Power function of Auto TCSR(Temperature Compensated Self Refresh) to reduce self refresh current consumption. Since an internal temperature sensor is implanted, it enables to automatically adjust refresh rate according to temperature without external EMRS command. A burst of Read or Write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst Read or Write command on any cycle(This pipelined design is not restricted by a 2N rule).
Deep Power Down Mode is a additional operating mode for Low Power SDRAM. This mode can achieve maximum power reduction by removing power to the memory array within each SDRAM. By using this feature, the system can cut off alomost all DRAM power without adding the cost of a power switch and giving up mother-board power-line layout flexibility.

FEATURES

Standard SDRAM Protocol

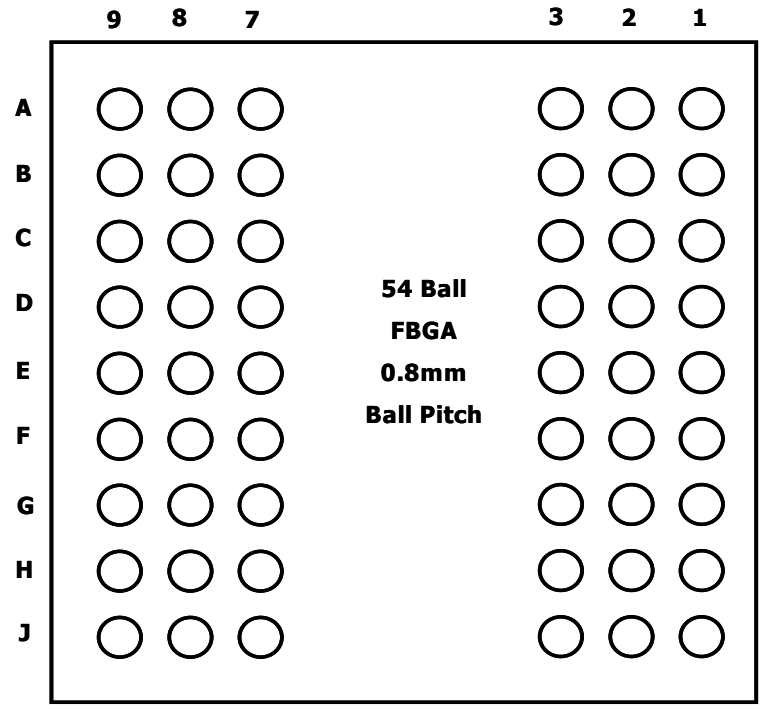
Internal 4bank operation

- Power Supply Voltage : VDD = 1.8V, VDDQ = 1.8V
- LVCMOS compatible I/O Interface
- Low Voltage interface to reduce I/O power
- Low Power Features
  - PASR(Partial Array Self Refresh)
  - AUTO TCSR (Temperature Compensated Self Refresh)
  - DS (Drive Strength)
  - Deep Power Down Mode
- Programmable CAS latency of 1, 2 or 3
- Package Type : 54ball, 0.8mm pitch FBGA (Lead Free, Lead)
  HY5S6B6D(L/S)FP : Lead Free
  HY5S6B6D(L/S)F : Lead

ORDERING INFORMATION

Part Number	Clock Frequency	CAS Latency	Organization	Interface
HY5S6B6D(L/S)F(P)-SE	105MHz	3	4banks x 1Mb x 16	LVCMOS
HY5S6B6D(L/S)F(P)-BE	66MHz	2		

BALL ASSIGNMENTS



<Bottom View>

1	2	3		7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
DQ14	DQ13	VDDQ	B	VSSQ	DQ2	DQ1
DQ12	DQ11	VSSQ	C	VDDQ	DQ4	DQ3
DQ10	DQ9	VDDQ	D	VSSQ	DQ6	DQ5
DQ8	NC	VSS	E	VDD	LDQM	DQ7
UDQM	CLK	CKE	F	/CAS	/RAS	/WE
NC	A11	A9	G	BA0	BA1	/CS
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

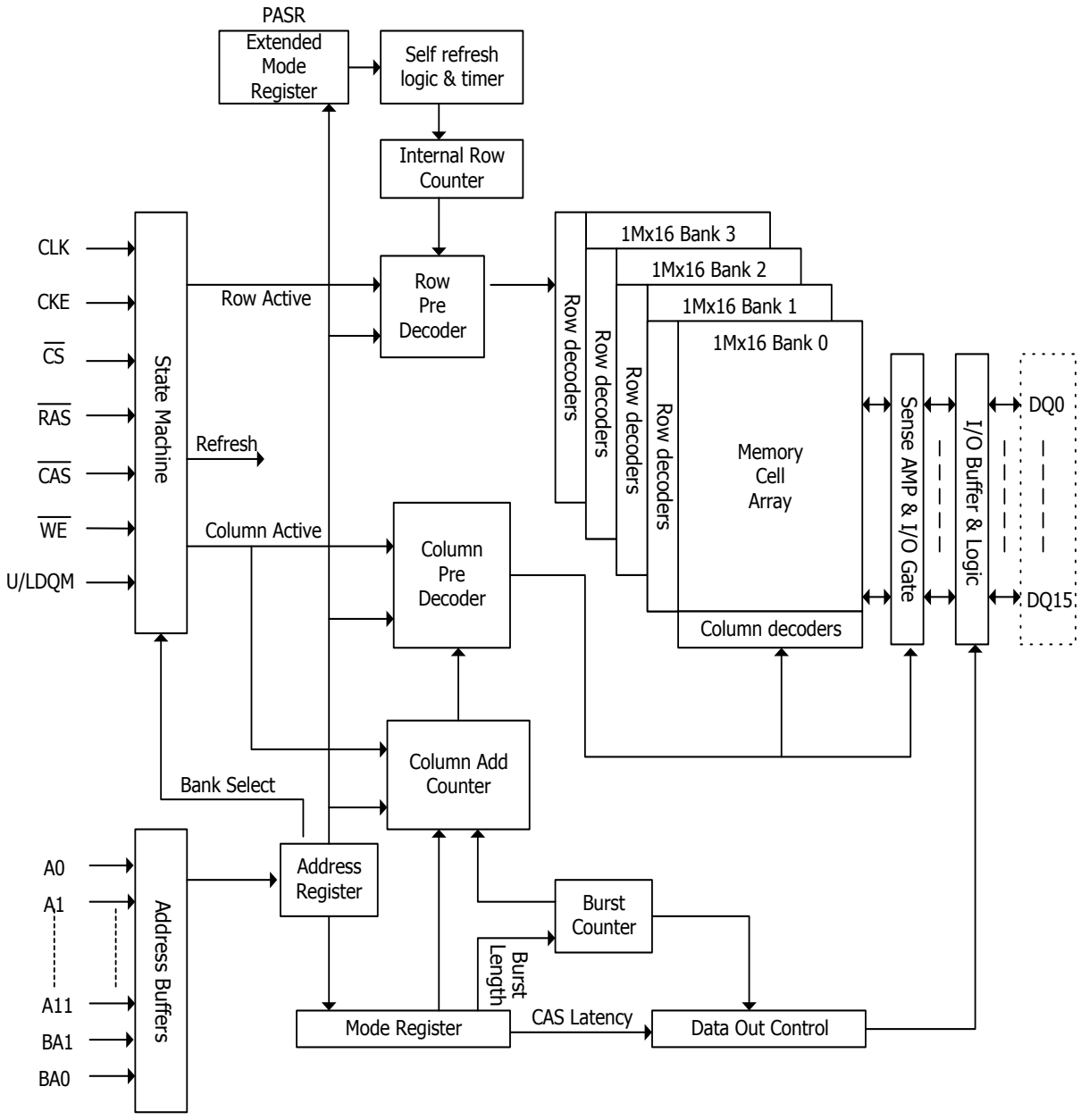
< Top View >

BALL DESCRIPTION

Ball Out	SYMBOL	TYPE	DESCRIPTION
F2	CLK	INPUT	Clock : The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
F3	CKE	INPUT	Clock Enable : Controls internal clock signal and when deactivated, the SDRAM will be one of the states among (deep) power down, suspend or self refresh
G9	$\overline{CS}$	INPUT	Chip Select : Enables or disables all inputs except CLK, CKE, UDQM and LDQM
G7,G8	BA0, BA1	INPUT	Bank Address : Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2	A0 ~ A11	INPUT	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
F8, F7, F9	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	INPUT	Command Inputs : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
F1, E8	UDQM, LDQM	INPUT	Data Mask : Controls output buffers in read mode and masks input data in write mode
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	DQ0 ~ DQ15	I/O	Data Input/Output : Multiplexed data input/output pin
A9, E7, J9, A1, E3, J1	VDD/VSS	SUPPLY	Power supply for internal circuits
A7, B3, C7, D3, A3, B7, C3, D7	VDDQ/VSSQ	SUPPLY	Power supply for output buffers
E2, G1	NC	-	No connection

FUNCTIONAL BLOCK DIAGRAM

1Mbit x 4banks x 16 I/O Low Power Synchronous DRAM



BASIC FUNCTIONAL DESCRIPTION

Mode Register

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	OP Code	0	0	CAS Latency			BT	Burst Length		

OP Code

A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

BASIC FUNCTIONAL DESCRIPTION (Continued)

Extended Mode Register

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	DS		0	0	PASR		

DS (Driver Strength)

A6	A5	Driver Strength
0	0	Full
0	1	1/2 Strength
1	0	1/4 Strength
1	1	Reserved

PASR (Partial Array Self Refresh)

A2	A1	A0	Self Refresh Coverage
0	0	0	All Banks
0	0	1	Half of Total Bank (BA1=0 or Bank 0,1)
0	1	0	Quarter of Total Bank (BA1=BA0=0 or Bank 0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Half of Bank 0(Bank 0 and Row Address MSB=0)
1	1	0	Quarter of Bank 0(Bank 0 and Row Address 2 MSBs=0)
1	1	1	Reserved

Power Up and Initialization

Like a Synchronous DRAM, Low Power(LP) SDRAM must be powered up and initialized in a predefined manner. Power must be applied to V_{DD} and V_{DDQ}(simultaneously). The clock signal must be started at the same time. After power up, an initial pause of 200 usec is required. And a precharge all command will be issued to the LP SDRAM. Then, 8 or more Auto refresh cycles will be provided. After the Auto refresh cycles are completed, a mode register set(MRS) command will be issued to program the specific mode of operation (Cas Latency, Burst length, etc.) And a extended mode register set command will be issued to program specific mode of self refresh operation(PASR). The following these cycles, the LP SDRAM is ready for normal opeartion.

Programming the registers

Mode Register

The mode register contains the specific mode of operation of the LP SDRAM. This register includes the selection of a burst length(1, 2, 4, 8, Full Page), a cas latency(1, 2 or 3), a burst type. The mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of mode register set command.

Extended Mode Register

The extended mode register contains the specific features of self refresh opeartion of the LP SDRAM. This register includes the selection of partial arrays to be refreshed(half array, quarter array, etc.). The extended mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of extended mode register set command.

Bank(Row) Active

The Bank Active command is used to activate a row in a specified bank of the device. This command is initiated by activating $\overline{CS}$, $\overline{RAS}$ and deasserting $\overline{CAS}$, $\overline{WE}$ at the positive edge of the clock. The value on the BA1 and BA0 selects the bank, and the value on the A0-A11 selects the row. This row remains active for column access until a precharge command is issued to that bank. Read and write opeartions can only be initiated on this activated bank after the minimum t_{RCD} time is passed from the activate command.

Read

The READ command is used to initiate the burst read of data. This command is initiated by activating $\overline{CS}$, $\overline{CAS}$, and deasserting $\overline{WE}$, $\overline{RAS}$ at the positive edge of the clock. BA1 and BA0 inputs select the bank, A7-A0 address inputs select the sarting column location. The value on input A10 determines whether or not Auto Precharge is used. If Auto Precharge is selected the row being accessed will be precharged at the end of the READ burst; if Auto Precharge is not selected, the row will remain active for subsequent accesses.
The length of burst and the CAS latency will be determined by the values programmed during the MRS command.

Write

The WRITE command is used to initiate the burst write of data. This command is initiated by activating $\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ and deasserting $\overline{RAS}$ at the positive edge of the clock. BA1 and BA0 inputs select the bank, A7-A0 address inputs select the starting column location. The value on input A10 determines whether or not Auto Precharge is used.
If Auto Precharge is selected the row being accessed will be precharged at the end of the WRITE burst; if Auto Precharge is not selected, the row will remain active for subsequent accesses.

Precharge
The Precharge command is used to close the open row in a particular bank or the open row in all banks. When the precharge command is issued with address A10, high, then all banks will be precharged, and If A10 is low, the open row in a particular bank will be precharged. The bank(s) will be available when the minimum t_{RP} time is met after the precharge command is issued.

Auto Precharge
The Auto Precharge command is issued to close the open row in a particular bank after READ or WRITE operation. If A10 is high when a READ or WRITE command is issued, the READ or WRITE with Auto Precharge is initiated.

Burst Termination
The Burst Termination is used to terminate the burst operation. This function can be accomplished by asserting a Burst Stop command or a Precharge command during a burst READ or WRITE operation. The Precharge command interrupts a burst cycle and close the active bank, and the Burst Stop command terminates the existing burst operation leave the bank open.

Data Mask
The Data Mask comamnd is used to mask READ or WRITE data. During a READ operation, When this command is issued, data ouputs are disabled and become high impedance after two clock delay. During a WRITE operation, When this command is issued, data inputs can't be written with no clock delay.

Clock Suspend
The Clock Suspend command is used to suspend the internal clock of LP SDRAM. During normal access mode, CKE is keeping High. When CKE is low, it freezes the internal clock and extends data Read and Write operations.

Power Down
The Power Down command is used to reduce standby current. Before this command is issued, all banks must be pre-charged and tRP must be passed after a precharge command. Once the Power Down command is initiated by keeping CKE low, all of the input buffer except CKE are gated off.

Auto Refresh
The Auto Refresh command is used during normal operation and is similar to C_{BR} refresh in Coventional DRAMs.
This command must be issued each time a refresh is required. When an Auto Refresh command is issued , the address bits is "Don't care", because the specific address bits is generated by internal refresh address counter.

Self Refresh
The Self Refresh command is used to retain cell data in the LP SDRAM. In the Self Refresh mode, the LP SDRAM operates refresh cycle asynchronously.
The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled(Low). The LP SDRAM can accomplish an special Self Refresh operation by the specific modes(PASR) programmed in extended mode registers. The LP SDRAM can control the refresh rate automatically by the temperature value of Auto TCSR(Temperature Compensated Self Refresh) to reduce self refresh current and select the memory array to be refreshed by the value of PASR(Partial Array Self Refresh). The LP SDRAM can reduce the self refresh current(I_{DD6}) by using these two modes.

Deep Power Down
The Deep Power Down Mode is used to achieve maximum power reduction by cutting the power of the whole memory array of the devices.
For more information, see the special operation for Low Power consumption of this data sheet.

COMMAND TRUTH TABLE

Function	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	A10/AP	BA 0,1	Note
Mode Register Set	H	X	L	L	L	L	OP CODE			2
Extended Mode Register Set	H	X	L	L	L	L	OP CODE			2
No Operation	H	X	L	H	H	H	X			
Device Deselect	H	X	H	X	X	X	X			
Bank Active	H	X	L	L	H	H	Row Address		V	
Read	H	X	L	H	L	H	Column	L	V	
Read with Autoprecharge	H	X	L	H	L	H	Column	H	V	
Write	H	X	L	H	L	L	Column	L	V	
Write with Autoprecharge	H	X	L	H	L	L	Column	H	V	
Precharge All Banks	H	X	L	L	H	L	X	H	X	
Precharge selected Bank	H	X	L	L	H	L	X	L	V	
Burst stop	H	X	L	H	H	L	X			
Auto Refresh	H	H	L	L	L	H	X			
Self Refresh Entry	H	L	L	L	L	H	X			
Self Refresh Exit	L	H	H	X	X	X	X			1
			L	H	H	H				
Precharge Power Down Entry	H	L	H	X	X	X	X			
			L	H	H	H				
Precharge Power Down Exit	L	H	H	X	X	X	X			
			L	H	H	H				
Clock Suspend Entry	H	L	H	X	X	X	X			
			L	V	V	V				
Clock Suspend Exit	L	H	X				X			
Deep Power Down Entry	H	L	L	H	H	L	X			
Deep Power Down Exit	L	H	X				X			

Note : 1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high.
2. BA1/BA0 must be issued 0/0 in the mode register set, and 1/0 in the extended mode register set.

DQM TRUTH TABLE

Function	CKEn-1	CKEn	LDQM	UDQM
Data Write/Output enable	H	X	L	L
Data Mask/Output disable	H	X	H	H
Lower byte write/Output enable, Upper byte mask/Output disable	H	X	L	H
Lower byte Mask/Output disable, Upper byte write/Output enable	H	X	H	L

Note : 1. H: High Level, L: Low Level, X: Don't Care
2. Write DQM Latency is 0 CLK and Read DQM Latency is 2 CLK

CURRENT STATE TRUTH TABLE (Sheet 1 of 4)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0/ BA1	A11-A0	Description		
idle	L	L	L	L	OP CODE		Mode Register Set	Set the Mode Register	14
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto or Self Refresh	5
	L	L	H	L	BA	X	Precharge	No Operation	
	L	L	H	H	BA	Row Add.	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4
	L	H	H	H	X	X	No Operation	No Operation	3
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	3
Row Active	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Precharge	7
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Start Write : optional AP(A10=H)	6
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Start Read : optional AP(A10=H)	6
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Read	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Termination Burst: Start the Precharge	
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Termination Burst: Start Write(optional AP)	8,9
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Termination Burst: Start Read(optional AP)	8
	L	H	H	H	X	X	No Operation	Continue the Burst	

CURRENT STATE TRUTH TABLE (Sheet 2 of 4)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0/ BA1	A11-A0	Description		
Read	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Termination Burst: Start the Precharge	10
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Termination Burst: Start Write(optional AP)	8
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Termination Burst: Start Read(optional AP)	8,9
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Read with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	12
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	12
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

CURRENT STATE TRUTH TABLE (Sheet 3 of 4)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0/ BA1	A11-A0	Description		
Precharging	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	No Operation: Bank(s) idle after tRP	
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,12
	L	H	H	H	X	X	No Operation	No Operation: Bank(s) idle after tRP	
	H	X	X	X	X	X	Device Deselect	No Operation: Bank(s) idle after tRP	
Row Activating	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,11,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,12
	L	H	H	H	X	X	No Operation	No Operation: Row Active after tRCD	
	H	X	X	X	X	X	Device Deselect	No Operation: Row Active after tRCD	
Write Recovering	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Start Write: Optional AP(A10=H)	
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Start Read: Optional AP(A10=H)	9
	L	H	H	H	X	X	No Operation	No Operation: Row Active after tDPL	

CURRENT STATE TRUTH TABLE (Sheet 4 of 4)

Current State	Command							Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0/ BA1	A11-A0	Description		
Write Recovering	H	X	X	X	X	X	Device Deselect	No Operation: Row Active after tDPL	
Write Recovering with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,9,12
	L	H	H	H	X	X	No Operation	No Operation: Precharge after tDPL	
	H	X	X	X	X	X	Device Deselect	No Operation: Precharge after tDPL	
Refreshing	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	13
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	13
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	13
	L	H	H	H	X	X	No Operation	No Operation: idle after tRC	
	H	X	X	X	X	X	Device Deselect	No Operation: idle after tRC	
Mode Register Accessing	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13,14
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	13
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	13
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	13
	L	H	H	H	X	X	No Operation	No Operation: idle after 2 clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation: idle after 2 clock cycles	

Note :

1. H: Logic High, L: Logic Low, X: Don't care, BA: Bank Address, AP: Auto Precharge.
2. All entries assume that CKE was active during the preceding clock cycle.
3. If both banks are idle and CKE is inactive, then in power down cycle
4. Illegal to bank in specified states. Function may be legal in the bank indicated by Bank Address, depending on the state of that bank.
5. If both banks are idle and CKE is inactive, then Self Refresh mode.
6. Illegal if t_{RCD} is not satisfied.
7. Illegal if t_{RAS} is not satisfied.
8. Must satisfy burst interrupt condition.
9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
10. Must mask preceding data which don't satisfy t_{DPL}.
11. Illegal if t_{RRD} is not satisfied
12. Illegal for single bank, but legal for other banks in multi-bank devices.
13. Illegal for all banks.
14. Mode Register Set and Extended Mode Register Set is same command truth table except BA1.

CKE Enable(CKE) Truth TABLE (Sheet 1 of 2)

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0, BA1	A11-A0		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	2
	L	H	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	L	X	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down mode exit, all banks idle	2
			L	H	H	H	X	X		
	L	H	L	L	X	X	X	X	ILLEGAL	2
				X	L	X	X	X		
				X	X	L	X	X		
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
Deep Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	X	X	X	X	X	X	Deep Power Down mode exit	5
	L	L	X	X	X	X	X	X	Maintain Deep Power Down Mode	

CKE Enable(CKE) Truth TABLE (Sheet 2 of 2)

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0, BA1	A11-A0		
All Banks Idle	H	H	H	X	X	X			Refer to the idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				3
	H	H	L	L	H	X				3
	H	H	L	L	L	H	X	X	Auto Refresh	
	H	H	L	L	L	L	OP CODE		Mode Register Set	4
	H	L	H	X	X	X			Refer to the idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				3
	H	L	L	L	H	X				3
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	L	L	L	L	L	OP CODE		Mode Register Set	
	L	X	X	X	X	X	X	X	Power Down	4
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to operations of the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

Note :

1. For the given current state CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. When exiting power down mode, a NOP (or Device Deselect) command is required on the first positive edge of clock after CKE goes high.
3. The address inputs depend on the command that is issued.
4. The Precharge Power Down mode, the Self Refresh mode, and the Mode Register Set can only be entered from the all banks idle state.
5. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. When exiting deep power down mode, a NOP (or Device Deselect) command is required on the first positive edge of clock after CKE goes high and is maintained for a minimum 200usec.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	-25 ~ 85	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 2.6	V
Voltage on VDD relative to VSS	VDD	-1.0 ~ 2.6	V
Voltage on VDDQ relative to VSS	VDDQ	-1.0 ~ 2.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

DC OPERATING CONDITION (TA= -25 to 85 °C)

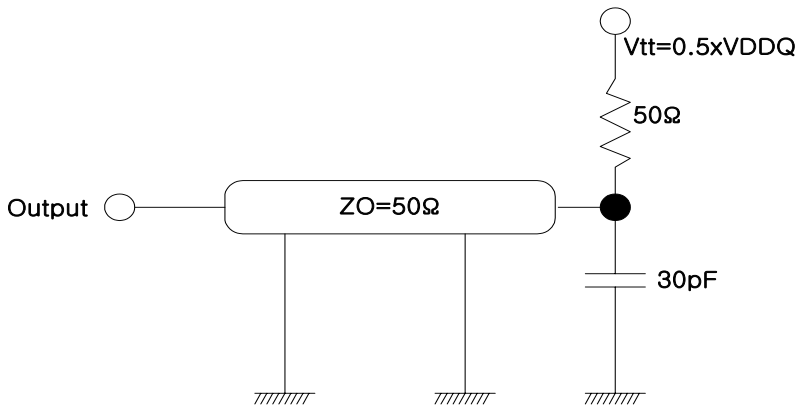
Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD	1.65	1.8	1.95	V	1
Power Supply Voltage	VDDQ	1.65	1.8	1.95	V	1, 2
Input High Voltage	VIH	0.8*VDDQ	-	VDDQ+0.3	V	1, 2
Input Low Voltage	VIL	-0.3	-	0.3	V	1, 2

Note :
1. All Voltages are referenced to VSS = 0V
2. VDDQ must not exceed the level of VDD

AC OPERATING TEST CONDITION (TA= -25 to 85 °C, VDD = 1.8V, VSS = 0V)

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	VIH / VIL	0.9*VDDQ/0.2	V	
Input Timing Measurement Reference Level Voltage	Vtrip	0.5*VDDQ	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	0.5*VDDQ	V	
Output Load Capacitance for Access Time Measurement	CL		pF	1

Note 1.



CAPACITANCE (TA= 25 °C, f=1MHz)

Parameter	Pin	Symbol	-H		-/P/S/B		Unit
			Min	Max	Min	Max	
Input capacitance	CLK	CI1	2	4.0	2	4.0	pF
	A0~A11, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, UDQM, LDQM	CI2	2	4.0	2	4.0	pF
Data input/output capacitance	DQ0 ~ DQ15	CI/O	3.5	6.0	3.5	6.0	pF

DC CHARACTERRISTICS I (TA= 25 to 85°C)

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	ILI	-1	1	uA	1
Output Leakage Current	ILO	-1.5	1.5	uA	2
Output High Voltage	VOH	VDDQ-0.2	-	V	3
Output Low Voltage	VOL	-	0.2	V	4

Note :

1. VIN = 0 to 1.8V. All other pins are not tested under VIN=0V.

2. DOUT is disabled. VOUT= 0 to 1.95V.

3. IOUT = - 0.1mA

4. IOUT = + 0.1mA

DC CHARACTERISTICS II (TA= 25 to 85°C)

Parameter	Symbol	Test Condition	Speed		Unit	Note
			-S	-B		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA	50	35	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns	0.5		mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞	0.3		mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	5.5		mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	2			
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns	1.5		mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞	1			
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	12		mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	6			
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	60	40	mA	1
Auto Refresh Current	IDD5	tRC ≥ tARFC(min), All banks active	80	60	mA	
Self Refresh Current	IDD6	CKE ≤ 0.2V	See Next Page		mA	2
Standby Current in Deep Power Down Mode	IDD7	See p.25~26	50		uA	

Note :

1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
2. See the tables of next page for more specific IDD6 current values.

- Low Power : HY5S6B6DLF Series
- Super Low Power : HY5S6B6DSF Series

DC CHARACTERISTICS III - Low Power (IDD6)

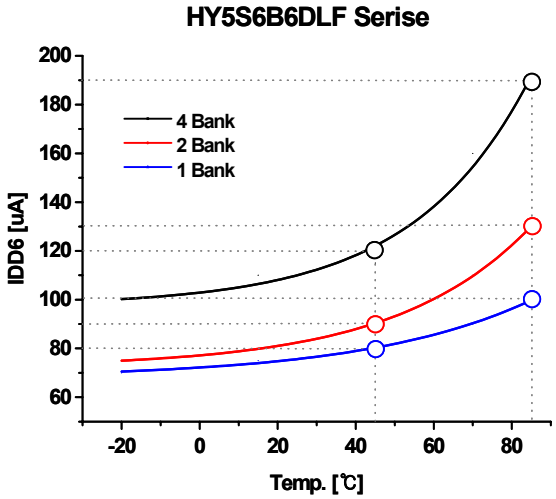
Temp. (°C)	Memory Array			Unit
	4 Banks	2 Banks	1 Bank	
85	190	130	100	μA
45	120	90	80	μA

* HY5S6B6DLF Series [1)]

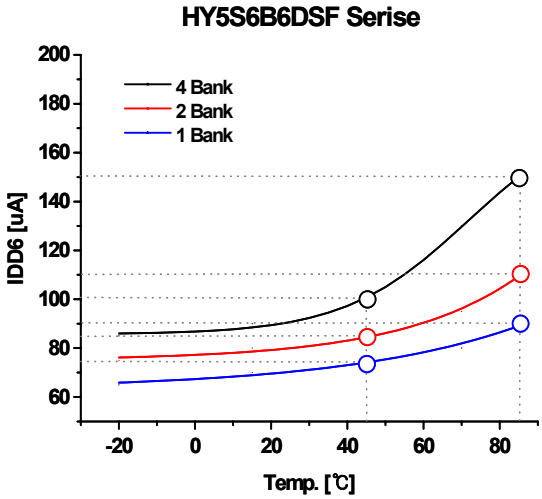
DC CHARACTERISTICS III - Super Low Power (IDD6)

Temp. (°C)	Memory Array			Unit
	4 Banks	2 Banks	1 Bank	
85	150	110	90	μA
45	100	85	75	μA

* HY5S6B6DSF Series [2)]



Note 1) IDD6 vs Temp. Graph for HY5S6B6DLF



Note 2) IDD6 vs Temp. Graph for HY5S6B6DSF

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	S		B		Unit	Note
			Min	Max	Min	Max		
System Clock Cycle Time	$\overline{CAS}$ Latency=3	tCK3	9.5	1000	15	1000	ns	
	$\overline{CAS}$ Latency=2	tCK2	15		15		ns	
Clock High Pulse Width		tCHW	3.5	-	3.5	-	ns	1
Clock Low Pulse Width		tCLW	3.5	-	3.5	-	ns	1
Access Time From Clock	$\overline{CAS}$ Latency=3	tAC3	-	7	-	9	ns	2
	$\overline{CAS}$ Latency=2	tAC2	-	8	-	9	ns	
Data-out Hold Time		tOH	2.5	-	2.5	-	ns	
Data-Input Setup Time		tDS	3	-	4	-	ns	1
Data-Input Hold Time		tDH	1.5	-	2	-	ns	1
Address Setup Time		tAS	3	-	4	-	ns	1
Address Hold Time		tAH	1.5	-	2	-	ns	1
CKE Setup Time		tCKS	3	-	4	-	ns	1
CKE Hold Time		tCKH	1.5	-	2.0	-	ns	1
Command Setup Time		tCS	3	-	4	-	ns	1
Command Hold Time		tCH	1.5	-	2	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1	-	1	-	ns	
CLK to Data Output in High-Z Time	$\overline{CAS}$ Latency=3	tOHZ3		7		9	ns	
	$\overline{CAS}$ Latency=2	tOHZ2		8		9	ns	

Note :

1. Assume t_R / t_F (input rise and fall time) is 1ns. If t_R & t_F > 1ns, then [(t_R+t_F)/2-1]ns should be added to the parameter.
2. Access time to be measured with input signals of 1V/ns edge rate, from 0.8V to 0.2V. If t_R > 1ns, then (t_R/2-0.5)ns should be added to the parameter.

AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

Parameter		Symbol	S		B		Unit	Note
			Min	Max	Min	Max		
$\overline{RAS}$ Cycle Time		tRC	90	-	90	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay		tRCD	28.5	-	30	-	ns	
$\overline{RAS}$ Active Time		tRAS	60	100K	60	100K	ns	
$\overline{RAS}$ Precharge Time		tRP	28.5	-	30	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay		tRRD	19	-	30	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ Delay		tCCD	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	CLK	
Data-in to Precharge Command		tDPL	2	-	2	-	CLK	
Data-In to Active Command		tDAL	tDPL+tRP					
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	CLK	
Precharge to Data Output High-Z	$\overline{CAS}$ Latency=3	tPROZ3	3	-	3	-	CLK	
	$\overline{CAS}$ Latency=2	tPROZ2	2		2		CLK	
Power Down Exit Time		tDPE	1	-	1	-	CLK	
Auto Refresh Cycle Time		tARFC	90		105		ns	
Self Refresh Exit Time		tSRE	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	ms	

Note : 1. A new command can be given tRC after self refresh exit.

Special Operation for Low Power Consumption

Deep Power Down Mode

Deep Power Down Mode is an operating mode to achieve maximum power reduction by cutting the power of the whole memory array of the devices.

Data will not be retained once the device enters Deep Power Down Mode.

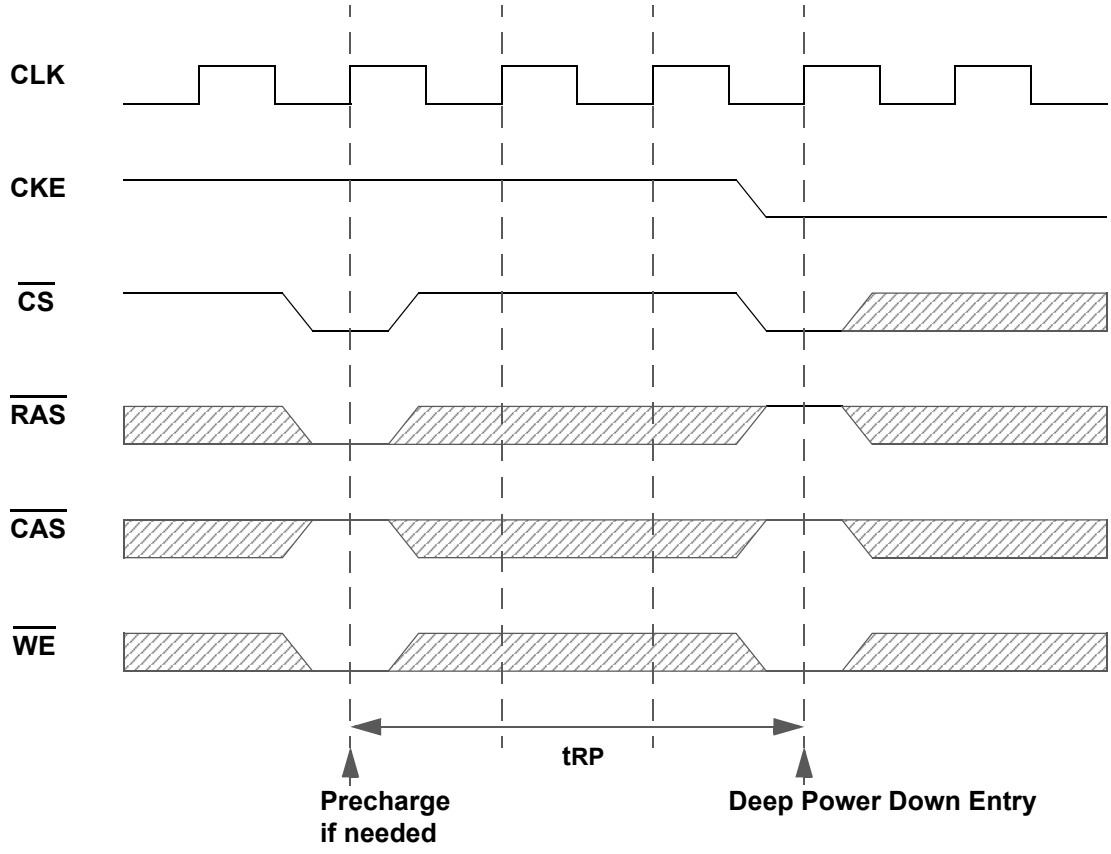
Full initialization is required when the device exits from Deep Power Down Mode.

Truth Table

Current State	Command	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Idle	Deep Power Down Entry	H	L	L	H	H	L
Deep Power Down	Deep Power Down Exit	L	H	X	X	X	X

Deep Power Down Mode Entry

The Deep Power Down Mode is entered by having $\overline{CS}$ and $\overline{WE}$ held low with $\overline{RAS}$ and $\overline{CAS}$ high at the rising edge of the clock, while CKE is low. The following diagram illustrates deep power down mode entry.



Deep Power Down Mode (Continued)

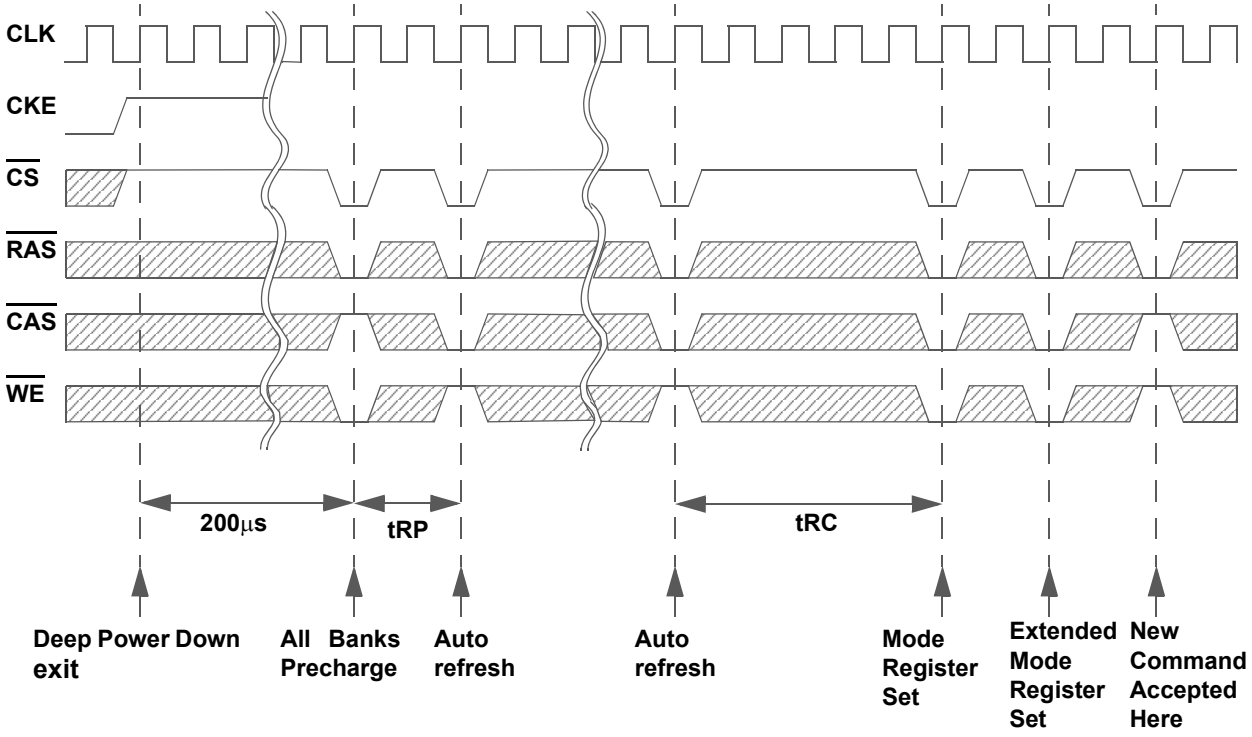
Deep Power Down Mode Exit Sequence

The Deep Power Down mode is exited by asserting CKE high.

After the exit, the following sequence is needed to enter a new command.

1. Maintain NOP input conditions for a minimum of 200usec
2. Issue precharge commands for all banks of the device
3. Issue 8 or more auto refresh commands
4. Issue a mode register set command to initialize the mode register
5. Issue an extended mode register set command to initialize the extended mode register

The following timing diagram illustrates deep power down mode exit sequence.



PACKAGE INFORMATION

54 Ball 0.8mm pitch 8mm FBGA

Unit [mm]