

HY638256 Series

32Kx8bit CMOS FAST SRAM



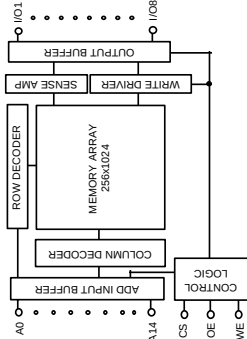
DESCRIPTION

The HY638256 is a high-speed 32,768 x 8-bits CMOS static RAM fabricated using Hyundai's high performance twin tub CMOS process technology. This high reliability process coupled with high-speed circuit design techniques, yields maximum access time of 15ns. The HY638256 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. It is suitable for use in high-density high-speed system applications.

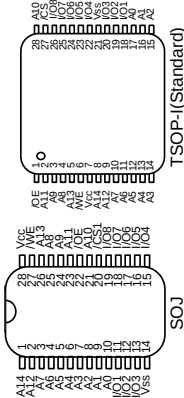
FEATURES

- Single 5V±10% Power Supply
- High speed - 15/20/25ns(max.)
- Low power consumption(Max.)
- Mode Conditions Current Units
- Operating 15ns 100 mA
- 20/25ns 90 mA
- TTL 30 mA
- Standby CMOS L 2 mA
- 100 uA
- Battery backup(L-part)
- 2.0V(min) data retention
- Fully static operation and Tri-state outputs
- No clock or refresh required
- TTL compatible inputs and outputs
- Standard pin configuration
- 28pin 300mil SOJ
- 28pin 8 x 13.4 mm TSOP-I

BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
/CS	Chip Select
/WE	Write Enable
/OE	Output Enable
A0-A14	Address Input
I/O1-I/O8	Data Input/Output
VCC	Power(+5.0V)
VSS	Ground

ORDERING INFORMATION

Part No.	Speed	Power	Package
HY638256J	15/20/25		SOJ
HY638256LJ	15/20/25	L-part	SOJ
HY638256T1	15/20/25		TSOP-I Standard
HY638256L.T1	15/20/25	L-part	TSOP-I Standard

This document is a general product description and is subject to change without notice. Hyundai Electronics does not assume any responsibility for use of circuits described. No patent licenses are implied.

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V±10%, TA = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Type	Max	Unit
I _{II}	Input Leakage Current	VSS ≤ VIN ≤ VCC	-2	-	2	uA
I _{LO}	Output Leakage Current	VSS ≤ VOUT ≤ VCC, /CS = VIH or OE = VIH or /WE = VIL	-2	-	2	uA
I _{CC1}	Average Operating Current	/CS = VIL, I _{IO} = 0mA, Min. Duty Cycle = 100%	-	-	100	mA
I _{SB}	TTL Standby Current (TTL Inputs)	Min. Duty Cycle = 100%, /CS = VIH, VIN = VIH or VIL, Min. Cycle	-	-	90	mA
I _{SB1}	CMOS Standby Current (CMOS Inputs)	/CS ≥ VCC-0.2V, VIN ≥ L	-	-	2	mA
I _{OL}	Output Low Voltage	VCC-0.2V or VIN ≤ 0.2V I _{OL} = 8.0mA	-	-	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4.0mA	2.4	-	-	V

Note : Typical values are at VCC = 5.0V, TA = 25°C

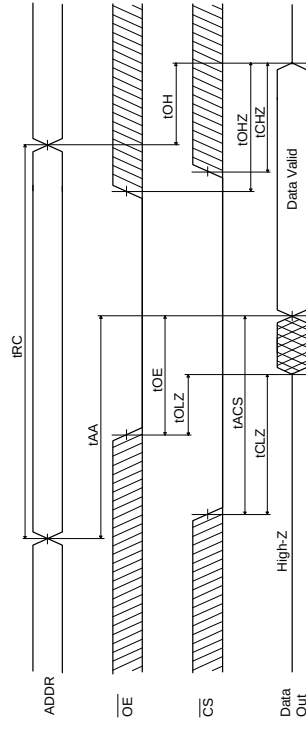
AC CHARACTERISTICS

VCC = 5.0V±10%, TA = 0°C to 70°C, unless otherwise specified.

#	Symbol	Parameter	-15		-20		-25		Unit
			Min	Max	Min	Max	Min	Max	
READ CYCLE									
1	t _{RC}	Read Cycle Time	15	-	20	-	25	-	ns
2	t _{AA}	Address Access Time	-	15	-	20	-	25	ns
3	t _{ACS}	Chip Select Access Time	-	15	-	20	-	25	ns
4	t _{OE}	Output Enable to Output Valid	-	8	-	10	-	12	ns
5	t _{CLZ}	Chip Select to Output in Low Z	3	-	3	-	3	-	ns
6	t _{OLZ}	Output Enable to Output in Low Z	3	-	3	-	3	-	ns
7	t _{CHZ}	Chip Deselecting to Output in High Z	0	8	0	10	0	10	ns
8	t _{OHZ}	Out Disable to Output in High Z	0	8	0	8	0	8	ns
9	t _{OH}	Output Hold from Address Change	3	-	3	-	3	-	ns
WRITE CYCLE									
10	t _{WC}	Write Cycle Time	15	-	20	-	25	-	ns
11	t _{CW}	Chip Select to End of Write	12	-	13	-	15	-	ns
12	t _{AW}	Address Valid to End of Write	12	-	13	-	15	-	ns
13	t _{AS}	Address Set-up Time	0	-	0	-	0	-	ns
14	t _{WP}	Write Pulse Width	12	-	13	-	15	-	ns
15	t _{WR}	Write Recovery Time	0	-	0	-	-	-	ns
16	t _{WHZ}	Write to Output in High Z	0	7	0	9	0	10	ns
17	t _{DW}	Data to Write Time Overlap	8	-	9	-	10	-	ns
18	t _{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
19	t _{OW}	Output Active from End of Write	3	-	3	-	3	-	ns

TIMING DIAGRAM

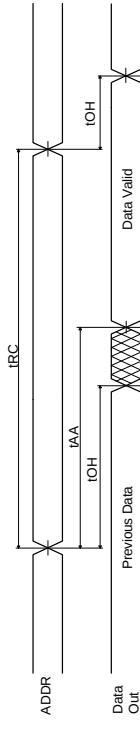
READ CYCLE 1



Note (Read Cycle)

1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tCHZ max. is less than tCLZ min. both for a given device and from device to device.
3. /WE is high for read cycle.

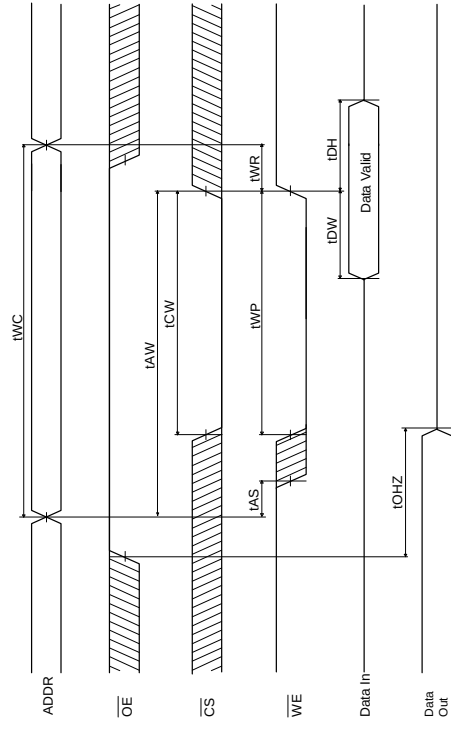
READ CYCLE 2



Note (Read Cycle)

1. /WE is high for read cycle.
2. Device is continuously selected /CS=VIL.
3. /OE=VIL.

WRITE CYCLE 1(/OE Low Clocked)



WRITE CYCLE 2(/OE Low Fixed)

