Document Title

1M x 16 bit Low Low Power 1T/1C Pseudo SRAM

Revision history

Revision No.	History	Draft Date	Remark
1.0	Initial	Jan. 04.'01	Preliminary
1.1	Revised - Change Pin Connection - Improve tOE from 45ns to 30ns - Correct State Diagram	Jul. 03.'01	Preliminary
1.2	Revised - Correct Package Dimension - Change Absolute Maximum Ratings	Jul.18.'01	Preliminary
1.3	Revised - DC Electrical Characteristics (I_{DPD},I_{CC1}) - State Diagram - Power Up Sequence - Deep Power Down Sequence - Read/Write Cycle Note	Oct. 07.'01	Preliminary
1.4	Revised - DC Electrical Characteristics (ICC1: 3mA - > 5mA)	Nov. 14.'01	Preliminary
1.5	Revised - Improve Standby Current I_{SB1} from 100uA to 80uA - Power Up Sequence	Dec. 20.'01	Preliminary
1.6	Revised - Improve ISB1 80uA to 75uA - Improve ICC2 30mA to 20mA - Improve Ambient Temperature C/E to E/I (0°C~85°C/-25°C~85°C → -25°C~85°C/-40°C~85°C) - Improve Maximum Absolute Ratings (Vdd : -0.3V to 3.3V → -0.3V to 3.6V) - Improve tOE 30ns to 20ns	Feb. 27.'02	Preliminary
1.7	Revised - Pin Description - Power Up & Deep Power Down Exit Sequence	Mar. 11.'02	Final

1M x 16 bit Low Low Power 1T/1C SRAM

DESCRIPTION

The HY64LD16162M is a 16Mbit 1T/1C SRAM featured by high-speed operation and super low power consumption. The HY64LD16162M adopts one transistor memory cell and is organized as 1,048,576 words by 16bits. The HY64LD16162M operates in the extended range of temperature and supports a wide operating voltage range. The HY64LD16162M also supports the deep power down mode for a super low standby current. The HY64LD16162M delivers the high-density low power SRAM capability to the high-speed low power system.

FEATURES

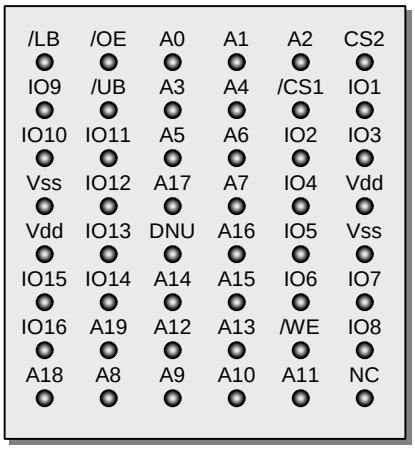
- CMOS Process Technology
- 1M x 16 bit Organization
- TTL compatible and Tri-state outputs
- Deep Power Down : Memory cell data hold invalid
- Standard pin configuration : 48-FBGA
- Data mask function by /LB, /UB

PRODUCT FAMILY

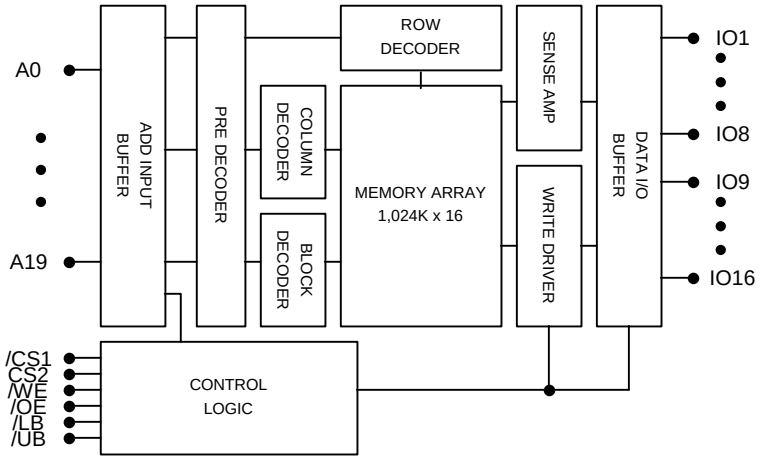
Product No.	Voltage [V]	Mode	Power Dissipation			Speed tRC[ns]	Temp. [°C]
			(I_{SB1},Max)	(I_{DPD},Max)	(I_{CC2},Max)		
HY64LD16162M-DF85E	2.3~2.7	1CS with /UB,/LB:tCS[1]	75µA	2µA	20mA	85	-25~85
HY64LD16162M-DF85I	2.3~2.7	1CS with /UB,/LB:tCS[1]	75µA	2µA	20mA	85	-40~85

Note 1. tCS - /UB,/LB=High : Chip Deselect.

PIN CONNECTION (Top View)



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Function	Pin Name	Pin Function
/CS1	Chip Select	/OE	Output Enable
CS2	Deep Power Down	IO1~IO8	Lower Data Inputs/Outputs
/WE	Write Enable	IO9~IO16	Upper Data Inputs/Outputs
/LB	Lower Byte(IO1~IO8)	A0~A19	Address Inputs
/UB	Upper Byte(IO9~IO16)	Vdd	Power(2.3V~2.7V)
DNU	Do Not Use	Vss	Ground
NC	No Connection		

ORDERING INFORMATION

Part Number	Speed	Power	Temperature	Package
HY64LD16162M-E	85	LL-Part	E[1]	FBGA
HY64LD16162M-I	85	LL-Part	I[2]	FBGA

Note

1. E : Extended Temp. (-25°C ~ 85°C)
2. I : Industrial Temp. (-40°C ~ 85°C)

ABSOLUTE MAXIMUM RATINGS [1]

Symbol	Parameter	Rating	Unit	Remark
V_{IN},V_{OUT}	Input/Output Voltage	-0.3 to Vdd+0.3	V	
Vdd	Power Supply	-0.3 to 3.6	V	
T_A	Ambient Temperature	-25 to 85	°C	HY64LD16162M-E
		-40 to 85	°C	HY64LD16162M-I
T_{STG}	Storage Temperature	-55 to 150	°C	
P_D	Power Dissipation	1.0	W	
T_{SOLDER}	Ball Soldering Temperature & Time	260•10	°C•sec	

Note

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

TRUTH TABLE

/CS1	CS2	/WE	/OE	/LB	/UB	Mode	I/O Pin		Power
							I/O1~I/O8	I/O9~I/O16	
H	H	X	X	X	X	Deselected	High-Z	High-Z	Standby
X	L	X	X	X	X	Deselected	High-Z	High-Z	Deep Power Down
X	H	X	X	H	H	Deselected	High-Z	High-Z	Standby
L	H	L	X	L	H	Write	D_{IN}	High-Z	Active
L	H	H	L	L	H	Read	D_{OUT}	High-Z	Active
L	H	H	H	L	H	Output Disabled	High-Z	High-Z	Active
L	H	L	X	H	L	Write	High-Z	D_{IN}	Active
L	H	H	L	H	L	Read	High-Z	D_{OUT}	Active
L	H	H	H	H	L	Output Disabled	High-Z	High-Z	Active
L	H	L	X	L	L	Write	D_{IN}	D_{IN}	Active
L	H	H	L	L	L	Read	D_{OUT}	D_{OUT}	Active
L	H	H	H	L	L	Output Disabled	High-Z	High-Z	Active

Note
1. H=V_{IH}, L=V_{IL}, X=don't care(V_{IL} or V_{IH})
2. /UB, /LB(Upper, Lower Byte enable)
   These active LOW inputs allow individual bytes to be written or read.
   When /LB is LOW, data is written or read to the lower byte, I/O1 - I/O8.
   When /UB is LOW, data is written or read to the upper byte, I/O9 - I/O16.

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vdd	Supply Voltage	2.3	2.5	2.7	V
V_{SS}	Ground	0	-	0	V
V_{IH}	Input High Voltage	2.0	-	Vdd+0.3	V
V_{IL}	Input Low Voltage	-0.3[1]	-	0.6	V

Note 1. VIL=-1.5V for pulse width less than 10ns

Undershoot is sampled, not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Vdd=2.3~2.7V, T_A= -25°C to 85°C(E) / -240°C to 85°C(I)

Sym.	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le Vdd$	-1	-	1	µA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le Vdd$, /CS1=$V_{IH}$, CS2=$V_{IH}$, /OE=$V_{IH}$ or /WE=V_{IL}	-1	-	1	µA
I_{CC}	Operating Power Supply Current	/CS1=V_{IL}, CS2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, $I_{I/O}$=0mA	-	-	3	mA
I_{CC1}	Average Operating Current	/CS1≤ 0.2V, CS2 ≥Vdd-0.2V, V_{IN} ≤0.2V or V_{IN}≥Vdd-0.2V, Cycle Time=1µs. 100% Duty, $I_{I/O}$=0mA	-	-	5	mA
I_{CC2}		/CS1=V_{IL}, CS2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, Cycle Time=Min. 100% Duty, $I_{I/O}$=0mA	-	-	20	mA
I_{SB}	TTL Standby Current	/CS1,CS2=V_{IH} or /UB,/LB= V_{IH}	-	-	0.5	mA
I_{SB1}	Standby Current(CMOS Input)	/CS1, CS2≥Vdd-0.2V or /UB,/LB ≥Vdd-0.2V	-	-	75	µA
I_{DPD}	Deep Power Down Current	CS2≤V_{SS}+0.2V	-	-	2	µA
V_{OL}	Output Low Voltage	I_{OL}=0.5mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=-0.5mA	2.0	-	-	V

CAPACITANCE

(Temp = 25°C, f=1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance(Add, /CS1, CS2, /WE, /OE, /UB, /LB)	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance(I/O)	$V_{I/O}$=0V	10	pF

Note : These parameters are sampled and not 100% tested

AC CHARACTERISTICS

Vdd=2.3V~2.7V, T_A = -25°C to 85°C(E) / -40°C to 85°C(I), unless otherwise specified

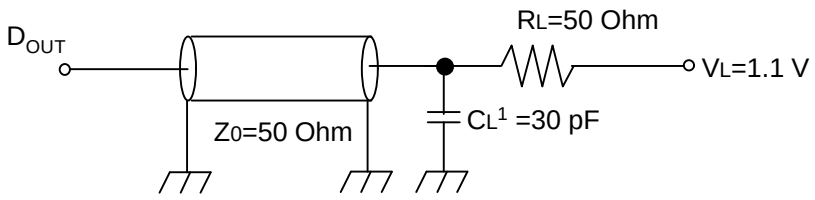
#	Symbol	Parameter	-85		Unit
			Min.	Max.	
Read Cycle					
1	tRC	Read Cycle Time	85	-	ns
2	tAA	Address Access Time	-	85	ns
3	tACS	Chip Select Access Time	-	85	ns
4	tOE	Output Enable to Output Valid	-	20	ns
5	tBA	/LB, /UB Access Time	-	85	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	10	-	ns
9	tCHZ	Chip Disable to Output in High Z	0	30	ns
10	tOHZ	Out Disable to Output in High Z	0	30	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	30	ns
12	tOH	Output Hold from Address Change	10	-	ns
Write Cycle					
13	tWC	Write Cycle Time	85	-	ns
14	tCW	Chip Selection to End of Write	70	-	ns
15	tAW	Address Valid to End of Write	70	-	ns
16	tBW	/LB, /UB Valid to End of Write	70	-	ns
17	tAS	Address Set-up Time	0	-	ns
18	tWP	Write Pulse Width	60	-	ns
19	tWR	Write Recovery Time	0	-	ns
20	tWHZ	Write to Output in High Z	0	30	ns
21	tDW	Data to Write Time Overlap	30	-	ns
22	tDH	Data Hold from Write Time	0	-	ns
23	tOW	Output Active from End of Write	5	-	ns

AC TEST CONDITIONS

T_A = -25°C to 85°C(E) / -40°C to 85°C(I), unless otherwise specified

Parameter	Value
Input Pulse Level	0.4V to 2.2V
Input Rising and Fall Time	5ns
Input and Output Timing Reference Level	1.1V
Output Load	See Below

AC TEST LOADS



Note

1. Including jig and scope capacitance.

Power-Up Sequence

1. Supply power.
2. Maintain stable power for longer than 200µs.

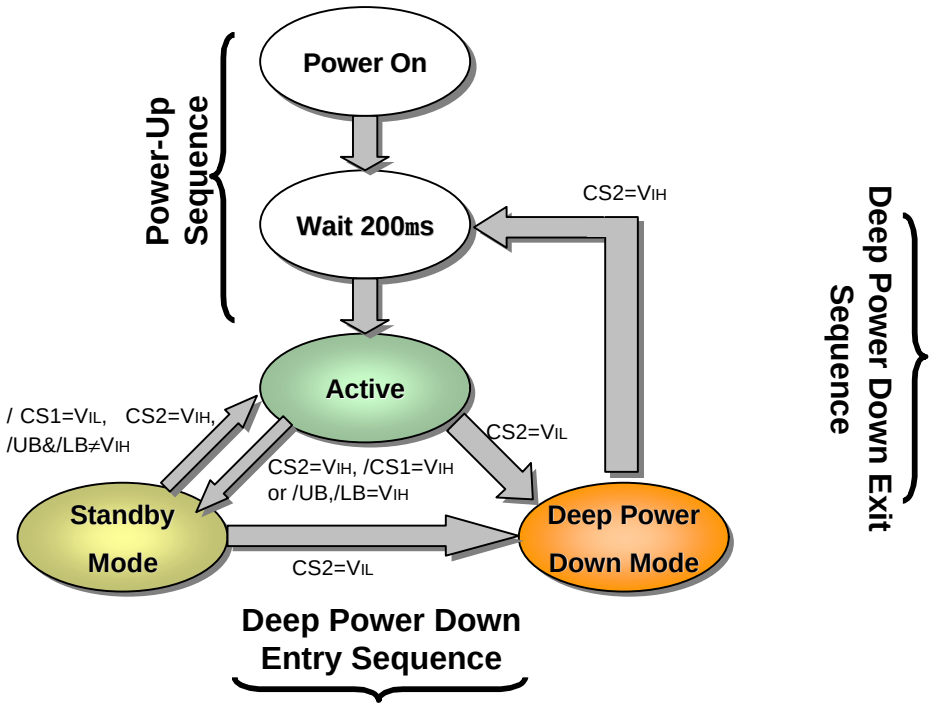
Deep Power Down Entry Sequence

1. Keep CS2 low state.
   Deep power down mode is maintained while CS2 is low state.

Deep Power Down Exit Sequence

1. Keep CS2 high state.
2. Maintain stable power for longer than 200µs.

STATE DIAGRAM

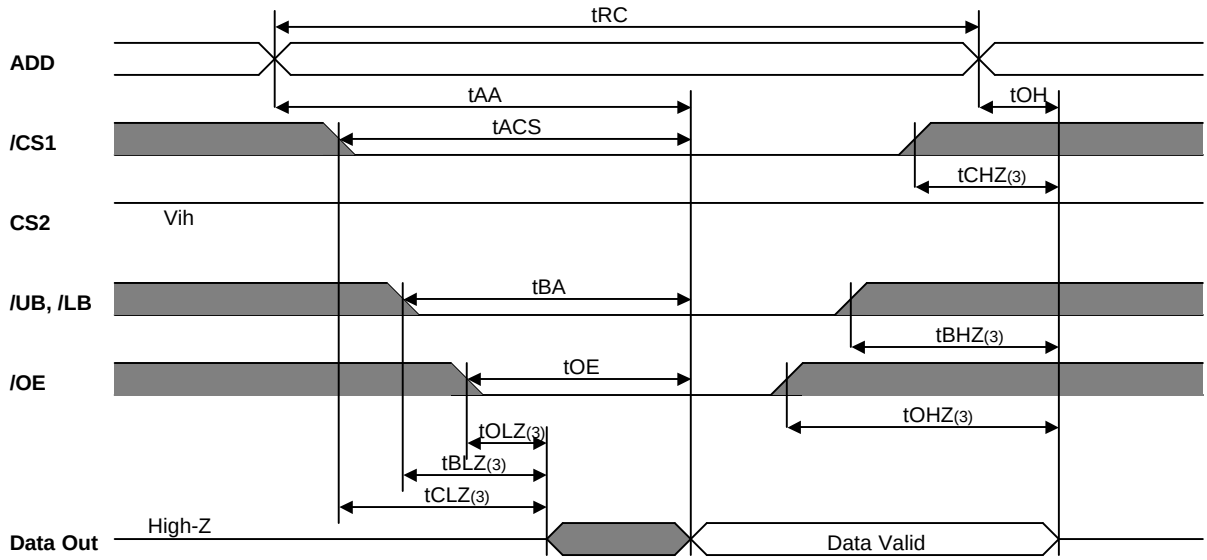


STANDBY MODE CHARACTERISTICS

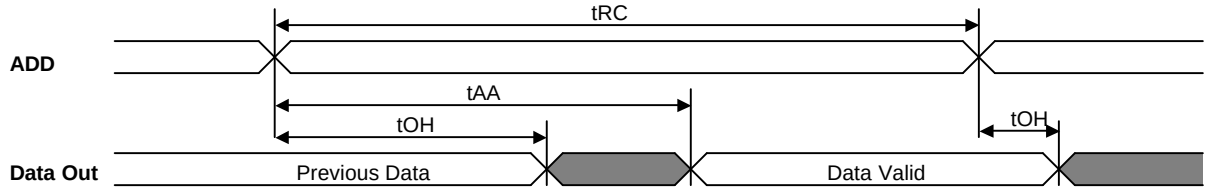
Mode	Memory Cell Data	Standby Current[µA]	Wait Time[µs]
Standby	Valid	75	0
Deep Power Down	Invalid	2	200

TIMING DIAGRAM

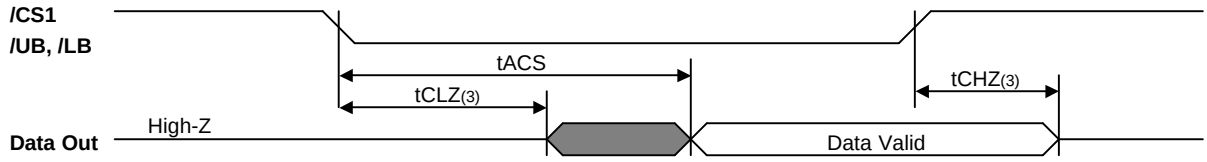
READ CYCLE 1 (Note 1, 4)



READ CYCLE 2 (Note 1, 2, 4)(CS2=Vih)



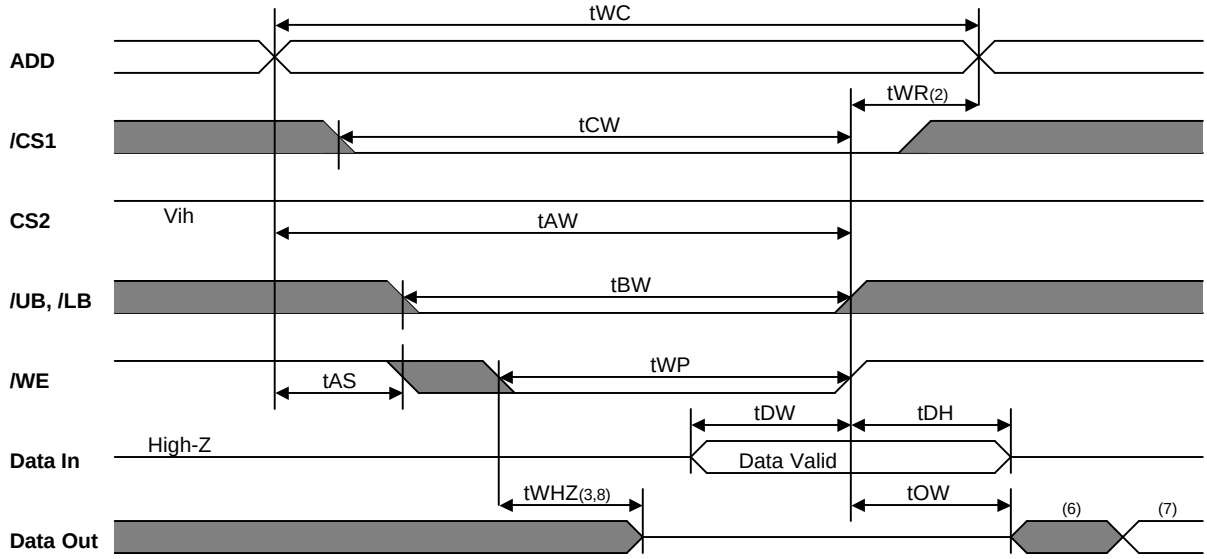
READ CYCLE 3 (Note 1, 2, 4)(CS2=Vih)



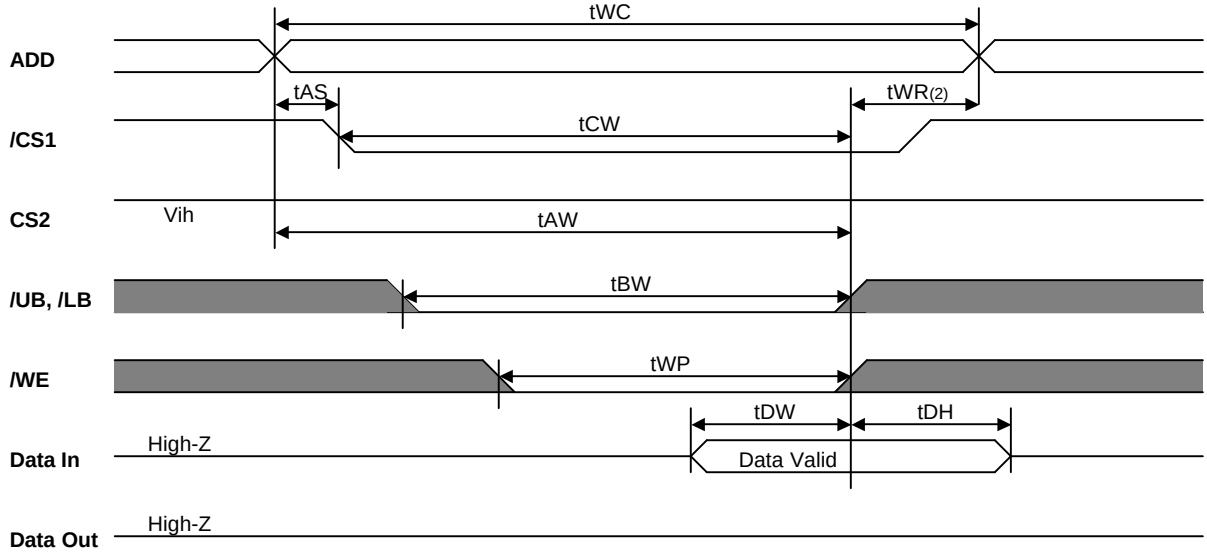
Notes :

1. Read Cycle occurs whenever a high on the /WE and /OE is low, while /UB and/or /LB and /CS1 and CS2 are in active status.
2. /OE = V_{IL}
3. tCHZ, tBHZ and tOHZ are defined as the time at which the outputs achieve the high impedance state and tOLZ,tBLZ and tCLZ are defined as the time at which the outputs achieve the low impedance state.
   These are not referenced to output voltage levels.
4. /CS1 in high for the standby, low for active.
   /UB and /LB in high for the standby, low for active.

WRITE CYCLE 1 (Note 1, 4, 5, 9, 10) (/WE Controlled)



WRITE CYCLE 2 (Note 1, 4, 5, 9, 10) (/CS1 Controlled)



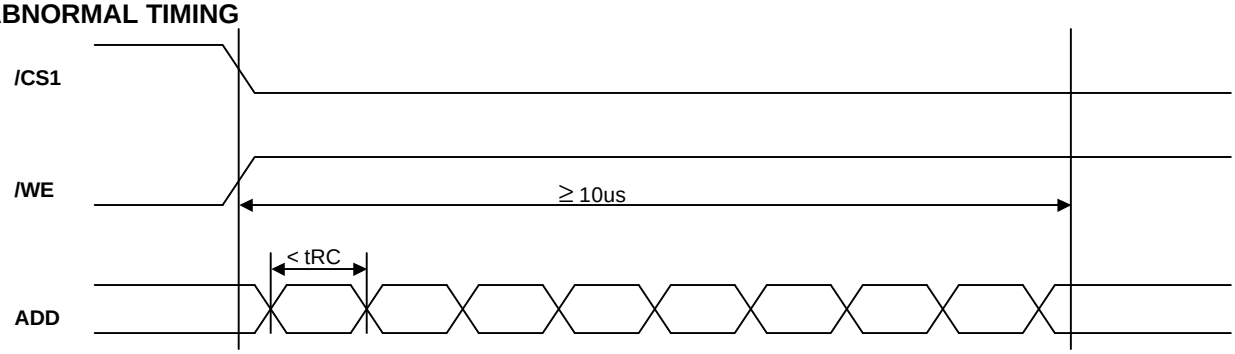
Notes :

1. A write occurs during the overlap of low /CS1, low /WE and low /UB and/or /LB.
2. tWR is measured from the earlier of /CS1, /LB, /UB, or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS1, /LB and /UB low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. /OE is continuously low (/OE=V_{IL})
6. Q(data out) is the invalid data.
7. Q(data out) is the read data of the next address.
8. tWHZ is defined as the time at which the outputs achieve the high impedance state. It is not referenced to output voltage levels.
9. /CS1 in high for the standby, low for active. /UB and /LB in high for the standby, low for active.
10. Do not input data to the I/O pins while they are in the output state.

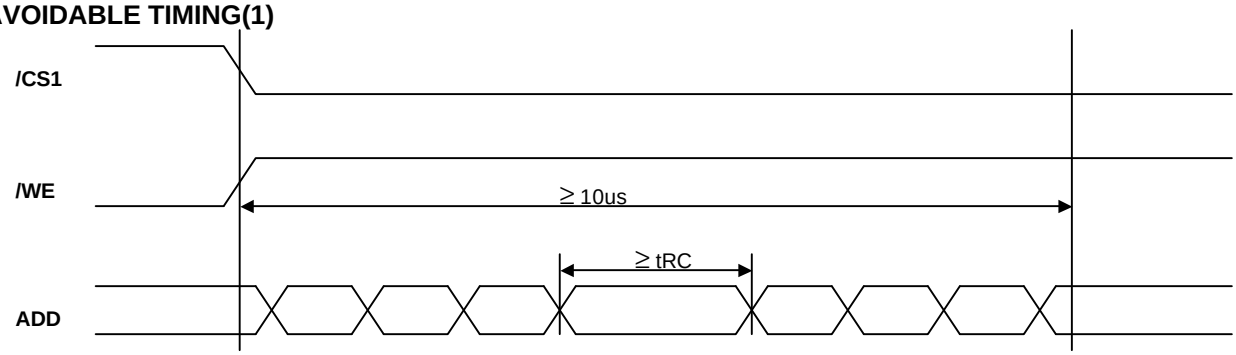
AVOID TIMING

Hynix 1T/1C SRAM has a timing which is not supported at read operation. If your system has multiple invalid address signal shorter than tRC during over 10us at read operation which showed in abnormal timing, Hynix 1T/1C SRAM needs a normal read timing at least during 10us which showed in avoidable timing(1) or toggle the /CS1 to high(≥tRC) one time at least which showed in avoidable timing(2)

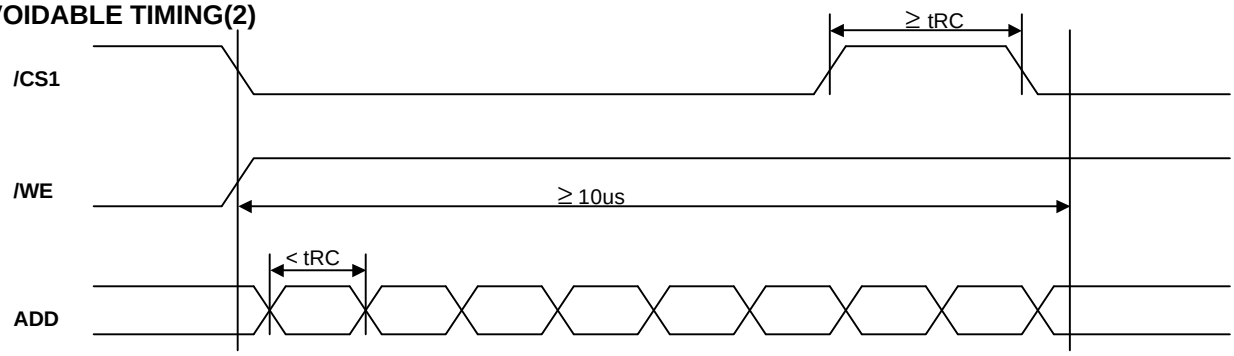
ABNORMAL TIMING



AVOIDABLE TIMING(1)

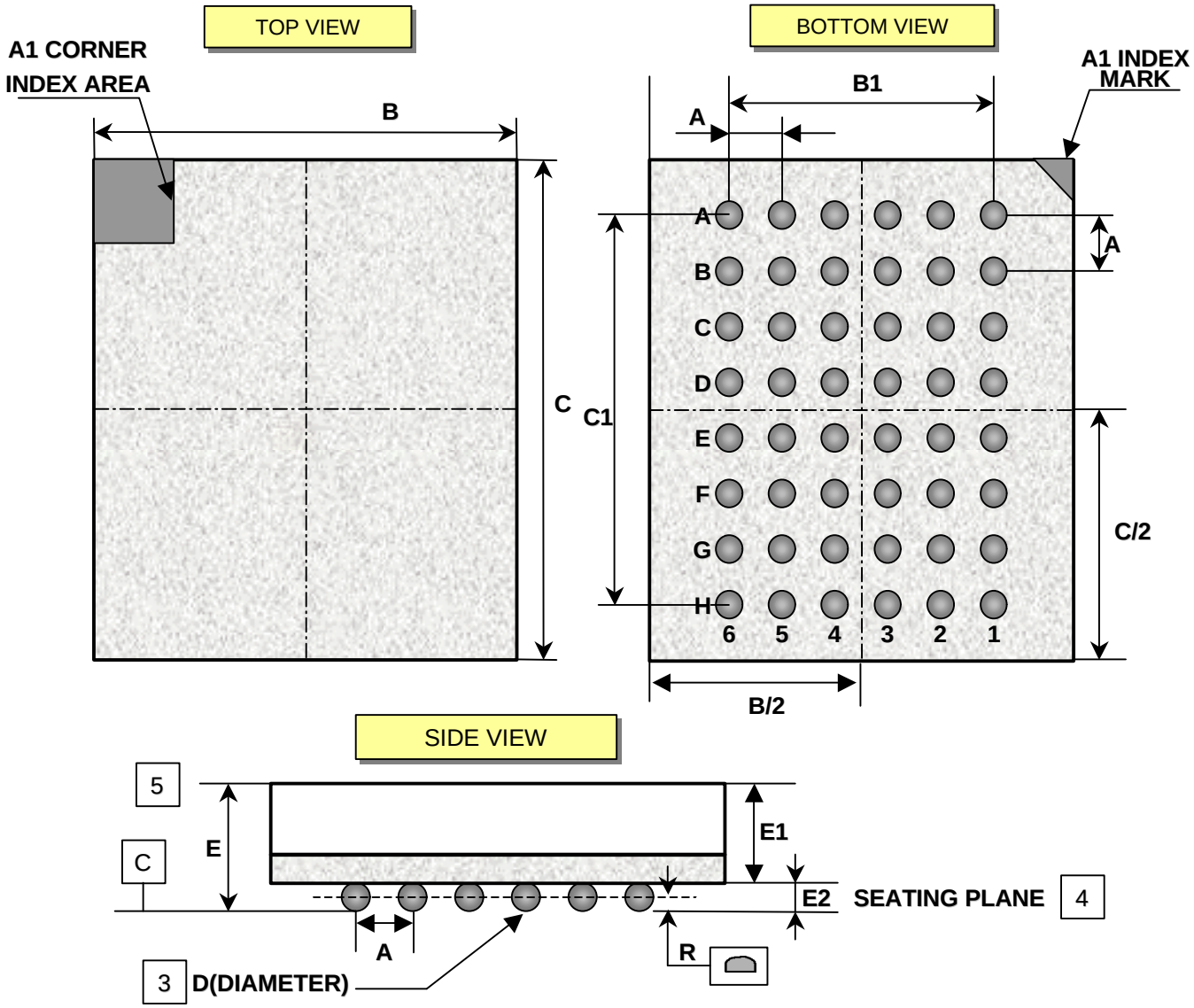


AVOIDABLE TIMING(2)



PACKAGE DIMENSION

48ball Fine Pitch Ball Grid Array Package(F)



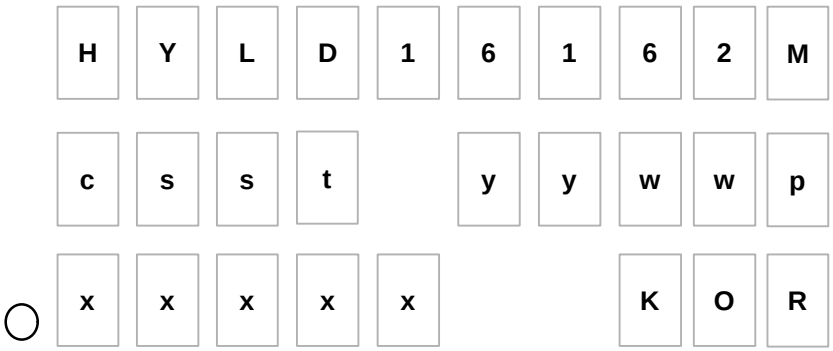
unit : mm

Symbol	Min.	Typ.	Max.
A	-	0.75	-
B	6.90	7.00	7.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.00	1.10
E1	-	0.75	-
E2	0.20	0.25	0.30
R	-	-	0.08

NOTE.

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE MILLIMETERS.
3. DIMENSION "D" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
4. PRIMARY DATUM C(SEATING PLANE) IS DEFINED BY THE CROWN OF THE SOLDER BALLS.
5. THIS IS A CONTROLLING DIMENSION.

MARKING INFORMATION

Package	Marking Example
FBGA	

Index

- **HYLD16162M** : Part Name
  - **HY** : HYNIX
  - **L** : Power Supply : 2.5V(2.3V~2.7V)
  - **D** : Tech. + Classification : 1T+1C
  - **16** : Bit Organization : x16
  - **16** : Density : 16M
  - **2** : Mode : 1CS with /UB,/LB;tCS
  - **M** : Version : 1st Generation

- **c** : Power Consumption : D – Low Low Power
- **ss** : Speed : 85 – 85ns
- **t** : Temperature : E – Extended(-25 ~ 85°C)
  I – Industrial(-40 ~ 85°C)

- **yy** : Year (ex : 01 = year 2001, 02= year 2002)
- **ww** : Work Week (ex : 12 = work week 12)
- **p** : Process Code

- **xxxxx** : Lot No.

- **KOR** : Origin Country

Note

- Capital Letter : Fixed Item
- Small Letter : Non-fixed Item