# HYM1302
## Serial Real Time Clock/Calendar With 31×8 RAM
Data Sheet

### *Features*

- 31 x 8 RAM for scratchpad data storage
- Dual power supply pins
- Serial I/O transmission
- Clock registers store BCD format
- Operating voltage: 2.0V-5.5V
- Uses less than 300 nA at 2.0 volts
- Two data transmission modes: single-byte，or burst mode
- 8–pin DIP or 8–pin SOP package
- Maximum input serial clock: 500kHz at $V_{CC}$ =2V, 2MHz at $V_{CC}$ =5V
- TTL–compatible ($V_{CC}$ = 5V)
- DS1302 compatible

### *Applications*

- Cash Register
- Security Access Controller, Door Controller
- Time Recorder
- Mobile Telephones
- Public Phone Bill Meter, Smart Card Payphone
- MP3/MP4 Player
- IC Water-Flow Meter, IC Gas Meter

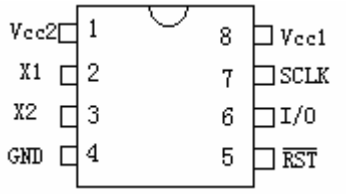
### *General Description*

The HYM1302 is a serial timekeeper IC which provides seconds, minutes, hours, day, date, month, and year information. A 32.768KHz crystal is required to provide the correct timing. The number of days in each month and leap years are automatically adjusted. The clock can operate in two modes: one is the 12-hour mode with an AM/PM indicator, the other is the 24-hour mode. In addition, the HYM1302 has additional features of dual power pins for primary and functions of the back-up power supplies, programmable trickle charger for $V_{CC1}$, and 31 bytes of static RAM for scratchpad data storage.

In order to minimize the pin number, The HYM1302 uses a serial I/O transmission method to interface with a microprocessor. Only three wires are required: (1) $\overline{RST}$ (Reset), (2) I/O (Data line), and (3) SCLK (Serial clock). Data can be transferred to and from the clock/RAM 1 byte at a time or in a burst of up to 31 bytes. The HYM1302 is designed to operate on very low power.

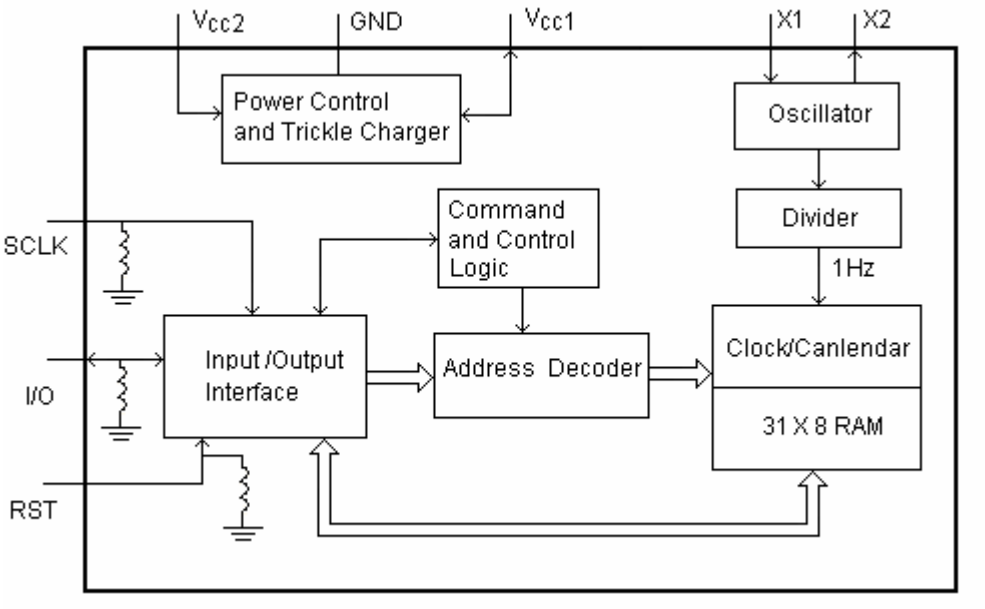
### *Block Diagram and Pin Description*

#### *Pin Assignment*




**HYM1302 (N)—8DIP**

**HYM1302Z (N) —8SOP**




### *Pin Description*

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | $V_{CC2}$ | The Primary Power Supply Pin |
| 2 | X1 | Connections for a standard 32.768kHz quartz crystal |
| 3 | X2 | Connections for a standard 32.768kHz quartz crystal |
| 4 | GND | Ground |
| 5 | $\overline{RST}$ | The reset signal must be asserted high during a read or a write, |
| 6 | I/O | The I/O pin is the bi-directional data pin for the 3-wire interface |
| 7 | SCLK | The SCLK pin is used to synchronize data movement on the serial interface |
| 8 | $V_{CC1}$ | the Back-up Power Supply Pin |

## *Absolute Maximum Rating*

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| Voltage on Any Pin Relative to Ground | $V_P$ | | -0.5～+7.0 | V |
| Operating Temperature | $T_A$ | | 0～70 | ℃ |
| Storage Temperature | $T_S$ | | -55～+125 | ℃ |
| Soldering Temperature | $T_H$ | | 260（10 Sec） | ℃ |

Note: These stress ratings only. Stress exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification, not implied and prolonged to extreme conditions may affect device reliability.

## *Electrical Characteristics*

### *Recommended DC Operating Conditions* (0ºC to 70ºC)

| Parameter | Symbol | Test Condition | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage $V_{CC1}$, $V_{CC2}$ | $V_{CC1}$, $V_{CC2}$ | | 2.0 | | 5.5 | V |
| Logic 1 Input | $V_{IH}$ | | 2.0 | | $V_{CC}$+0.3 | V |
| Logic 0 Input | $V_{IL}$ | $V_{CC}$ =2.0V | -0.3 | | +0.3 | V |
| | | $V_{CC}$ =5V | -0.3 | | +0.8 | V |

All voltages are referenced to ground.

### *Capacitance*

| Parameter | Symbol | Test Condition | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_I$ | | | 10 | | pF |
| I/O Capacitance | $C_{I/O}$ | | | 15 | | pF |
| Crystal Capacitance | $C_X$ | | | 6 | | pF |

### *DC Electrical Characteristics* *(0ºC to 70ºC; $V_{CC}$ = 2.0 to 5.5V, Unless otherwise noted.)*

| Parameter | Symbol | Test Condition | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| Input Leakage | $I_{LI}$ | | | | 500 | µA |
| I/O Leakage | $I_{LO}$ | | | | 500 | µA |
| Logic 1 Output | $V_{OH}$ | $V_{CC}$=2.0V | 1.6 | | | V |
| | | $V_{CC}$=5V | 2.4 | | | |
| Logic 0 Output | $V_{OL}$ | $V_{CC}$=2.0V | | | 0.4 | V |
| | | $V_{CC}$=5V | | | 0.4 | |
| Active Supply Current | $I_{CC1A}$ | $V_{CC1}$=2.0V, $V_{CC2}$=0V, I/O pin open, $\overline{RST}$ =1, SCLK=500KMHz | | | 0.4 | mA |
| | | $V_{CC1}$=5V, $V_{CC2}$=0V, I/O pin open, $\overline{RST}$ =1, SCLK=2 MHz | | | 1.2 | |
| Timekeeping Current | $I_{CC1T}$ | $V_{CC1}$=2.0V, $V_{CC2}$=0V,I/O pin open, $\overline{RST}$ =0,Oscillator enabled | | | 0.3 | µA |
| | | $V_{CC1}$=5V, $V_{CC2}$=0V,I/O pin open, $\overline{RST}$ =0,Oscillator enabled | | | 1 | |
| Standby Current | $I_{CC1S}$ | $V_{CC1}$=2.0V,$V_{CC2}$=0V, $\overline{RST}$ ,I/O,and SCLK open. Oscillator disabled | 100 | 200 | 300 | nA |
| | | $V_{CC1}$=5V,$V_{CC2}$=0V, $\overline{RST}$ ,I/O,and SCLK open. Oscillator disabled | 100 | 200 | 300 | |
| Active Supply Current | $I_{CC2A}$ | $V_{CC2}$=2.0V, $V_{CC1}$=0V，I/O pin open, $\overline{RST}$ =1, SCLK=500KHz | | | 0.425 | mA |
| | | $V_{CC2}$=5V, $V_{CC1}$=0V，I/O pin open, $\overline{RST}$ =1, SCLK=2 MHz | | | 1.28 | |
| Timekeeping Current | $I_{CC2T}$ | $V_{CC2}$=2.0V, $V_{CC1}$=0V,I/O pin open, $\overline{RST}$ =0,Oscillator enabled | | | 25.3 | µA |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | $V_{CC2}$=5V, $V_{CC1}$=0V,I/O pin open, RST=0,Oscillator enabled | | | 81 | |
| Standby Current | $I_{CC2S}$ | $V_{CC2}$=2.0V, $V_{CC1}$=0V, $\overline{RST}$, I/O, and SCLK open. Oscillator disabled | | | 25 | μA |
| | | $V_{CC2}$=5V, $V_{CC1}$=0V, $\overline{RST}$, I/O, and SCLK open. Oscillator disabled | | | 80 | |
| Trickle Charge Resistors | R1 | | | 2 | | kΩ |
| | R2 | | | 4 | | |
| | R3 | | | 8 | | |
| Trickle Charge Diode Voltage Drop | $V_{TD}$ | | | 0.7 | | V |

**Note:** Typical values are at 25°C.

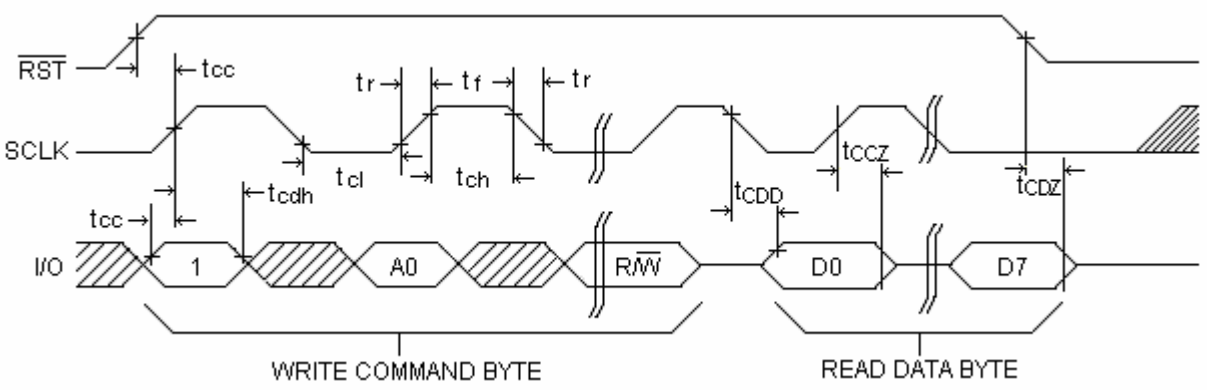
### *AC Electrical Characteristics* *(0ºC to 70ºC; $V_{CC}$ = 2.0 to 5.5V, Unless otherwise noted.)*

| Parameter | Symbol | Test Condition | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| CLK to $\overline{RST}$ Hold | $t_{cch}$ | $V_{CC}$=2.0V | 240 | | | ns | 2 |
| | | $V_{CC}$=5V | 60 | | | | |
| $\overline{RST}$ Inactive Time | $t_{cwh}$ | $V_{CC}$=2.0V | 4 | | | ns | 2 |
| | | $V_{CC}$=5V | 1 | | | | |
| $\overline{RST}$ to I/O High Z | $t_{cdz}$ | $V_{CC}$=2.0V | | | 280 | ns | 2 |
| | | $V_{CC}$=5V | | | 70 | | |
| SCLK to I/O High Z | $t_{ccz}$ | $V_{CC}$=2.0V | | | 280 | ns | 2 |
| | | $V_{CC}$=5V | | | 70 | | |
| Data to CLK Setup | $t_{dc}$ | $V_{CC}$=2.0V | 200 | | | ns | 2 |
| | | $V_{CC}$=5V | 50 | | | | |
| CLK to Data Hold | $t_{cdh}$ | $V_{CC}$=2.0V | 280 | | | ns | 2 |
| | | $V_{CC}$=5V | 70 | | | | |
| CLK to Data Delay | $t_{cdd}$ | $V_{CC}$=2.0V | | | 800 | ns | 2,3,4 |
| | | $V_{CC}$=5V | | | 200 | | |
| CLK Low Time | $t_{cl}$ | $V_{CC}$=2.0V | 1000 | | | ns | 2 |
| | | $V_{CC}$=5V | 250 | | | | |
| CLK High Time | $t_{ch}$ | $V_{CC}$=2.0V | 1000 | | | ns | 2 |
| | | $V_{CC}$=5V | 250 | | | | |
| CLK Frequency | $t_{clk}$ | $V_{CC}$=2.0V | | | 0.5 | MHz | 2 |
| | | $V_{CC}$=5V | DC | | 2.0 | | |
| CLK Rise and Fall | $t_r$, $t_f$ | $V_{CC}$=2.0V | | | 2000 | ns | |
| | | $V_{CC}$=5V | | | 500 | | |
| $\overline{RST}$ to CLK Setup | $t_{CC}$ | $V_{CC}$=2.0V | 4 | | | μs | 2 |
| | | $V_{CC}$=5V | 1 | | | | |

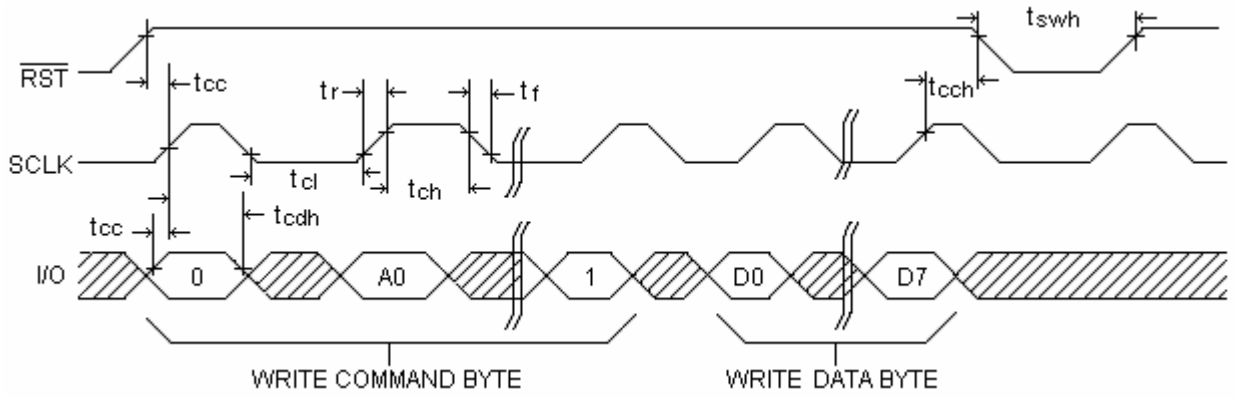
**Notes:**

1. Typical values are at 25°C.
2. Measured at $V_{IH}$=2.0V or $V_{IL}$=0.8V and 10 ms maximum rise and fall time.
3. Measured at $V_{OH}$=2.4V or $V_{OL}$=0.4V.
4. Load capacitance = 50pF.

***Timing Diagram: Read Data Transfer***




***Timing Diagram: Write Data Transfer***




## *Application Information*

### *Command Byte*

For each data transfer, a command byte is initiated to specify which register is accessed. This is to determine whether a read or write is operated and whether a single byte or burst mode transfer is to occur. The command byte is shown in Table 1.

**Table 1.Address/ Command Byte**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | R/C | A4 | A3 | A2 | A1 | A0 | R/W |

The MSB (Bit 7) must be logic 1. If it is 0, HYM1302 will not be written. R/C (Bit 6) specifies clock/calendar data if logic 0 or RAM data if logic 1. A4-A0 (Bits 1 through 5) specify the designated registers to be input or output, and the R/W (bit 0) specifies a write operation if logic 0 or read operation if logic 1. The command byte is always input starting with the LSB (bit 0).

### *Clock/Calendar and RAM*

The clock/calendar is contained in seven write/read registers. Data contained in the clock/ calendar registers is in binary coded decimal format (BCD). The static RAM is 31x8 bytes addressed consecutively in the RAM address space. The registers and data format summary is shown in Table 2.

**Table 2.Registers Address/Definition**

| Register Name | Range Data | Register Definition | | | | | | | | The command byte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 1 | R/C | A4 | A3 | A2 | A1 | A0 | R/W |
| Seconds | 00-59 | CH | 10SEC | | | SEC | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1/0 |
| Minutes | 00-59 | 0 | 10MIN | | | MIN | | | | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1/0 |
| Hours | 01-12 | 12/ | 0 | AP | HR | HOUR | | | | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1/0 |
| | 00-23 | 24 | 0 | 10 | HR | | | | | | | | | | | | |
| Date | 01-31 | 0 | 0 | 10DATE | | DATE | | | | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1/0 |
| Month | 01-12 | 0 | 0 | 0 | 10M | MONTH | | | | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1/0 |
| Day | 01-07 | 0 | 0 | 0 | 0 | DAY | | | | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1/0 |
| Year | 00-99 | 10 YEAR | | | | YEAR | | | | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1/0 |
| Control | | WP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1/0 |
| Charger | | TS | TS | TS | TS | DS | DS | RS | RS | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1/0 |
| RAM0 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1/0 |
| RAM1 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1/0 |
| …… | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 1 | 1 | 0 0 0 1 0 —1 1 1 0 1 | | | | | 1/0 |
| RAM30 | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1/0 |

### *Data Transfer*

To initiate any transfer of data, $\overline{RST}$ is taken high and the command word is loaded into the shift register providing both address and command information. Data is serially input on the rising edge of the SCLK. The first 8 bits specify which of 40 bytes will be accessed, whether a read or write cycle will take place, and whether a byte or burst mode transfer is to occur. After the first eight clock cycles have loaded the command word into the shift register, additional clocks will output data for a read or input data for a write. All data is serially input on the rising edge of SCLK and outputs on the falling edge of SCLK. The data transfer summary is shown in Figure 1.

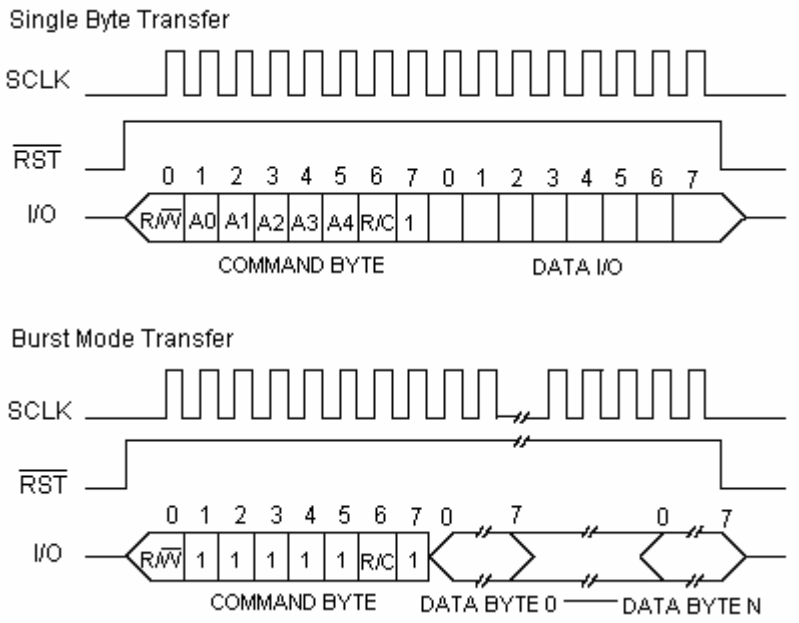



**Figure 1.Data Transfer Summary**

In writing a data byte with HYM1302, following the eight SCLK cycles that input a write command byte, a data

byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

In reading a data on the register of HYM1302, following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as $\overline{RST}$ remains high. This operation permits continuous burst mode read capability. Also, the I/O pin is tri–stated upon each rising edge of SCLK. Data is output starting with bit 0.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the $\overline{RST}$ input is low all data transfer terminates and the I/O pin goes to a high impedance state. Data transfer is illustrated in Figure 3.

### *Burst Mode*

The command byte of burst mode is shown in Table 3.

**Table 3.The command byte of burst mode**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | R /C | 1 | 1 | 1 | 1 | 1 | R/W |

The R/C bit (bit 6) specifies clock/calendar burst mode if logic 0 or RAM burst mode if logic 1. The R/W bit (bit 0) specifies a write operation if logic 0 or read operation if logic 1.

In the clock/calendar burst mode, the first eight clock/calendar registers can be consecutively read or written starting with bit 0 of address 0, and in RAM burst mode, the 31 RAM registers can be consecutively read or written starting with bit 0 of address 0. The trickle charger is not accessible in burst mode.

### *Clock Halt Flag and Write-Protect Bit*

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock oscillator is stopped, when this bit is written to logic 0, the clock will start.

The WP bit (bit 7) of the control register is the write-protect bit. Before any write operation to the clock or RAM, bit 7 must be 0. When bit7 is set to logic 0, the write protect bit prevents a write operation to any other register. The initial power on state is not defined. The first seven bits (bits 0 – 6) are forced to 0 and will always read a 0 when read.

### *AM-PM/12-24 Mode*

Bit 7 of the hours register is defined as the 12– or 24–hour mode select bit. When high, the 12–hour mode is selected. In the 12–hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24–hour mode, bit 5 is the second 10-hour bit (20 – 23 hours).

### *Trickle Charge Register*

This register controls the trickle charge characteristics of the HYM1302. The simplified schematic of Figure 2 shows the basic components of the trickle charger.

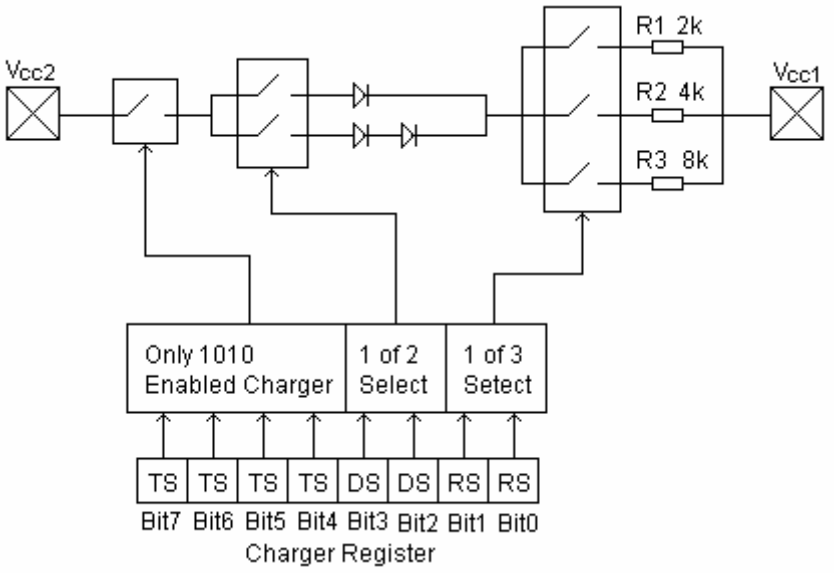



**Figure 2.Trickle Charger**

The trickle charge select (TS) bits (bits 4 – 7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 will enable the trickle charger. All other patterns will disable the trickle charger. The HYM1302 powers up with the trickle charger disabled. The DS bits (bits 2 – 3) select whether one diode or two diodes are connected between $V_{CC2}$ and $V_{CC1}$. The diode selected by the DS bits is as follows:

| DS Bits | Diode Number |
|---|---|
| 00 | None |
| 01 | 1 |
| 10 | 2 |
| 11 | None |

If DS is 00 or 11, the trickle charger is disabled independently of TCS.

The RS bits (bits 0 –1) select the resistor that is connected between $V_{CC2}$ and $V_{CC1}$. The resistor selected by the RS bits is as follows:

| RS Bits | Resistor | Typical Value |
|---|---|---|
| 00 | None | None |
| 01 | R1 | 2kΩ |
| 10 | R2 | 4kΩ |
| 11 | R3 | 8kΩ |

If RS is 00, the trickle charger is disabled independently of TCS.

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to $V_{CC2}$ and a super cap is connected to $V_{CC1}$. Also assume that the trickle charger has been enabled with one diode and resistor R1 between $V_{CC2}$ and $V_{CC1}$. The maximum current $I_{MAX}$ would therefore be calculated as follows:

$$I_{MAX} = (5.0V - \text{diode drop}) / R1 \approx (5.0V - 0.7V) / 2K\Omega \approx 2.2\ mA$$

Obviously, as the super cap charges, the voltage drop between $V_{CC2}$ and $V_{CC1}$ will decrease and therefore the charge current will decrease.

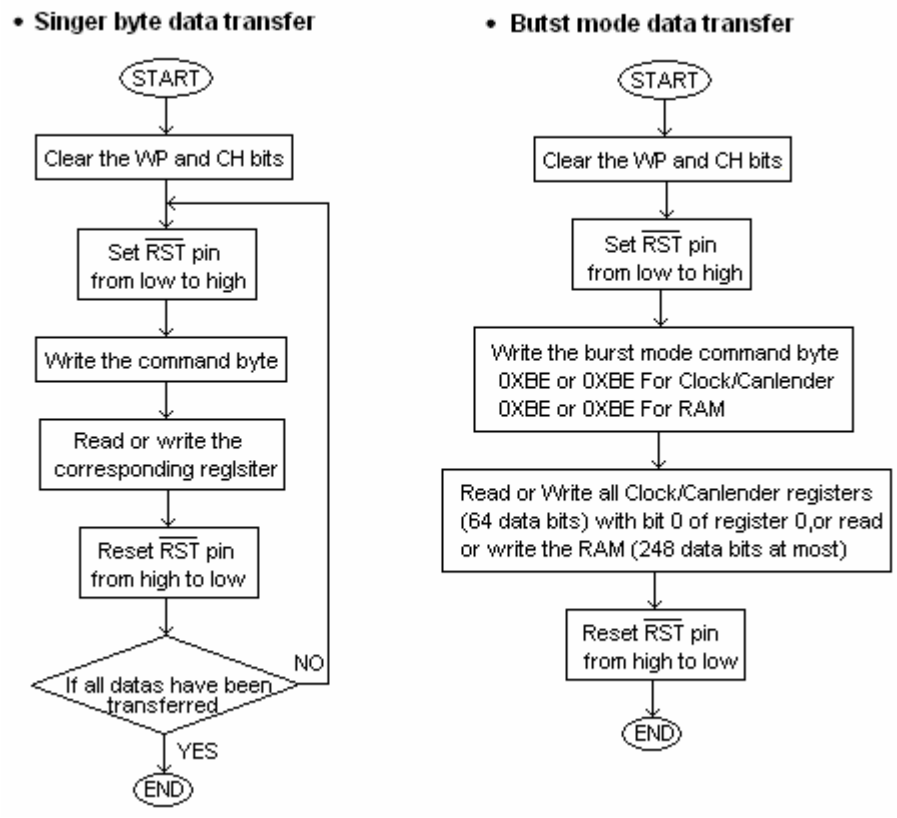
### *Crystal Selection*

A 32.768 kHz crystal can be directly connected to the HYM1302 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (CL) of 6pF.

### *Operating Flowchart*

To initiate any transfer of data, $\overline{RST}$ is taken high and an 8-bit command byte is first loaded into the control logic to provide the register address and command information. Following the command word, the clock/calendar data is serially transferred to or from the corresponding register. The $\overline{RST}$ pin must be taken low again after the transfer operation is completed. All data enter on the rising edge of SCLK and outputs on the falling edge of SCLK. In total, 16 clock pulses are needed for a single byte mode and 72 for clock/calendar burst mode. Both input and output data starts with bit 0.

The read or write operating flowcharts are shown on below.

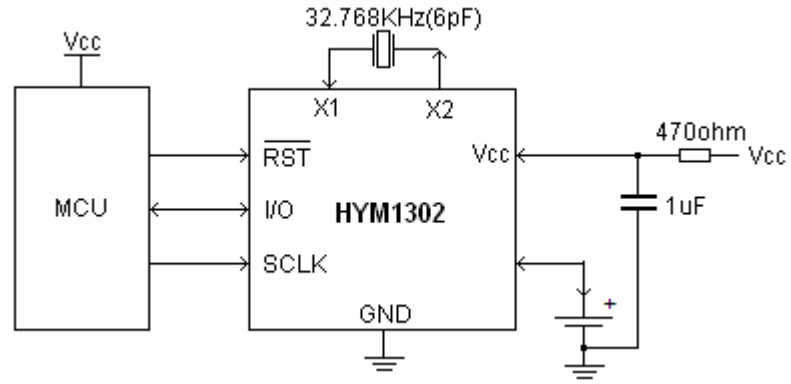



### *Power Control*

$V_{CC1}$ provides low power operation in single supply and battery operated systems as well as low power battery backup. $V_{CC2}$ provides the primary power in dual supply systems where $V_{CC1}$ is connected to a backup source to maintain the time and data in the absence of primary power.

The HYM1302 will operate from the larger of $V_{CC1}$ or $V_{CC2}$. When $V_{CC2}$ is greater than $V_{CC1}$ + 0.2V, $V_{CC2}$ will power the HYM1302. When $V_{CC2}$ is less than $V_{CC1}$, $V_{CC1}$ will power the HYM1302.

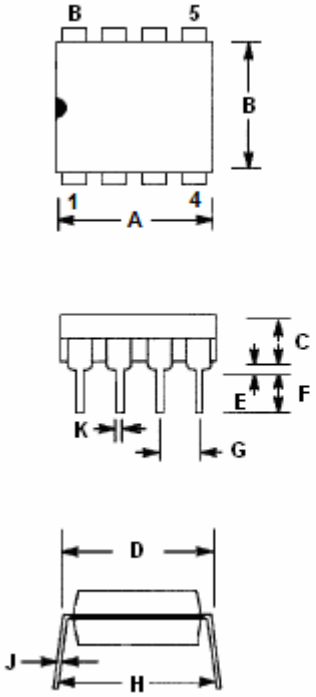
### *Typical Operating Circuit*




## *Ordering Information*

| Part | Temp Range | Pin-Package | Top Mark |
|---|---|---|---|
| HYM1302 | 0°C to +70°C | 8 PDIP | HYM1302 |
| HYM1302N | -40°C to +85°C | 8 PDIP | HYM1302N |
| HYM1302Z | 0°C to +70°C | 8 SO(150mils) | HYM1302Z |
| HYM1302ZN | -40°C to +85°C | 8 SO | HYM1302ZN |

## *Package Information*




| PKG | 8-PIN DIP | |
|---|---|---|
| DIM | MIN | MAX |
| A IN. | 0.360 | 0.400 |
| MM | 9.14 | 10.16 |
| B IN. | 0.240 | 0.260 |
| MM | 6.10 | 6.60 |
| C IN. | 0.120 | 0.140 |
| MM | 3.05 | 3.56 |
| D IN. | 0.300 | 0.325 |
| MM | 7.62 | 8.26 |
| E IN. | 0.015 | 0.040 |
| MM | 0.38 | 1.02 |
| F IN. | 0.120 | 0.140 |
| MM | 3.04 | 3.56 |
| G IN. | 0.090 | 0.110 |
| MM | 2.29 | 2.79 |
| H IN. | 0.320 | 0.370 |
| MM | 8.13 | 9.40 |
| J IN. | 0.008 | 0.012 |
| MM | 0.20 | 0.30 |
| K IN. | 0.015 | 0.021 |
| MM | 0.38 | 0.53 |