SIEMENS

2M x 32-Bit Dynamic RAM Module HYM 322030S/GS-50/-60/-70

Advanced Information

- 2 097 152 words by 32-bit organization
- 1 memory bank
- Fast access and cycle time
  50 ns access time
  90 ns cycle time (-50 version)
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
- Fast page mode capability
  35 ns cycle time (-50 version)
  40 ns cycle time (-60 version)
  45 ns cycle time (-70 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 2640 mW active (-50 version)
  max. 2420 mW active (-60 version)
  max. 2200 mW active (-70 version)
  CMOS – 22 mW standby
  TTL –44 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  $\overline{\text{RAS}}$-only-refresh
  Hidden-refresh
- 4 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- 72 pin Single in-Line Memory Module (L-SIM-72-9) with 20.32 mm (800 mil) height
- Utilizes four 2M × 8 -DRAMs in 400 mil SOJ packages
- 2048 refresh cycles / 32 ms with 11/10 addressing
- Optimized for use in byte-write non-parity applications
- Tin-Lead contact pads (S-version)
- Gold contact pads (GS - version)

The HYM 322030S/GS-50/-60/-70 is a 8 MByte DRAM module organized as 2 097 152 words by 32-bit in a 72-pin single-in-line package comprising four HYB 5117800BSJ 2M × 8 DRAMs in 400 mil wide SOJ-packages mounted together with four 0.2 µF ceramic decoupling capacitors on a PC board.

Each HYB 5117800BSJ is described in the data sheet and is fully electrical tested and processed according to SIEMENS standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The speed of the module can be detected by the use of four presence detect pins.

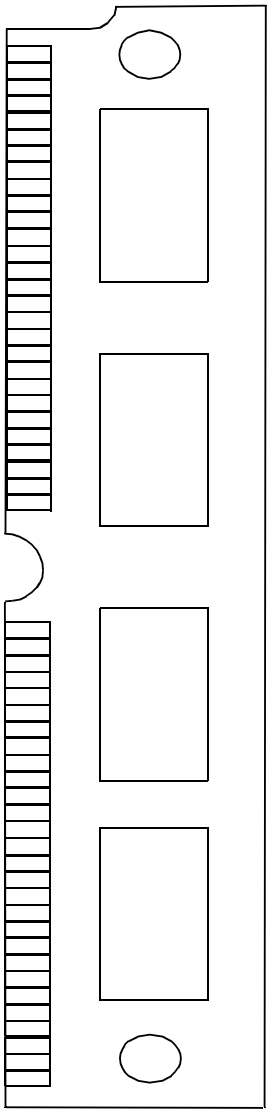
The common I/O feature on the HYM 322030S/GS-60/-70 dictates the use of early write cycles.

Ordering Information

Type	Ordering Code	Package	Description
HYM 322030S-50	on request	L-SIM-72-9	DRAM Module (access time 50 ns)
HYM 322030S-60	Q67100-Q976	L-SIM-72-9	DRAM Module (access time 60 ns)
HYM 322030S-70	Q67100-Q977	L-SIM-72-9	DRAM Module (access time 70 ns)
HYM 322030GS-50	on request	L-SIM-72-9	DRAM Module (access time 50 ns)
HYM 322030GS-60	Q67100-Q2018	L-SIM-72-9	DRAM Module (access time 60 ns)
HYM 322030GS-70	Q67100-Q2019	L-SIM-72-9	DRAM Module (access time 70 ns)

Pin Configuration

VSS	1	DQ0	2
DQ16	3	DQ1	4
DQ17	5	DQ2	6
DQ18	7	DQ3	8
DQ19	9	VCC	10
N.C.	11	A0	12
A1	13	A2	14
A3	15	A4	16
A5	17	A6	18
A10	19	DQ4	20
DQ20	21	DQ5	22
DQ21	23	DQ6	24
DQ22	25	DQ7	26
DQ23	27	A7	28
N.C.	29	VCC	30
A8	31	A9	32
N.C.	33	$\overline{RAS2}$	34
N.C.	35	N.C.	36
N.C.	37	N.C.	38
VSS	39	$\overline{CAS0}$	40
$\overline{CAS2}$	41	$\overline{CAS3}$	42
$\overline{CAS1}$	43	$\overline{RAS0}$	44
N.C.	45	N.C.	46
$\overline{WE}$	47	N.C.	48
DQ8	49	DQ24	50
DQ9	51	DQ25	52
DQ10	53	DQ26	54
DQ11	55	DQ27	56
DQ12	57	DQ28	58
VCC	59	DQ29	60
DQ13	61	DQ30	62
DQ14	63	DQ31	64
DQ15	65	N.C.	66
PD0	67	PD1	68
PD2	69	PD3	70
N.C.	71	VSS	72

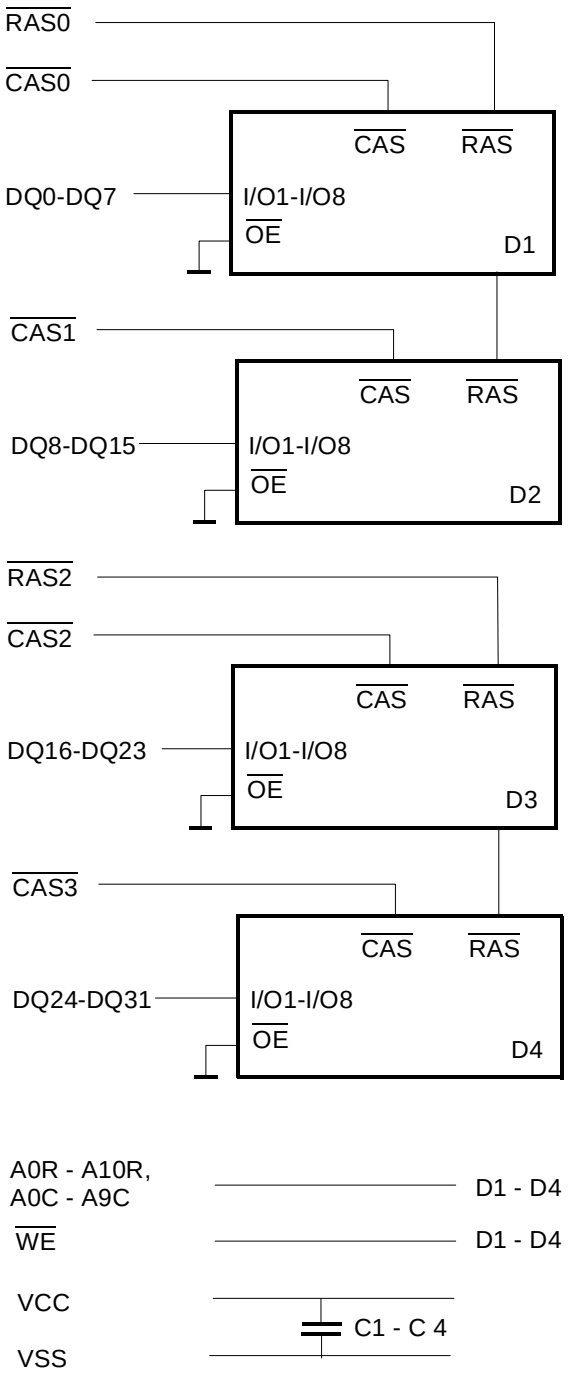


Pin Names

A0R-A10R	Row Address Inputs
A0C-A9C	Column Address Inputs
DQ0-DQ31	Data Input/Output
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
PD	Presence Detect Pin
N.C.	No Connection

Presence Detect Pins

	-50	-60	-70
PD0	N.C.	N.C.	N.C.
PD1	N.C.	N.C.	N.C.
PD2	V_{SS}	N.C.	V_{SS}
PD3	V_{SS}	N.C.	N.C.



Block Diagram

Absolute Maximum Ratings

Operation temperature range ..... 0 to + 70 ℃
Storage temperature range..... – 55 to 125 ℃
Input/output voltage .....–0.5V to min (Vcc+0.5, 7.0) V
Power supply voltage..... – 1 to + 7 V
Power dissipation..... 4.2 W
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics
T_A = 0 to 70 ℃, V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	Vcc+0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min) -50 version -60 version -70 version	I_{CC1}	 – – –	 480 440 400	 mA mA mA	2),3),4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	8	mA	
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min) -50 version -60 version -70 version	I_{CC3}	 – – –	 480 440 400	 mA mA mA	2), 4)

DC Characteristics[1] (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min)	I_{CC4}				
-50 version		–	160	mA	2), 3), 4)
-60 version		–	140	mA	
-70 version		–	120	mA	
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	4	mA	
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min)	I_{CC6}				
-50 version		–	480	mA	2), 4)
-60 version		–	440	mA	
-70 version		–	400	mA	

Capacitance

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	40	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	45	pF
Input capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{I3}	–	45	pF
Input capacitance ($\overline{WE}$)	C_{I4}	–	45	pF
I/O capacitance (DQ0-DQ31)	C_{IO}	–	25	pF

AC Characteristics [5)6)] 16F

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
common parameters									
Random read or write cycle time	t_{RC}	90	–	110	–	130	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	–	40	–	50	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10k	15	10k	20	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	10	–	15	–	15	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	37	20	45	20	50		
$\overline{RAS}$ to column address delay time	t_{RAD}	13	25	15	30	15	35	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15	–	20	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	50		60	–	70	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	–	32	–	32	–	32	ms	
Read Cycle									
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	20	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	–	35	ns	8,10
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	0	–	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	ns	12

AC Characteristics (cont'd) [5)6)] 16F

T_A = 0 to 70 °C, V_{CC} = 5 V ± 10 %, t_T = 5 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Early Write Cycle									
Write command hold time	t_{WCH}	8	–	10	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	–	15	–	20	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	–	15	–	20	–	ns	
Data setup time	t_{DS}	0	–	0	–	0	–	ns	16
Data hold time	t_{DH}	10	–	10	–	15	–	ns	16
Fast Page Mode Cycle									
Fast page mode cycle time	t_{PC}	35	–	40	–	45	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	30	–	35	–	40	ns	7
$\overline{RAS}$ pulse width	t_{RAS}	50	200k	60	200k	70	200k	ns	
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHPC}	30	–	35	–	40	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle									
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	–	10	–	10	–	ns	

Notes:

1) All voltages are referenced to VSS.

2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.

3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = VIL. In the case of ICC4 it can be changed once or less during a fast page mode cycle (tPC).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) AC measurements assume tT = 5 ns.

7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Transition times are also measured between VIH and VIL.

8) Measured with a load equivalent to 2 TTL loads and 100 pF.

9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.

10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.

11) Either tRCH or tRRH must be satisfied for a read cycle.

12) tOFF (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels

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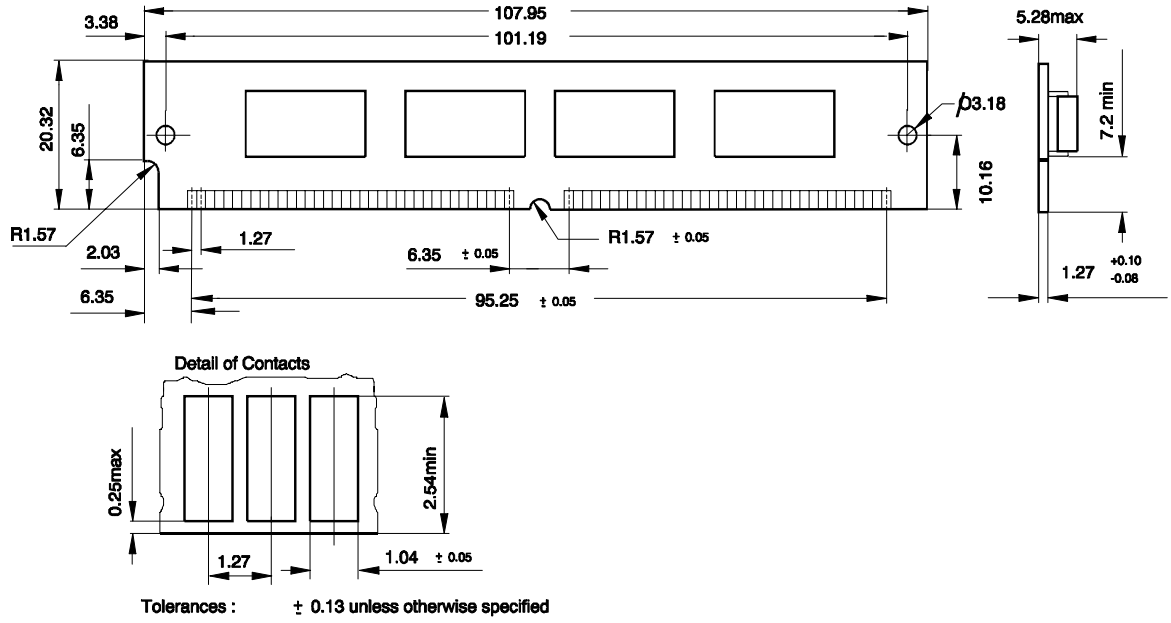
13) tWCS is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If tWCS > tWCS (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle.

14) These parameters are referenced to the $\overline{CAS}$ leading edge.

Package Outline



Module Package L-SIM-72-9
(Single in-Line Memory Module)