HYM536100 Series

1M x 36-bit CMOS DRAM MODULE

DESCRIPTION

The HYM536100 is a 1M x 36-bit Fast page mode CMOS DRAM module consisting of eight HY514400 and four HY531000 in 20/26 pin SOJ on a 72 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitor is mounted for each DRAM.
The HYM536100M is a Tin-Lead plated and HYM536100MG is a Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 4M byte memory.

FEATURES

- **Low power dissipation**
  Max. CMOS standby 66.0mW
  Max. TTL standby 132.0mW
  Max. operating

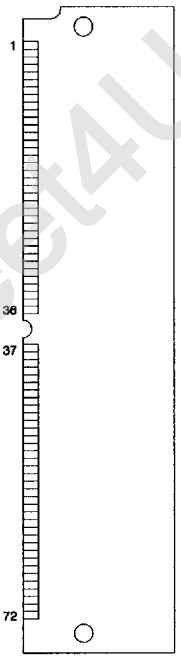
Speed	Power
70	5.83W
80	5.17W

- **Single power supply of 5V±10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	t_{RAC}	t_{CAC}	t_{PC}
70	70ns	20ns	50ns
80	80ns	25ns	50ns

- **Fast page mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh**
- **1024 refresh cycles / 16ms**

PIN CONNECTION



PIN DESCRIPTION

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0-A9	Address Input
DQ0-DQ35	Data Input/Output
PD1-PD4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground

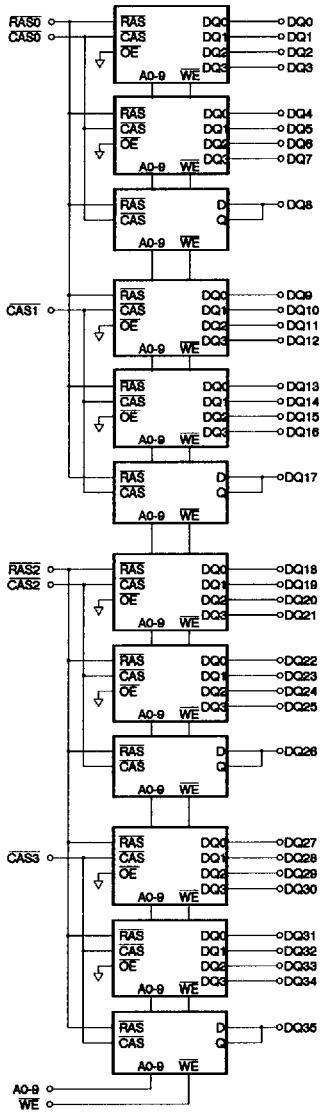
PIN NAME

#	NAME	#	NAME
1	Vss	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	Vss
4	DQ1	40	$\overline{CAS0}$
5	DQ19	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ20	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ21	45	NC
10	Vcc	46	NC
11	NC	47	$\overline{WE}$
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	NC	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	Vcc
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC	65	DQ16
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	$\overline{RAS2}$	70	PD4
35	DQ26	71	NC
36	DQ8	72	Vss

PRESENCE DETECT PINS

PIN	-70	-80
PD1	Vss	Vss
PD2	Vss	Vss
PD3	Vss	NC
PD4	NC	Vss

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	7.76	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	–1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V±10%, V_{SS} = 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \le V_{IN} \le V_{CC}+1.0$, All other pins not under test = V_{SS}		-120	120	μA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	μA	
I_{CC1}	V_{CC} Supply Current, Operating	$t_{RC} = t_{RC}$ (min.)	70 80	- -	1060 940	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs ≥ V_{SS}		-	24	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	$t_{RC} = t_{RC}$ (min.)	70 80	- -	1060 940	mA	1,3
I_{CC4}	V_{CC} Supply Current, Fast Page mode	$t_{PC} = t_{PC}$ (min.)	70 80	- -	860 740	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ V_{CC}–0.2V		-	12	mA	
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$t_{RC} = t_{RC}$ (min.)	70 80	- -	1060 940	mA	1,3
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH} = –5mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

AC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V±10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM536100M/MG				UNIT	NOTE
			-70		-80			
			MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	130	-	150	-	ns	
2	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
3	tPC	Fast Page Mode Cycle Time	50	-	50	-	ns	
4	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	-	45	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	20	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	35	-	40	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	45	-	45	ns	4
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	70	10K	80	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100K	80	100K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	20	-	25	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	70	-	80	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	20	10K	25	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	60	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	55	-	60	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	55	-	60	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	ms	
40	tWCS	Write Command Set-up Time	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HM536100M/MG				UNIT	NOTE
			-70		-80			
			MIN.	MAX.	MIN.	MAX.		
41	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	30	-	30	-	ns	
42	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	10	-	10	-	ns	
43	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	40	-	40	-	ns	
44	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	ns	
45	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ iinitilization cycles nstead of 8 $\overline{RAS}$-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
3. Refer to the HY514400 and HY531000 data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

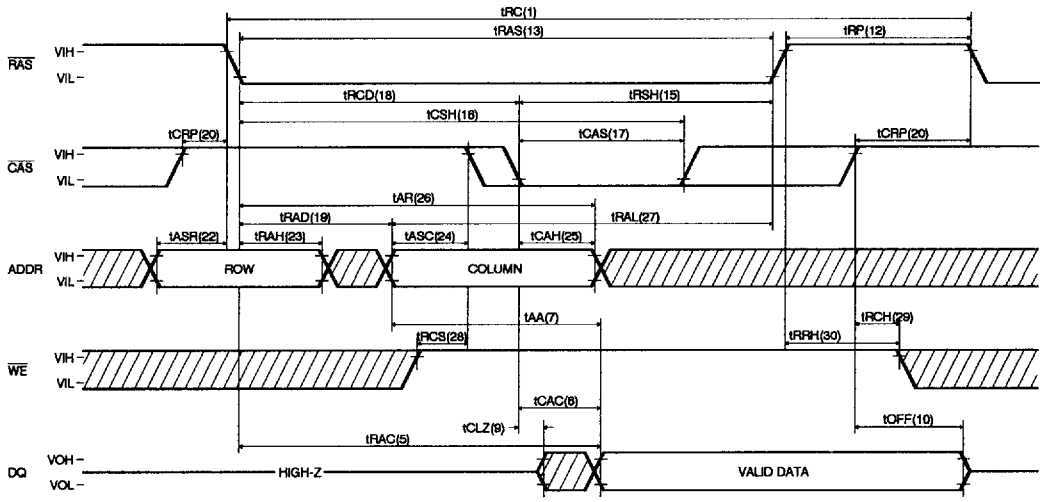
CAPACITANCE

(T_A=25°C, V_{CC}=5V±10%, V_{SS}=0V, f=1MHz, unless otherwise noted.)

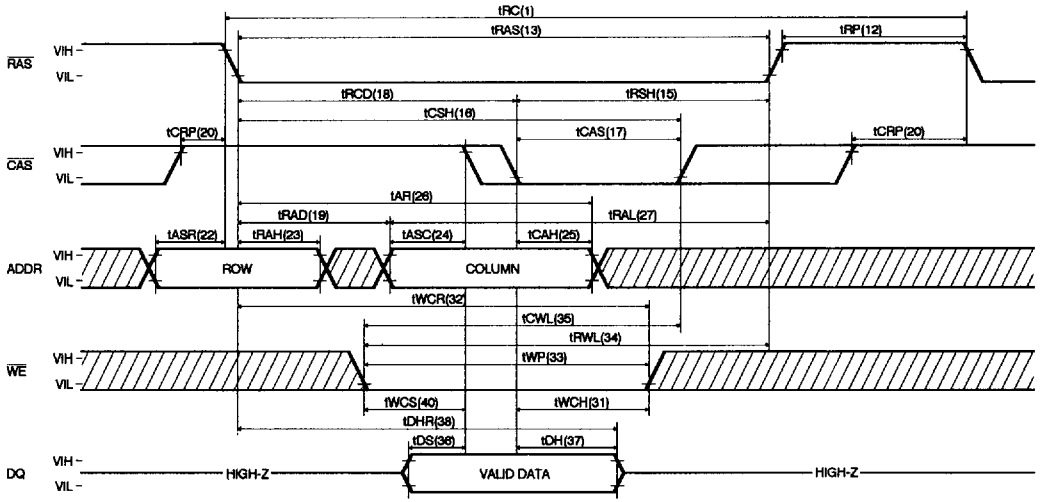
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A9)	-	88	pF
C_{IN2}	Input Capacitance ($\overline{WE}$)	-	104	pF
C_{IN3}	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	-	57	pF
C_{IN4}	Input Capacitance ($\overline{CAS0}$-$\overline{CAS3}$)	-	36	pF
C_{DQ1}	I/O Capacitance (DQ0-DQ7, DQ9-16, DQ18-25, DQ27-34)	-	17	pF
C_{DQ2}	I/O Capacitance (DQ8, DQ17, DQ26, DQ35)	-	22	pF

TIMING DIAGRAM

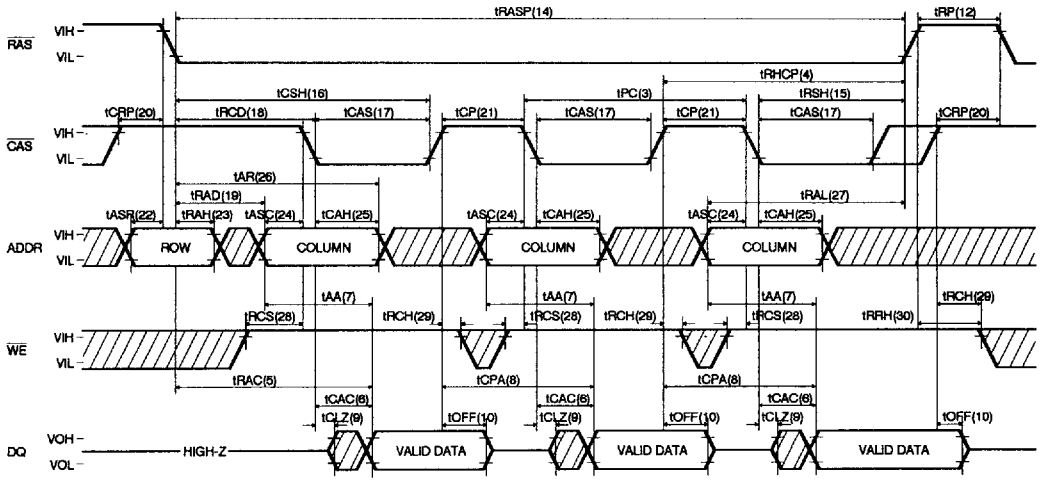
READ CYCLE



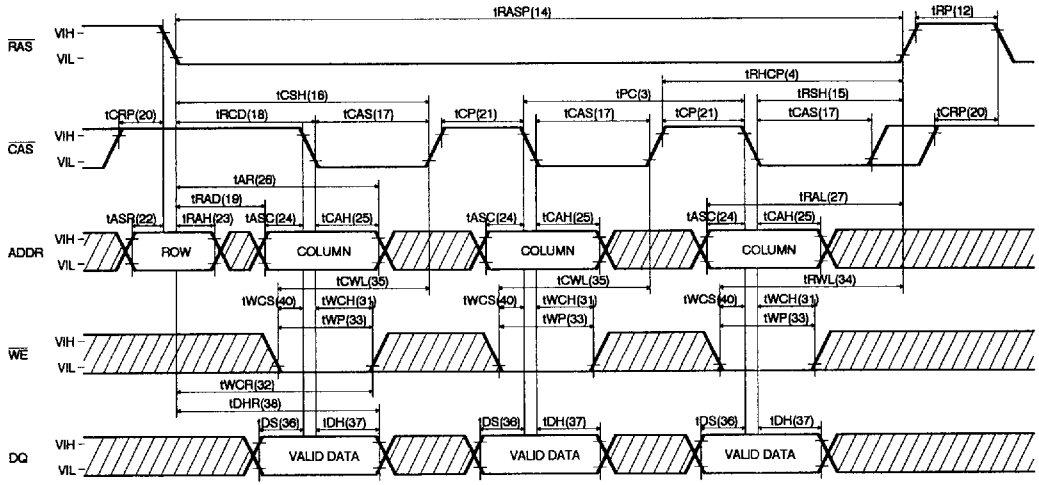
EARLY WRITE CYCLE



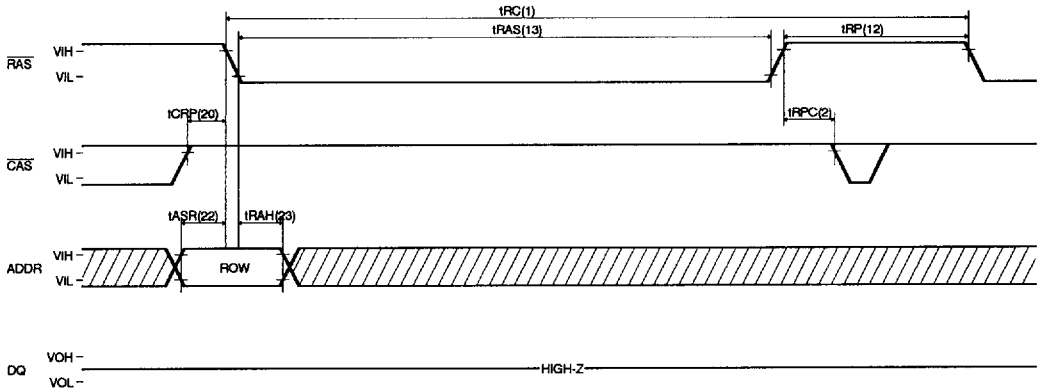
FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE

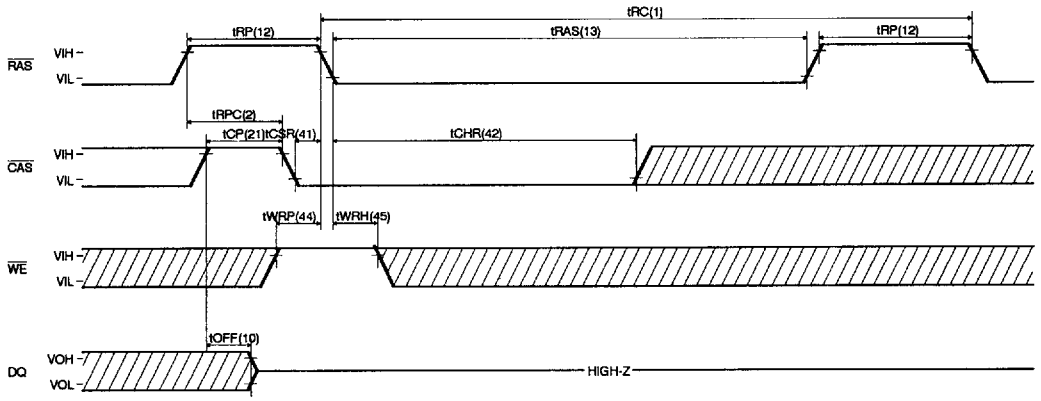


$\overline{RAS}$-ONLY REFRESH CYCLE



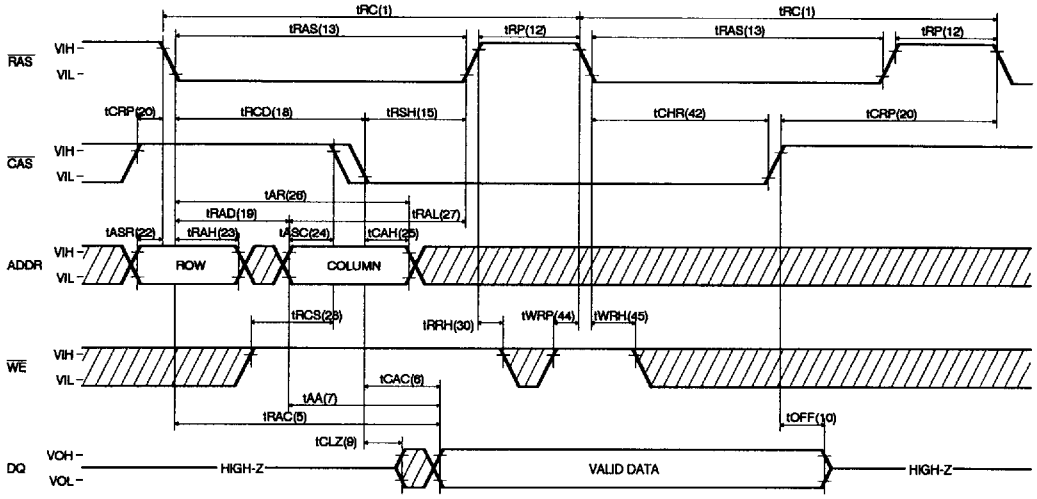
NOTE : $\overline{WE}$ = "H" or "L"

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

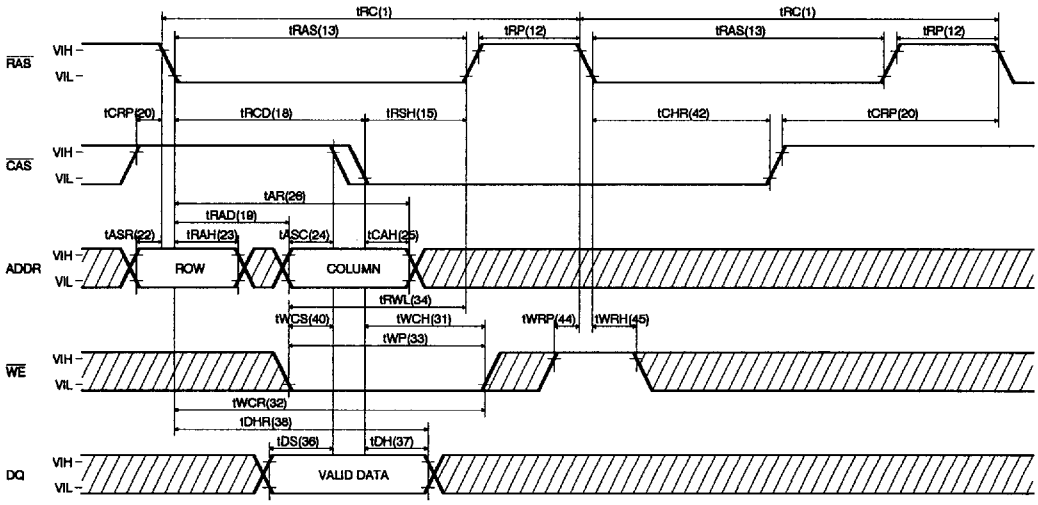


NOTE : ADDR = "H" or "L"

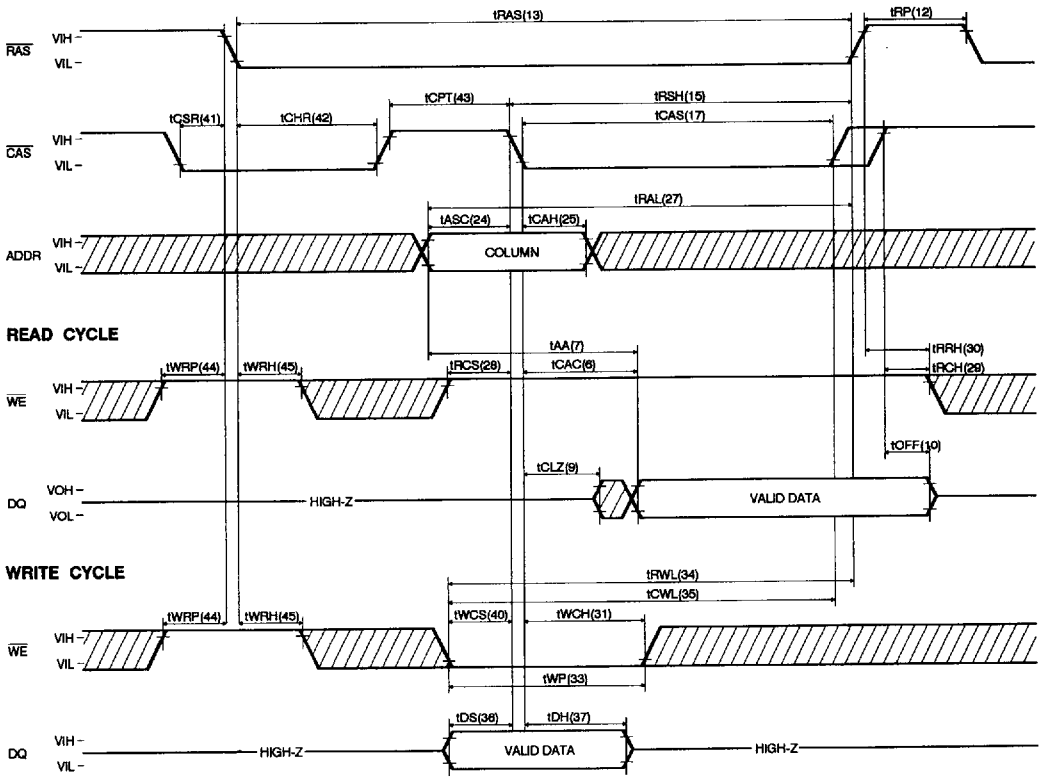
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

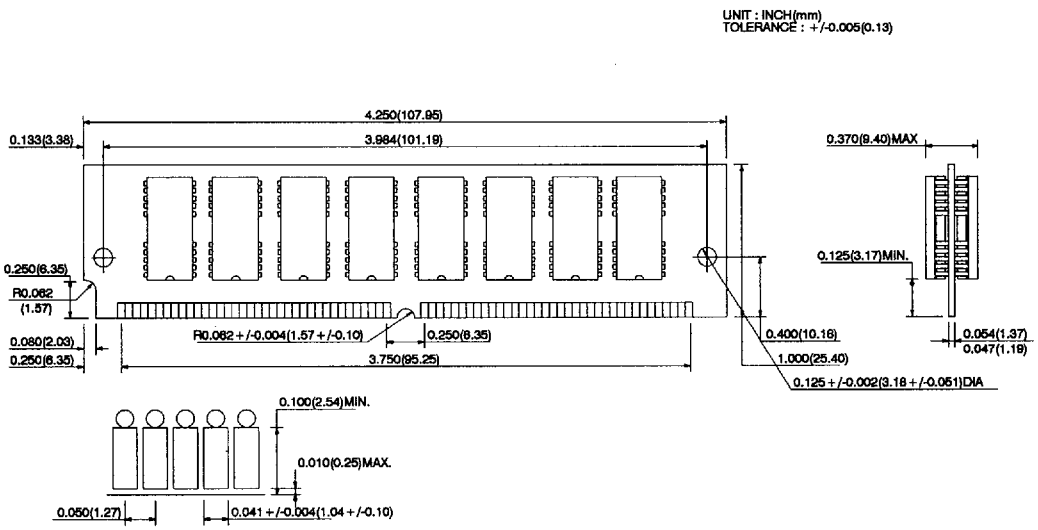


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE INFORMATION

72 pin Single In-line Memory Module (M ; Tin-Lead plated, MG ; Gold plated)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM536100M	70/80		SIMM	Tin-Lead
HYM536100MG	70/80		SIMM	Gold