

DESCRIPTION

The HYM536400 is a 4M x 36-bit Fast page mode CMOS DRAM module consisting of thirty six HY514100 in 20/26 pin SOJ on a 72 pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM. The HYM536400M is a Tin-Lead plated and HYM536400MG is a Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 16M byte memory.

FEATURES

- Low power dissipation
Max. CMOS standby 198mW
Max. TTL standby 398mW
Max. operating

Speed	Power
70	17.82W
80	15.84W

- Single power supply of 5V $\pm$ 10%
- TTL compatible inputs and outputs
- Fast access time

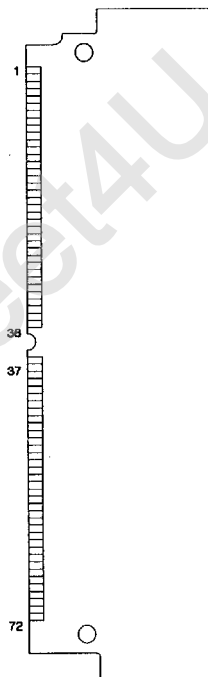
Speed	tRAC	tCAC	tPC
70	70ns	20ns	50ns
80	80ns	25ns	50ns

- Fast page mode operation
- CAS-before-RAS, RAS-only, Hidden refresh
- 1024 refresh cycles / 16ms

PIN DESCRIPTION

RAS0, RAS2	Row Address Strobe
CAS0-CAS3	Column Address Strobe
WE	Write Enable
A0-A10	Address Input
DQ0-DQ35	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+5V)
Vss	Ground

PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to Vss	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
Pd	Power Dissipation	22.68	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC + 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
I _{LI}	Input Leakage Current (Any Input Pin)	VSS ≤ VIN ≤ VCC + 1.0, All other pins not under test = VSS		-360	360	μA	
I _{LO}	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC, RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	trC = trC (min.)	70 80	-	3240 2880	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	72	mA	
ICC3	VCC Supply Current, RAS-only refresh	trC = trC (min.)	70 80	-	3240 2880	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tpC = tpC (min.)	70 80	-	2520 2160	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC - 0.2V		-	36	mA	
ICC6	VCC Supply Current, CAS-before-RAS refresh	trC = trC (min.)	70 80	-	3240 2880	mA	1,3
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS = VIL and CAS = VIH.

AC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM536400M/MG				UNIT	NOTE
			-70		-80			
			MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	130	-	150	-	ns	
2	tRPC	RAS to CAS Precharge Time	0	-	0	-	ns	
3	tPC	Fast Page Mode Cycle Time	50	-	50	-	ns	
4	tRHCP	RAS Hold Time from CAS Precharge	40	-	45	-	ns	
5	tRAC	Access Time from RAS	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	20	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	45	-	45	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	70	200K	80	200K	ns	
15	tRSH	RAS Hold Time	20	-	25	-	ns	
16	tCSH	CAS Hold Time	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	20	10K	25	10K	ns	
18	tRCD	RAS to CAS Delay	20	50	20	55	ns	9
19	tRAD	RAS to Column Address Delay Time	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	20	-	25	-	ns	
35	tCWL	Write Command to CAS Lead Time	20	-	25	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	55	-	60	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	ms	
40	tWCS	Write Command Set-up Time	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM536400M/MG				UNIT	NOTE
			-70		-80			
			MIN.	MAX.	MIN.	MAX.		
41	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	ns	
42	tCHR	CAS Hold Time (CBR Cycle)	30	-	30	-	ns	
43	tCPT	CAS Precharge Time (CBR Counter Test)	40	-	40	-	ns	
44	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	ns	
45	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
3. Refer to the HY514100 data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .

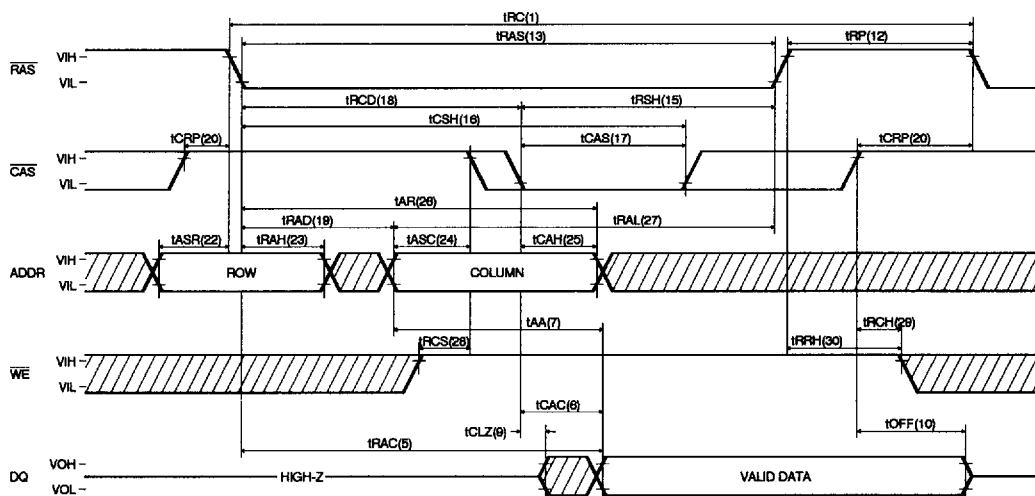
CAPACITANCE

(TA = 25°C, VCC = 5V $\pm$ 10%, VSS = 0V, f = 1MHz, unless otherwise noted.)

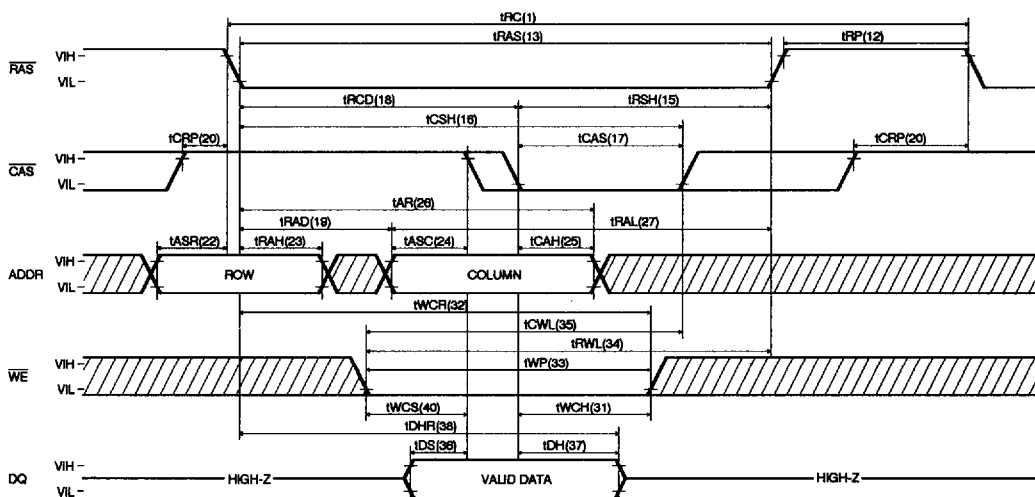
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A10, WE)	-	240	pF
CIN2	Input Capacitance (RAS0, RAS2)	-	100	pF
CIN3	Input Capacitance (CAS0-CAS3)	-	68	pF
CDO	Data Input/Output Capacitance (DQ0-DQ35)	-	35	pF

TIMING DIAGRAM

READ CYCLE



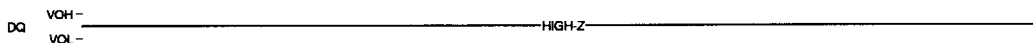
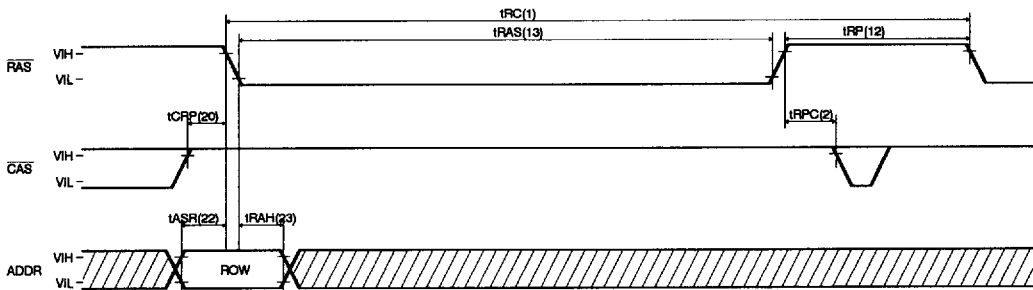
EARLY WRITE CYCLE



The timing diagram illustrates the relationship between the RAS, CAS, ADDR, WE, and DQ signals. The signals are shown as digital waveforms with specific timing parameters indicated by arrows and labels. The parameters include:

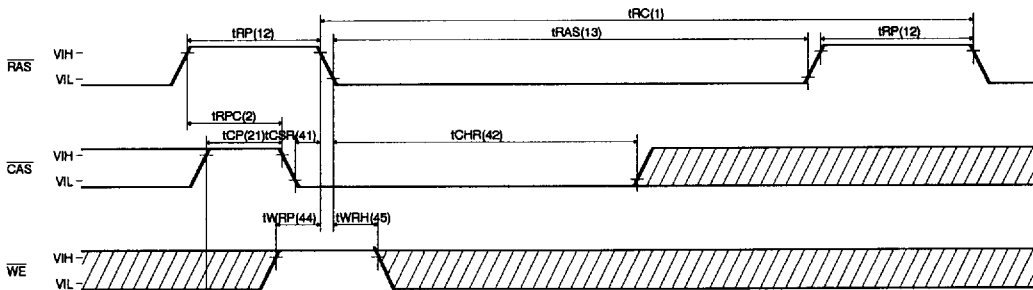
- RAS:** $t_{RASP}(14)$ (RAS pulse width), $t_{RHP}(4)$ (RAS hold time), $t_{RSH}(15)$ (RAS setup time), $t_{RCP}(4)$ (RAS capture time).
- CAS:** $t_{CSP}(20)$ (CAS pulse width), $t_{CSD}(18)$ (CAS setup time), $t_{CAS}(17)$ (CAS pulse width), $t_{CP}(21)$ (CAS capture time), $t_{CASH}(17)$ (CAS hold time), $t_{CIP}(21)$ (CAS capture time), $t_{CASH}(17)$ (CAS hold time), $t_{CRP}(20)$ (CAS capture time).
- ADDR:** $t_{ASHP}(22)$ (Address setup time), $t_{RAD}(19)$ (Address read delay), $t_{RAH}(23)$ (Address read hold time), $t_{CAH}(25)$ (Column address hold time), $t_{ASC}(24)$ (Address setup time), $t_{CAH}(25)$ (Column address hold time), $t_{ASC}(24)$ (Address setup time), $t_{CAH}(25)$ (Column address hold time), $t_{RAL}(27)$ (Row address latch time).
- WE:** $t_{RCS}(28)$ (Row control setup time), $t_{AA}(7)$ (Address to data delay), $t_{RCH}(29)$ (Row control hold time), $t_{RCS}(28)$ (Row control setup time), $t_{RCH}(29)$ (Row control hold time), $t_{RCS}(28)$ (Row control setup time), $t_{RCH}(29)$ (Row control hold time), $t_{RRH}(30)$ (Row control hold time), $t_{RCH}(29)$ (Row control hold time).
- DQ:** $t_{FAC}(5)$ (Data access time), $t_{CAC}(8)$ (Data capture time), $t_{CLZ}(8)$ (Data capture time), $t_{OFF}(10)$ (Data output delay), $t_{CAC}(8)$ (Data capture time), $t_{CLZ}(8)$ (Data capture time), $t_{OFF}(10)$ (Data output delay), $t_{CAC}(8)$ (Data capture time), $t_{CLZ}(8)$ (Data capture time), $t_{OFF}(10)$ (Data output delay), $t_{OFF}(10)$ (Data output delay).

RAS-ONLY REFRESH CYCLE



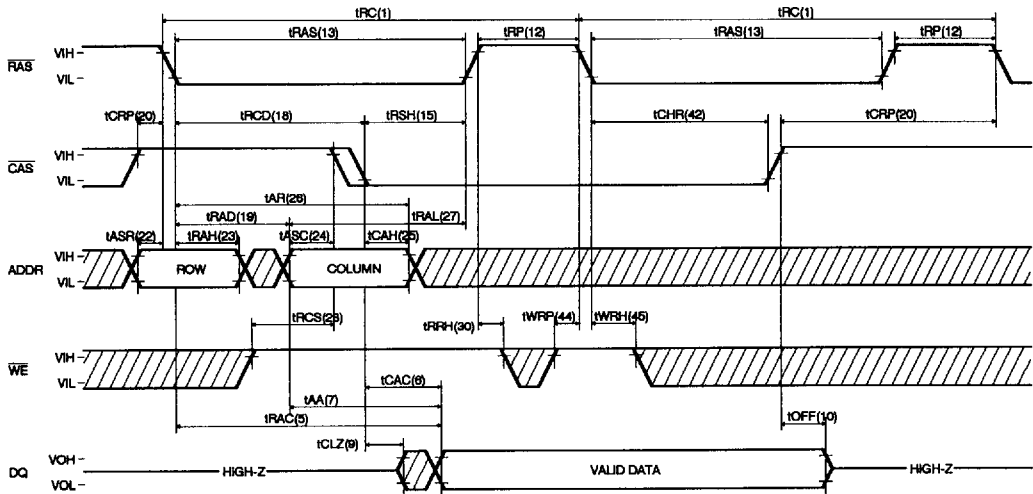
NOTE : WE = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

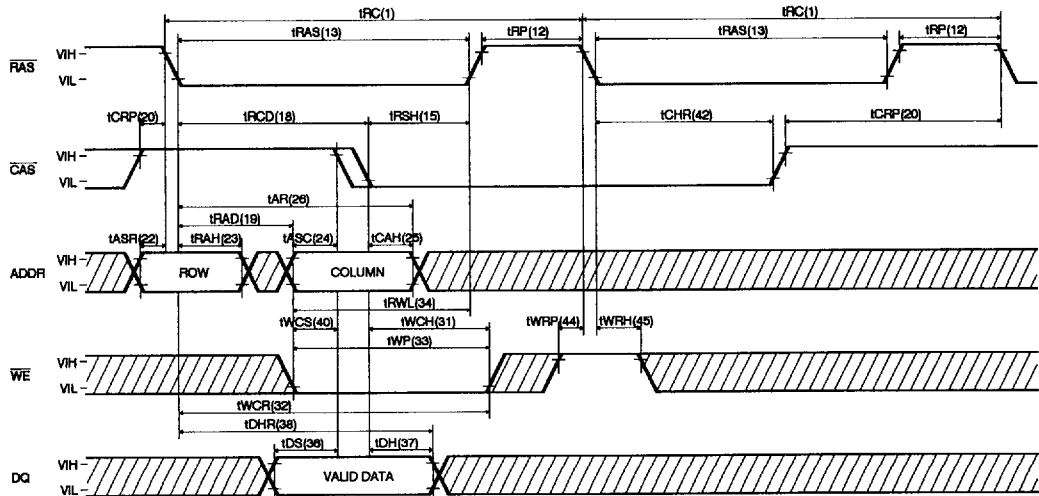


NOTE : ADDR = "H" or "L"

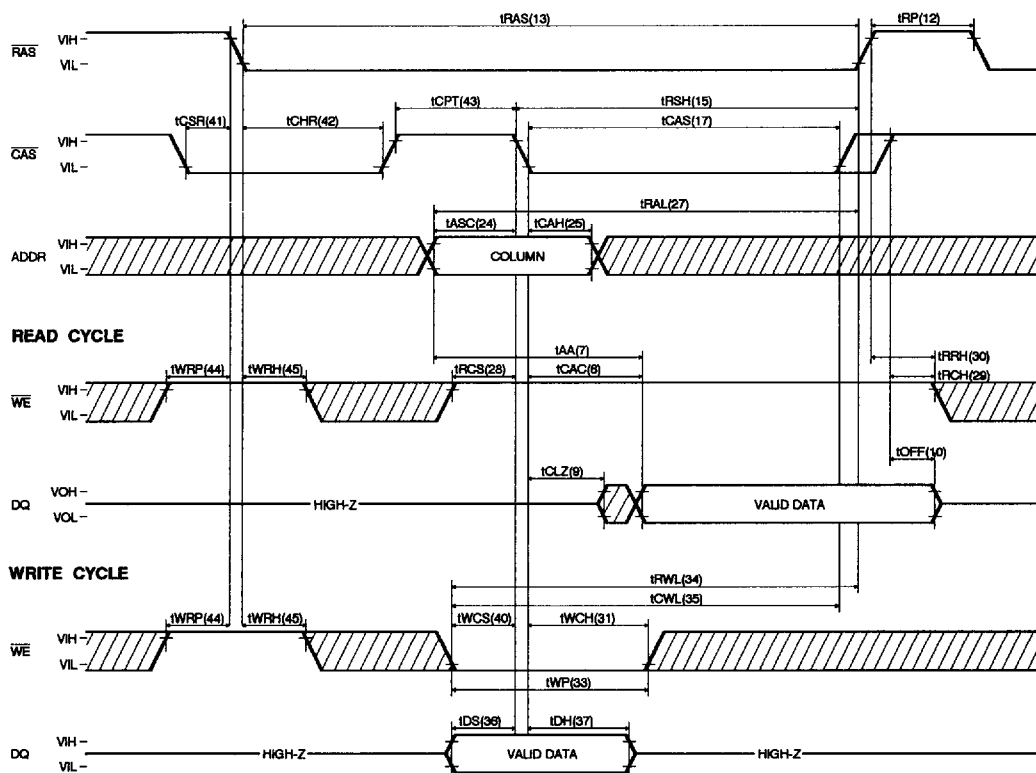
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

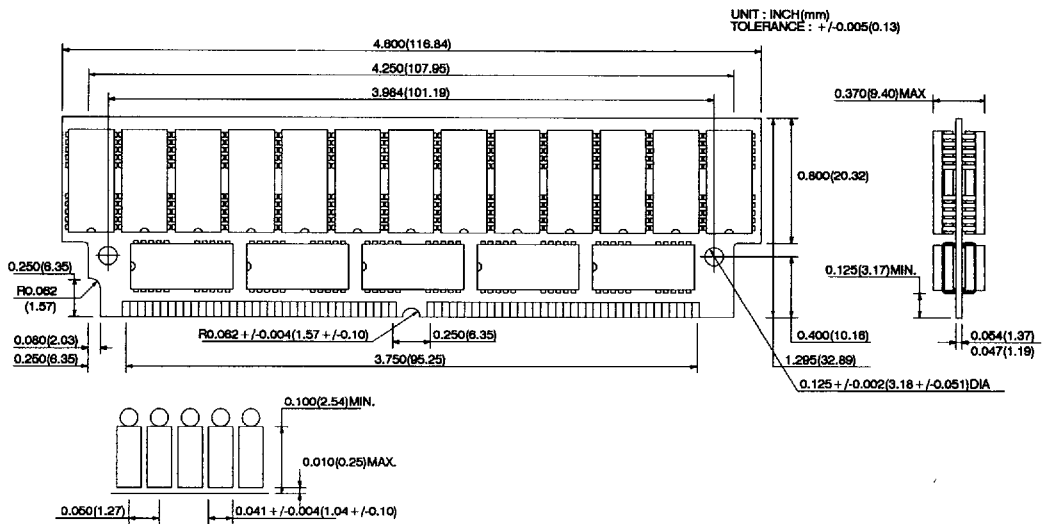


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE INFORMATION

72 pin Single In-line Memory Module (M ; Tin-Lead plated, MG ; Gold plated)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM536400M	70/80		SIMM	Tin-Lead
HYM536400MG	70/80		SIMM	Gold