HYM536A414A M-Series

4M x 36-bit CMOS DRAM MODULE with EXTENDED DATA OUT

DESCRIPTION

The HYM536A414A is a 4M x 36-bit EDO mode CMOS DRAM module consisting of nine HY5117404A in 24/26 pin SOJ on a 72 pin glass-epoxy printed circuit board. 0.1μF and 0.01μF decoupling capacitors are mounted for each DRAM.

The HYM536A414AM/ASLM are Tin-Lead plated and HYM536A414AMG/ASLMG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 16M byte memory.

FEATURES

- **Low power dissipation**
  Max. self-refresh 14.85mW (SL-part)
  Max. battery back-up 29.7mW (SL-part)
  Max. CMOS standby 19.8mW (SL-part)
  49.5mW
  Max. TTL standby 99.0mW
  Max. operating

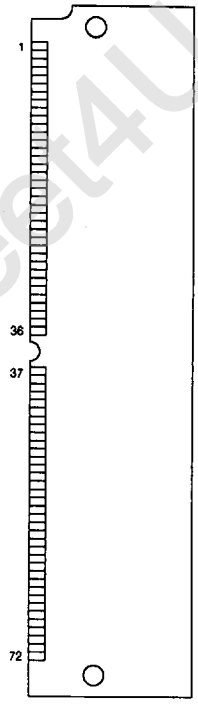
Speed	Power
60	5.94W
70	4.95W
80	4.45W

- **Single power supply of 5V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	tRAC	tCAC	tHPC
60	60ns	15ns	25ns
70	70ns	20ns	30ns
80	80ns	20ns	35ns

- **EDO mode operation**
- **CAS-before-RAS, RAS-only, Hidden refresh and Self-refresh**
- **2048 refresh cycles / 256ms (SL-part)**
  2048 refresh cycles / 32ms
- **1st and 2nd generation JEDEC standard compatible**

PIN CONNECTION



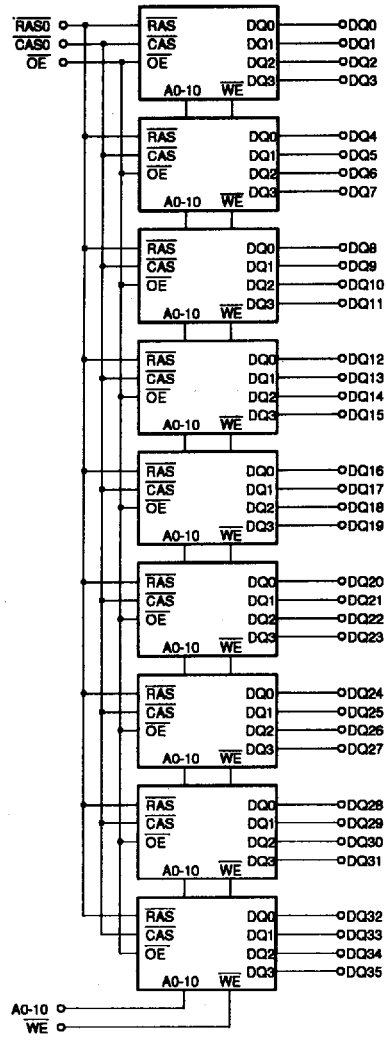
PIN DESCRIPTION

$\overline{RAS0}$	Row Address Strobe
$\overline{CAS0}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A10	Address Input
DQ0-DQ35	Data Input/Output
PD1-PD5	Presence Detect
Vcc	Power (+ 5V)
Vss	Ground

PIN NAME

#	NAME	#	NAME
1	Vss	37	DQ19
2	DQ0	38	DQ20
3	DQ1	39	Vss
4	DQ2	40	$\overline{CAS0}$
5	DQ3	41	A10
6	DQ4	42	NC
7	DQ5	43	NC
8	DQ6	44	$\overline{RAS0}$
9	DQ7	45	NC
10	Vcc	46	DQ21
11	PD5	47	$\overline{WE}$
12	A0	48	Vss
13	A1	49	DQ22
14	A2	50	DQ23
15	A3	51	DQ24
16	A4	52	DQ25
17	A5	53	DQ26
18	A6	54	DQ27
19	$\overline{OE}$	55	DQ28
20	DQ8	56	DQ29
21	DQ9	57	DQ30
22	DQ10	58	DQ31
23	DQ11	59	Vcc
24	DQ12	60	DQ32
25	DQ13	61	DQ33
26	DQ14	62	DQ34
27	DQ15	63	DQ35
28	A7	64	NC
29	DQ16	65	NC
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	NC	70	PD4
35	DQ17	71	NC
36	DQ18	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PIN

PIN	-60	-70	-80
PD1	Vss	Vss	Vss
PD2	NC	NC	NC
PD3	NC	Vss	NC
PD4	NC	NC	Vss
PD5	Vss	Vss	Vss

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 125	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to Vss	–1.0 to 7.0	V
V_{CC}	Voltage on Vcc Relative to Vss	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	9	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	Vcc+ 1.0	V
V_{IL}	Input Low Voltage	–1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 5V± 10%, V_{SS}= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \le V_{IN} \le V_{CC}$+ 1.0, All other pins not under test= V_{SS}		-90	90	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	V_{CC} Supply Current, Operating	t_{RC}= t_{RC} (min.)	60 70 80	- - -	1080 900 810	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs≥ V_{SS}		-	18	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	t_{RC}= t_{RC} (min.)	60 70 80	- - -	1080 900 810	mA	1,3
I_{CC4}	V_{CC} Supply Current, EDO mode	t_{HPC}= t_{HPC} (min.)	60 70 80	- - -	900 810 640	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ V_{CC}–0.2V	 SL-part	- -	9 3.6	mA	 5
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}= t_{RC} (min.)	60 70 80	- - -	1080 900 810	mA	1,3
I_{CC7}	V_{CC} Supply Current, Battery Back Up (SL-part only)	t_{RC}= 62.5µs, $\overline{CAS}$= CBR cycling or 0.2V, $\overline{WE}$= V_{CC}–0.2V, A0-A10= V_{CC}–0.2V or 0.2V, DQ0-DQ35= V_{CC}–0.2V, 0.2V, or open	$t_{RAS} \le$ 300ns	-	3.6	mA	1,4,5
			$t_{RAS} \le$ 1µs	-	5.4		
I_{CC8}	V_{CC} Supply Current Self Refresh (SL-part only)	$\overline{RAS}$ & $\overline{CAS}$= V_{IL}, $\overline{OE}$ & $\overline{WE}$ & A0-A10= Vcc-0.2V or 0.2V, DQ0-DQ35= Vcc - 0.2V, 0.2V or open			2.7	mA	5
V_{OL}	Output Low Voltage	I_{OL}= 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= –5mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on output loading. Specified values are obtained with the output open.
3. I_{CC1} is specified as average current. for I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum two times while $\overline{RAS}$= V_{IL}. for I_{CC4}, address can be changed maximum once while $\overline{CAS}$= V_{IH}.
4. Only t_{RAS}(max.)= 1µs is applied to refresh of battery backup but t_{RAS}(max.)= 10µs is applied to normal functional operation.
5. I_{CC5}(max.)= 3.6mA , I_{CC7} and I_{CC8} are applied to SL-part only (HYM536A414ASLM/ASLMG).

AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM536A414A M-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	160	-	180	-	200	-	ns	
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	85	-	90	-	100	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	18	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	4
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (EDO Mode)	60	125K	70	125K	80	125K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	15	-	18	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	40	-	50	-	60	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	12	10K	15	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	50	20	60	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	30	17	40	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	8	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	12	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	15	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	50	-	55	-	60	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	10	-	15	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	45	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	15	-	18	-	20	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	15	-	18	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	13	-	13	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		SL-part	-	256	-	256	-	256	ms	12
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM536A414A M-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	38	-	43	-	45	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	-	95	-	105	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	53	-	60	-	65	-	ns	8
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	0	-	0	-	0	-	ns	
49	tOEA	$\overline{OE}$ Access Time	-	15	-	18	-	20	ns	
50	tOED	$\overline{OE}$ to Data Delay	15	-	15	-	15	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	15	0	15	0	15	ns	5
52	tOEH	$\overline{OE}$ Command Hold Time	10	-	10	-	10	-	ns	
53	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	60	-	65	-	70	-	ns	8
54	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
55	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tRASS	$\overline{RAS}$ Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	µs	
58	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh Cycle)	110	-	130	-	150		ns	
59	tCHS	$\overline{CAS}$ Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
60	tDOH	Output Data Hold Time	3	-	3	-	3	-	ns	
61	tREZ	Output Buffer Turn-off Delay ($\overline{RAS}$)	-	15	-	15	-	15	ns	5,15
62	tWEZ	Output Buffer Turn-off Delay ($\overline{WE}$)	-	15	-	15	-	15	ns	5
63	tWPE	$\overline{WE}$ Pulse Width for Output Disable	10	-	10	-	10	-	ns	
64	tOEP	$\overline{OE}$ Pulse Width for Output Disable	10	-	10	-	10	-	ns	
65	tOCH	$\overline{OE}$ Low to $\overline{CAS}$ High Delay Time	0	-	0	-	0	-	ns	
66	tCHO	$\overline{CAS}$ High to $\overline{OE}$ High Hold Time	10	-	10	-	10	-	ns	
67	tWED	$\overline{WE}$ to Data Delay Time	15	-	15	-	15	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initilization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If $\overline{RAS}$= Vss during power-up, the HYM536A414A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. Refer to the HY5117404A data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF. (V_{OH}= 2.0V, V_{OL}= 0.8V)
5. tCEZ(max.) tOEZ(MAX), tREZ(MAX) and tWEZ(MAX) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in late write or read-modify-write cycles.
8. twcs is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twcs≥ twcs(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. Measured with the specified current load and 100pF.
12. A burst of 2048 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 32ms after exiting self refresh (for SL-part).
13. If tCWD ≥ tWCS(MIN.), tRWD ≥ tRWD(MIN.), tAWD ≥ tAWD(MIN.) and tCPWD ≥ tCPWD(MIN.), the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{CAS}$ goes bach to VIH) is indeterminated.
14. In $\overline{CAS}$ before $\overline{RAS}$ self refresh mode.
    In case of using distributed $\overline{CAS}$ before $\overline{RAS}$ refresh, refresh 2048 times during a 256ms after reset
    In case of using burst $\overline{CAS}$ before $\overline{RAS}$ refresh, refresh 2048 times during a 32ms after reset
    Incase of use $\overline{RAS}$ only refresh, refresh against all refresh address during a 32ms after reset
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

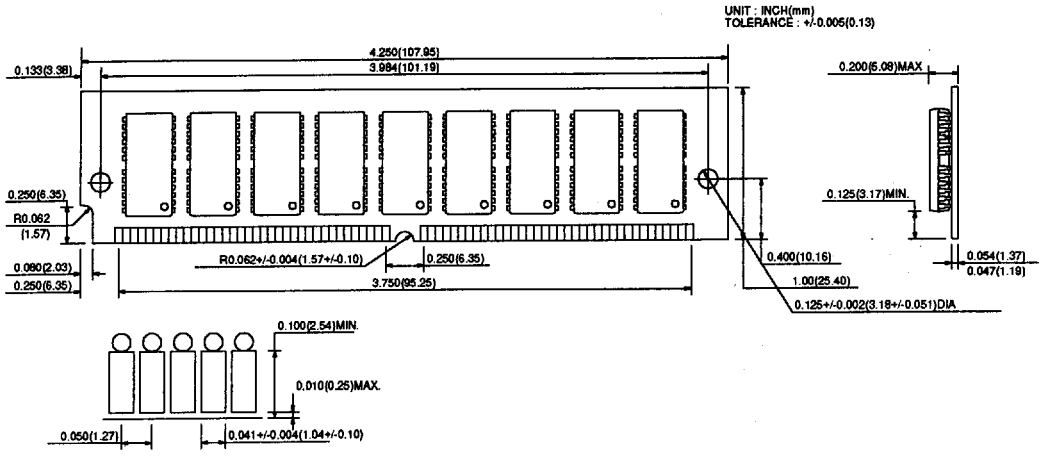
CAPACITANCE

(T_A= 25°C, V_{CC}= 5V± 10%, V_{SS}= 0V, f= 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A10)	-	65	pF
CIN2	Input Capacitance ($\overline{WE}$, $\overline{OE}$)	-	80	pF
CIN3	Input Capacitance ($\overline{RAS0}$)	-	80	pF
CIN4	Input Capacitance ($\overline{CAS0}$)	-	80	pF
CDQ	Data Input/output Capacitance (DQ0-DQ35)	-	17	pF

PACKAGE INFORMATION

72 pin Single In-line Memory Module (M ; Tin-Lead plated, MG ; Gold plated)
HYM536A414A/ASL (SOJ Mounted)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM536A414AM	60/70/80		SIMM	Tin-Lead
HYM536A414ASLM	60/70/80	SL-part	SIMM	Tin-Lead
HYM536A414AMG	60/70/80		SIMM	Gold
HYM536A414ASLMG	60/70/80	SL-part	SIMM	Gold