Features

- Provides Year, Month, Day, Weekday, Hours, Minutes and Seconds Information
- Century Flag
- Wide Operating Voltage: 1.8V to 5.5V
- Low Power Consumption: 0.25μA at V_{DD} = 3.0 V
- I^2C-bus Interface
- Programmable Clock Output (32.768 kHz, 1024 Hz, 32 Hz and 1 Hz)
- Alarm and Timer Functions
- Built-in Power Voltage Detecting Circuit
- I^2C -bus Slave Address: Read A3H and Write A2H
- Open-Drain Interrupt Pin

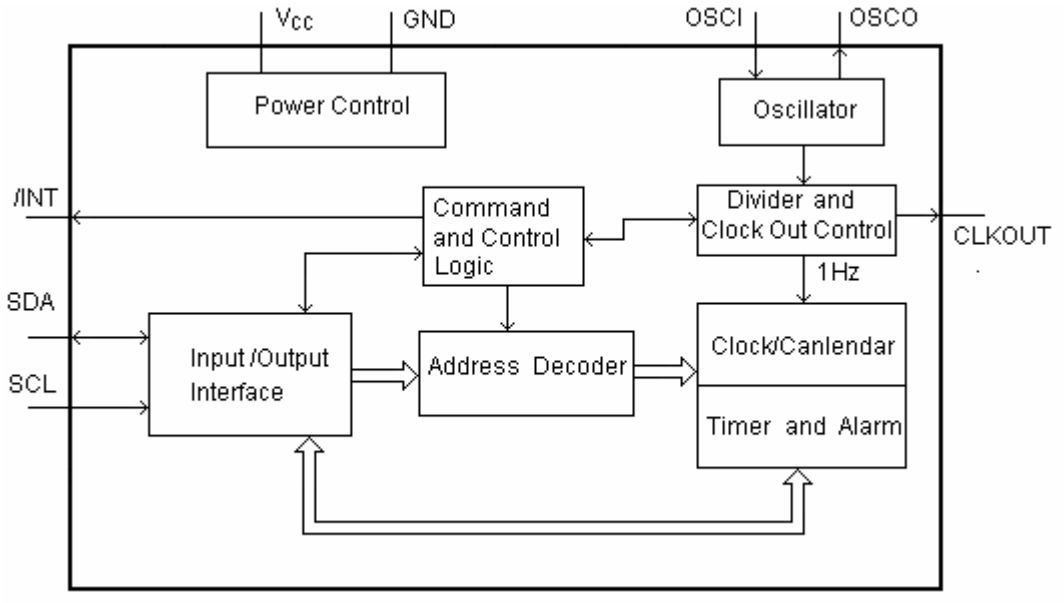
Applications

- Cash Register
- Security Access Controller, Door Controller
- Time Recorder
- Mobile Telephones
- Public Phone Bill Meter, Smart Card Payphone
- MP3/MP4 Player
- IC Water-Flow Meter, IC Gas Meter

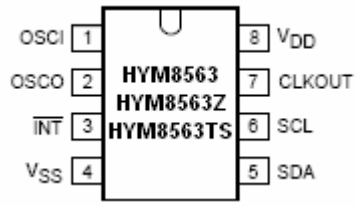
General Description

The HYM8563 is a CMOS real time clock/calendar, which provides seconds, minutes, hours, day, date, month, and year information. The number of days in each month and leap years are automatically adjusted. The clock can operate in two modes: one is the 12-hour mode with an AM/PM indicator，the other is the 24-hour mode. The clock/calendar is full binary-coded decimal (BCD). In addition, the HYM8563 contains a programmable clock output, a timer, an alarm, a voltage-low detector. All address and data are transferred serially via I^2C bus and The HYM8563 operates as a slave device on the serial bus. The built-in word address register is incremented automatically after each written or read data byte. The HYM8563 is designed to operate on very low power consumption.

Block Diagram



Pin Assignment



Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	-0.5	+6.5	V
Supply Current	I_{DD}	-0.5	+50	mA
Input Voltage on pins SCL and SDA	V_I	-0.5	+6.5	V
Input Voltage on pin OSCI		-0.5	V_{DD}+0.5	V
Output Voltage on CLKOUT and $\overline{INT}$	V_O	-0.5	+6.5	V
DC input current at any input	I_I	-10	+10	mA
DC output current at any output	I_O	-10	+10	mA
Total power dissipation	P		300	mW
Ambient temperature	T_A	-40	+85	^{O}C
Storage temperature	T_S	-65	+150	^{O}C

Electricity characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	I^2C-bus inactive; T_A = 25ºC	1.0[1]		5.5	V
Supply voltage for clock data integrity		I^2C-bus active; f_{SCL} = 400 kHz	1.8[1]		5.5	V
		T_A = 25ºC	V_{low}		5.5	V
Supply current1(interface active)	I_{DD1}	f_{SCL} = 400 kHz			800	A
		f_{SCL} = 100 kHz			200	A
Supply current2(interface inactive) CLKOUT disabled	I_{DD2}	f_{SCL} = 0 Hz, T_A = 25ºC[2]				
		V_{DD} = 5.0 V		275	550	nA
		V_{DD} = 3.0 V		250	500	nA
		V_{DD} = 2.0 V		225	450	nA
		f_{SCL} = 0 Hz, T_A = -40 ～+85ºC[2]				
		V_{DD} = 5.0 V		500	750	nA
		V_{DD} = 3.0 V		400	650	nA
		V_{DD} = 2.0 V		400	600	nA
Supply current3(interface inactive) CLKOUT enabled at 32kHz	I_{DD3}	f_{SCL} = 0 Hz, T_A = 25ºC[2]				
		V_{DD} = 5.0 V		825	1600	nA
		V_{DD} = 3.0 V		550	1000	nA
		V_{DD} = 2.0 V		425	800	nA
		f_{SCL} = 0 Hz, T_A = -40 ～+85ºC[2]				
		V_{DD} = 5.0 V		950	1700	nA

		V_{DD} = 3.0 V		650	1100	nA
		V_{DD} = 2.0 V		500	900	nA
LOW-level input voltage	V_{IL}		V_{SS}		0.3 V_{DD}	V
HIGH-level input voltage	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input leakage current	I_{LI}	V_I= V_{DD} or V_{SS}	-1	0	+1	A
Input capacitance	C_I	[3]			7	pF
SDA LOW-level output current	I_{OLS}	V_{OL} = 0.4 V; V_{DD} = 5 V	-3			mA
$\overline{INT}$ LOW-level output current	I_{OLI}	V_{OL} = 0.4 V; V_{DD} = 5 V	-1			mA
CLKOUT LOW-level output current	I_{OLC}	V_{OL} = 0.4 V; V_{DD} = 5 V	-1			mA
CLKOUT HIGH-level output current	I_{OHC}	V_{OH} = 4.6 V; V_{DD} = 5 V	-1			mA
Output leakage current	I_{LO}	V_O = V_{DD} or V_{SS}	-1	0	+1	A
Low voltage detection	V_{low}	T_A = 25ºC		0.9	1.0	V

Note: [1] For reliable oscillator start-up at power-up: V_{DD}(min, power-up) = V_{DD}(min) + 0.3 V.

[2] Timer source clock = 1/60 Hz, level of pins SCL and SDA is V_{DD}

[3] Tested on sample basis.

Alternating Characteristics

(V_{DD}=1.8 to 5.5V, V_{SS}=0V; T_A=-40 to +85ºC; f_{osc}=32.768kHz; quartz RS=40kΩ, C_L=8pF; unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
oscillator						
integrated load capacitance	$C_{\overline{INT}}$		15	25	35	pF
oscillator stability	$D_{fosc/fosc}$			$2*10^{-7}$		
Quartz crystal parameters(f=32.768 kHz)						
series resistance	Rs				40	kΩ
parallel load capacitance	C_L			10		pF
trimmer capacitance	C_T		5		25	pF
CLKOUT output						
CLKOUT duty cycle	δ_{CLKOUT}	[1]		50		%
I^2C-bus timing characteristics[2]						
SCL clock frequency	f_{SCL}	[3]			400	kHz
START condition hold time	$t_{HD;STA}$		0.6			µs
set-up time for a repeated START condition	$t_{SU;STA}$		0.6			µs

SCL LOW time	t_{LOW}		1.3			µs
SCL HIGH time	t_{HIGH}		0.6			
SCL and SDA rise time	t_r				0.3	µs
SCL and SDA fall time	t_f				0.3	µs
capacitive bus line load	Cb				400	pF
data set-up time	$t_{SU;DAT}$		100			ns
data hold time	$t_{HD;DAT}$		0			ns
set-up time for STOP condition	$t_{SU;STO}$		4.0			µs
tolerable spike width on bus	t_{SW}				50	ns

Note: [1] Unspecified for f_{CLKOUT} = 32.768 kHz.

[2] All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

[3] I^2C-bus access time between two STARTS or between a START and a STOP condition to this device must be less than one second.

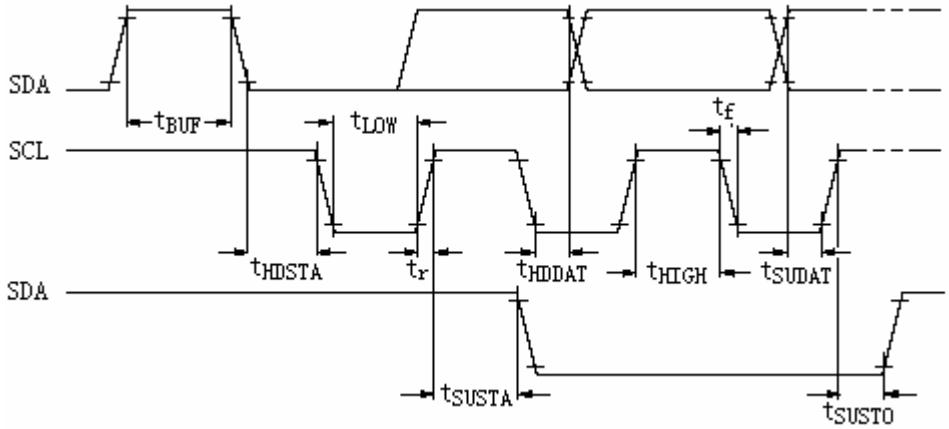


Figure1: I^2C-bus timing waveform

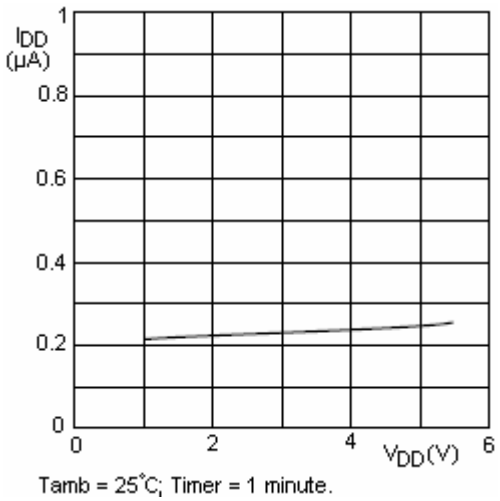


Figure 2: I_{DD} as a function of V_{DD}; CLKOUT disabled

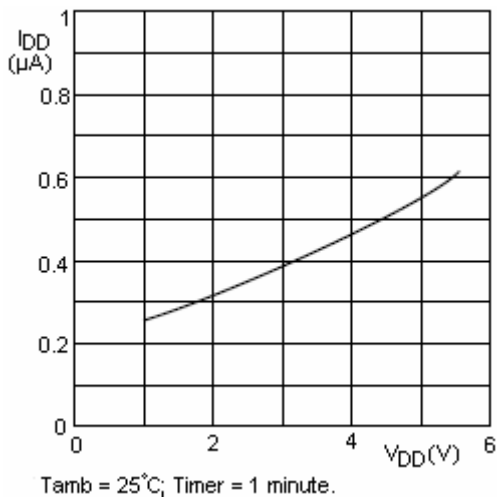


Figure 3: I_{DD} as a function of V_{DD}; CLKOUT = 32KHz

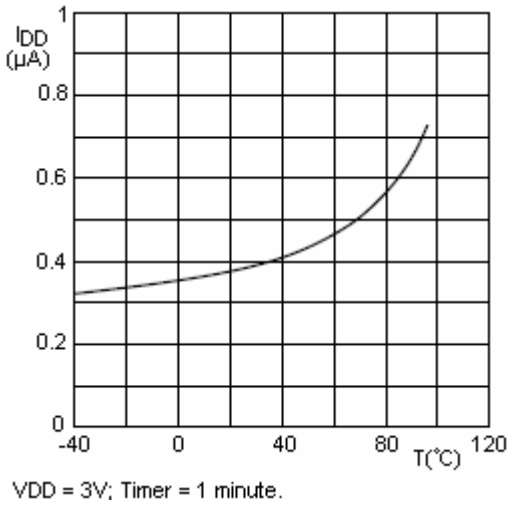


Figure 4: I_{DD} as a function of T; CLKOUT = 32KHz

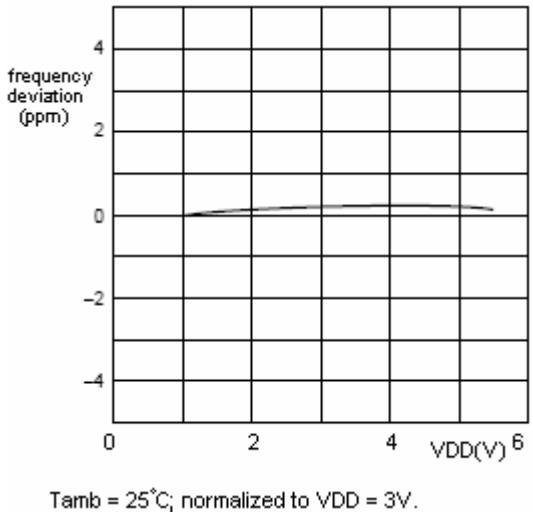


Figure 5: Frequency deviation as a function of V_{DD}

Application Information

Register Organization

The HYM8563 contains 16 registers with an auto-incrementing address register as shown on Table1.

Table 1.Registers Overview

Address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	Control/status1	TEST	0	STOP	0	TESTC	0	0	0
01H	Control/status2	0	0	0	TI/TP	AF	TF	AIE	TIE
02H	Seconds	VL	Seconds 00 to 59 coded in BCD						
03H	Minutes	-	Minutes 00to 59 coded in BCD						
04H	Hours	-	-	Hours 00 to 23 coded in BCD					
05H	Days	-	-	Days 01 to 31 coded in BCD					
06H	Weekdays	-	-	-	-	-	Weekdays 0 to 6		
07H	Months/century	C	-	-	Months 01 to 12 coded in BCD				
08H	Years	Years 00 to 99 coded in BCD							
09H	Minute alarm	AE	Minute alarm 00 to 59 coded in BCD						
0AH	Hour alarm	AE	-	Hour alarm 00 to 23 coded in BCD					
0BH	Date alarm	AE	-	Day alarm 01 to 31 coded in BCD					
0CH	Weekday alarm	AE	-	-	-	-	Weekday alarm 0 to 6		
0DH	CLKOUT control	FE	-	-	-	-	-	FD1	FD0
0EH	Timer control	TE	-	-	-	-	-	TD1	TD0
0FH	Timer countdown	Timer countdown value							

Note: Bit positions labeled as"-" are not implemented. Bit positions labeled with 0 should always be written with logic 0.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (00H and 01H) are used as control and status registers. Registers 02H to 08H are used as counters for clock function (seconds up to year's counters). Registers 09H through 0CH contain alarm

registers which define the conditions for an alarm. Register 0DH controls the CLKOUT output frequency. Registers 0EH and 0FH are the timer control and timer register, respectively. The seconds, minutes, hours, days, months, year as well as the minute alarm, hour alarm and day alarm registers are all coded in BCD format. Weekday and weekday alarm are not coded in BCD format.

Control/ Status 1 Register

The TEST and TESTC bits of Control/Status 1 register must be set to logic 0. When these bits are set to logic 1, the device enters test mode for manufacturer (see Table2).

Table 2. Control/Status 1 (address 00H) Register

Bit	Symbol	Description
7	TEST	TEST=0:normal mode; TEST=1: test mode for manufacturer
5	STOP	STOP=0:RTC clock runs; STOP=1:All RTC divider chain flip-flops are asynchronously set to logic 0,the RTC clock is stopped(CLKOUT at 32.768 kHz is still available)
3	TESTC	TESTC=0: normal operation; TESTC=1: test mode for manufacturer
6,4,2 to 0		Default value is logic 0

Control/ Status 2 Register

Bit TF and AF: When an alarm occurs, AF is set to logic 1.Similary, at the end of a timer countdown, TF is set to 1.These bits maintain their value until overwritten by software. If both timer and alarm interrupts are required in the application, the source of the interrupts can be determined by reading these bits. To prevent one flag being overwritten while clearing, another logic AND is performed during a write access.

Bit TIE and AIE: These bits activate the generation of an interrupt, when TF or AF is asserted. The interrupt is the logical OR.

Table 3 . Control/ Status 2 Register (address 01H) Register

Bit	Symbol	Description
7 to 5		Default value is logic 0
4	TI/TP	TI/TP=0: $\overline{\text{INT}}$ is active when TF is active (subject to the status of TIE) TI/TP=1: $\overline{\text{INT}}$ pulses active according to Table 5 (subject to the status of TIE); Note that if AF and AIE are active then $\overline{\text{INT}}$ will be permanently active
3	AF	AF=0: Reading, alarm flag inactive; Writing, alarm flag is cleared AF=1: Reading, alarm flag active; Writing, alarm flag remains unchanged
2	TF	TF=0: Reading, timer flag inactive; Writing, timer flag is cleared
		TF=1: Reading, timer flag active; Writing, timer flag remains unchanged
1	AIE	AIE=0: alarm interrupt disabled; AIE=1: alarm interrupt enabled
0	TIE	TIE=0: timer interrupt disabled; TIE=0: timer interrupt enabled

Table 4. $\overline{\text{INT}}$ Operation (Bit TI/TP=1)

Source clock(Hz)	$\overline{\text{INT}}$ [1] period	
	n[2]=1	n>1
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64

1/60	1/64	1/64

Note: [1]. TF and $\overline{\text{INT}}$ become simultaneously active.

[2]. n=loaded countdown value. Timer stopped when n=0.

Alarm Function

By clearing the MSB of one or more of the alarm registers (bit AE=alarm enable), the corresponding alarm condition will be active. When one or more of these alarm registers are loaded with a valid minute, hour, day or weekday, then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set. The asserted AF can be used to generate an interrupt ($\overline{\text{INT}}$). The AF can only be cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. In this way, an alarm can be generated from once per minute up to once per week (see Table1).

Timer Function

The 8-bit countdown timer is controlled by timer control register (see Table1). The timer control register determiners one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 Hz, or 1/64 Hz), and enables or disables end of every countdown. When bit7 (TE bit) of The timer control register is set to logic 0, timer is disabled; when TE=1, timer is enabled. The TD1 and TD0 bits determine the source clock for the countdown timer(see Table 5), when not in use, TD1 and TD0 should be set to 1/60 Hz for power saving. The timer counts down from a software-loaded 8-bit binary value. At the end of countdown, the timer sets the Timer Flag (TF). The asserted TF can be used to generate an interrupt ($\overline{\text{INT}}$). The interrupt may be generated as a pulsed signal every countdown period, the TF may only be cleared by software. Bit TI/TP is used to control generated conditions of interrupt. When reading the timer, the current countdown value is returned.

Table 5. Timer Frequency Selection

TD1	TD0	Timer Source clock frequency(Hz)
0	0	4096
0	1	64
1	0	1
1	1	1/60

Clock Output

A programmable square wave is available at pin CLKOUT. The CLKOUT control register is used to control the operation of the CLKOUT pin. Bit7 (FE bit) of the CLKOUT control register is square wave enable bit, when set to logic 0, the square wave output is enable, when set to logic 1, the CLKOUT output is inhibited. CLKOUT is an open-drain output and enabled at power-on. If disabled it becomes high-impedance. The frequency of the square wave output depends upon the value of the FD0 and FD1 bits. The FD bits control the frequency of the square wave output when the square wave output has been enabled. Table 6 lists the square wave frequencies that can be selected with the FD bits.

Table 6. CLKOUT frequency selection

FD1	FD0	f_{CLKOUT}
0	0	32.768 kHz
0	1	1024Hz
1	0	32Hz
1	1	1Hz

Reset

The HYM8563 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C-bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, VL, TD1, TD0, TESTC and AE which are set to logic 1.

Voltage-Low Detector and Clock Surveillance

The HYM8563 has an on-chip voltage-low detector. When V_{DD} drops below $V_{LOW,}$ bit VL in the seconds register is set to indicate that the integrity of the clock/calendar information is no longer guaranteed. The VL flag can only be cleared by software. When V_{DD} decreased slowly up to V_{LOW}, bit VL will be set. This will indicate that the time may be corrupted.

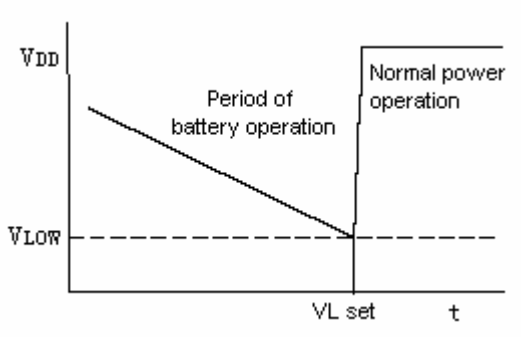


Figure 6. Voltage-low detection

I^2C-Bus Description

I^2C-Bus Interface

The HYM8563 supports I^2C-bus transmission protocol. The I^2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The master device generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The HYM8563 operates as a slave on the I^2C-bus. A typical bus configuration using this 2-wire protocol is show in Figure 7.

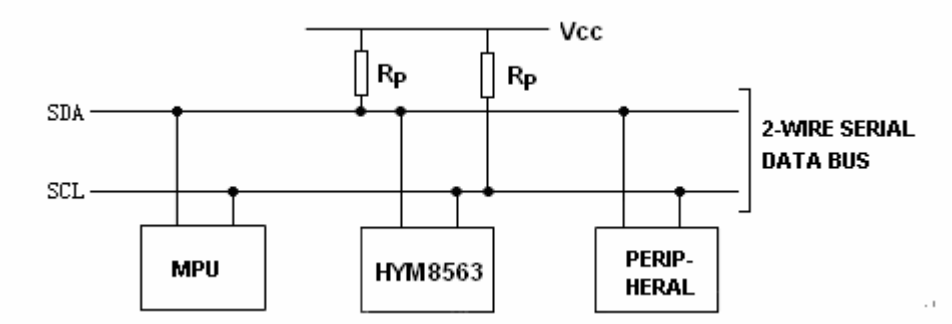


Figure 7. Typical I²C-Bus Configuration

Data transfer may be initiated only when the bus is not busy. Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition(S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P), see Figure 8.

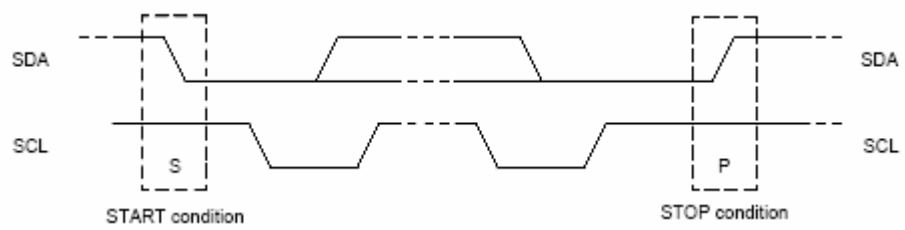


Figure 8. Definition of Start and Stop Condition

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see Figure 9).

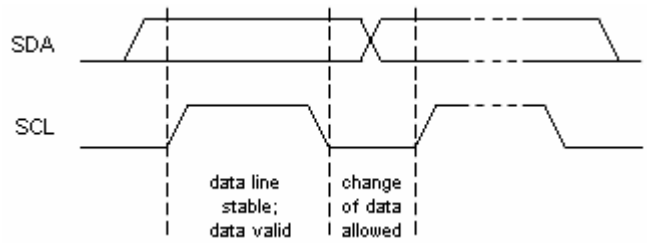


Figure 9. Bit Transfer

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit

(see Figure 10). The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

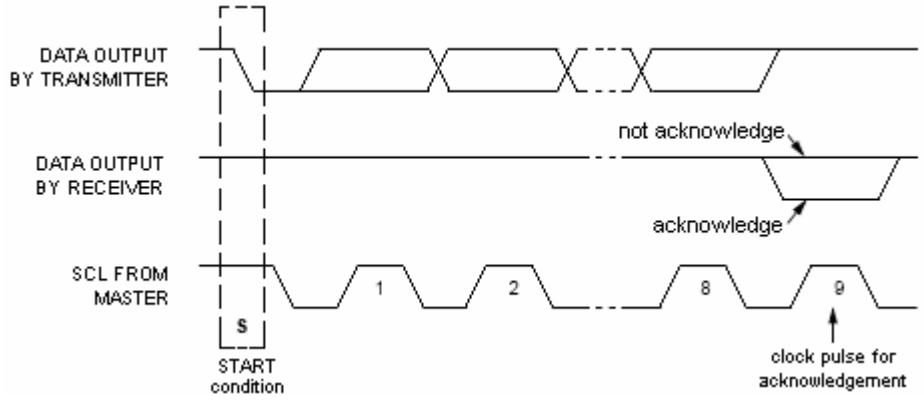


Figure 10. Acknowledgement on the I2C bus

Device Addressing

Before any data is transmitted on the I^2C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure. The HYM8563 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The HYM8563 slave address is shown in Table 7.

Table 7. Slave address

1	0	1	0	0	0	1	R/W

The address byte contains the 7-bit HYM8563 address, which is 1010001, followed by the direction bit (R/W). The R/W bit is a 1 for a read, and a 0 for a write. After receiving and decoding the address byte the device inputs an acknowledge on the SDA line. The HYM8563 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer.

Read/Write Cycles

The I^2C-bus configuration for the different HYM8563 read and write cycles is shown in Figure 11, Figure 12 and Figure 13. The word address is a 4-bit value that defines which register is to be accessed next. The upper four bits of the word address are not use.

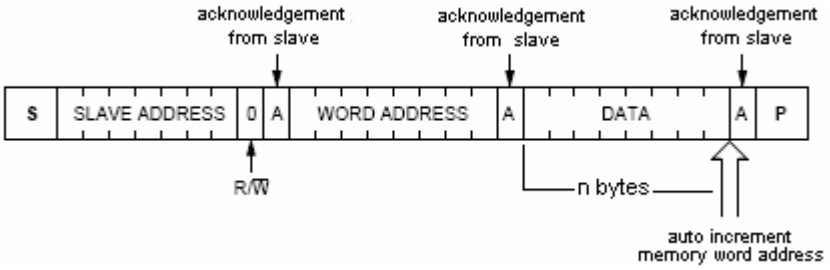


Figure 11. Master transmit to slave receiver(write mode)

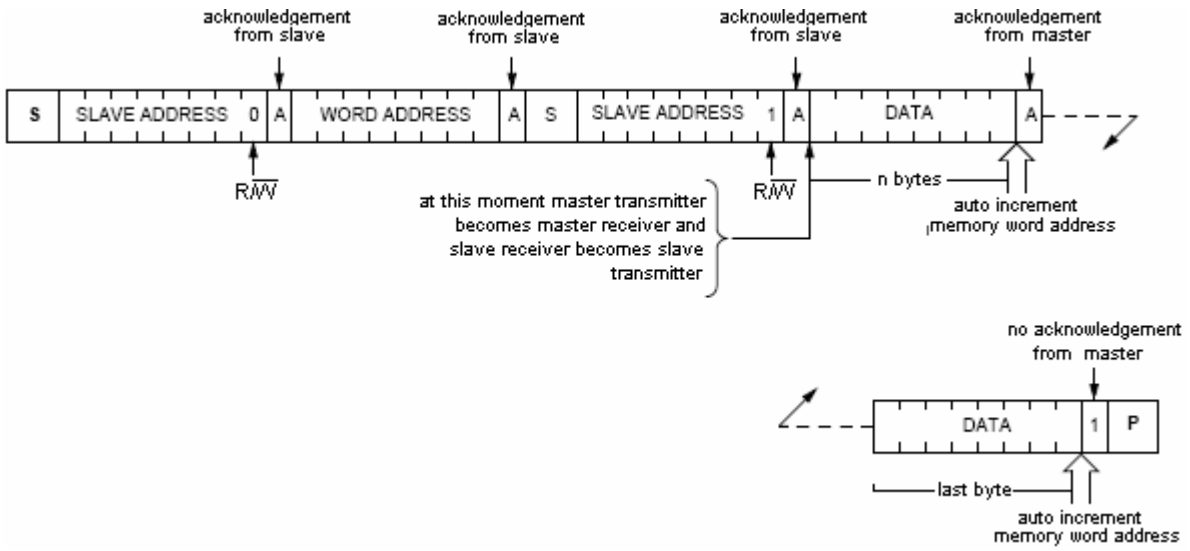


Figure 12. Master reads after setting word address(write word address; read data)

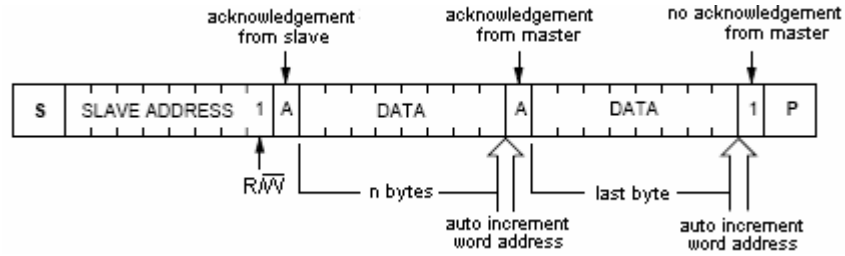
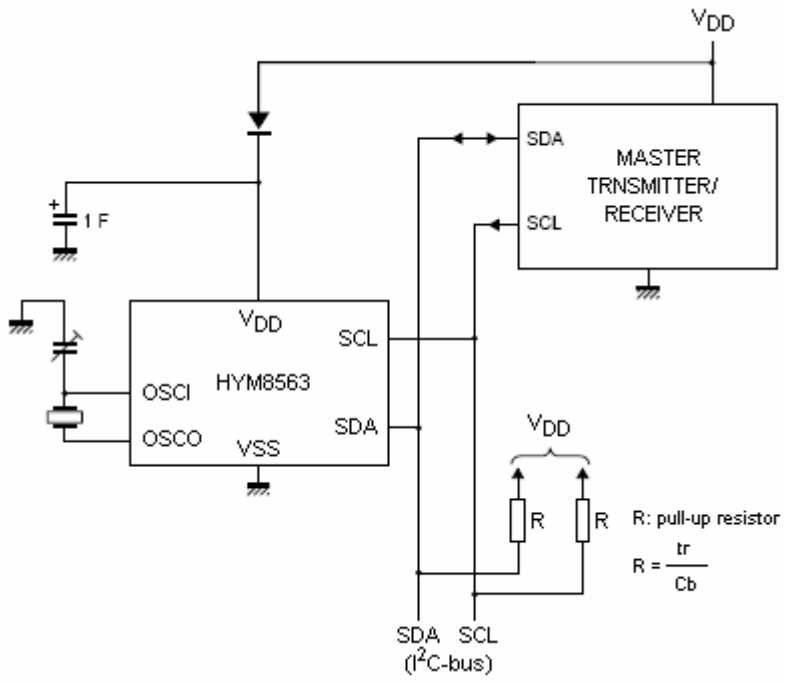


Figure 13.Master reads slave immediately after first byte(read mode)

Typical Application Circuit Diagram



Ordering Information

Type	Temperature range	Package
HYM8563	-40 to +85ºC	DIP8
HYM8563Z		SOP8
HYM8563TS		TSSOP8

Package