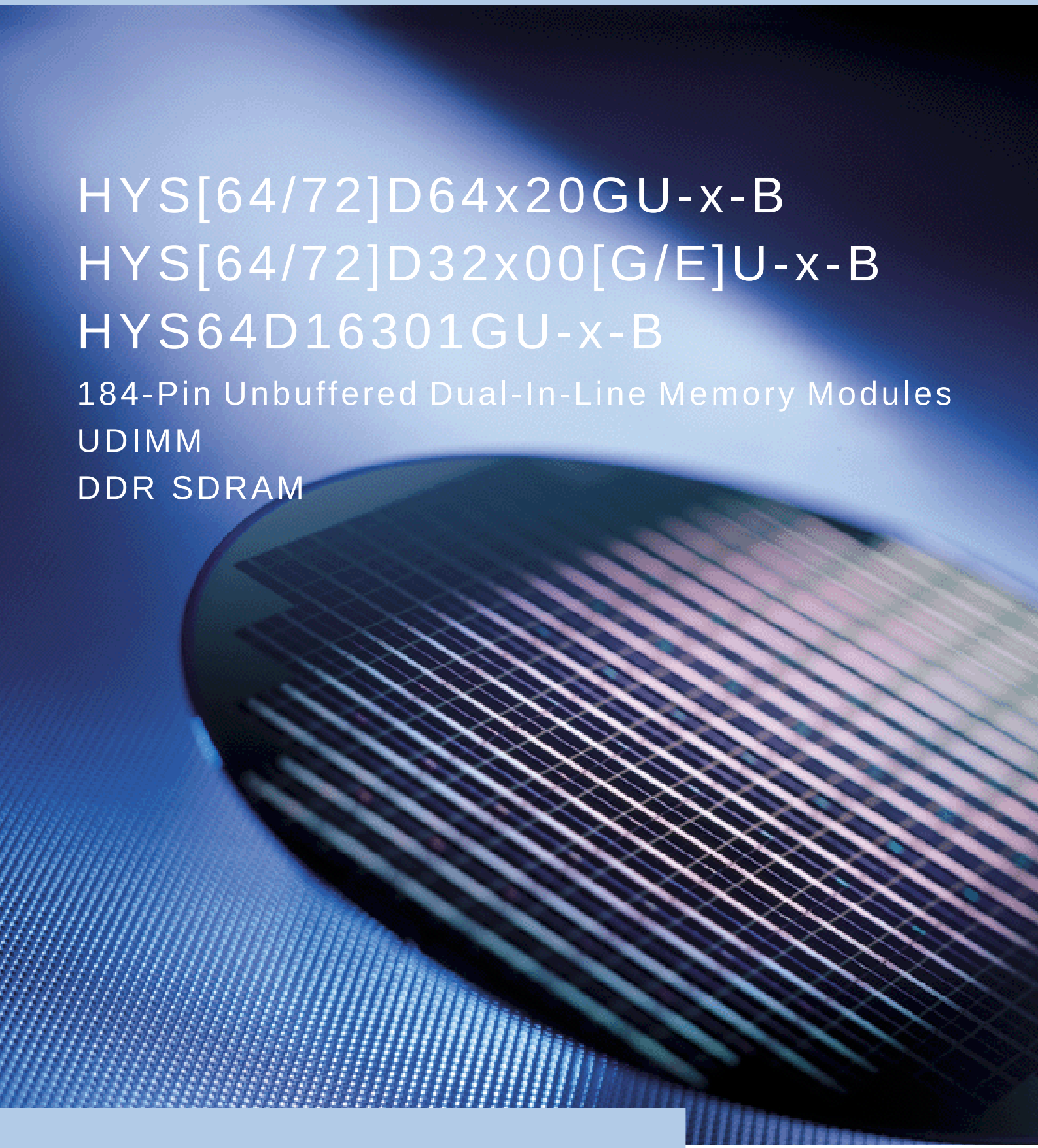
# HYS[64/72]D64x20GU-x-B
# HYS[64/72]D32x00[G/E]U-x-B
# HYS64D16301GU-x-B

## 184-Pin Unbuffered Dual-In-Line Memory Modules
## UDIMM
## DDR SDRAM



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184-Pin Unbuffered Dual-In-Line Memory Modules
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DDR SDRAM

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| **Revision History:** | **V1.1** | **2003-07** |
|---|---|---|
| Previous Version: | V1.01 | 2003-01 |

| Page | Subjects (major changes since last revision) |
|---|---|
| all | new data sheet template |
| all | replace bank by rank if DIMM related (4 bank SDRAM on 1 or 2 rank DIMM) |
| **10** | **Table 6**: Address Table updated |
| **19**ff | **Table 10**ff: IDD conditions now in seperate table |
| **20**ff | **Table 11**ff: added part numbers to IDD tables |
| **24**f | **Table 15**: split in two tables (now 15 & 16) |
| **26**f | **Table 16**: add –5 (DDR400) |
| **29**ff | **Chapter 4**: added part numbers to SPD tables |
| **41**ff | **Table 21**: set Bytes 47-55 to not used (00hex); set byte 62 to SPD rev. 0.0 (00hex); update Checksum (TPCR) |
| **8** | **Table 4**: Changed $\overline{\text{RAS}}$/$\overline{\text{CAS}}$/$\overline{\text{WE}}$ description to command inputs and amended CLK to CK |
| **9** | **Table 5**: Changed CLK to CK |
| **44**ff | **Figure 7** - **Figure 13** Amended and updated package outline drawings |

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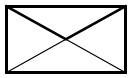

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# 1 Overview

## 1.1 Features

- 184-Pin Unbuffered Dual-In-Line Memory Modules (ECC and non-parity) for PC and Server main memory applications
- One rank 16M x 64, 32M × 64, 32M × 72 and two ranks 64M × 64, 64M × 72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM) Single +2.5V (±0.2V) power supply
- Built with 256 Mbit DDR SDRAM in P-TSOPII-66-1 package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Serial Presence Detect with $E^2$PROM
- JEDEC standard MO-206 form factor: 133.35 mm × 31.75 mm × 4.00 mm max.
- Jedec standard reference layout
- Gold plated contacts
- DDR400 Speed Grade supported
- Lead- & halogene-free DIMM available

**Table 1 Performance**

| Part Number Speed Code | | | –5 | –6 | –7F | –7 | –8 | Unit |
|---|---|---|---|---|---|---|---|---|
| Module Speed Grade | | | DDR400B | DDR333B | DDR266 | DDR266A | DDR200 | – |
| Component Module | | | PC3200 -3033 | PC2700 -2533 | PC2100 -2022 | PC2100 -2033 | PC1600 -2022 | – |
| max. Clock Frequency | @ CL = 3 | $f_{CK3}$ | 200 | 166 | – | – | – | MHz |
| | @ CL = 2.5 | $f_{CK2.5}$ | 166 | 166 | 143 | 143 | 125 | MHz |
| | @ CL = 2 | $f_{CK2}$ | 133 | 133 | 133 | 133 | 100 | MHz |

## 1.2 Description

The HYS[64/72]D64x20GU-x-B, HYS[64/72]D32x00[G/E]U-x-B, and HYS64D16301GU-x-B are industry standard 184-Pin Unbuffered Dual-In-Line Memory Modules (UDIMM) organized as 32M × 64 and 64M × 64 for non-parity and 32M × 72 and 64M × 72 for ECC main memory applications. The memory array is designed with 256 Mbit Double Data Rate Synchronous DRAMs. A variety of decoupling capacitors are mounted on the printed circuit board. The DIMMs feature serial presence detect (SPD) based on a serial $E^2$PROM device using the 2-pin $I^2C$ protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer

**Table 2 Ordering Information**

| Type | Compliance Code | Description | SDRAM Technology |
|---|---|---|---|
| **PC3200 (CL=3)** | | | |
| HYS64D16301GU-5-B | PC3200U-30330-C0 | one rank 128MB DIMM | 256 Mbit (×16) |
| HYS64D32300GU-5-B | PC3200U-30330-A0 | one rank 256MB DIMM | 256 Mbit (×8) |
| HYS72D32300GU-5-B | PC3200U-30330-A0 | one rank 256MB ECC-DIMM | 256 Mbit (×8) |
| HYS64D64320GU-5-B | PC3200U-30330-B0 | two ranks 512MB DIMM | 256 Mbit (×8) |
| HYS72D64320GU-5-B | PC3200U-30330-B0 | two ranks 512MB ECC-DIMM | 256 Mbit (×8) |
| **PC2700 (CL=2.5)** | | | |
| HYS64D16301GU-6-B | PC2700U-25330-C0 | one rank 128MB DIMM | 256 Mbit (×16) |
| HYS64D32300GU-6-B | PC2700U-25330-A0 | one rank 256MB DIMM | 256 Mbit (×8) |
| HYS72D32300GU-6-B | PC2700U-25330-A0 | one rank 256MB ECC-DIMM | 256 Mbit (×8) |
| HYS64D64320GU-6-B | PC2700U-25330-B0 | two ranks 512MB DIMM | 256 Mbit (×8) |
| HYS72D64320GU-6-B | PC2700U-25330-B0 | two ranks 512MB ECC-DIMM | 256 Mbit (×8) |
| **PC2100 (CL=2)** | | | |
| HYS64D16301GU-7-B | PC2100U-20330-C2 | one rank 128MB DIMM | 256 Mbit (×16) |
| HYS64D32000GU-7-B | PC2100U-20330-A1 | one rank 256MB DIMM | 256 Mbit (×8) |
| HYS72D32000GU-7F-B | PC2100U-20220-A1 | one rank 256MB ECC-DIMM | 256 Mbit (×8) |
| HYS72D32000GU-7-B | PC2100U-20330-A1 | one rank 256MB ECC-DIMM | 256 Mbit (×8) |
| HYS64D64020GU-7-B | PC2100U-20330-B1 | two ranks 512MB DIMM | 256 Mbit (×8) |
| HYS72D64020GU-7F-B | PC2100U-20220-B1 | two ranks 512MB ECC-DIMM | 256 Mbit (×8) |
| HYS72D64020GU-7-B | PC2100U-20330-B1 | two ranks 512MB ECC-DIMM | 256 Mbit (×8) |
| **PC1600 (CL=2)** | | | |
| HYS64D16301GU-8-B | PC1600U-20330-C2 | one rank 128MB DIMM | 256 Mbit (×16) |
| HYS64D32000GU-8-B | PC1600U-20220-A1 | one rank 256MB DIMM | 256 Mbit (×8) |
| HYS72D32000GU-8-B | PC1600U-20220-A1 | one rank 256MB ECC-DIMM | 256 Mbit (×8) |
| HYS64D64020GU-8-B | PC1600U-20220-B1 | two ranks 512MB DIMM | 256 Mbit (×8) |
| HYS72D64020GU-8-B | PC1600U-20220-B1 | two ranks 512MB ECC-DIMM | 256 Mbit (×8) |

**Table 3 Lead- and Halogene-Free DIMM**

| Type | Compliance Code | Description | SDRAM Technology |
|---|---|---|---|
| **PC2100 (CL=2)** | | | |
| HYS64D32300EU-7-B | PC2100U-20330-A1 | one rank 256MB DIMM | 256 Mbit (×8) |

*Note: All part numbers end with a place code designating the silicon-die revision. Reference information available on request. Example: HYS72D32000GU-6-B, indicating rev. B dies are used for SDRAM components. The Compliance Code is printed on the module labels describing the speed sort (for example "PC2700"), the latencies and SPD code definition (for example "20330" means CAS latency of 2.0 clocks, RCD[1)] latency of 3 clocks, Row Precharge latency of 3 clocks, and JEDEC SPD code definiton version 0), and the Raw Card used for this module.*

1) RCD: Row-Column-Delay

# 2 Pin Configuration

**Table 4 Pin Definitions and Functions**

| Symbol | Type[1)] | Function |
|---|---|---|
| A0 - A12 | I | Address Inputs |
| BA0, BA1 | I | Bank Selects |
| DQ0 - DQ63 | I/O | Data Input/Output |
| CB0 - CB7 | I/O | Check Bits (×72 organization only) |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | I | Command Inputs |
| CKE0 - CKE1 | I | Clock Enable |
| DQS0 - DQS8 | I/O | SDRAM low data strobes |
| CK0 - CK2, | I | SDRAM clock (positive lines) |
| $\overline{CK0}$ - $\overline{CK2}$ | I | SDRAM clock (negative lines) |
| DM0 - DM8<br>DQS9 - DQS17 | I<br>I/O | SDRAM low data mask/<br>high data strobes |
| $\overline{S0}$, $\overline{S1}$ | I | Chip Selects for Rank0 and Rank1 |
| $V_{DD}$ | PWR | Power (+2.5 V) |
| $V_{SS}$ | GND | Ground |
| $V_{DDQ}$ | PWR | I/O Driver power supply |
| $V_{DDID}$ | PWR | VDD Indentification flag |
| $V_{REF}$ | AI | I/O reference supply |
| $V_{DDSPD}$ | PWR | Serial EEPROM power supply |
| SCL | I | Serial bus clock |
| SDA | I/O | Serial bus data line |
| SA0 - SA2 | I | slave address select |
| NC | NC | Not Connected |

1) I: Input; O: Output; I/O: bidirectional In-/Output; AI: Analog Input; PWR: Power Supply; GND: Signal Ground; NC: Not Connected

*Note: S1 and CKE1 are used on two rank modules only*

**Table 5 Pin Configuration**

| Frontside | | | | Backside | | | |
|---|---|---|---|---|---|---|---|
| **PIN#** | **Symbol** | **PIN#** | **Symbol** | **PIN#** | **Symbol** | **PIN#** | **Symbol** |
| 1 | $V_{REF}$ | 48 | A0 | 93 | $V_{SS}$ | 140 | NC / DM8/DQS17 |
| 2 | DQ0 | 49 | NC / CB2 | 94 | DQ4 | 141 | A10 |
| 3 | $V_{SS}$ | 50 | $V_{SS}$ | 95 | DQ5 | 142 | NC / CB6 |
| 4 | DQ1 | 51 | NC / CB3 | 96 | $V_{DDQD}$ | 143 | $V_{DDQD}$ |
| 5 | DQS0 | 52 | BA1 | 97 | DM0/DQS9 | 144 | NC / CB7 |
| 6 | DQ2 | **Key** | | 98 | DQ6 | **Key** | |
| 7 | $V_{DD}$ | | | 99 | DQ7 | | |
| 8 | DQ3 | 53 | DQ32 | 100 | $V_{SS}$ | 145 | $V_{SS}$ |
| 9 | NC | 54 | $V_{DDQ}$ | 101 | NC | 146 | DQ36 |
| 10 | NC | 55 | DQ33 | 102 | NC | 147 | DQ37 |
| 11 | $V_{SS}$ | 56 | DQS4 | 103 | NC | 148 | $V_{DD}$ |
| 12 | DQ8 | 57 | DQ34 | 104 | $V_{DDQ}$ | 149 | DM4/DQS13 |
| 13 | DQ9 | 58 | $V_{SS}$ | 105 | DQ12 | 150 | DQ38 |
| 14 | DQS1 | 59 | BA0 | 106 | DQ13 | 151 | DQ39 |
| 15 | $V_{DDQ}$ | 60 | DQ35 | 107 | DM1/DQS10 | 152 | $V_{SS}$ |
| 16 | CK1 | 61 | DQ40 | 108 | $V_{DD}$ | 153 | DQ44 |
| 17 | $\overline{CK1}$ | 62 | $V_{DDQ}$ | 109 | DQ14 | 154 | $\overline{RAS}$ |
| 18 | $V_{SS}$ | 63 | $\overline{WE}$ | 110 | DQ15 | 155 | DQ45 |
| 19 | DQ10 | 64 | DQ41 | 111 | CKE1 | 156 | $V_{DDQ}$ |
| 20 | DQ11 | 65 | $\overline{CAS}$ | 112 | $V_{DDQ}$ | 157 | $\overline{S0}$ |
| 21 | CKE0 | 66 | $V_{SS}$ | 113 | NC (BA2) | 158 | $\overline{S1}$ |
| 22 | $V_{DDQ}$ | 67 | DQS5 | 114 | DQ20 | 159 | DM5/DQS14 |
| 23 | DQ16 | 68 | DQ42 | 115 | NC / A12 | 160 | $V_{SS}$ |
| 24 | DQ17 | 69 | DQ43 | 116 | $V_{SS}$ | 161 | DQ46 |
| 25 | DQS2 | 70 | $V_{DD}$ | 117 | DQ21 | 162 | DQ47 |
| 26 | $V_{SS}$ | 71 | NC | 118 | A11 | 163 | NC |
| 27 | A9 | 72 | DQ48 | 119 | DM2/DQS11 | 164 | $V_{DDQ}$ |
| 28 | DQ18 | 73 | DQ49 | 120 | $V_{DD}$ | 165 | DQ52 |
| 29 | A7 | 74 | $V_{SS}$ | 121 | DQ22 | 166 | DQ53 |
| 30 | $V_{DDQ}$ | 75 | CK2 | 122 | A8 | 167 | NC (A13) |
| 31 | DQ19 | 76 | $\overline{CK2}$ | 123 | DQ23 | 168 | $V_{DD}$ |
| 32 | A5 | 77 | $V_{DDQ}$ | 124 | $V_{SS}$ | 169 | DM6/DQS15 |
| 33 | DQ24 | 78 | DQS6 | 125 | A6 | 170 | DQ54 |
| 34 | $V_{SS}$ | 79 | DQ50 | 126 | DQ28 | 171 | DQ55 |
| 35 | DQ25 | 80 | DQ51 | 127 | DQ29 | 172 | $V_{DDQ}$ |
| 36 | DQS3 | 81 | $V_{SS}$ | 128 | $V_{DDQ}$ | 173 | NC |
| 37 | A4 | 82 | $V_{DDID}$ | 129 | DM3/DQS12 | 174 | DQ60 |
| 38 | $V_{DD}$ | 83 | DQ56 | 130 | A3 | 175 | DQ61 |
| 39 | DQ26 | 84 | DQ57 | 131 | DQ30 | 176 | $V_{SS}$ |

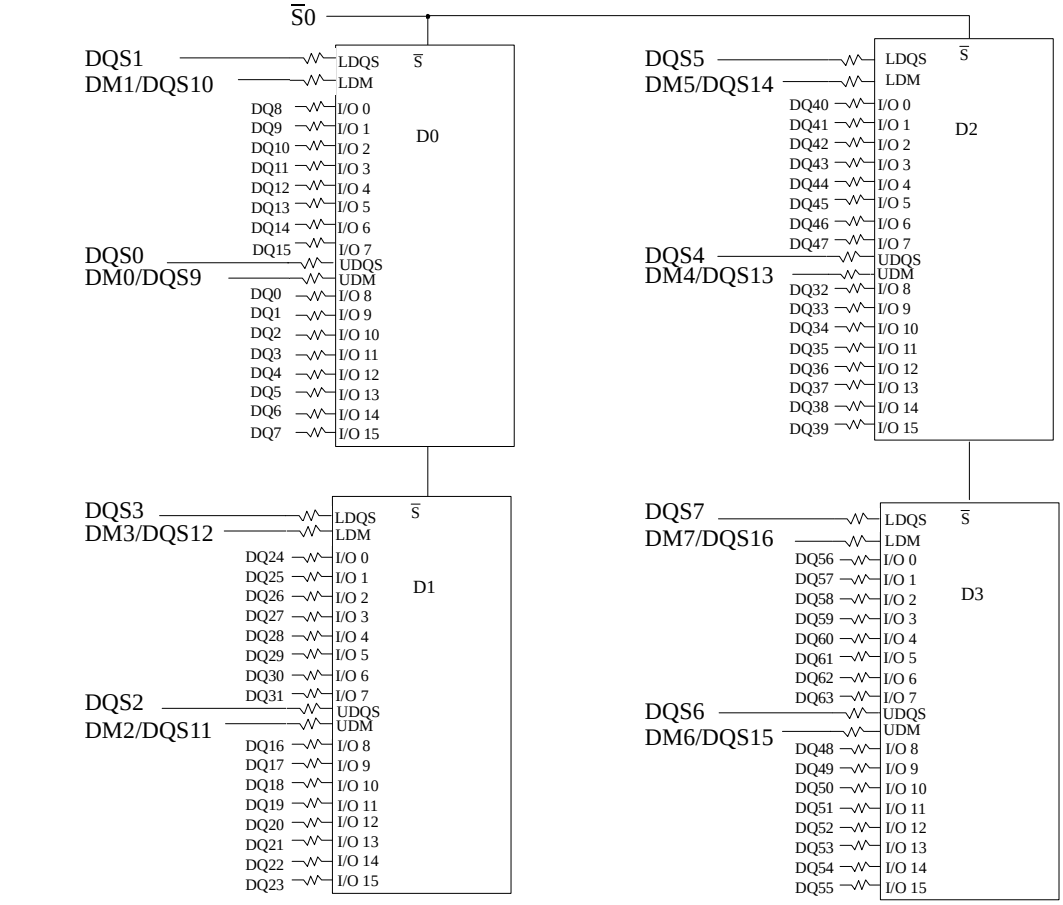
**Table 5 Pin Configuration** (cont'd)

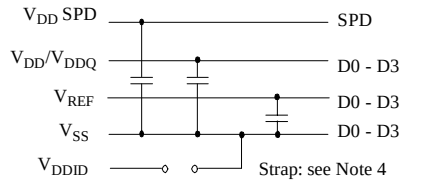
| Frontside | | | | Backside | | | |
|---|---|---|---|---|---|---|---|
| **PIN#** | **Symbol** | **PIN#** | **Symbol** | **PIN#** | **Symbol** | **PIN#** | **Symbol** |
| 40 | DQ27 | 85 | $V_{DD}$ | 132 | $V_{SS}$ | 177 | DM7/DQS16 |
| 41 | A2 | 86 | DQS7 | 133 | DQ31 | 178 | DQ62 |
| 42 | $V_{SS}$ | 87 | DQ58 | 134 | NC / CB4 | 179 | DQ63 |
| 43 | A1 | 88 | DQ59 | 135 | NC / CB5 | 180 | $V_{DDQ}$ |
| 44 | NC / CB0 | 89 | $V_{SS}$ | 136 | $V_{DDQ}$ | 181 | SA0 |
| 45 | NC / CB1 | 90 | NC | 137 | CK0 | 182 | SA1 |
| 46 | $V_{DD}$ | 91 | SDA | 138 | $\overline{CK0}$ | 183 | SA2 |
| 47 | NC / DQS8 | 92 | SCL | 139 | $V_{SS}$ | 184 | $V_{DDSPD}$ |

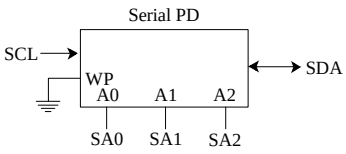
*Note: Pins 44, 45, 47, 49, 51, 134, 135, 140 and 144 are NC ("not connected") on ×64 organised non-ECC modules.*

**Table 6 Address Format**

| Density | Organization | Memory Ranks | SDRAMs | # of SDRAMs | # of row/bank/ columns bits | Refresh | Period | Interval |
|---|---|---|---|---|---|---|---|---|
| 128 MB | 16M × 64 | 1 | 16M × 16 | 4 | 13/2/10 | 8 K | 64 ms | 7.8 µs |
| 256 MB | 32M × 64 | 1 | 32M × 8 | 8 | 13/2/11 | 8 K | 64 ms | 7.8 µs |
| 256 MB | 32M × 72 | 1 | 32M × 8 | 9 | 13/2/11 | 8 K | 64 ms | 7.8 µs |
| 512 MB | 64M × 64 | 2 | 32M × 8 | 16 | 13/2/11 | 8 K | 64 ms | 7.8 µs |
| 512 MB | 64M × 72 | 2 | 32M × 8 | 18 | 13/2/11 | 8 K | 64 ms | 7.8 µs |

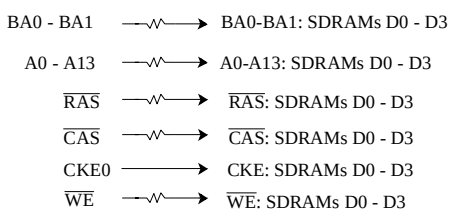



| * Clock Wiring | |
|---|---|
| Clock Input | SDRAMs |
| *CK0/$\overline{CK0}$ | NC |
| *CK1/$\overline{CK1}$ | 2 SDRAMs |
| *CK2/$\overline{CK2}$ | 2 SDRAMs |

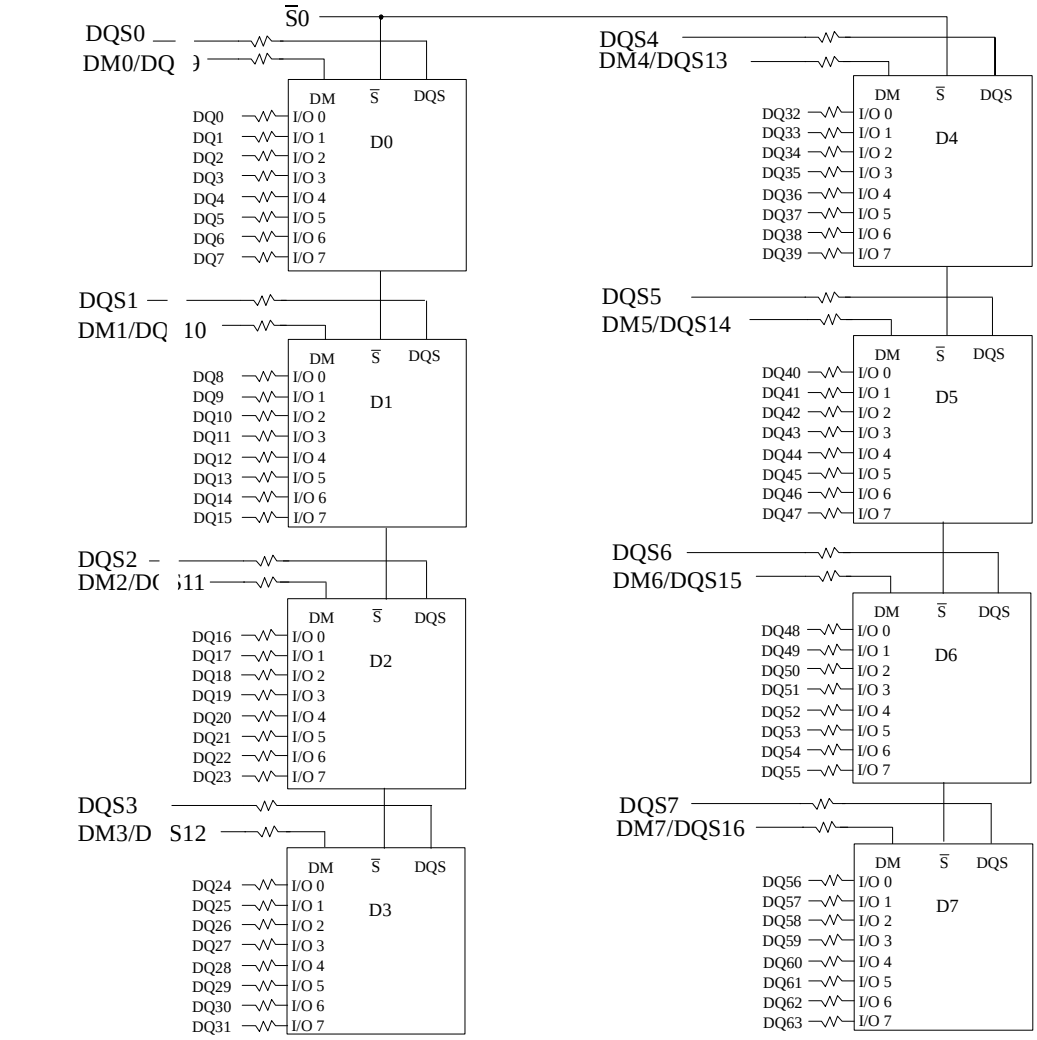
* Wire per Clock Loading Table/Wiring Diagrams

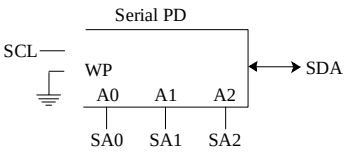



**Notes:**

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%.
4. $V_{DDID}$ strap connections
   (for memory device $V_{DD}$, $V_{DDQ}$):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN ($V_{SS}$): $V_{DD} \neq V_{DDQ}$
5. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: 7.5 ohms ± 5%

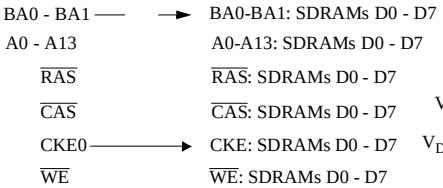
**Figure 1 Block Diagram - One Rank 16M × 64 DDR SDRAM DIMM HYS64D16301GU using ×16 organized SDRAMs**

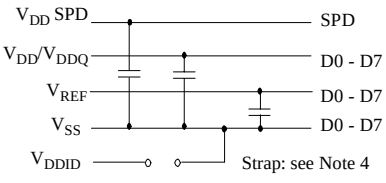



| * Clock Wiring | |
|---|---|
| Clock Input | SDRAMs |
| *CK0/$\overline{CK0}$ | 2 SDRAMs |
| *CK1/$\overline{CK1}$ | 3 SDRAMs |
| *CK2/$\overline{CK2}$ | 3 SDRAMs |

* Wire per Clock Loading Table/Wiring Diagrams




**Notes:**

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%
4. $V_{DDID}$ strap connections
   (for memory device $V_{DD}$, $V_{DDQ}$):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN ($V_{SS}$): $V_{DD} \neq V_{DDQ}$.
5. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: 5.1 ohms ±5%

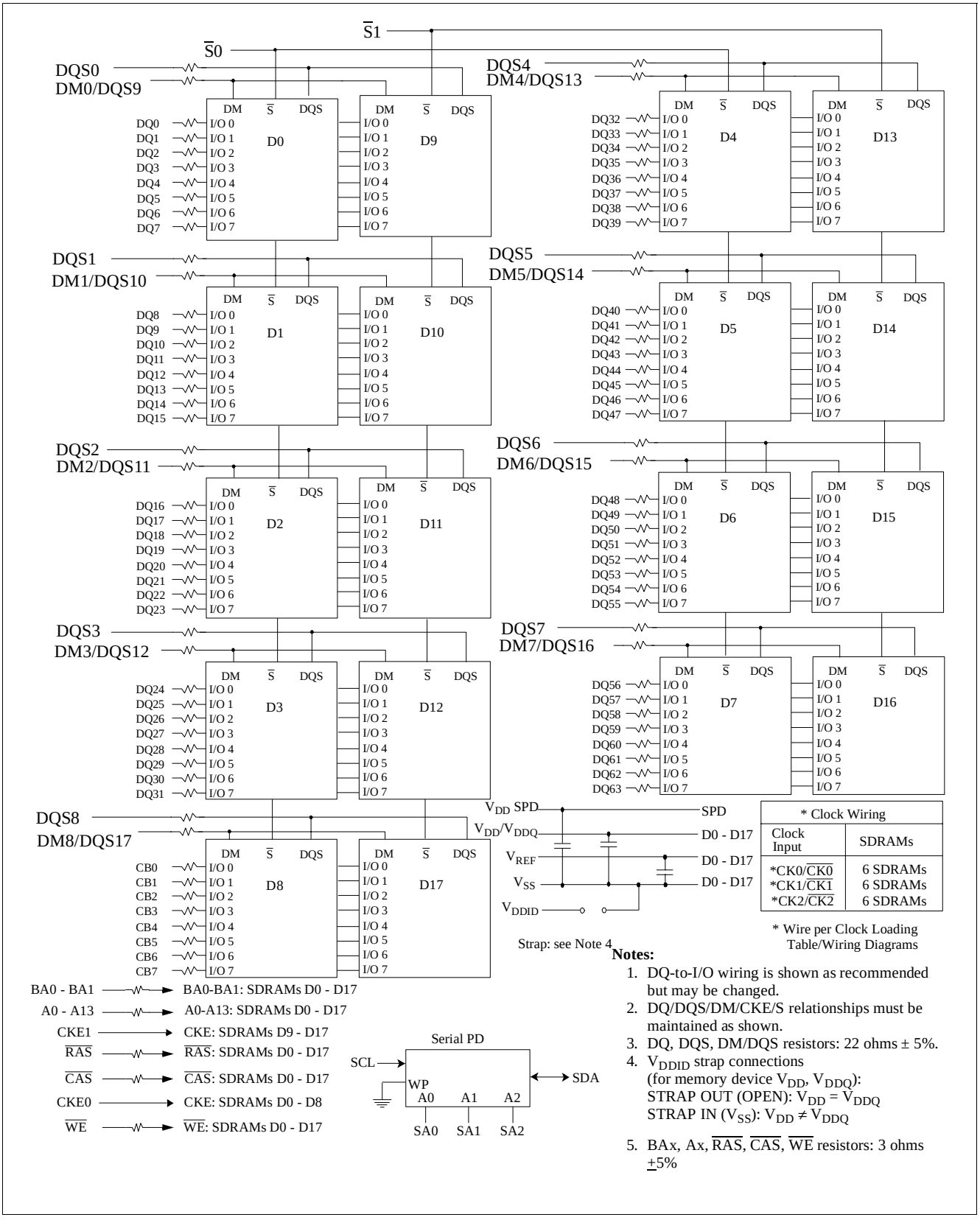



**Figure 5 Block Diagram - Two Rank 64M × 72 DDR-I SDRAM DIMM HYS72D64x20GU using ×8 organized SDRAMs**

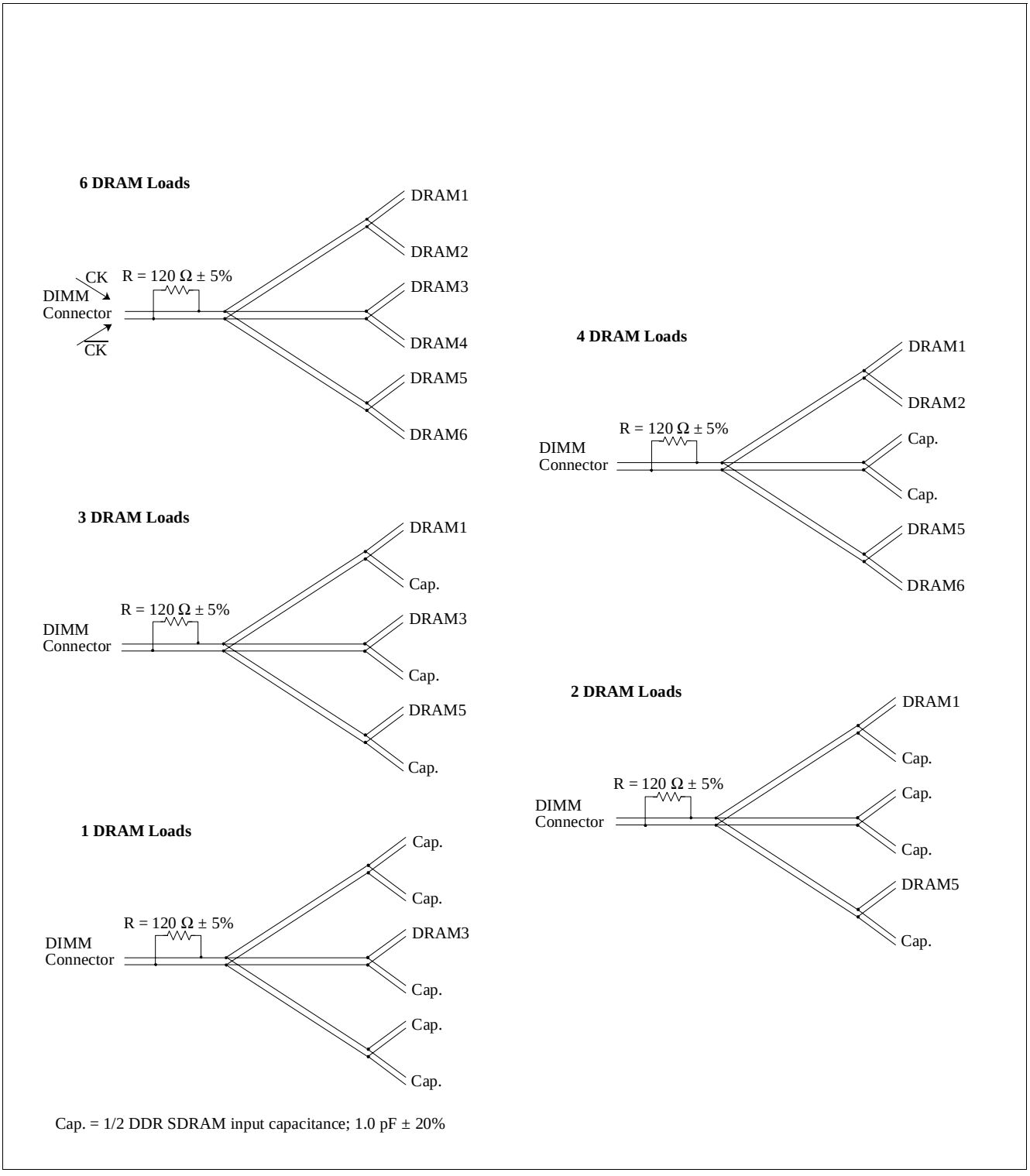



**Figure 6 Clock Net Wiring**

# 3 Electrical Characteristics

## 3.1 Operating Conditions

**Table 7 Absolute Maximum Ratings**

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Voltage on I/O pins relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -0.5 | – | $V_{DDQ}$ + 0.5 | V | – |
| Voltage on Inputs relative to $V_{SS}$ | $V_{IN}$ | -0.5 | – | +3.6 | V | – |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}$ | -0.5 | – | +3.6 | V | – |
| Voltage on $V_{DDQ}$ supply relative to $V_{SS}$ | $V_{DDQ}$ | -0.5 | – | +3.6 | V | – |
| Operating Temperature (Ambient) | $T_A$ | 0 | – | +70 | °C | – |
| Storage Temperature | $T_{STG}$ | -55 | – | +150 | °C | – |
| Power dissipation (per SDRAM component) | $P_D$ | – | 1 | – | W | – |
| Short Circuit Output Current | $I_{OUT}$ | – | 50 | – | mA | – |

***Attention: Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to recommended operation conditions. Exceeding only one of these values for extended periods of time affect device reliability and may cause irreversible damage to the integrated circuit.***

**Table 8 Supply Voltage Levels**

| Parameter | Symbol | Limit Values | | | Unit | Note/ Test Condition |
|---|---|---|---|---|---|---|
| | | min. | nom. | max. | | |
| Device Supply Voltage | $V_{DD}$ | 2.3 | 2.5 | 2.7 | V | $f_{CK}$ ≤166 MHz |
| Device Supply Voltage | $V_{DD}$ | 2.5 | 2.6 | 2.7 | V | $f_{CK}$ > 166 MHz 1) |
| Output Supply Voltage | $V_{DDQ}$ | 2.3 | 2.5 | 2.7 | V | $f_{CK}$ ≤166 MHz 2) |
| Output Supply Voltage | $V_{DDQ}$ | 2.5 | 2.6 | 2.7 | V | $f_{CK}$ > 166 MHz 1)2) |
| Input Reference Voltage | $V_{REF}$ | 0.49 × $V_{DDQ}$ | 0.5 × $V_{DDQ}$ | 0.51 × $V_{DDQ}$ | V | $f_{CK}$ ≤166 MHz 3) |
| Input Reference Voltage | $V_{REF}$ | $V_{DDQ}$ / 2 –50 mV | $V_{DDQ}$ / 2 | $V_{DDQ}$/ 2 + 50 mV | V | $f_{CK}$ > 166 MHz 1)3) |
| Termination Voltage | $V_{TT}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V | 4) |
| EEPROM supply voltage | $V_{DDSPD}$ | 2.3 | 2.5 | 3.6 | V | — |

1) DDR400 conditions apply for all clock frequencies above 166 MHz

2) Under all conditions, $V_{DDQ}$ must be less than or equal to $V_{DD}$.

3) Peak to peak AC noise on $V_{REF}$ may not exceed ± 2% $V_{REF\ (DC)}$. $V_{REF}$ is also expected to track noise variations in $V_{DDQ}$.

4) $V_{TT}$ of the transmitting device must track $V_{REF}$ of the receiving device.

**Table 9 DC Operating Conditions (SSTL_2 Inputs)**

| Parameter | Symbol | Values | | Unit | **Note/ Test Condition [1)]** |
|---|---|---|---|---|---|
| | | **min.** | **max.** | | |
| DC Input Logic High | $V_{IH\ (DC)}$ | $V_{REF}$ + 0.15 | $V_{DDQ}$ + 0.3 | V | [2)] |
| DC Input Logic Low | $V_{IL\ (DC)}$ | – 0.30 | $V_{REF}$ – 0.15 | V | – |
| Input Leakage Current | $I_{IL}$ | – 5 | 5 | µA | [3)] |
| Output Leakage Current | $I_{OL}$ | – 5 | 5 | µA | [3)] |

1) $V_{DDQ}$ = 2.5 V, $T_A$ = 70 °C, Voltage Referenced to $V_{SS}$

2) The relationship between the $V_{DDQ}$ of the driving device and the $V_{REF}$ of the receiving device is what determines noise margins. However, in the case of $V_{IH\ (max.)}$ (input overdrive), it is the $V_{DDQ}$ of the receiving device that is referenced. In the case where a device is implemented such that it supports SSTL_2 inputs but has no SSTL_2 outputs (such as a translator), and therefore no $V_{DDQ}$ supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner $V_{DDQ}$ + 300 mV).

3) For any pin under test input of 0 V ≤$V$IN ≤$V_{DDQ}$ + 0.3 V. Values are shown per DDR SDRAM component

## 3.2 Current Conditions and Specification

**Table 10 $I_{DD}$ Conditions**

| Parameter | Symbol |
|---|---|
| **Operating Current 0**<br>one bank; active/ precharge; $t_{RC} = t_{RC,MIN}$;<br>DQ, DM, and DQS inputs changing once per clock cycle;<br>address and control inputs changing once every two clock cycles. | $I_{DD0}$ |
| **Operating Current 1**<br>one bank; active/read/precharge; Burst Length = 4; see component data sheet. | $I_{DD1}$ |
| **Precharge Power-Down Standby Current**<br>all banks idle; power-down mode; CKE $\leq V_{IL,MAX}$ | $I_{DD2P}$ |
| **Precharge Floating Standby Current**<br>$\overline{CS} \geq V_{IH,,MIN}$, all banks idle; CKE $\geq V_{IH,MIN}$;<br>address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS and DM. | $I_{DD2F}$ |
| **Precharge Quiet Standby Current**<br>$\overline{CS} \geq V_{IHMIN}$, all banks idle; CKE $\geq V_{IH,MIN}$;<br>address and other control inputs stable at $\geq V_{IH,MIN}$ or $\leq V_{IL,MAX}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM. | $I_{DD2Q}$ |
| **Active Power-Down Standby Current**<br>one bank active; power-down mode; CKE $\leq V_{ILMAX}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM. | $I_{DD3P}$ |
| **Active Standby Current**<br>one bank active; $\overline{CS} \geq V_{IH,MIN}$; CKE $\geq V_{IH,MIN}$; $t_{RC} = t_{RAS,MAX}$;<br>DQ, DM and DQS inputs changing twice per clock cycle;<br>address and control inputs changing once per clock cycle. | $I_{DD3N}$ |
| **Operating Current Read**<br>one bank active; Burst Length = 2; reads; continuous burst;<br>address and control inputs changing once per clock cycle;<br>50% of data outputs changing on every clock edge;<br>CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; $I_{OUT}$ = 0 mA | $I_{DD4R}$ |
| **Operating Current Write**<br>one bank active; Burst Length = 2; writes; continuous burst;<br>address and control inputs changing once per clock cycle;<br>50% of data outputs changing on every clock edge;<br>CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B | $I_{DD4W}$ |
| **Auto-Refresh Current**<br>$t_{RC} = t_{RFCMIN}$, distributed refresh | $I_{DD5}$ |
| **Self-Refresh Current**<br>CKE $\leq$0.2 V; external clock on | $I_{DD6}$ |
| **Operating Current 7**<br>four bank interleaving with Burst Length = 4; see component data sheet. | $I_{DD7}$ |

**Table 11 Operating, Standby and Refresh Currents (PC2100, –8)**

| Part Number & Organization | HYS64D16301GU–8–B | | HYS64D32300GU–8–B | | HYS72D32300GU–8–B | | HYS64D64320GU–8–B | | HYS72D64320GU–8–B | | Unit | Note[1)2)] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 128MB ×64 | | 256MB ×64 | | 256MB ×72 | | 512MB ×64 | | 512MB ×72 | | | |
| | 1 rank | | 1 rank | | 1 rank | | 2 ranks | | 2 ranks | | | |
| **Symbol** | **typ.** | **max.** | **typ.** | **max.** | **typ.** | **max.** | **typ.** | **max.** | **typ.** | **max.** | | |
| $I_{DD0}$ | 288 | 380 | 560 | 720 | 630 | 810 | 880 | 1080 | 990 | 1215 | mA | 3) |
| $I_{DD1}$ | 332 | 420 | 640 | 800 | 720 | 900 | 960 | 1160 | 1080 | 1305 | mA | 3)4) |
| $I_{DD2P}$ | 20 | 28 | 40 | 56 | 45 | 63 | 80 | 112 | 90 | 126 | mA | 5) |
| $I_{DD2F}$ | 120 | 140 | 240 | 280 | 270 | 315 | 480 | 560 | 540 | 630 | mA | 5) |
| $I_{DD2Q}$ | 72 | 88 | 144 | 176 | 162 | 198 | 288 | 352 | 324 | 396 | mA | 5) |
| $I_{DD3P}$ | 52 | 64 | 104 | 128 | 117 | 144 | 208 | 256 | 234 | 288 | mA | 5) |
| $I_{DD3N}$ | 168 | 200 | 320 | 360 | 360 | 405 | 640 | 720 | 720 | 810 | mA | 5) |
| $I_{DD4R}$ | 356 | 440 | 632 | 760 | 711 | 855 | 952 | 1120 | 1071 | 1260 | mA | 3)4) |
| $I_{DD4W}$ | 384 | 480 | 680 | 840 | 765 | 945 | 1000 | 1200 | 1125 | 1350 | mA | 3) |
| $I_{DD5}$ | 504.8 | 680 | 1010 | 1360 | 1136 | 1530 | 1330 | 1720 | 1496 | 1935 | mA | 3) |
| $I_{DD6}$ | 6 | 10 | 12 | 20 | 13.5 | 22.5 | 24 | 40 | 27 | 45 | mA | 5) |
| $I_{DD7}$ | 632 | 880 | 1200 | 1680 | 1350 | 1890 | 1520 | 2040 | 1710 | 2295 | mA | 3)4) |

1) DRAM component currents only

2) Test condition for maximum values: $V_{DD}$ = 2.7 V, $T_A$ = 10 °C

3) The module $I_{DDx}$ values are calculated from the component $I_{DDx}$ data sheet values as:
**m** × $I_{DDx}$[component] + **n** × $I_{DD3N}$[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O ($I_{DDQ}$) currents are not included into calculations: module $I_{DD}$ values will be measured differently depending on load conditions

5) The module $I_{DDx}$ values are calculated from the corrponent $I_{DDx}$ data sheet values as: (**m** + **n**) × $I_{DDx}$[component]

**Table 12 Operating, Standby and Refresh Currents (PC2100, –7 & –7F)**

| Part Number & Organization | HYS64D16301GU–7–B | | HYS64D32300GU–7–B HYS64D32300EU–7–B | | HYS72D32300GU–7–B | | HYS64D64320GU–7–B | | HYS64D64320GU–7F–B | | HYS72D64320GU–7–B | | HYS72D64320GU–7F–B | | Unit | Note 1)2) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 128MB ×64 | | 256MB ×64 | | 256MB ×72 | | 512MB ×64 | | 512MB ×72 | | 512MB ×72 | | 512MB ×72 | | | |
| | 1 rank | | 1 rank | | 1 rank | | 1 rank | | 1 rank | | 2 ranks | | 2 ranks | | | |
| Sym-bol | typ. | max. | typ. | max. | typ. | max. | typ. | max. | typ. | max. | typ. | max. | typ. | max. | | |
| $I_{DD0}$ | 308 | 420 | 600 | 800 | 675 | 900 | 747 | 990 | 1000 | 1240 | 1125 | 1395 | 1197 | 1485 | mA | 3) |
| $I_{DD1}$ | 376 | 460 | 720 | 880 | 810 | 990 | 882 | 1080 | 1120 | 1320 | 1260 | 1485 | 1332 | 1575 | mA | 3)4) |
| $I_{DD2P}$ | 22 | 32 | 44 | 64 | 49.5 | 72 | 49.5 | 72 | 88 | 128 | 99 | 144 | 99 | 144 | mA | 5) |
| $I_{DD2F}$ | 140 | 160 | 280 | 320 | 315 | 360 | 315 | 360 | 560 | 640 | 630 | 720 | 630 | 720 | mA | 5) |
| $I_{DD2Q}$ | 80 | 100 | 160 | 200 | 180 | 225 | 180 | 225 | 320 | 400 | 360 | 450 | 360 | 450 | mA | 5) |
| $I_{DD3P}$ | 60 | 72 | 120 | 144 | 135 | 162 | 135 | 162 | 240 | 288 | 270 | 324 | 270 | 324 | mA | 5) |
| $I_{DD3N}$ | 208 | 240 | 400 | 440 | 450 | 495 | 450 | 495 | 800 | 880 | 900 | 990 | 900 | 990 | mA | 5) |
| $I_{DD4R}$ | 428 | 520 | 760 | 920 | 855 | 1035 | 855 | 1035 | 1160 | 1360 | 1305 | 1530 | 1305 | 1530 | mA | 3)4) |
| $I_{DD4W}$ | 476 | 560 | 840 | 1000 | 945 | 1125 | 945 | 1125 | 1240 | 1440 | 1395 | 1620 | 1395 | 1620 | mA | 3) |
| $I_{DD5}$ | 540 | 720 | 1080 | 1440 | 1215 | 1620 | 1217 | 1620 | 1480 | 1880 | 1665 | 2115 | 1667 | 2115 | mA | 3) |
| $I_{DD6}$ | 6 | 10 | 12 | 20 | 13.5 | 22.5 | 13.5 | 22.5 | 24 | 40 | 27 | 45 | 27 | 45 | mA | 5) |
| $I_{DD7}$ | 720 | 940 | 1369 | 1800 | 1540 | 2025 | 1540 | 2025 | 1769 | 2240 | 1990 | 2520 | 1990 | 2520 | mA | 3)4) |

1) DRAM component currents only

2) Test condition for maximum values: $V_{DD}$ = 2.7 V, $T_A$ = 10 °C

3) The module $I_{DDx}$ values are calculated from the component $I_{DDx}$ data sheet values as:
**m** × $I_{DDx}$[component] + **n** × $I_{DD3N}$[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O ($I_{DDQ}$) currents are not included into calculations: module $I_{DD}$ values will be measured differently depending on load conditions

5) The module $I_{DDx}$ values are calculated from the corrponent $I_{DDx}$ data sheet values as: (**m** + **n**) × $I_{DDx}$[component]

**Table 13 Operating, Standby and Refresh Currents (PC2700, –6)**

| Part Number & Organization | HYS64D16301GU–6–B | | HYS64D32300GU–6–B | | HYS72D32300GU–6–B | | HYS64D64320GU–6–B | | HYS72D64320GU–6–B | | Unit | Note 1)2) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 128MB ×64 | | 256MB ×64 | | 256MB ×72 | | 512MB ×64 | | 512MB ×72 | | | |
| | 1 rank | | 1 rank | | 1 rank | | 2 ranks | | 2 ranks | | | |
| **Symbol** | **typ.** | **max.** | **typ.** | **max.** | **typ.** | **max.** | **typ.** | **max.** | **typ.** | **max.** | | |
| $I_{DD0}$ | 352 | 460 | 680 | 880 | 765 | 990 | 1160 | 1400 | 1305 | 1575 | mA | 3) |
| $I_{DD1}$ | 416 | 500 | 800 | 960 | 900 | 1080 | 1280 | 1480 | 1440 | 1665 | mA | 3)4) |
| $I_{DD2P}$ | 24 | 36 | 48 | 72 | 54 | 81 | 96 | 144 | 108 | 162 | mA | 5) |
| $I_{DD2F}$ | 180 | 220 | 360 | 440 | 405 | 495 | 720 | 880 | 810 | 990 | mA | 5) |
| $I_{DD2Q}$ | 98.8 | 112 | 197.6 | 224 | 222.3 | 252 | 395.2 | 448 | 444.6 | 504 | mA | 5) |
| $I_{DD3P}$ | 72 | 84 | 144 | 168 | 162 | 189 | 288 | 336 | 324 | 378 | mA | 5) |
| $I_{DD3N}$ | 252 | 280 | 480 | 520 | 540 | 585 | 960 | 1040 | 1080 | 1170 | mA | 5) |
| $I_{DD4R}$ | 496 | 640 | 880 | 1120 | 990 | 1260 | 1360 | 1640 | 1530 | 1845 | mA | 3)4) |
| $I_{DD4W}$ | 564 | 660 | 1000 | 1160 | 1125 | 1305 | 1480 | 1680 | 1665 | 1890 | mA | 3) |
| $I_{DD5}$ | 574 | 760 | 1148 | 1520 | 1292 | 1710 | 1628 | 2040 | 1832 | 2295 | mA | 3) |
| $I_{DD6}$ | 6 | 10 | 12 | 20 | 13.5 | 22.5 | 24 | 40 | 27 | 45 | mA | 5) |
| $I_{DD7}$ | 872 | 1140 | 1662 | 2160 | 1870 | 2430 | 2142 | 2680 | 2410 | 3015 | mA | 3)4) |

1) DRAM component currents only

2) Test condition for maximum values: $V_{DD}$ = 2.7 V, $T_A$ = 10 °C

3) The module $I_{DDx}$ values are calculated from the component $I_{DDx}$ data sheet values as:
**m** × $I_{DDx}$[component] + **n** × $I_{DD3N}$[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O ($I_{DDQ}$) currents are not included into calculations: module $I_{DD}$ values will be measured differently depending on load conditions

5) The module $I_{DDx}$ values are calculated from the corrponent $I_{DDx}$ data sheet values as: (**m** + **n**) × $I_{DDx}$[component]

**Table 14 Operating, Standby and Refresh Currents (PC3200, –5)**

| Part Number & Organization | HYS64D16301GU–5–B | | HYS64D32300GU–5–B | | HYS72D32300GU–5–B | | HYS64D64320GU–5–B | | HYS72D64320GU–5–B | | Unit | Note[1)2)] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 128MB ×64 | | 256MB ×64 | | 256MB ×72 | | 512MB ×64 | | 512MB ×72 | | | |
| | 1 rank | | 1 rank | | 1 rank | | 2 ranks | | 2 ranks | | | |
| **Symbol** | **typ.** | **max.** | **typ.** | **max.** | **typ.** | **max.** | **typ.** | **max.** | **typ.** | **max.** | | |
| $I_{DD0}$ | 400 | 480 | 720 | 920 | 810 | 1035 | 1176 | 1472 | 132 | 1656 | mA | 3) |
| $I_{DD1}$ | 460 | 540 | 840 | 1000 | 945 | 1125 | 1296 | 1552 | 1458 | 1746 | mA | 3)4) |
| $I_{DD2P}$ | 24 | 36 | 48 | 72 | 54 | 81 | 96 | 144 | 108 | 162 | mA | 5) |
| $I_{DD2F}$ | 184 | 224 | 368 | 448 | 414 | 504 | 736 | 896 | 828 | 1008 | mA | 5) |
| $I_{DD2Q}$ | 96 | 136 | 192 | 272 | 216 | 306 | 384 | 544 | 432 | 612 | mA | 5) |
| $I_{DD3P}$ | 68 | 96 | 136 | 192 | 153 | 216 | 272 | 384 | 306 | 432 | mA | 5) |
| $I_{DD3N}$ | 240 | 296 | 456 | 552 | 513 | 621 | 912 | 1104 | 1026 | 1242 | mA | 5) |
| $I_{DD4R}$ | 560 | 700 | 920 | 1160 | 1035 | 1305 | 1376 | 1712 | 1548 | 1926 | mA | 3)4) |
| $I_{DD4W}$ | 600 | 720 | 1000 | 1200 | 1125 | 1350 | 1456 | 1752 | 1638 | 1971 | mA | 3) |
| $I_{DD5}$ | 620 | 780 | 1240 | 1560 | 1395 | 1755 | 1696 | 2112 | 1908 | 2376 | mA | 3) |
| $I_{DD6}$ | 6.4 | 10.4 | 12.8 | 20.8 | 14.4 | 23.4 | 25.6 | 41.6 | 28.8 | 46.8 | mA | 5) |
| $I_{DD7}$ | 1040 | 1240 | 1920 | 2240 | 2160 | 2520 | 2376 | 2792 | 2673 | 3141 | mA | 3)4) |

1) DRAM component currents only

2) Test condition for maximum values: $V_{DD}$ = 2.7 V, $T_A$ = 10 °C

3) The module $I_{DDx}$ values are calculated from the component $I_{DDx}$ data sheet values as:
**m** × $I_{DDx}$[component] + **n** × $I_{DD3N}$[component] with **m** and **n** number of components of rank 1 and 2; **n**=0 for 1 rank modules

4) DQ I/O ($I_{DDQ}$) currents are not included into calculations: module $I_{DD}$ values will be measured differently depending on load conditions

5) The module $I_{DDx}$ values are calculated from the corrponent $I_{DDx}$ data sheet values as: (**m** + **n**) × $I_{DDx}$[component]

## 3.3 AC Characteristics

**Table 15 AC Timing - Absolute Specifications –8/–7/–7F**

| Parameter | Symbol | –8 | | –7 | | –7F | | Unit | Note/ Test Condition [1] |
|---|---|---|---|---|---|---|---|---|---|
| | | DDR200 | | DDR266A | | DDR266 | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| DQ output access time from CK/$\overline{CK}$ | $t_{AC}$ | –0.8 | +0.8 | –0.75 | +0.75 | –0.75 | +0.75 | ns | 2)3)4)5) |
| DQS output access time from CK/$\overline{CK}$ | $t_{DQSCK}$ | –0.8 | +0.8 | –0.75 | +0.75 | –0.75 | +0.75 | ns | 2)3)4)5) |
| CK high-level width | $t_{CH}$ | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ | 2)3)4)5) |
| CK low-level width | $t_{CL}$ | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ | 2)3)4)5) |
| Clock Half Period | $t_{HP}$ | min. ($t_{CL}$, $t_{CH}$) | | min. ($t_{CL}$, $t_{CH}$) | | min. ($t_{CL}$, $t_{CH}$) | | ns | 2)3)4)5) |
| Clock cycle time | $t_{CK3}$ | 8 | 12 | 7 | 12 | 7 | 12 | ns | CL = 3.0 2)3)4)5) |
| | $t_{CK2.5}$ | 8 | 12 | 7 | 12 | 7 | 12 | ns | CL = 2.5 2)3)4)5) |
| | $t_{CK2}$ | 10 | 12 | 7.5 | 12 | 7.5 | 12 | ns | CL = 2.0 2)3)4)5) |
| | $t_{CK1.5}$ | 10 | 12 | — | — | — | — | ns | CL = 1.5 2)3)4)5) |
| DQ and DM input hold time | $t_{DH}$ | 0.6 | — | 0.5 | — | 0.5 | — | ns | 2)3)4)5) |
| DQ and DM input setup time | $t_{DS}$ | 0.6 | — | 0.5 | — | 0.5 | — | ns | 2)3)4)5) |
| Control and Addr. input pulse width (each input) | $t_{IPW}$ | 2.5 | — | 2.2 | — | 2.2 | — | ns | 2)3)4)5)6) |
| DQ and DM input pulse width (each input) | $t_{DIPW}$ | 2.0 | — | 1.75 | — | 1.75 | — | ns | 2)3)4)5)6) |
| Data-out high-impedance time from CK/$\overline{CK}$ | $t_{HZ}$ | –0.8 | +0.8 | –0.75 | +0.75 | –0.75 | +0.75 | ns | 2)3)4)5)7) |
| Data-out low-impedance time from CK/$\overline{CK}$ | $t_{LZ}$ | –0.8 | +0.8 | –0.75 | +0.75 | –0.75 | +0.75 | ns | 2)3)4)5)7) |
| Write command to 1st DQS latching transition | $t_{DQSS}$ | 0.75 | 1.25 | 0.75 | 1.25 | 0.75 | 1.25 | $t_{CK}$ | 2)3)4)5) |
| DQS-DQ skew (DQS and associated DQ signals) | $t_{DQSQ}$ | — | +0.6 | — | +0.5 | — | +0.5 | ns | 2)3)4)5) |
| Data hold skew factor | $t_{QHS}$ | — | 1.0 | — | 0.75 | — | 0.75 | ns | 2)3)4)5) |
| DQ/DQS output hold time | $t_{QH}$ | $t_{HP}$ – $t_{QHS}$ | — | $t_{HP}$ – $t_{QHS}$ | — | $t_{HP}$ – $t_{QHS}$ | — | ns | 2)3)4)5) |
| DQS input low (high) pulse width (write cycle) | $t_{DQSL,H}$ | 0.35 | — | 0.35 | — | 0.35 | — | $t_{CK}$ | 2)3)4)5) |
| DQS falling edge to CK setup time (write cycle) | $t_{DSS}$ | 0.2 | — | 0.2 | — | 0.2 | — | $t_{CK}$ | 2)3)4)5) |
| DQS falling edge hold time from CK (write cycle) | $t_{DSH}$ | 0.2 | — | 0.2 | — | 0.2 | — | $t_{CK}$ | 2)3)4)5) |
| Mode register set command cycle time | $t_{MRD}$ | 2 | — | 2 | — | 2 | — | $t_{CK}$ | 2)3)4)5) |
| Write preamble setup time | $t_{WPRES}$ | 0 | — | 0 | — | 0 | — | ns | 2)3)4)5)8) |
| Write postamble | $t_{WPST}$ | 0.40 | 0.60 | 0.40 | 0.60 | 0.40 | 0.60 | $t_{CK}$ | 2)3)4)5)9) |
| Write preamble | $t_{WPRE}$ | 0.25 | — | 0.25 | — | 0.25 | — | $t_{CK}$ | 2)3)4)5) |

**Table 15 AC Timing - Absolute Specifications –8/–7/–7F** (cont'd)

| Parameter | Symbol | –8 | | –7 | | –7F | | Unit | Note/ Test Condition [1] |
|---|---|---|---|---|---|---|---|---|---|
| | | DDR200 | | DDR266A | | DDR266 | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Address and control input setup time | $t_{IS}$ | 1.1 | — | 0.9 | — | 0.9 | — | ns | fast slew rate 3)4)5)6)10) |
| | | 1.1 | — | 1.0 | — | 1.0 | — | ns | slow slew rate 3)4)5)6)10) |
| Address and control input hold time | $t_{IH}$ | 1.1 | — | 0.9 | — | 0.9 | — | ns | fast slew rate 3)4)5)6)10) |
| | | 1.1 | — | 1.0 | — | 1.0 | — | ns | slow slew rate 3)4)5)6)10) |
| Read preamble | $t_{RPRE}$ | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ | CL > 1.5 2)3)4)5) |
| | $t_{RPRE1.5}$ | 0.9 | 1.1 | NA | | NA | | $t_{CK}$ | CL = 1.5 2)3)4)5)11) |
| Read preamble setup time | $t_{RPRES}$ | 1.5 | — | NA | | NA | | ns | 2)3)4)5)12) |
| Read postamble | $t_{RPST}$ | 0.40 | 0.60 | 0.40 | 0.60 | 0.40 | 0.60 | $t_{CK}$ | 2)3)4)5) |
| Active to Precharge command | $t_{RAS}$ | 50 | 120 E+3 | 45 | 120 E+3 | 45 | 120 E+3 | ns | 2)3)4)5) |
| Active to Active/Auto-refresh command period | $t_{RC}$ | 70 | — | 65 | — | 60 | — | ns | 2)3)4)5) |
| Auto-refresh to Active/Auto-refresh command period | $t_{RFC}$ | 80 | — | 75 | — | 75 | — | ns | 2)3)4)5) |
| Active to Read or Write delay | $t_{RCD}$ | 20 | — | 20 | — | 15 | — | ns | 2)3)4)5) |
| Precharge command period | $t_{RP}$ | 20 | — | 20 | — | 15 | — | ns | 2)3)4)5) |
| Active to Autoprecharge delay | $t_{RAP}$ | 20 | — | 20 | — | 15 | — | ns | 2)3)4)5) |
| Active bank A to Active bank B command | $t_{RRD}$ | 15 | — | 15 | — | 15 | — | ns | 2)3)4)5) |
| Write recovery time | $t_{WR}$ | 15 | — | 15 | — | 15 | — | ns | 2)3)4)5) |
| Auto precharge write recovery + precharge time | $t_{DAL}$ | $(t_{wr}/t_{CK}) + (t_{rp}/t_{CK})$ | | | | | | $t_{CK}$ | 2)3)4)5)13) |
| Internal write to read command delay | $t_{WTR}$ | 1 | — | 1 | — | 1 | — | $t_{CK}$ | CL > 1.5 2)3)4)5) |
| | $t_{WTR1.5}$ | 2 | — | — | — | — | — | $t_{CK}$ | CL = 1.5 2)3)4)5) |
| Exit self-refresh to non-read command | $t_{XSNR}$ | 80 | — | 75 | — | 75 | — | ns | 2)3)4)5) |
| Exit self-refresh to read command | $t_{XSRD}$ | 200 | — | 200 | — | 200 | — | $t_{CK}$ | 2)3)4)5) |
| Average Periodic Refresh Interval | $t_{REFI}$ | — | 7.8 | — | 7.8 | — | 7.8 | µs | 2)3)4)5)14) |

1) 0 °C ≤$T_A$ ≤70 °C; $V_{DDQ}$ = 2.5 V ±0.2 V, $V_{DD}$ = +2.5 V ±0.2 V

2) Input slew rate ≥ 1 V/ns for DDR400, DDR333, DDR266, and = 1 V/ns for DDR200

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is $V_{REF}$. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until $V_{REF}$ stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is $V_{TT}$.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) $t_{HZ}$ and $t_{LZ}$ transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on $t_{DQSS}$.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.

11) CAS Latency 1.5 operation is supported on DDR200 devices only

12) $t_{RPRES}$ is defined for CL = 1.5 operation only

13) For each of the terms, if not already an integer, round to the next highest integer. $t_{CK}$ is equal to the actual system clock cycle time.

14) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

**Table 16 AC Timing - Absolute Specifications –6/–5**

| Parameter | Symbol | –6 | | –5 | | Unit | Note/ Test Condition [1] |
|---|---|---|---|---|---|---|---|
| | | DDR333 | | DDR400B | | | |
| | | Min. | Max. | Min. | Max. | | |
| DQ output access time from CK/$\overline{CK}$ | $t_{AC}$ | –0.7 | +0.7 | –0.6 | +0.6 | ns | 2)3)4)5) |
| DQS output access time from CK/$\overline{CK}$ | $t_{DQSCK}$ | –0.6 | +0.6 | –0.5 | +0.5 | ns | 2)3)4)5) |
| CK high-level width | $t_{CH}$ | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ | 2)3)4)5) |
| CK low-level width | $t_{CL}$ | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ | 2)3)4)5) |
| Clock Half Period | $t_{HP}$ | min. ($t_{CL}$, $t_{CH}$) | | min. ($t_{CL}$, $t_{CH}$) | | ns | 2)3)4)5) |
| Clock cycle time | $t_{CK}$ | 6 | 12 | 5 | 12 | ns | CL = 3.0 2)3)4)5) |
| | | 6 | 12 | 6 | 12 | ns | CL = 2.5 2)3)4)5) |
| | | 7.5 | 12 | 7.5 | 12 | ns | CL = 2.0 2)3)4)5) |
| DQ and DM input hold time | $t_{DH}$ | 0.45 | — | 0.4 | — | ns | 2)3)4)5) |
| DQ and DM input setup time | $t_{DS}$ | 0.45 | — | 0.4 | — | ns | 2)3)4)5) |
| Control and Addr. input pulse width (each input) | $t_{IPW}$ | 2.2 | — | tbd | — | ns | 2)3)4)5)6) |
| DQ and DM input pulse width (each input) | $t_{DIPW}$ | 1.75 | — | tbd | — | ns | 2)3)4)5)6) |
| Data-out high-impedance time from CK/$\overline{CK}$ | $t_{HZ}$ | –0.7 | +0.7 | –0.6 | +0.6 | ns | 2)3)4)5)7) |
| Data-out low-impedance time from CK/$\overline{CK}$ | $t_{LZ}$ | –0.7 | +0.7 | –0.6 | +0.6 | ns | 2)3)4)5)7) |
| Write command to 1st DQS latching transition | $t_{DQSS}$ | 0.75 | 1.25 | 0.75 | 1.25 | $t_{CK}$ | 2)3)4)5) |
| DQS-DQ skew (DQS and associated DQ signals) | $t_{DQSQ}$ | — | +0.40 | — | +0.40 | ns | TFBGA 2)3)4)5) |
| | | — | +0.45 | — | +0.40 | ns | TSOPII 2)3)4)5) |
| Data hold skew factor | $t_{QHS}$ | — | +0.50 | — | +0.50 | ns | TFBGA 2)3)4)5) |
| | | — | +0.55 | — | +0.50 | ns | TSOPII 2)3)4)5) |
| DQ/DQS output hold time | $t_{QH}$ | $t_{HP} - t_{QHS}$ | — | $t_{HP} - t_{QHS}$ | — | ns | 2)3)4)5) |
| DQS input low (high) pulse width (write cycle) | $t_{DQSL,H}$ | 0.35 | — | 0.35 | — | $t_{CK}$ | 2)3)4)5) |

**Table 16 AC Timing - Absolute Specifications –6/–5** (cont'd)

| Parameter | Symbol | –6 | | –5 | | Unit | Note/ Test Condition [1] |
|---|---|---|---|---|---|---|---|
| | | DDR333 | | DDR400B | | | |
| | | Min. | Max. | Min. | Max. | | |
| DQS falling edge to CK setup time (write cycle) | $t_{DSS}$ | 0.2 | — | 0.2 | — | $t_{CK}$ | 2)3)4)5) |
| DQS falling edge hold time from CK (write cycle) | $t_{DSH}$ | 0.2 | — | 0.2 | — | $t_{CK}$ | 2)3)4)5) |
| Mode register set command cycle time | $t_{MRD}$ | 2 | — | 2 | — | $t_{CK}$ | 2)3)4)5) |
| Write preamble setup time | $t_{WPRES}$ | 0 | — | 0 | — | ns | 2)3)4)5)8) |
| Write postamble | $t_{WPST}$ | 0.40 | 0.60 | 0.40 | 0.60 | $t_{CK}$ | 2)3)4)5)9) |
| Write preamble | $t_{WPRE}$ | 0.25 | — | 0.25 | — | $t_{CK}$ | 2)3)4)5) |
| Address and control input setup time | $t_{IS}$ | 0.75 | — | 0.6 | — | ns | fast slew rate 3)4)5)6)10) |
| | | 0.8 | — | NA | | ns | slow slew rate 3)4)5)6)10) |
| Address and control input hold time | $t_{IH}$ | 0.75 | — | 0.6 | — | ns | fast slew rate 3)4)5)6)10) |
| | | 0.8 | — | NA | | ns | slow slew rate 3)4)5)6)10) |
| Read preamble | $t_{RPRE}$ | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ | 2)3)4)5) |
| Read postamble | $t_{RPST}$ | 0.40 | 0.60 | 0.40 | 0.60 | $t_{CK}$ | 2)3)4)5) |
| Active to Precharge command | $t_{RAS}$ | 42 | 70E+3 | 40 | 70E+3 | ns | 2)3)4)5) |
| Active to Active/Auto-refresh command period | $t_{RC}$ | 60 | — | 55 | — | ns | 2)3)4)5) |
| Auto-refresh to Active/Auto-refresh command period | $t_{RFC}$ | 72 | — | 65 | — | ns | 2)3)4)5) |
| Active to Read or Write delay | $t_{RCD}$ | 18 | — | 15 | — | ns | 2)3)4)5) |
| Precharge command period | $t_{RP}$ | 18 | — | 15 | — | ns | 2)3)4)5) |
| Active to Autoprecharge delay | $t_{RAP}$ | 18 | — | 15 | — | ns | 2)3)4)5) |
| Active bank A to Active bank B command | $t_{RRD}$ | 12 | — | 10 | — | ns | 2)3)4)5) |
| Write recovery time | $t_{WR}$ | 15 | — | 15 | — | ns | 2)3)4)5) |
| Auto precharge write recovery + precharge time | $t_{DAL}$ | | | | | $t_{CK}$ | 2)3)4)5)11) |
| Internal write to read command delay | $t_{WTR}$ | 1 | — | 1 | — | $t_{CK}$ | 2)3)4)5) |
| Exit self-refresh to non-read command | $t_{XSNR}$ | 75 | — | 75 | — | ns | 2)3)4)5) |
| Exit self-refresh to read command | $t_{XSRD}$ | 200 | — | 200 | — | $t_{CK}$ | 2)3)4)5) |
| Average Periodic Refresh Interval | $t_{REFI}$ | — | 7.8 | — | 7.8 | µs | 2)3)4)5)12) |

1) 0 °C ≤$T_A$ ≤70 °C; $V_{DDQ}$ = 2.5 V ±0.2 V, $V_{DD}$ = +2.5 V ±0.2 V (DDR333); $V_{DDQ}$ = 2.6 V ±0.1 V, $V_{DD}$ = +2.6 V ±0.1 V (DDR400)

2) Input slew rate ≥ 1 V/ns for DDR400, DDR333

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is $V_{REF}$. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until $V_{REF}$ stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is $V_{TT}$.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) $t_{HZ}$ and $t_{LZ}$ transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on $t_{DQSS}$.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.

11) For each of the terms, if not already an integer, round to the next highest integer. $t_{CK}$ is equal to the actual system clock cycle time.

12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

# 4 SPD Contents

**Table 17 Operating, Standby and Refresh Currents (PC1600, –8)**

| | | Part Number & Organization | HYS64D16301GU–8–B | HYS64D32300GU–8–B | HYS72D32300GU–8–B | HYS64D64320GU–8–B | HYS72D64320GU–8–B |
|---|---|---|---|---|---|---|---|
| | | | 128MB | 256MB | 256MB | 512MB | 512MB |
| | | | ×64 | ×64 | ×72 | ×64 | ×72 |
| | | | 1 rank | 1 rank | 1 rank | 2 ranks | 2 ranks |
| **Byte** | **Description** | | **HEX** | **HEX** | **HEX** | **HEX** | **HEX** |
| 0 | Number of SPD Bytes | 128 | 80 | 80 | 80 | 80 | 80 |
| 1 | Total Bytes in Serial PD | 256 | 08 | 08 | 08 | 08 | 08 |
| 2 | Memory Type | DDR-SDRAM | 07 | 07 | 07 | 07 | 07 |
| 3 | Number of Row Addresses | 13 | 0D | 0D | 0D | 0D | 0D |
| 4 | Number of Column Addresses | 9/10 | 09 | 0A | 0A | 0A | 0A |
| 5 | Number of DIMM Banks | 1/2 | 01 | 01 | 01 | 02 | 01 |
| 6 | Module Data Width | ×64/×72 | 40 | 40 | 48 | 40 | 48 |
| 7 | Module Data Width (cont'd) | 0 | 00 | 00 | 00 | 00 | 00 |
| 8 | Module Interface Levels | SSTL_2.5 | 04 | 04 | 04 | 04 | 04 |
| 9 | SDRAM Cycle Time at CL = 2.5 | 8 ns | 80 | 80 | 80 | 80 | 80 |
| 10 | Access Time from Clock at CL = 2.5 | 0.8 ns | 80 | 80 | 80 | 80 | 80 |
| 11 | DIMM config | non-ECC/ECC | 00 | 00 | 02 | 00 | 02 |
| 12 | Refresh Rate/Type | Self-Refresh 7.8 µs | 82 | 82 | 82 | 82 | 82 |
| 13 | SDRAM Width, Primary | ×16/ ×8 | 10 | 08 | 08 | 08 | 08 |
| 14 | Error Checking SDRAM Data Witdh | na/ ×8 | 00 | 00 | 08 | 00 | 08 |
| 15 | Minimum Clock Delay for Back-to-Back Random Column Address | $t_{CCD}$ = 1 CLK | 01 | 01 | 01 | 01 | 01 |
| 16 | Burst Length Supported | 2, 4 & 8 | 0E | 0E | 0E | 0E | 0E |

**Table 17 Operating, Standby and Refresh Currents (PC1600, –8)** (cont'd)

| | | Part Number & Organization | HYS64D16301GU–8–B | HYS64D32300GU–8–B | HYS72D32300GU–8–B | HYS64D64320GU–8–B | HYS72D64320GU–8–B |
|---|---|---|---|---|---|---|---|
| | | | 128MB | 256MB | 256MB | 512MB | 512MB |
| | | | ×64 | ×64 | ×72 | ×64 | ×72 |
| | | | 1 rank | 1 rank | 1 rank | 2 ranks | 2 ranks |
| **Byte** | **Description** | | **HEX** | **HEX** | **HEX** | **HEX** | **HEX** |
| 17 | Number of SDRAM Banks | 4 | 04 | 04 | 04 | 04 | 04 |
| 18 | Supported CAS Latencies | CAS latency = 2 & 2.5 | 0C | 0C | 0C | 0C | 0C |
| 19 | CS Latencies | CS latency = 0 | 01 | 01 | 01 | 01 | 01 |
| 20 | WE Latencies | Write latency = 1 | 02 | 02 | 02 | 02 | 02 |
| 21 | SDRAM DIMM Module Attributes | unbuffered | 20 | 20 | 20 | 20 | 20 |
| 22 | SDRAM Device Attributes: General | – | C0 | C0 | C0 | C0 | C0 |
| 23 | Min. Clock Cycle Time at CAS Latency = 2 | 10 ns | A0 | A0 | A0 | A0 | A0 |
| 24 | Access Time from Clock for CL = 2 | 0.8 ns | 80 | 80 | 80 | 80 | 80 |
| 25 | Minimum Clock Cycle Time for CL = 1.5 | not supported | 00 | 00 | 00 | 00 | 00 |
| 26 | Access Time from Clock at CL = 1.5 | not supported | 00 | 00 | 00 | 00 | 00 |
| 27 | Minimum Row Precharge Time | 20 ns | 50 | 50 | 50 | 50 | 50 |
| 28 | Minimum Row Act. to Row Act. Delay $t_{RRD}$ | 15 ns | 3C | 3C | 3C | 3C | 3C |
| 29 | Minimum RAS to CAS Delay $t_{RCD}$ | 20 ns | 50 | 50 | 50 | 50 | 50 |
| 30 | Minimum RAS Pulse Width $t_{RAS}$ | 50 ns | 32 | 32 | 32 | 32 | 32 |
| 31 | Module Bank Density (per Bank) | 256 MByte | 20 | 40 | 40 | 40 | 40 |
| 32 | Addr. and Command Setup Time | 1.1 ns | B0 | B0 | B0 | B0 | B0 |
| 33 | Addr. and Command Hold Time | 1.1 ns | B0 | B0 | B0 | B0 | B0 |

**Table 17 Operating, Standby and Refresh Currents (PC1600, –8)** (cont'd)

| | | Part Number & Organization | HYS64D16301GU–8–B | HYS64D32300GU–8–B | HYS72D32300GU–8–B | HYS64D64320GU–8–B | HYS72D64320GU–8–B |
|---|---|---|---|---|---|---|---|
| | | | 128MB | 256MB | 256MB | 512MB | 512MB |
| | | | ×64 | ×64 | ×72 | ×64 | ×72 |
| | | | 1 rank | 1 rank | 1 rank | 2 ranks | 2 ranks |
| **Byte** | **Description** | | **HEX** | **HEX** | **HEX** | **HEX** | **HEX** |
| 34 | Data Input Setup Time | 0.6 ns | 60 | 60 | 60 | 60 | 60 |
| 35 | Data Input Hold Time | 0.6 ns | 60 | 60 | 60 | 60 | 60 |
| 36 to 40 | Superset Information | – | 00 | 00 | 00 | 00 | 00 |
| 41 | Minimum Core Cycle Time $t_{RC}$ | 70 ns | 46 | 46 | 46 | 46 | 46 |
| 42 | Min. Auto Refresh Cmd Cycle Time $t_{FRC}$ | 80 ns | 50 | 50 | 50 | 48 | 50 |
| 43 | Maximum Clock Cycle Time $t_{CK}$ | 12 ns | 30 | 30 | 30 | 30 | 30 |
| 44 | Max. DQS-DQ Skew $t_{DQSQ}$ | 0.6 ns | 3C | 3C | 3C | 3C | 3C |
| 45 | X-Factor tQHS | 1.0 ns | A0 | A0 | A0 | A0 | A0 |
| 46 to 61 | Superset Information | – | 00 | 00 | 00 | 00 | 00 |
| 62 | SPD Revision | Revision 0.0 | 00 | 00 | 00 | 00 | 00 |
| 63 | Checksum for Bytes 0 - 62 | – | E8 | A7 | B9 | A8 | B9 |
| 64 | Manufacturers JEDEC ID Codes | – | C1 | C1 | C1 | C1 | C1 |
| 65 to 71 | Manufacturer | – | Infineon | Infineon | Infineon | Infineon | Infineon |
| 72 | Module Assembly Location | – | – | – | – | – | – |
| 73 to 90 | Module Part Number | – | – | – | – | – | – |
| 91 to 92 | Module Revision Code | – | – | – | – | – | – |
| 93 to 94 | Module Manufacturing Date | – | – | – | – | – | – |
| 95 to 98 | Module Serial Number | – | – | – | – | – | – |
| 99 to 127 | – | – | – | – | – | – | – |
| 128 to 255 | open for Customer use | – | – | – | – | – | – |

**Table 18 SPD Codes for PC2100 Modules “–7”**

| | | Part Number & Organization | HYS64D16301GU–7–B | HYS64D32300GU–7–B HYS64D32300EU–7–B | HYS72D32300GU–7–B | HYS64D64320GU–7–B | HYS72D64320GU–7–B |
|---|---|---|---|---|---|---|---|
| | | | 128MB | 256MB | 256MB | 512MB | 512MB |
| | | | ×64 | ×64 | ×72 | ×64 | ×72 |
| | | | 1 rank | 1 rank | 1 rank | 2 ranks | 2 ranks |
| **Byte** | **Description** | | **HEX** | **HEX** | **HEX** | **HEX** | **HEX** |
| 0 | Number of SPD Bytes | 128 | 80 | 80 | 80 | 80 | 80 |
| 1 | Total Bytes in Serial PD | 256 | 08 | 08 | 08 | 08 | 08 |
| 2 | Memory Type | DDR-SDRAM | 07 | 07 | 07 | 07 | 07 |
| 3 | Number of Row Addresses | 13 | 0D | 0D | 0D | 0D | 0D |
| 4 | Number of Column Addresses | 9/10 | 09 | 0A | 0A | 0A | 0A |
| 5 | Number of DIMM Banks | 1/2 | 01 | 01 | 01 | 02 | 01 |
| 6 | Module Data Width | ×64/×72 | 40 | 40 | 48 | 40 | 48 |
| 7 | Module Data Width (cont’d) | 0 | 00 | 00 | 00 | 00 | 00 |
| 8 | Module Interface Levels | SSTL_2.5 | 04 | 04 | 04 | 04 | 04 |
| 9 | SDRAM Cycle Time at CL = 2.5 | 7 ns | 70 | 70 | 70 | 70 | 70 |
| 10 | Access Time from Clock at CL = 2.5 | 0.75 ns | 75 | 75 | 75 | 75 | 75 |
| 11 | DIMM config | non-ECC/ECC | 00 | 00 | 02 | 00 | 02 |
| 12 | Refresh Rate/Type | Self-Refresh 7.8 µs | 82 | 82 | 82 | 82 | 82 |
| 13 | SDRAM Width, Primary | ×16/×8 | 10 | 08 | 08 | 08 | 08 |
| 14 | Error Checking SDRAM Data Witdh | na/×8 | 00 | 00 | 08 | 00 | 08 |
| 15 | Minimum Clock Delay for Back-to-Back Random Column Address | $t_{CCD}$ = 1 CLK | 01 | 01 | 01 | 01 | 01 |
| 16 | Burst Length Supported | 2, 4 & 8 | 0E | 0E | 0E | 0E | 0E |
| 17 | Number of SDRAM Banks | 4 | 04 | 04 | 04 | 04 | 04 |

**Table 18 SPD Codes for PC2100 Modules "–7"** (cont'd)

| | | Part Number & Organization | HYS64D16301GU–7–B | HYS64D32300GU–7–B HYS64D32300EU–7–B | HYS72D32300GU–7–B | HYS64D64320GU–7–B | HYS72D64320GU–7–B |
|---|---|---|---|---|---|---|---|
| | | | **128MB** | **256MB** | **256MB** | **512MB** | **512MB** |
| | | | **×64** | **×64** | **×72** | **×64** | **×72** |
| | | | **1 rank** | **1 rank** | **1 rank** | **2 ranks** | **2 ranks** |
| **Byte** | **Description** | | **HEX** | **HEX** | **HEX** | **HEX** | **HEX** |
| 18 | Supported CAS Latencies | CAS latency = 2 & 2.5 | 0C | 0C | 0C | 0C | 0C |
| 19 | CS Latencies | CS latency = 0 | 01 | 01 | 01 | 01 | 01 |
| 20 | WE Latencies | Write latency = 1 | 02 | 02 | 02 | 02 | 02 |
| 21 | SDRAM DIMM Module Attributes | unbuffered | 20 | 20 | 20 | 20 | 20 |
| 22 | SDRAM Device Attributes: General | – | C0 | C0 | C0 | C0 | C0 |
| 23 | Min. Clock Cycle Time at CAS Latency = 2 | 7.5 ns | 75 | 75 | 75 | 75 | 75 |
| 24 | Access Time from Clock for CL = 2 | 0.75 ns | 75 | 75 | 75 | 75 | 75 |
| 25 | Minimum Clock Cycle Time for CL = 1.5 | not supported | 00 | 00 | 00 | 00 | 00 |
| 26 | Access Time from Clock at CL = 1.5 | not supported | 00 | 00 | 00 | 00 | 00 |
| 27 | Minimum Row Precharge Time | 20 ns | 50 | 50 | 50 | 50 | 50 |
| 28 | Minimum Row Act. to Row Act. Delay $t_{RRD}$ | 15 ns | 3C | 3C | 3C | 3C | 3C |
| 29 | Minimum RAS to CAS Delay $t_{RCD}$ | 20 ns | 50 | 50 | 50 | 50 | 50 |
| 30 | Minimum RAS Pulse Width $t_{RAS}$ | 45 ns | 2D | 2D | 2D | 2D | 2D |
| 31 | Module Bank Density (per Bank) | 128 MByte/256 MByte | 20 | 40 | 40 | 40 | 40 |
| 32 | Addr. and Command Setup Time | 0.9 ns | 90 | 90 | 90 | 90 | 90 |
| 33 | Addr. and Command Hold Time | 0.9 ns | 90 | 90 | 90 | 90 | 90 |
| 34 | Data Input Setup Time | 0.5 ns | 50 | 50 | 50 | 50 | 50 |
| 35 | Data Input Hold Time | 0.5 ns | 50 | 50 | 50 | 50 | 50 |

**Table 18 SPD Codes for PC2100 Modules "–7"** (cont'd)

| | | Part Number & Organization | HYS64D16301GU–7–B | HYS64D32300GU–7–B HYS64D32300EU–7–B | HYS72D32300GU–7–B | HYS64D64320GU–7–B | HYS72D64320GU–7–B |
|---|---|---|---|---|---|---|---|
| | | | 128MB | 256MB | 256MB | 512MB | 512MB |
| | | | ×64 | ×64 | ×72 | ×64 | ×72 |
| | | | 1 rank | 1 rank | 1 rank | 2 ranks | 2 ranks |
| **Byte** | **Description** | | **HEX** | **HEX** | **HEX** | **HEX** | **HEX** |
| 36 to 40 | Superset Information | – | 00 | 00 | 00 | 00 | 00 |
| 41 | Minimum Core Cycle Time $t_{RC}$ | 65 ns | 41 | 41 | 41 | 41 | 41 |
| 42 | Min. Auto Refresh Cmd Cycle Time $t_{FRC}$ | 75 ns | 4B | 4B | 4B | 4B | 4B |
| 43 | Maximum Clock Cycle Time $t_{CK}$ | 12 ns | 30 | 30 | 30 | 30 | 30 |
| 44 | Max. DQS-DQ Skew $t_{DQSQ}$ | 0.5 ns | 32 | 32 | 32 | 32 | 32 |
| 45 | X-Factor tQHS | 0.75 ns | 75 | 75 | 75 | 75 | 75 |
| 46 to 61 | Superset Information | – | 00 | 00 | 00 | 00 | 00 |
| 62 | SPD Revision | Revision 0.0 | 00 | 00 | 00 | 00 | 00 |
| 63 | Checksum for Bytes 0 - 62 | – | 99 | B2 | C4 | B3 | C4 |
| 64 | Manufacturers JEDEC ID Codes | – | C1 | C1 | C1 | C1 | C1 |
| 65 to 71 | Manufacturer | – | Infineon | Infineon | Infineon | Infineon | Infineon |
| 72 | Module Assembly Location | – | – | – | – | – | – |
| 73 to 90 | Module Part Number | – | – | – | – | – | – |
| 91 to 92 | Module Revision Code | – | – | – | – | – | – |
| 93 to 94 | Module Manufacturing Date | – | – | – | – | – | – |
| 95 to 98 | Module Serial Number | – | – | – | – | – | – |
| 99 to 127 | – | – | – | – | – | – | – |
| 128 to 255 | open for Customer use | – | – | – | – | – | – |

**Table 19 SPD Codes for PC2100 Modules "–7F"**

| | | Part Number & Organization | HYS72D32300GU–7F–B | HYS64D64320GU–7F–B |
|---|---|---|---|---|
| | | | 256MB | 512MB |
| | | | ×72 | ×72 |
| | | | 1 rank | 1 rank |
| **Byte** | **Description** | | **HEX** | **HEX** |
| 0 | Number of SPD Bytes | 128 | 80 | 80 |
| 1 | Total Bytes in Serial PD | 256 | 08 | 08 |
| 2 | Memory Type | DDR-SDRAM | 07 | 07 |
| 3 | Number of Row Addresses | 13 | 0D | 0D |
| 4 | Number of Column Addresses | 9/10 | 0A | 0A |
| 5 | Number of DIMM Banks | 1/2 | 01 | 02 |
| 6 | Module Data Width | ×64/×72 | 48 | 48 |
| 7 | Module Data Width (cont'd) | 0 | 00 | 00 |
| 8 | Module Interface Levels | SSTL_2.5 | 04 | 04 |
| 9 | SDRAM Cycle Time at CL = 2.5 | 7 ns | 70 | 70 |
| 10 | Access Time from Clock at CL = 2.5 | 0.75 ns | 75 | 75 |
| 11 | DIMM config | non-ECC/ECC | 02 | 02 |
| 12 | Refresh Rate/Type | Self-Refresh 7.8 µs | 82 | 82 |
| 13 | SDRAM Width, Primary | ×16/×8 | 08 | 08 |
| 14 | Error Checking SDRAM Data Witdh | na/×8 | 08 | 08 |
| 15 | Minimum Clock Delay for Back-to-Back Random Column Address | $t_{CCD}$ = 1 CLK | 01 | 01 |
| 16 | Burst Length Supported | 2, 4 & 8 | 0E | 0E |
| 17 | Number of SDRAM Banks | 4 | 04 | 04 |
| 18 | Supported CAS Latencies | CAS latency = 2 & 2.5 | 0C | 0C |
| 19 | CS Latencies | CS latency = 0 | 01 | 01 |
| 20 | WE Latencies | Write latency = 1 | 02 | 02 |
| 21 | SDRAM DIMM Module Attributes | unbuffered | 20 | 20 |
| 22 | SDRAM Device Attributes: General | – | C0 | C0 |

**Table 19 SPD Codes for PC2100 Modules "–7F"** (cont'd)

| | | Part Number & Organization | HYS72D32300GU–7F–B | HYS64D64320GU–7F–B |
|---|---|---|---|---|
| | | | 256MB | 512MB |
| | | | ×72 | ×72 |
| | | | 1 rank | 1 rank |
| **Byte** | **Description** | | **HEX** | **HEX** |
| 23 | Min. Clock Cycle Time at CAS Latency = 2 | 7.5 ns | 75 | 75 |
| 24 | Access Time from Clock for CL = 2 | 0.75 ns | 75 | 75 |
| 25 | Minimum Clock Cycle Time for CL = 1.5 | not supported | 00 | 00 |
| 26 | Access Time from Clock at CL = 1.5 | not supported | 00 | 00 |
| 27 | Minimum Row Precharge Time | 15 ns | 3C | 3C |
| 28 | Minimum Row Act. to Row Act. Delay $t_{RRD}$ | 15 ns | 3C | 3C |
| 29 | Minimum RAS to CAS Delay $t_{RCD}$ | 15 ns | 3C | 3C |
| 30 | Minimum RAS Pulse Width $t_{RAS}$ | 45 ns | 2D | 2D |
| 31 | Module Bank Density (per Bank) | 128 MByte/256 MByte | 40 | 40 |
| 32 | Addr. and Command Setup Time | 0.9 ns | 90 | 90 |
| 33 | Addr. and Command Hold Time | 0.9 ns | 90 | 90 |
| 34 | Data Input Setup Time | 0.5 ns | 50 | 50 |
| 35 | Data Input Hold Time | 0.5 ns | 50 | 50 |
| 36 to 40 | Superset Information | – | 00 | 00 |
| 41 | Minimum Core Cycle Time $t_{RC}$ | 60 ns | 3C | 3C |
| 42 | Min. Auto Refresh Cmd Cycle Time $t_{FRC}$ | 75 ns | 4B | 4B |
| 43 | Maximum Clock Cycle Time $t_{CK}$ | 12 ns | 30 | 30 |
| 44 | Max. DQS-DQ Skew $t_{DQSQ}$ | 0.5 ns | 32 | 32 |
| 45 | X-Factor tQHS | 0.75 ns | 75 | 75 |

**Table 19 SPD Codes for PC2100 Modules "–7F"** (cont'd)

| | | Part Number & Organization | HYS72D32300GU–7F–B | HYS64D64320GU–7F–B |
|---|---|---|---|---|
| | | | **256MB** | **512MB** |
| | | | **×72** | **×72** |
| | | | **1 rank** | **1 rank** |
| **Byte** | **Description** | | **HEX** | **HEX** |
| 46 to 61 | Superset Information | – | 00 | 00 |
| 62 | SPD Revision | Revision 0.0 | 00 | 00 |
| 63 | Checksum for Bytes 0 - 62 | – | 97 | 98 |
| 64 | Manufactures JEDEC ID Codes | – | C1 | C1 |
| 65 to 71 | Manufacturer | – | Infineon | Infineon |
| 72 | Module Assembly Location | – | – | – |
| 73 to 90 | Module Part Number | – | – | – |
| 91 to 92 | Module Revision Code | – | – | – |
| 93 to 94 | Module Manufacturing Date | – | – | – |
| 95 to 98 | Module Serial Number | – | – | – |
| 99 to 127 | – | – | – | – |
| 128 to 255 | open for Customer use | – | – | – |

**Table 20 SPD Codes for PC2700 Modules “–6”**

| | | Part Number & Organization | HYS64D16301GU–6–B | HYS64D32300GU–6–B | HYS72D32300GU–6–B | HYS64D64320GU–6–B | HYS72D64320GU–6–B |
|---|---|---|---|---|---|---|---|
| | | | 128MB | 256MB | 256MB | 512MB | 512MB |
| | | | ×64 | ×64 | ×72 | ×64 | ×72 |
| | | | 1 rank | 1 rank | 1 rank | 2 ranks | 2 ranks |
| **Byte** | **Description** | | **HEX** | **HEX** | **HEX** | **HEX** | **HEX** |
| 0 | Number of SPD Bytes | 128 | 80 | 80 | 80 | 80 | 80 |
| 1 | Total Bytes in Serial PD | 256 | 08 | 08 | 08 | 08 | 08 |
| 2 | Memory Type | DDR-SDRAM | 07 | 07 | 07 | 07 | 07 |
| 3 | Number of Row Addresses | 13 | 0D | 0D | 0D | 0D | 0D |
| 4 | Number of Column Addresses | 9/10 | 09 | 0A | 0A | 0A | 0A |
| 5 | Number of DIMM Banks | 1/2 | 01 | 01 | 01 | 02 | 01 |
| 6 | Module Data Width | ×64/×72 | 40 | 40 | 48 | 40 | 48 |
| 7 | Module Data Width (cont’d) | 0 | 00 | 00 | 00 | 00 | 00 |
| 8 | Module Interface Levels | SSTL_2.5 | 04 | 04 | 04 | 04 | 04 |
| 9 | SDRAM Cycle Time at CL = 2.5 | 6 ns | 60 | 60 | 60 | 60 | 60 |
| 10 | Access Time from Clock at CL = 2.5 | 0.75 ns | 70 | 70 | 70 | 70 | 70 |
| 11 | DIMM config | non-ECC/ECC | 00 | 00 | 02 | 00 | 02 |
| 12 | Refresh Rate/Type | Self-Refresh 7.8 µs | 82 | 82 | 82 | 82 | 82 |
| 13 | SDRAM Width, Primary | ×16/×8 | 10 | 08 | 08 | 08 | 08 |
| 14 | Error Checking SDRAM Data Witdh | na/×8 | 00 | 00 | 08 | 00 | 08 |
| 15 | Minimum Clock Delay for Back-to-Back Random Column Address | $t_{CCD}$ = 1 CLK | 01 | 01 | 01 | 01 | 01 |
| 16 | Burst Length Supported | 2, 4 & 8 | 0E | 0E | 0E | 0E | 0E |
| 17 | Number of SDRAM Banks | 4 | 04 | 04 | 04 | 04 | 04 |

**Table 20 SPD Codes for PC2700 Modules "–6"** (cont'd)

| | | Part Number & Organization | HYS64D16301GU–6–B | HYS64D32300GU–6–B | HYS72D32300GU–6–B | HYS64D64320GU–6–B | HYS72D64320GU–6–B |
|---|---|---|---|---|---|---|---|
| | | | 128MB | 256MB | 256MB | 512MB | 512MB |
| | | | ×64 | ×64 | ×72 | ×64 | ×72 |
| | | | 1 rank | 1 rank | 1 rank | 2 ranks | 2 ranks |
| **Byte** | **Description** | | **HEX** | **HEX** | **HEX** | **HEX** | **HEX** |
| 18 | Supported CAS Latencies | CAS latency = 2 & 2.5 | 0C | 0C | 0C | 0C | 0C |
| 19 | CS Latencies | CS latency = 0 | 01 | 01 | 01 | 01 | 01 |
| 20 | WE Latencies | Write latency = 1 | 02 | 02 | 02 | 02 | 02 |
| 21 | SDRAM DIMM Module Attributes | unbuffered | 20 | 20 | 20 | 20 | 20 |
| 22 | SDRAM Device Attributes: General | – | C0 | C0 | C0 | C0 | C0 |
| 23 | Min. Clock Cycle Time at CAS Latency = 2 | 7.5 ns | 75 | 75 | 75 | 75 | 75 |
| 24 | Access Time from Clock for CL = 2 | 0.70 ns | 70 | 70 | 70 | 70 | 70 |
| 25 | Minimum Clock Cycle Time for CL = 1.5 | not supported | 00 | 00 | 00 | 00 | 00 |
| 26 | Access Time from Clock at CL = 1.5 | not supported | 00 | 00 | 00 | 00 | 00 |
| 27 | Minimum Row Precharge Time | 18 ns | 48 | 48 | 48 | 48 | 48 |
| 28 | Minimum Row Act. to Row Act. Delay $t_{RRD}$ | 12 ns | 30 | 30 | 30 | 30 | 30 |
| 29 | Minimum RAS to CAS Delay $t_{RCD}$ | 18 ns | 48 | 48 | 48 | 48 | 48 |
| 30 | Minimum RAS Pulse Width $t_{RAS}$ | 42 ns | 2A | 2A | 2A | 2A | 2A |
| 31 | Module Bank Density (per Bank) | 128 MByte/256 MByte | 20 | 40 | 40 | 40 | 40 |
| 32 | Addr. and Command Setup Time | 0.75 ns | 75 | 75 | 75 | 75 | 75 |
| 33 | Addr. and Command Hold Time | 0.75 ns | 75 | 75 | 75 | 75 | 75 |
| 34 | Data Input Setup Time | 0.45 ns | 45 | 45 | 45 | 45 | 45 |
| 35 | Data Input Hold Time | 0.45 ns | 45 | 45 | 45 | 45 | 45 |

**Table 20 SPD Codes for PC2700 Modules "–6"** (cont'd)

| | | Part Number & Organization | HYS64D16301GU–6–B | HYS64D32300GU–6–B | HYS72D32300GU–6–B | HYS64D64320GU–6–B | HYS72D64320GU–6–B |
|---|---|---|---|---|---|---|---|
| | | | 128MB | 256MB | 256MB | 512MB | 512MB |
| | | | ×64 | ×64 | ×72 | ×64 | ×72 |
| | | | 1 rank | 1 rank | 1 rank | 2 ranks | 2 ranks |
| **Byte** | **Description** | | **HEX** | **HEX** | **HEX** | **HEX** | **HEX** |
| 36 to 40 | Superset Information | – | 00 | 00 | 00 | 00 | 00 |
| 41 | Minimum Core Cycle Time $t_{RC}$ | 60 ns | 3C | 3C | 3C | 3C | 3C |
| 42 | Min. Auto Refresh Cmd Cycle Time $t_{FRC}$ | 72 ns | 48 | 48 | 48 | 48 | 48 |
| 43 | Maximum Clock Cycle Time $t_{CK}$ | 12 ns | 30 | 30 | 30 | 30 | 30 |
| 44 | Max. DQS-DQ Skew $t_{DQSQ}$ | 0.45 ns | 2D | 2D | 2D | 2D | 2D |
| 45 | X-Factor tQHS | 0.55 ns | 55 | 55 | 55 | 55 | 55 |
| 46 to 61 | Superset Information | – | 00 | 00 | 00 | 00 | 00 |
| 62 | SPD Revision | Revision 0.0 | 00 | 00 | 00 | 00 | 00 |
| 63 | Checksum for Bytes 0 - 62 | – | E7 | 00 | 12 | 01 | 12 |
| 64 | Manufacturers JEDEC ID Codes | – | C1 | C1 | C1 | C1 | C1 |
| 65 to 71 | Manufacturer | – | Infineon | Infineon | Infineon | Infineon | Infineon |
| 72 | Module Assembly Location | – | – | – | – | – | – |
| 73 to 90 | Module Part Number | – | – | – | – | – | – |
| 91 to 92 | Module Revision Code | – | – | – | – | – | – |
| 93 to 94 | Module Manufacturing Date | – | – | – | – | – | – |
| 95 to 98 | Module Serial Number | – | – | – | – | – | – |
| 99 to 127 | – | – | – | – | – | – | – |
| 128 to 255 | open for Customer use | – | – | – | – | – | – |

**Table 21 SPD Codes for PC3200 Modules "–5"**

| | | Part Number & Organization | HYS64D16301GU–5–B | HYS64D32300GU–5–B | HYS72D32300GU–5–B | HYS64D64320GU–5–B | HYS72D64320GU–5–B |
|---|---|---|---|---|---|---|---|
| | | | 128MB | 256MB | 256MB | 512MB | 512MB |
| | | | ×64 | ×64 | ×72 | ×64 | ×72 |
| | | | 1 rank | 1 rank | 1 rank | 2 ranks | 2 ranks |
| **Byte** | **Description** | | **HEX** | **HEX** | **HEX** | **HEX** | **HEX** |
| 0 | Programmed SPD Bytes in E2PROM | 128 | 80 | 80 | 80 | 80 | 80 |
| 1 | Total number of Bytes in E2PROM | 256 | 08 | 08 | 08 | 08 | 08 |
| 2 | Memory Type DDR-I = 07h | DDR-SDRAM | 07 | 07 | 07 | 07 | 07 |
| 3 | # of Row Addresses | 13 | 0D | 0D | 0D | 0D | 0D |
| 4 | # Number of Column Addresses | 9/10 | 09 | 0A | 0A | 0A | 0A |
| 5 | # of DIMM Banks | 1/2 | 01 | 01 | 01 | 02 | 02 |
| 6 | Data Width (LSB) | ×64/×72 | 40 | 40 | 48 | 40 | 48 |
| 7 | Data Width (MSB) | 0 | 00 | 00 | 00 | 00 | 00 |
| 8 | Interface Voltage Levels | SSTL_2.5 | 04 | 04 | 04 | 04 | 04 |
| 9 | tCK @ CLmax (Byte 18) [ns] | 5 ns | 50 | 50 | 50 | 50 | 50 |
| 10 | tAC SDRAM @ CLmax (Byte 18) [ns] | 0.50 ns | 50 | 50 | 50 | 50 | 50 |
| 11 | DIMM Configuration Type (non- / ECC) | non-ECC/ECC | 00 | 00 | 02 | 00 | 02 |
| 12 | Refresh Rate | Self-Refresh 7.8 µs | 82 | 82 | 82 | 82 | 82 |
| 13 | Primary SDRAM width | ×16/ ×8 | 10 | 08 | 08 | 08 | 08 |
| 14 | Error Checking SDRAM width | na/ ×8 | 00 | 00 | 08 | 00 | 08 |
| 15 | tCCD [cycles] | $t_{CCD}$ = 1 CLK | 01 | 01 | 01 | 01 | 01 |
| 16 | Burst Length Supported | 2, 4 & 8 | 0E | 0E | 0E | 0E | 0E |
| 17 | Number of Banks on SDRAM | 4 | 04 | 04 | 04 | 04 | 04 |
| 18 | CAS Latency | CAS latency = 2, 2.5, 3 | 1C | 1C | 1C | 1C | 1C |
| 19 | CS Latency | CS latency = 0 | 01 | 01 | 01 | 01 | 01 |
| 20 | WE (Write) Latency | Write latency = 1 | 02 | 02 | 02 | 02 | 02 |
| 21 | DIMM Attributes | unbuffered | 20 | 20 | 20 | 20 | 20 |
| 22 | Component Attributes | – | C1 | C1 | C1 | C1 | C1 |
| 23 | tCK @ CLmax -0.5 (Byte 18) [ns] | 6.0 ns | 60 | 60 | 60 | 60 | 60 |
| 24 | tAC SDRAM @ CLmax -0.5 [ns] | 0.50 ns | 50 | 50 | 50 | 50 | 50 |
| 25 | tCK @ CLmax -1 (Byte 18) [ns] | 7.5 ns | 75 | 75 | 75 | 75 | 75 |
| 26 | tAC SDRAM @ CLmax -1 [ns] | not supported | 50 | 50 | 50 | 50 | 50 |
| 27 | tRPmin (ns) | 15 ns | 3C | 3C | 3C | 3C | 3C |
| 28 | tRRDmin [ns] | 10 ns | 28 | 28 | 28 | 28 | 28 |

**Table 21 SPD Codes for PC3200 Modules "–5"** (cont'd)

| | | Part Number & Organization | HYS64D16301GU–5–B | HYS64D32300GU–5–B | HYS72D32300GU–5–B | HYS64D64320GU–5–B | HYS72D64320GU–5–B |
|---|---|---|---|---|---|---|---|
| | | | 128MB | 256MB | 256MB | 512MB | 512MB |
| | | | ×64 | ×64 | ×72 | ×64 | ×72 |
| | | | 1 rank | 1 rank | 1 rank | 2 ranks | 2 ranks |
| **Byte** | **Description** | | **HEX** | **HEX** | **HEX** | **HEX** | **HEX** |
| 29 | tRCDmin [ns] | 15 ns | 3C | 3C | 3C | 3C | 3C |
| 30 | tRASmin [ns] | 40 ns | 28 | 28 | 28 | 28 | 28 |
| 31 | Module Density per Bank | 128 MByte/ 256 MByte | 20 | 40 | 40 | 40 | 40 |
| 32 | tAS, tCS [ns] | 0.60 ns | 60 | 60 | 60 | 60 | 60 |
| 33 | tAH, TCH [ns] | 0.60 ns | 60 | 60 | 60 | 60 | 60 |
| 34 | tDS [ns] | 0.40 ns | 40 | 40 | 40 | 40 | 40 |
| 35 | tDH [ns] | 0.40 ns | 40 | 40 | 40 | 40 | 40 |
| 36 - 40 | not used | – | 00 | 00 | 00 | 00 | 00 |
| 41 | tRCmin [ns] | 55 ns | 37 | 37 | 37 | 37 | 37 |
| 42 | tRFCmin [ns] | 65 ns | 41 | 41 | 41 | 41 | 41 |
| 43 | tCKmax [ns] | 10 ns | 28 | 28 | 28 | 28 | 28 |
| 44 | tDQSQmax [ns] | 0.40 ns | 28 | 28 | 28 | 28 | 28 |
| 45 | tQHSmax [ns] | 0.50 ns | 50 | 50 | 50 | 50 | 50 |
| 46 - 61 | not used | – | 00 | 00 | 00 | 00 | 00 |
| 62 | SPD Revision | Revision 0.0 | 00 | 00 | 00 | 00 | 00 |
| 63 | Checksum of Byte 0-62 (LSB only) | – | E4 | FD | 0F | FE | 10 |
| 64 | JEDEC ID Code for Infineon | – | C1 | C1 | C1 | C1 | C1 |
| 65 | JEDEC ID Code for Infineon | "I" | 49 | 49 | 49 | 49 | 49 |
| 66 | JEDEC ID Code for Infineon | "N" | 4E | 4E | 4E | 4E | 4E |
| 67 | JEDEC ID Code for Infineon | "F" | 46 | 46 | 46 | 46 | 46 |
| 68 | JEDEC ID Code for Infineon | "I" | 49 | 49 | 49 | 49 | 49 |
| 69 | JEDEC ID Code for Infineon | "N" | 4E | 4E | 4E | 4E | 4E |
| 70 | JEDEC ID Code for Infineon | "E" | 45 | 45 | 45 | 45 | 45 |
| 71 | JEDEC ID Code for Infineon | "O" | 4F | 4F | 4F | 4F | 4F |
| 72 | Module Manufacturer Location | – | xx | xx | xx | xx | xx |
| 73 | Module Part Number, Char 1 | – | 36 | 36 | 37 | 36 | 37 |
| 74 | Module Part Number, Char 2 | – | 34 | 34 | 32 | 34 | 32 |
| 75 | Module Part Number, Char 3 | – | 44 | 44 | 44 | 44 | 44 |

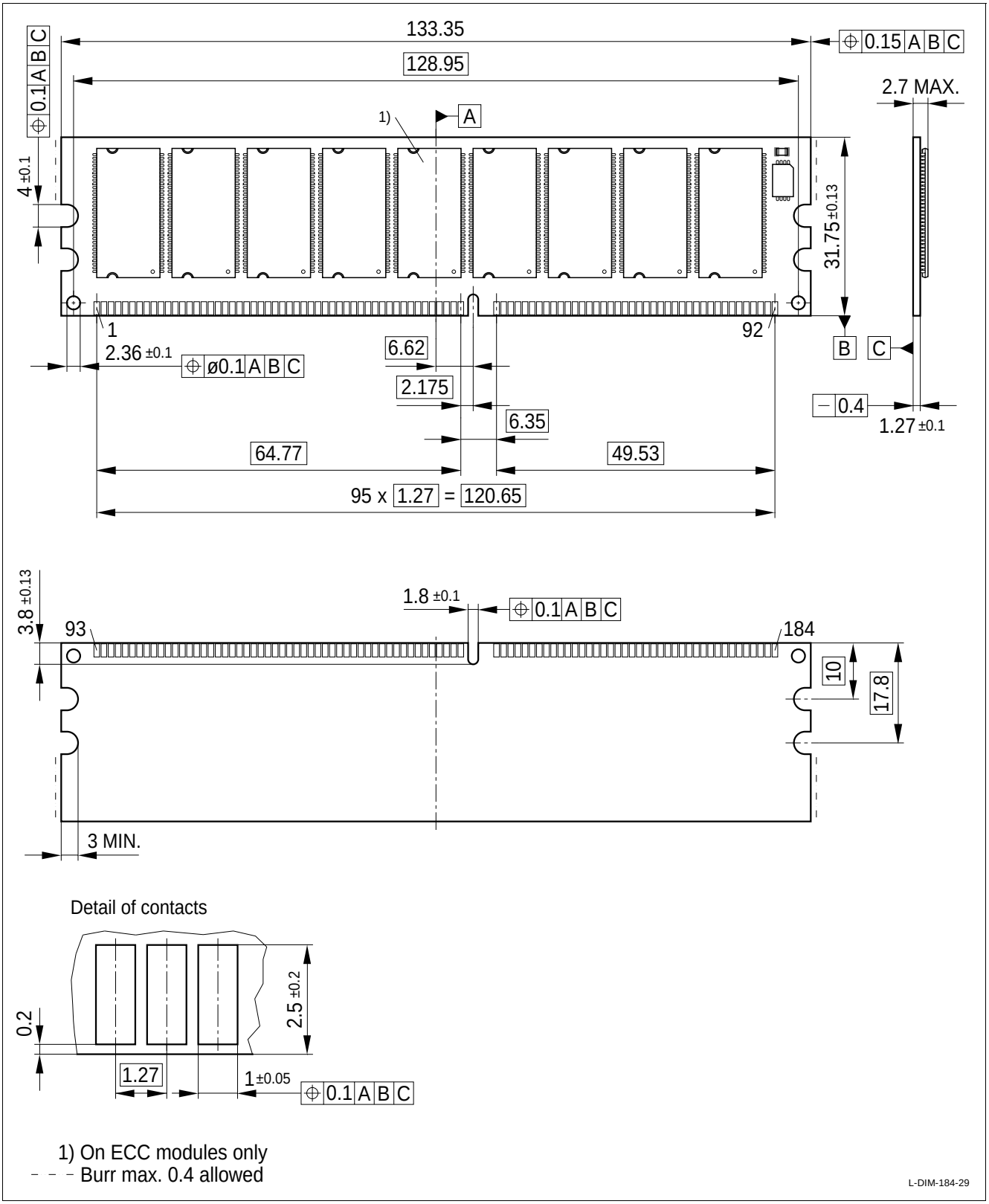



**Figure 8 Package Outline - Raw Card A (256 MByte, 1 Rank Module, –7 and –8)**

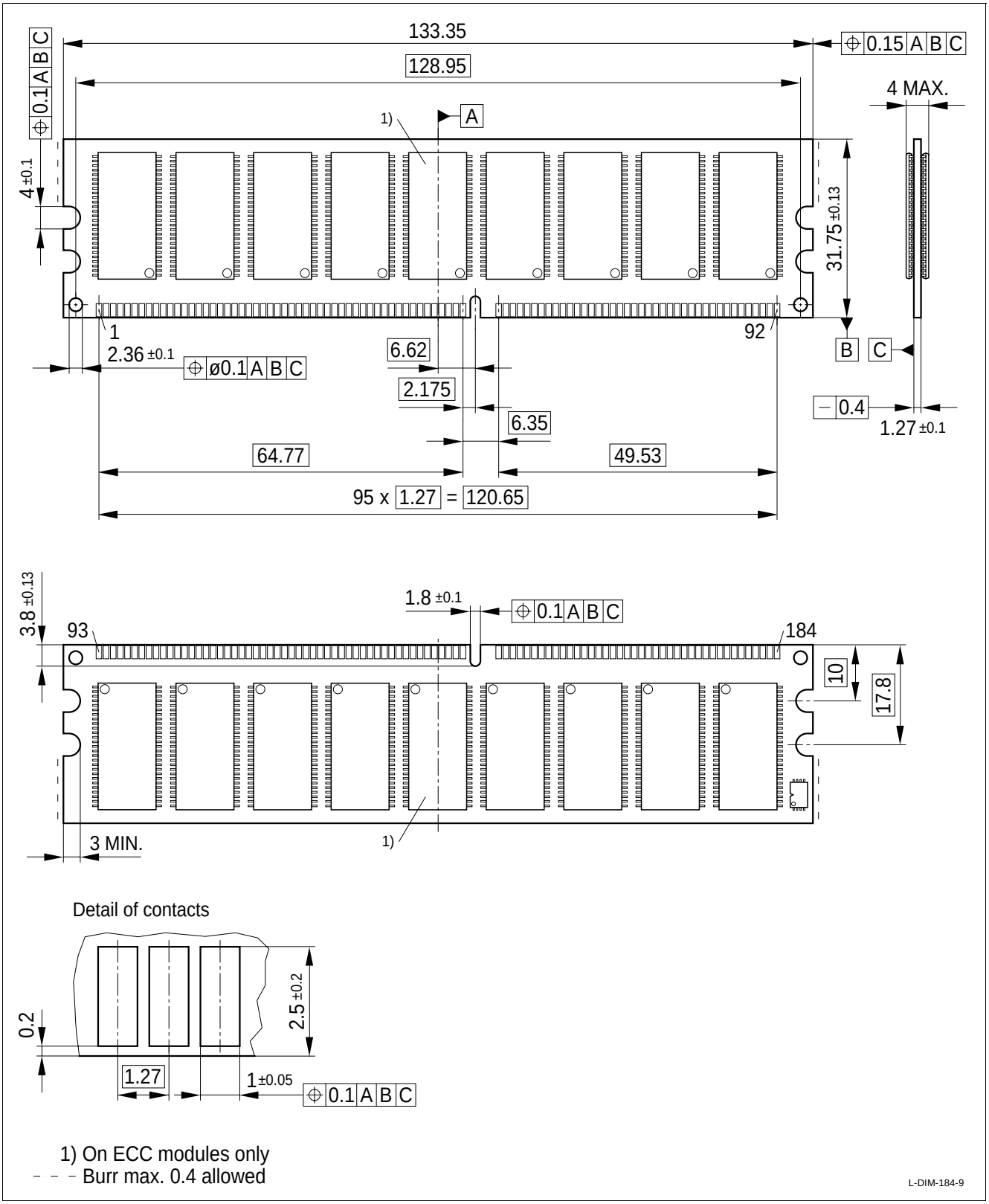



**Figure 9 Package Outline - Raw Card B (512 MByte, 2 Rank Module, –7 and –8)**

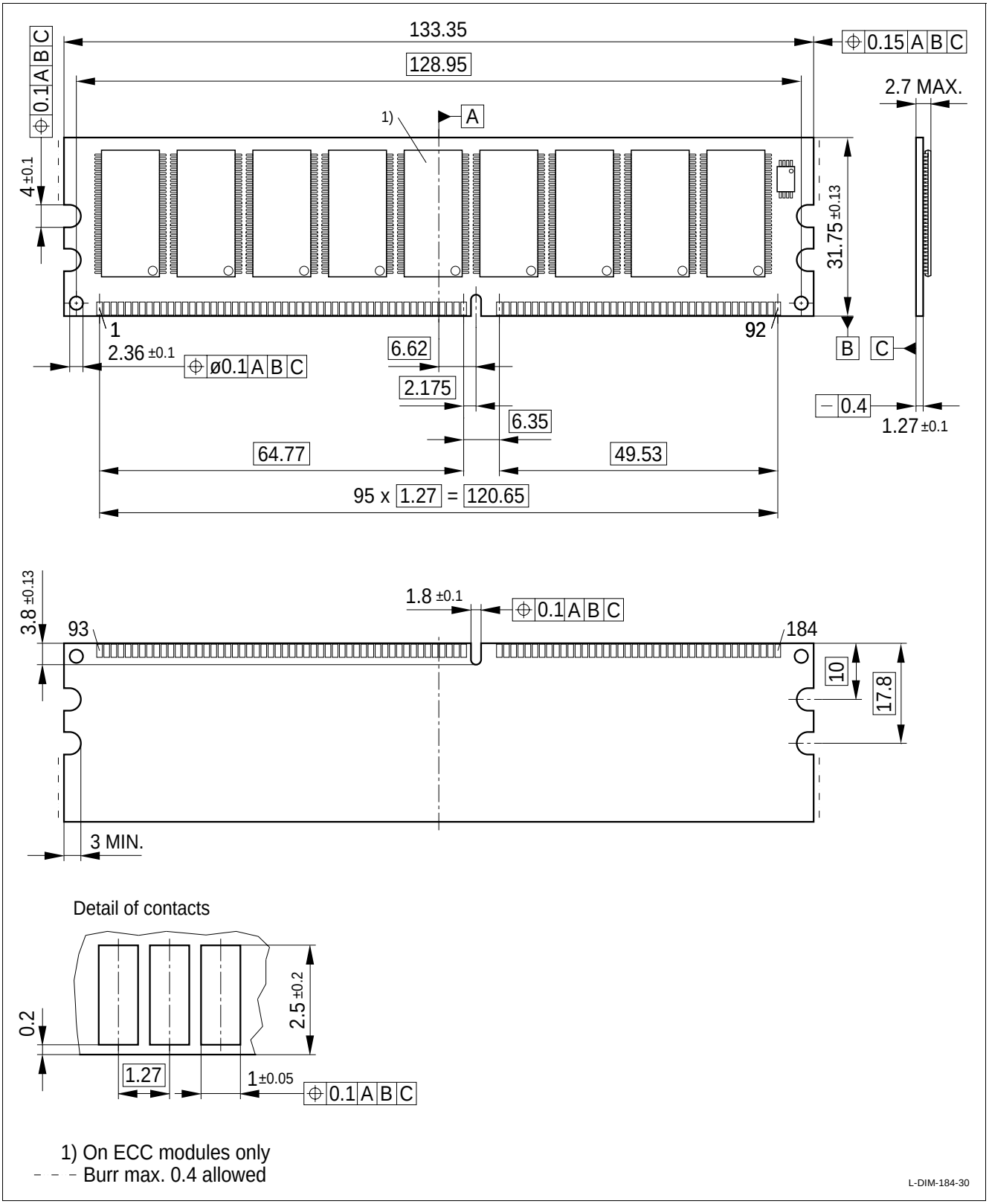



**Figure 10 Package Outline - Raw Card A (256 MByte, 1 Rank Module, –5 and –6, ECC)**

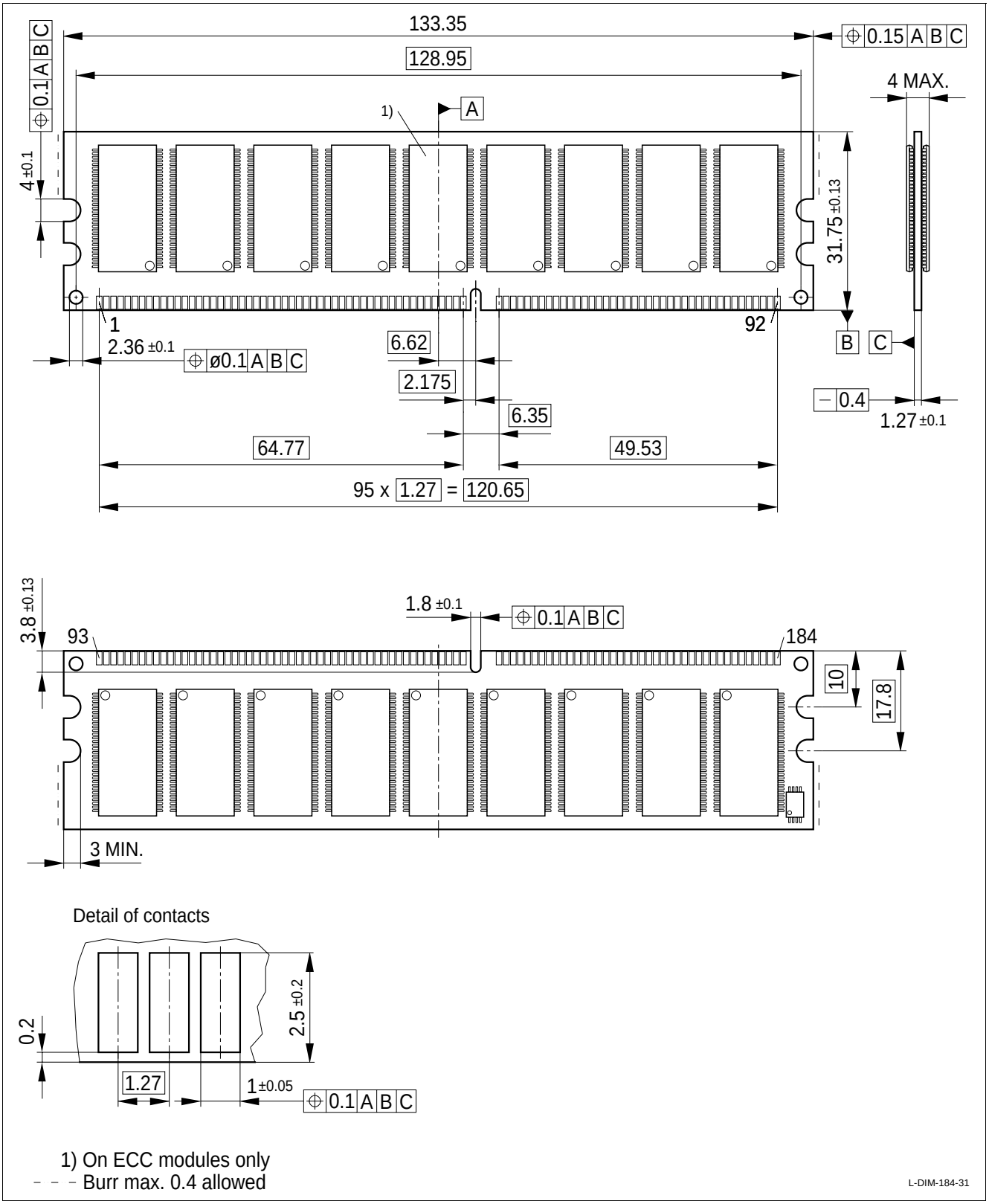



**Figure 11 Package Outline - Raw Card B (512 MByte, 2 Rank Module, –5 and –6, ECC)**

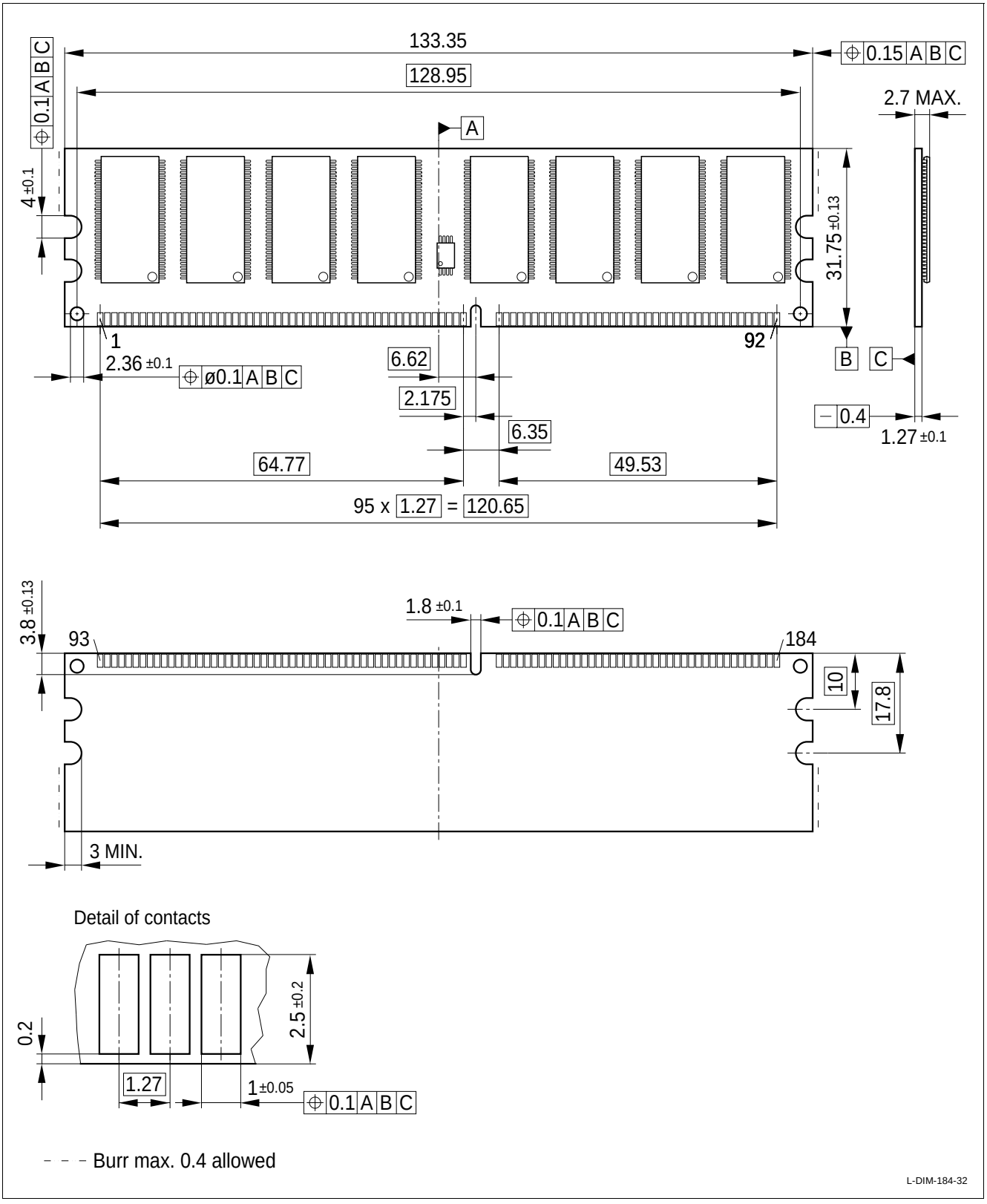
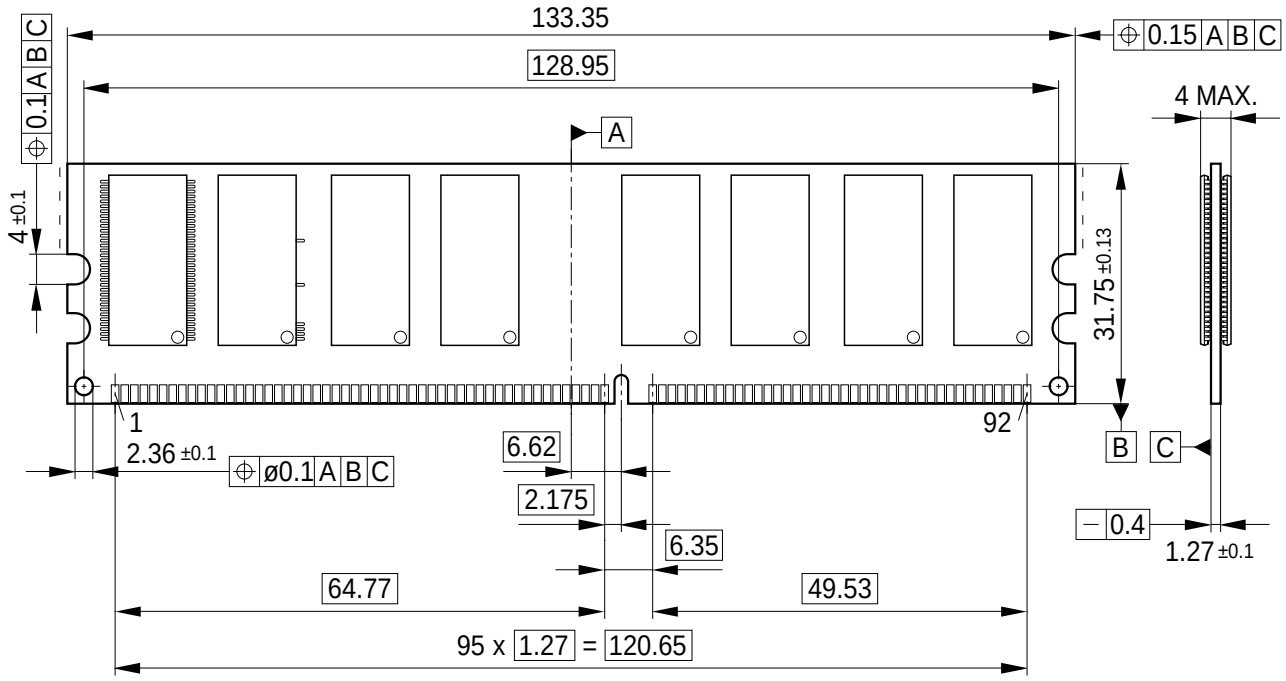
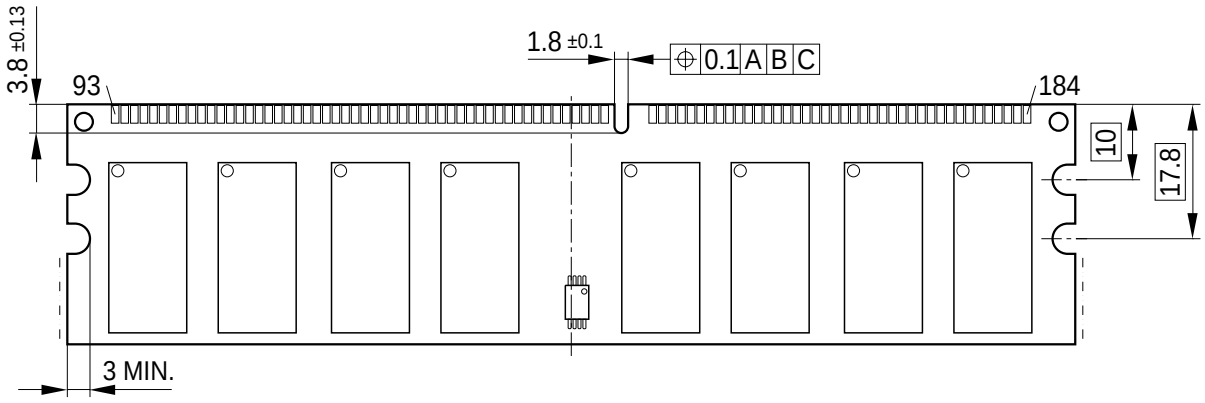
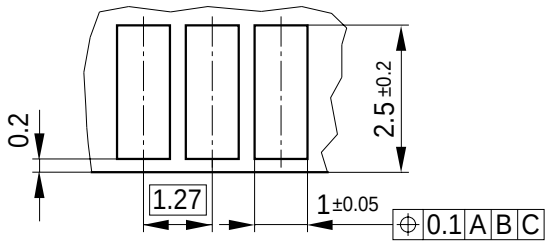



**Figure 12 Package Outline - Raw Card A (256 MByte, 1 Rank Module, –5 and –6, Non ECC)**




Detail of contacts




– – – Burr max. 0.4 allowed

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