3.3 V 16M x 64/72-Bit 1 Bank 128MByte SDRAM Module
3.3 V 32M x 64/72-Bit 2 Bank 256MByte SDRAM Module
168-Pin Unbuffered DIMM Modules

- 168-Pin unbuffered 8-Byte Dual-In-Line SDRAM Modules for PC main memory applications
- PC100-222, PC133-333 and PC133-222 versions
- 1 bank 16M × 64, 16M × 72 and 2 bank 32M × 64, 32M × 72 organzation
- Optimized for byte-write non-parity (x64) or ECC (x72) applications
- JEDEC standard Synchronous DRAMs (SDRAM)
- Fully PC board layout compatible to INTEL's Rev. 1.0 Module Specification
- SDRAM Performance:

		-7 /-7.5	-8	Unit
		PC133	PC100	
f_{CK}	Max. Clock Frequency	133	100	MHz
t_{AC}	Clock Access Time	5.4	6	ns

- Programmed Latencies:

Product Speed		CL	t_{RCD}	t_{RP}
-7	PC133-222	2	2	2
-7.5	PC133-333	3	3	3
-8	PC100-222	2	2	2

- Single +3.3 V(±0.3 V) Power Supply
- Programmable $\overline{CAS}$ Latency, Burst Length, and Wrap Sequence (Sequential and Interleave)
- Auto-Refresh (CBR) and Self-Refresh
- Decoupling capacitors mounted on substrate
- All inputs and outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- Utilizes 16M × 8 SDRAMs in TSOPII-54 packages with 4096 refresh cycles every 64 ms
- 133.35 mm × 31.75 mm × 4,00 mm card size with gold-contact pads (JEDEC MO-161-BA)

Description

The HYS 64(72)V16300GU and HYS 64(72)V32220GU are industry-standard 168-pin 8-byte Dual In-line Memory Modules (DIMMs) which are organized as 16M × 64, 16M × 72 in 1 bank and 32M × 64 and 32M × 72 in two banks of high-speed memory arrays designed with 128Mbit Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use -7 speed sorted 16M × 8 SDRAM devices in TSOP54 packages to meet the PC133-222 requirements, -7.5 speed sorted for PC133-333 and use -8 components for the standard PC100-222 applications. Decoupling capacitors are mounted on the PC board. The PC board design is in accordance with INTEL's Module Specification. The DIMMs have Serial Presence Detect, implemented with a serial E^2PROM using the two-pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user. All INFINEON 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long footprint, with 1.25" (31.75 mm) height.

Ordering Information

Type	Code	Package	Descriptions	Module Height
128 MByte DIMMs				
HYS 64V16300GU-7-C2	PC133-222-520	L-DIM-168-33	133 Mhz 16M × 64 1 bank SDRAM module	1.25“
HYS 64V16300GU-7.5-C2	PC133-333-520	L-DIM-168-33	133 Mhz 16M × 64 1 bank SDRAM module	1.25“
HYS 64V16300GU-8-C2	PC100-222-620	L-DIM-168-33	100 MHz 16M × 64 1 bank SDRAM module	1.25“
HYS 72V16300GU-7-C2	PC133-222-520	L-DIM-168-33	133 Mhz 16M × 72 1 bank SDRAM module	1.25“
HYS 72V16300GU-7.5-C2	PC133-333-520	L-DIM-168-33	133 Mhz 16M × 72 1 bank SDRAM module	1.25“
HYS 72V16300GU-8-C2	PC100-222-620	L-DIM-168-33	100 MHz 16M × 72 1 bank SDRAM module	1.25“
256 MByte DIMMs				
HYS 64V32220GU-7-C2	PC133-222-520	L-DIM-168-30	133 MHz 32M × 64 2 bank SDRAM module	1.25“
HYS 64V32220GU-7.5-C2	PC133-333-520	L-DIM-168-30	133 MHz 32M × 64 2 bank SDRAM module	1.25“
HYS 64V32220GU-8-C2	PC100-222-620	L-DIM-168-30	100 MHz 32M × 64 2 bank SDRAM module	1.25“
HYS 72V32220GU-7-C2	PC133-222-520	L-DIM-168-30	133 Mhz 32M × 72 2 bank SDRAM module	1.25“
HYS 72V32220GU-7.5-C2	PC133-333-520	L-DIM-168-30	133 Mhz 32M × 72 2 bank SDRAM module	1.25“
HYS 72V32220GU-8-C2	PC100-222-620	L-DIM-168-30	100 Mhz 32M × 72 2 bank SDRAM module	1.25“

Note: All part numbers end with a place code, designating the die revision. Consult factory for current revision. Example: HYS 64V16300GU-8-C2, indicates that Rev.C2 dies are used for SDRAM components.

Pin Definitions and Functions

A0-A11	Address Inputs	$\overline{WE}$	Read/Write Input	V_{SS}	Ground
BA0, BA1	Bank Selects	CKE0, CKE1 *)	Clock Enable	SCL	Clock for SPD
DQ0 - DQ63	Data Input/Output	CLK0 - CLK3	Clock Input	SDA	Serial Data Out
CB0-CB7	Check Bits (x72 modules only)	DQMB0 - DQMB7	Data Mask	N.C.	No Connection
$\overline{RAS}$	Row Address Strobe	$\overline{CS0}$ - $\overline{CS3}$ *)	Chip Select	–	–
$\overline{CAS}$	Column Address Strobe	V_{DD}	Power (+3.3 V)	–	–

*) CKE1, $\overline{CS1}$ and $\overline{CS3}$ on two bank modules only

Address Format

	Part Number	Rows	Columns	Bank Select	Refresh	Period	Interval
16M × 64	HYS 64V16300GU	12	10	2	4k	64 ms	15,6 µs
16M × 72	HYS 72V16300GU	12	10	2	4k	64 ms	15,6 µs
32M × 64	HYS 64V32220GU	12	10	2	4k	64 ms	15,6 µs
32M × 72	HYS 72V32220GU	12	10	2	4k	64 ms	15,6 µs

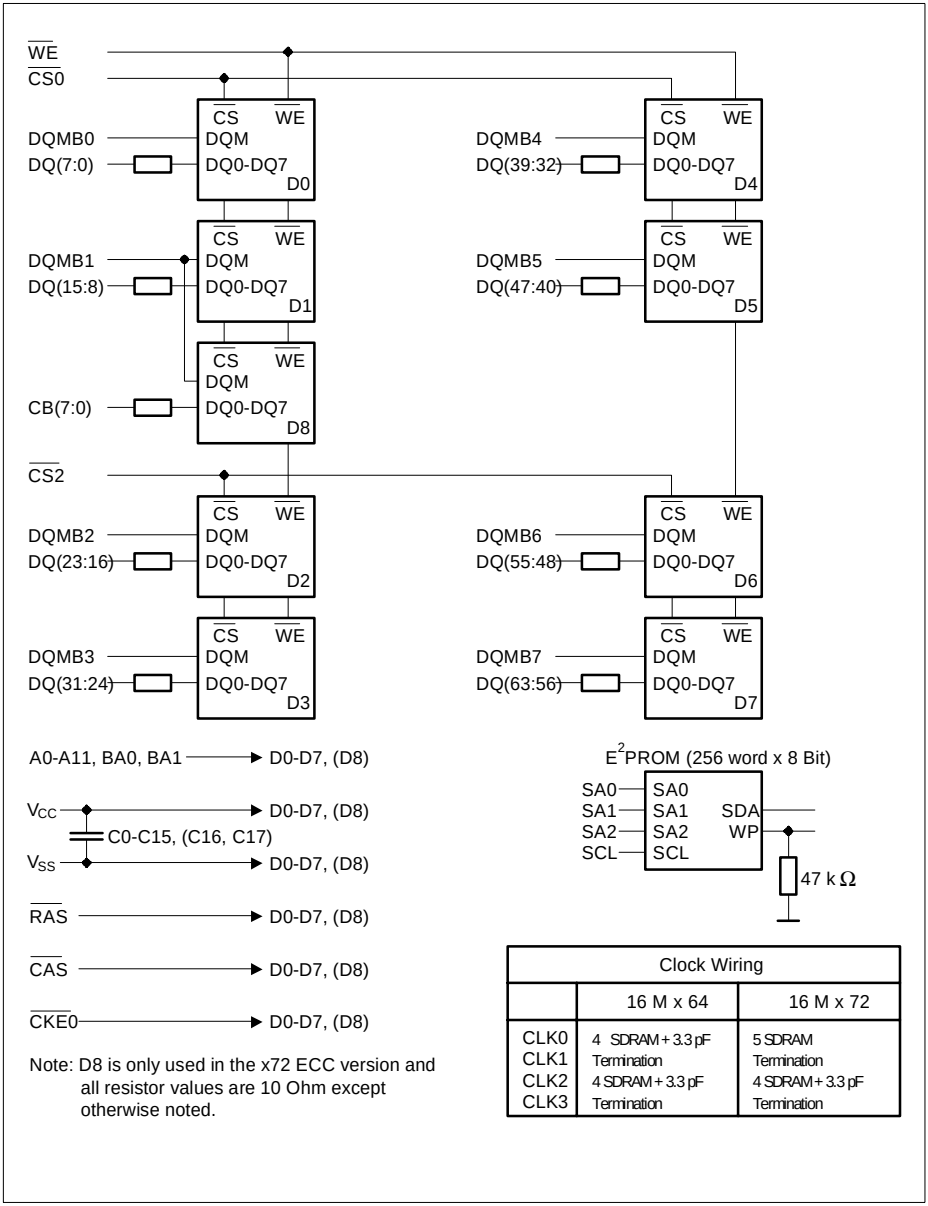
Pin Configuration

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	CS2	87	DQ33	129	CS3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{DD}	48	DU	90	V_{DD}	132	N.C.
7	DQ4	49	V_{DD}	91	DQ36	133	V_{DD}
8	DQ5	50	N.C.	92	DQ37	134	N.C.
9	DQ6	51	N.C.	93	DQ38	135	N.C.
10	DQ7	52	N.C. (CB2)	94	DQ39	136	CB6
11	DQ8	53	N.C. (CB3)	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50

Pin Configuration (cont'd)

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{DD}	101	DQ45	143	V_{DD}
18	V_{DD}	60	DQ20	102	V_{DD}	144	DQ52
19	DQ14	61	N.C.	103	DQ46	145	N.C.
20	DQ15	62	DU	104	DQ47	146	DU
21	N.C. (CB0)	63	CKE1	105	N.C. (CB4)	147	N.C.
22	N.C. (CB1)	64	V_{SS}	106	N.C. (CB5)	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	N.C.	66	DQ22	108	N.C.	150	DQ54
25	N.C.	67	DQ23	109	N.C.	151	DQ55
26	V_{DD}	68	V_{SS}	110	V_{DD}	152	V_{SS}
27	WE	69	DQ24	111	CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	CS0	72	DQ27	114	CS1	156	DQ59
31	DU	73	V_{DD}	115	RAS	157	V_{DD}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CLK2	121	A9	163	CLK3
38	A10	80	N.C.	122	BA0	164	N.C.
39	BA1	81	WP	123	A11	165	SA0
40	V_{DD}	82	SDA	124	V_{DD}	166	SA1
41	V_{DD}	83	SCL	125	CLK1	167	SA2
42	CLK0	84	V_{DD}	126	N.C.	168	V_{DD}

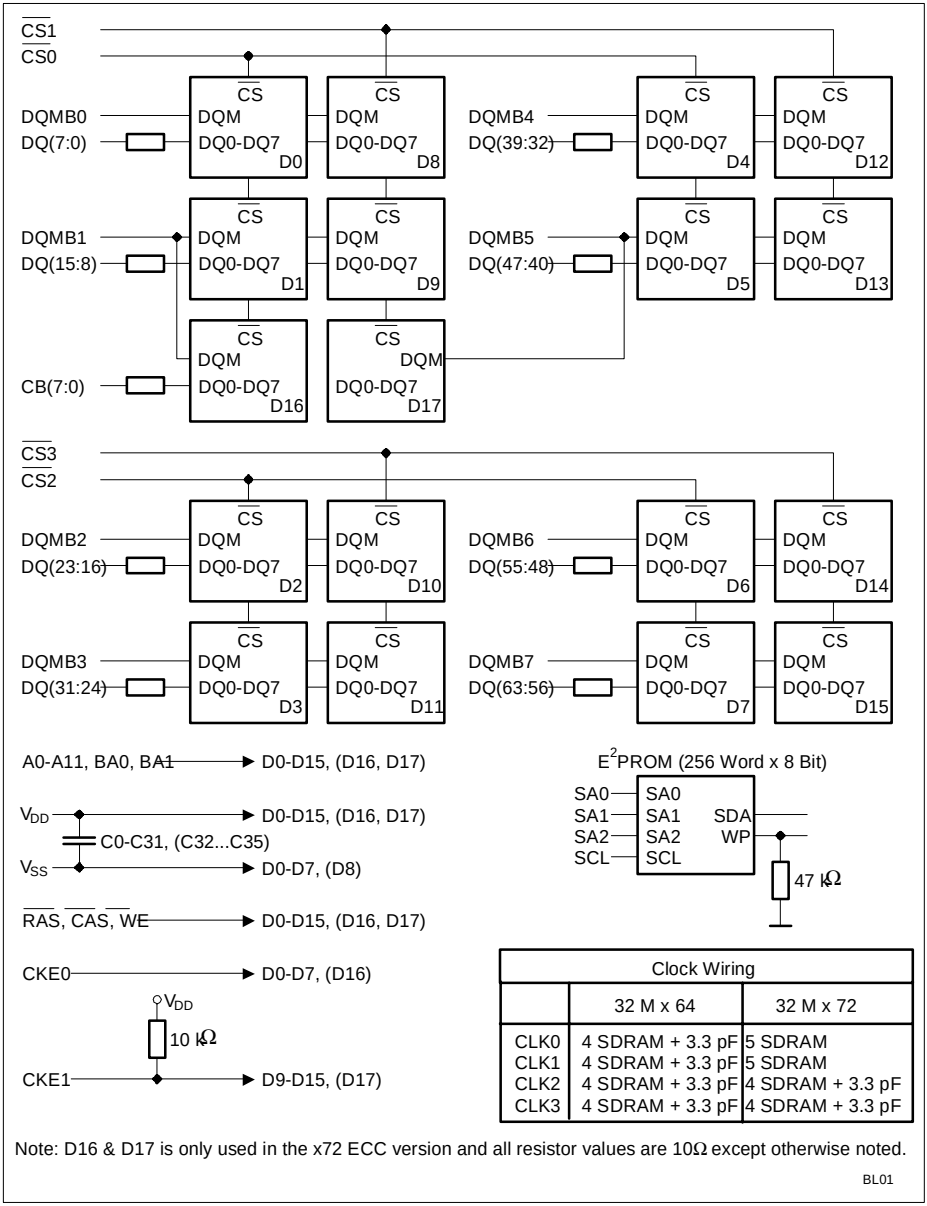
Note: Pin names in parentheses are for the x72 ECC versions; example: Pin 106 = (CB5).



Clock Wiring		
	16 M x 64	16 M x 72
CLK0 CLK1 CLK2 CLK3	4 SDRAM + 3.3 pF Termination 4 SDRAM + 3.3 pF Termination	5 SDRAM Termination 4 SDRAM + 3.3 pF Termination

Note: D8 is only used in the x72 ECC version and all resistor values are 10 Ohm except otherwise noted.

Block Diagram for 16M x 64/72 SDRAM DIMM Modules (HYS 64/72V16300GU)



Clock Wiring		
	32 M x 64	32 M x 72
CLK0	4 SDRAM + 3.3 pF	5 SDRAM
CLK1	4 SDRAM + 3.3 pF	5 SDRAM
CLK2	4 SDRAM + 3.3 pF	4 SDRAM + 3.3 pF
CLK3	4 SDRAM + 3.3 pF	4 SDRAM + 3.3 pF

Note: D16 & D17 is only used in the x72 ECC version and all resistor values are 10Ω except otherwise noted.

BL01

Block Diagram for 32M x 64/72 SDRAM DIMM Modules (HYS 64/72V32220GU)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	– 1.0	4.6	V
Power supply voltage on V_{DD}	V_{DD}	– 1.0	4.6	V
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation per SDRAM component	P_D	–	1	W
Data out current (short circuit)	I_{OS}	–	50	mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.
Functional operation should be restricted to recommended operation conditions.
Exposure to higher than recommended voltage for extended periods of time affect device reliability

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ±0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	–0.5	0.8	V
Output High Voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	–	V
Output Low Voltage (I_{OUT} = 4.0 mA)	V_{OL}	–	0.4	V
Input Leakage Current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	–40	40	µA
Output Leakage Current (DQ is disabled, 0 V < V_{OUT} < V_{DD})	$I_{O(L)}$	–40	40	µA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ±0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values				Unit
		max. 16M×64	max. 16M×72	max. 32M×64	max. 32M×72	
Input Capacitance (A0 to A11, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I1}	65	72	105	144	pF
Input Capacitance (CS0 - CS3)	C_{CS}	32	40	35	43	pF
Input Capacitance (CLK0 - CLK3)	C_{CLK}	38	40	42	45	pF
Input Capacitance (CKE0, CKE1)	C_{CKE}	65	72	65	72	pF
Input Capacitance (DQMB0 - DQMB7)	C_{I4}	13	13	20	20	pF
Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	C_{IO}	10	10	17	17	pF
Input Capacitance (SCL, SA0-2)	C_{SC}	8	8	8	8	pF
Input/Output Capacitance	C_{SD}	8	8	8	8	pF

Operating Currents per SDRAM Component

T_A = 0 to 70 °C, V_{DD} = 3.3 V ±0.3 V

Parameter	Test Condition	Symbol	-7 /7.5	-8	Unit	Note
			max.			
Operating Current $t_{RC} = t_{RCMIN.}$, $t_{CK} = t_{CKMIN.}$ Outputs open, Burst Length = 4, CL = 3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	–	I_{CC1}	160	150	mA	1)
Precharge Standby Current in Power Down Mode $\overline{CS} = V_{IH}$ (min.), CKE ≤ $V_{IL(MAX)}$	t_{CK} = min.	I_{CC2P}	1.5	1.5	mA	1)
Precharge Stand-by Current in Non-Power Down Mode $\overline{CS} = V_{IH\ (MIN.)}$, CKE ≥ $V_{IH(MIN)}$	t_{CK} = min.	I_{CC2N}	40	35	mA	1)
No Operating Current t_{CK} = min., $\overline{CS} = V_{IH(MIN)}$, active state (max. 4 banks)	CKE ≥ $V_{IH(MIN.)}$	I_{CC3N}	50	45	mA	1)
	CKE ≤ $V_{IL(MAX.)}$	I_{CC3P}	10	10	mA	1)
Burst Operating Current t_{CK} = min., Read command cycling	–	I_{CC4}	100	90	mA	1), 2)
Auto-Refresh Current t_{CK} = min., Auto-Refresh command cycling	–	I_{CC5}	230	210	mA	1)
Self-Refresh Current Self-Refresh Mode, CKE = 0.2 V	–	I_{CC6}	1.5	1.5	mA	1)

1. These parameters depend on the cycle rate. These values are measured at 133 MHz for -7 and 7.5 modules and at 100 Mhz for -8 modules. Input signals are changed once during t_{CK}, except for I_{CC6} and for standby currents when t_{CK} = infinity. All values are shown per memory component.
2. These parameters are measured with continuous data stream during read access and all DQ toggling. CL = 3 and BL = 4 assumed and the data-out current is excluded

AC Characteristics [3), 4)]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ±0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values						Unit	Note
		-7 PC133-222		-7.5 PC133-333		-8 PC100-222			
		min.	max.	min.	max.	min.	max.		
Clock and Access Time									
Clock Cycle Time	t_{CK}								–
$\overline{CAS}$ Latency = 3		7.5	–	7.5	–	10	–	ns	
$\overline{CAS}$ Latency = 2		7.5	–	10	–	10	–	ns	
System Frequency	f_{CK}								–
$\overline{CAS}$ Latency = 3		–	133	–	133	–	100	MHz	
$\overline{CAS}$ Latency = 2		–	133	–	100	–	100	MHz	
Clock Access Time	t_{AC}								4), 5)
$\overline{CAS}$ Latency = 3		–	5.4	–	5.4	–	6	ns	
$\overline{CAS}$ Latency = 2		–	5.4	–	6	–	6	ns	
Clock High Pulse Width	t_{CH}	2.5	–	2.5	–	3	–	ns	6)
Clock Low Pulse Width	t_{CL}	2.5	–	2.5	–	3	–	ns	6)
Setup & Hold Parameters									
Input Setup Time	t_{IS}	1.5	–	1.5	–	2	–	ns	7)
Input Hold Time	t_{IH}	0.8	–	0.8	–	1	–	ns	7)
Power Down Mode Entry Time	t_{SB}	–	1	–	1	–	1	CLK	8)
Power Down Mode Exit Setup Time	t_{PDE}	1	–	1	–	1	–	CLK	9)
Mode Register Setup Time	t_{RSC}	2	–	2	–	2	–	CLK	
Transition Time (rise and fall)	t_T	1	–	1	–	1	–	ns	–
Common Parameters									
$\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}	15	–	20	–	20	–	ns	–
Precharge Time	t_{RP}	15	–	20	–	20	–	ns	–
Active Command Period	t_{RAS}	42	100k	45	100k	50	100k	ns	–
Cycle Time	t_{RC}	60	–	67.5	–	70	–	ns	–
Bank-to-Bank Delay Time	t_{RRD}	14	–	15	–	16	–	ns	–

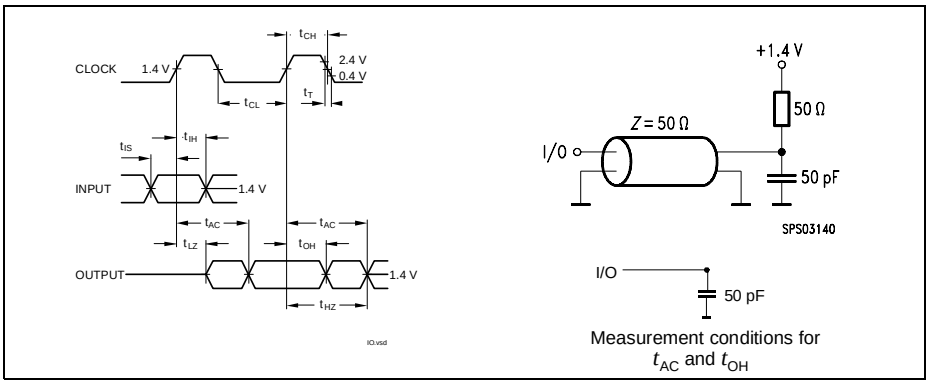
AC Characteristics (cont'd) [3), 4)]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ±0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values						Unit	Note
		-7 PC133-222		-7.5 PC133-333		-8 PC100-222			
		min.	max.	min.	max.	min.	max.		
$\overline{CAS}$ to $\overline{CAS}$ Delay Time (same bank)	t_{CCD}	1	–	1	–	1	–	CLK	–
Refresh Cycle									
Refresh Period (4096 cycles)	t_{REF}	–	64	–	64	–	64	ms	
Self-Refresh Exit Time	t_{SREX}	1	–	1	–	1	–	CLK	10)
Read Cycle									
Data Out Hold Time	t_{OH}	3	–	3	–	3	–	ns	4)
Data Out to Low Impedance	t_{LZ}	0	–	0	–	0	–	ns	–
Data Out to High Impedance	t_{HZ}	3	7	3	7	3	8	ns	11
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	–	2	CLK	–
Write Cycle									
Data Input to Precharge (write recovery)	t_{WR}	2	–	2	–	2	–	CLK	–
DQM Write Mask Latency	t_{DQW}	0	–	0	–	0	–	CLK	–

Notes

3. All AC characteristics are shown on SDRAM component level.
   An initial pause of 100 µs is required after power-up, then a Precharge All Banks command must be given followed by eight Auto-Refresh (CBR) cycles before the Mode Register Set Operation can begin.
4. AC timing tests have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit show. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1 V/ns edge rate between 0.8 V and 2.0 V.
5. If clock rising time is longer than 1 ns, a time (t_T/2 – 0.5) ns must be added to this parameter.
6. Rated at 1.4 V
7. If t_T is longer than 1 ns, a time (t_T – 1) ns has to be added to this parameter.
8. Anytime the Refresh Period has been exceeded, a minimum of two Auto-Refresh (CBR) commands must be given to “wake-up” the device.
9. Timing is asynchronous. If setup time is not met by rising edge of the clock then the CKE signal is assumed latched on the next cycle.
10. Self-Refresh Exit is a synchronous operation and begins on the second positive clock edge after CKE returns high. Self-Refresh Exit is not complete until a time period equal to t_{RC} is satisfied after the Self Refresh Exit command is registered.
11. This is referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.



Measurement conditions for t_{AC} and t_{OH}

A Serial Presence Detect storage device—E^{2}PROM—is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^{2}PROM device during module production using a Serial Presence Detect protocol (I^{2}C synchronous 2-wire bus).

SPD-Table for PC133-222 Modules:

Byte#	Description	SPD Entry Value	Hex			
			16Mx64 -7	16Mx72 -7	32Mx64 -7	32Mx72 -7
0	Number of SPD bytes	128	80			
1	Total bytes in Serial PD	256	08			
2	Memory Type	SDRAM	04			
3	Number of Row Addresses (without BS bits)	12	0C			
4	Number of Column Addresses	10	0A			
5	Number of DIMM Banks	1 / 2	01		02	
6	Module Data Width	64 / 72	40	48	40	48
7	Module Data Width (cont'd)	0	00			
8	Module Interface Levels	LVTTL	01			
9	SDRAM Cycle Time at CL=3	7.5 ns	75			
10	SDRAM Access time from Clock at CL=3	5.4 ns	54			
11	Dimm Config	none / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 15.6 µs	80			
13	SDRAM width, Primary	x8	08			
14	Error Checking SDRAM data width	n/a / x8	00	08	00	08
15	Minimum clock delay for back-to-back random column address	t_{ccd} = 1 CLK	01			
16	Burst Length supported	1, 2, 4 & 8	0F			
17	Number of SDRAM banks	4	04			
18	Supported CAS Latencies	CAS latency = 2 & 3	06			
19	CS Latencies	CS latency = 0	01			
20	WE Latencies	Write latency = 0	01			
21	SDRAM DIMM module attributes	non buffered/non reg.	00			
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	0E			
23	Min. Clock Cycle Time at CAS Latency = 2	7.5 ns	75			
24	Max. data access time from Clock for CL=2	5.4 ns	54			
25	Minimum Clock Cycle Time at CL = 1	not supported	FF			
26	Maximum Data Access Time from Clock at CL=1	not supported	FF			
27	Minimum Row Precharge Time	15 ns	0F			
28	Minimum Row Active to Row Active delay tRRD	14 ns	0E			

Byte#	Description	SPD Entry Value	Hex			
			16Mx64 -7	16Mx72 -7	32Mx64 -7	32Mx72 -7
29	Minimum RAS to CAS delay tRCD	15 ns	0F			
30	Minimum RAS pulse width tRAS	42 ns	2A			
31	Module Bank Density (per bank)	128 MByte	20			
32	SDRAM input setup time	1.5 ns	15			
33	SDRAM input hold time	0.8 ns	08			
34	SDRAM data input hold time	1.5 ns	15			
35	SDRAM data input setup time	0.8 ns	08			
62-61	Superset information (may be used in future)		FF			
62	SPD Revision	Revision 1.2	12			
63	Checksum for bytes 0 - 62		CE	E0	tbd	tbd
64-125	Manufacturers information		XX	XX	XX	XX
126	Frequency Specification		64			
127	Support Details		AF		FF	
128+	Unused storage locations		FF			

SPD-Table for PC133-333 Modules:

Byte#	Description	SPD Entry Value	Hex			
			16Mx64 -7.5	16Mx72 -7.5	32Mx64 -7.5	32Mx72 -7.5
0	Number of SPD bytes	128	80			
1	Total bytes in Serial PD	256	08			
2	Memory Type	SDRAM	04			
3	Number of Row Addresses (without BS bits)	12	0C			
4	Number of Column Addresses	10	0A			
5	Number of DIMM Banks	1 / 2	01		02	
6	Module Data Width	64 / 72	40	48	40	48
7	Module Data Width (cont'd)	0	00			
8	Module Interface Levels	LVTTL	01			
9	SDRAM Cycle Time at CL=3	7.5 ns	75			
10	SDRAM Access time from Clock at CL=3	5.4 ns	54			
11	Dimm Config	none / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 15.6 µs	80			
13	SDRAM width, Primary	x8	08			
14	Error Checking SDRAM data width	n/a / x8	00	08	00	08
15	Minimum clock delay for back-to-back random column address	t_{ccd} = 1 CLK	01			
16	Burst Length supported	1, 2, 4 & 8	0F			
17	Number of SDRAM banks	4	04			
18	Supported CAS Latencies	CAS latency = 2 & 3	06			
19	CS Latencies	CS latency = 0	01			
20	WE Latencies	Write latency = 0	01			
21	SDRAM DIMM module attributes	non buffered/non reg.	00			
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	0E			
23	Min. Clock Cycle Time at CAS Latency = 2	10.0 ns	A0			
24	Max. data access time from Clock for CL=2	6.0 ns	60			
25	Minimum Clock Cycle Time at CL = 1	not supported	FF			
26	Maximum Data Access Time from Clock at CL=1	not supported	FF			
27	Minimum Row Precharge Time	20 ns	14			
28	Minimum Row Active to Row Active delay tRRD	15 ns	0F			

Byte#	Description	SPD Entry Value	Hex			
			16Mx64 -7.5	16Mx72 -7.5	32Mx64 -7.5	32Mx72 -7.5
29	Minimum RAS to CAS delay tRCD	20 ns	14			
30	Minimum RAS pulse width tRAS	45 ns	2D			
31	Module Bank Density (per bank)	128 MByte	20			
32	SDRAM input setup time	1.5 ns	15			
33	SDRAM input hold time	0.8 ns	08			
34	SDRAM data input hold time	1.5 ns	15			
35	SDRAM data input setup time	0.8 ns	08			
62-61	Superset information (may be used in future)		FF			
62	SPD Revision	Revision 1.2	12			
63	Checksum for bytes 0 - 62		13	25	14	26
64-125	Manufacturers information		XX	XX	XX	XX
126	Frequency Specification		64			
127	Support Details		AF		FF	
128+	Unused storage locations		FF			

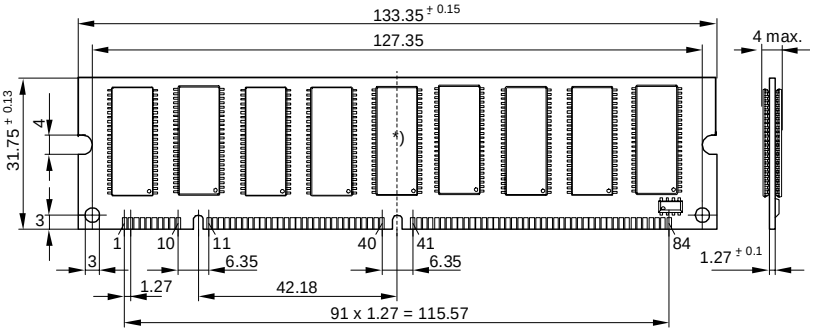
SPD-Table for PC100 Modules:

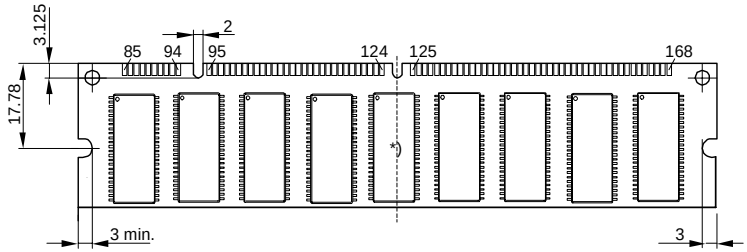
Byte#	Description	SPD Entry Value	Hex			
			16Mx64 -8	16Mx72 -8	32Mx64 -8	32Mx72 -8
0	Number of SPD bytes	128	80			
1	Total bytes in Serial PD	256	08			
2	Memory Type	SDRAM	04			
3	Number of Row Addresses (without BS bits)	12	0C			
4	Number of Column Addresses	10	0A			
5	Number of DIMM Banks	1 / 2	01		02	
6	Module Data Width	64 / 72	40	48	40	48
7	Module Data Width (cont'd)	0	00			
8	Module Interface Levels	LVTTL	01			
9	SDRAM Cycle Time at CL=3	10.0 ns	A0			
10	SDRAM Access time from Clock at CL=3	6.0 ns	60			
11	Dimm Config	none / ECC	00	02	00	02
12	Refresh Rate/Type	Self-Refresh, 15.6 µs	80			
13	SDRAM width, Primary	x8	08			
14	Error Checking SDRAM data width	n/a / x8	00	08	00	08
15	Minimum clock delay for back-to-back random column address	t_{ccd} = 1 CLK	01			
16	Burst Length supported	1, 2, 4 & 8	0F			
17	Number of SDRAM banks	4	04			
18	Supported CAS Latencies	CAS latency = 2 & 3	06			
19	CS Latencies	CS latency = 0	01			
20	WE Latencies	Write latency = 0	01			
21	SDRAM DIMM module attributes	non buffered/non reg.	00			
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	0E			
23	Min. Clock Cycle Time at CAS Latency = 2	10.0 ns	A0			
24	Max. data access time from Clock for CL=2	6.0 ns	60			
25	Minimum Clock Cycle Time at CL = 1	not supported	FF			
26	Maximum Data Access Time from Clock at CL=1	not supported	FF			
27	Minimum Row Precharge Time	20 ns	14			
28	Minimum Row Active to Row Active delay tRRD	16 ns	10			

Byte#	Description	SPD Entry Value	Hex			
			16Mx64 -8	16Mx72 -8	32Mx64 -8	32Mx72 -8
29	Minimum RAS to CAS delay tRCD	20 ns	14			
30	Minimum RAS pulse width tRAS	45 ns	2D			
31	Module Bank Density (per bank)	128 MByte	20			
32	SDRAM input setup time	2 ns	20			
33	SDRAM input hold time	1 ns	10			
34	SDRAM data input hold time	2 ns	20			
35	SDRAM data input setup time	1 ns	10			
62-61	Superset information (may be used in future)		FF			
62	SPD Revision	Revision 1.2	12			
63	Checksum for bytes 0 - 62		71	83	72	84
64-125	Manufacturers information		XX	XX	XX	XX
126	Frequency Specification	100 MHz	64			
127	Support Details		AF		FF	
128+	Unused storage locations		FF			

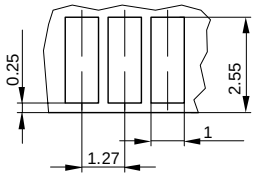
Package Outlines

L-DIM-168-30 (JEDEC MO-161-BA)
SDRAM DIMM Module Package





Detail of Contacts



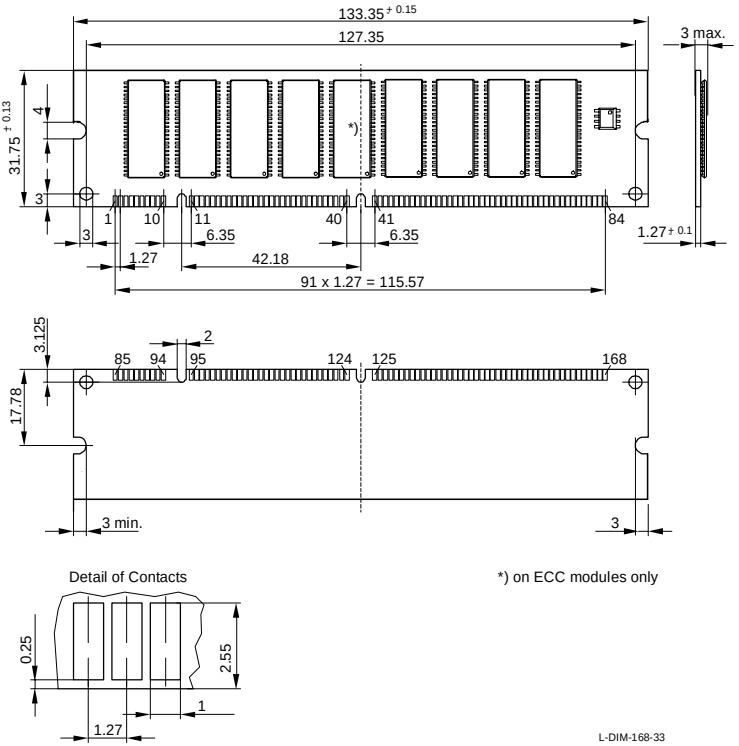
*) on ECC modules only

L-DIM-168-30

Note: All tolerances according to JEDEC standard

Package Outlines

L-DIM-168-33 (JEDEC MO-161-BA)
SDRAM DIMM Module Package
HYS 64/72V16300GU



Note: All tolerances according to JEDEC standard

Update Releases:

June 1, 1999	Explanation for factory specific code in part numbers added
June 17, 1999	Byte 22 for PC100 modules changed from 06 to 0E
August 3, 1999	PC133 spec incorpoated
August 5, 1999	SPD tables added
August 23, 1999	Byte 126 changed to 64h for PC133 modules
Sept.30, 1999	Some errors corrected, checksums added
Dec. 2, 1999	Some timing parameters adjusted according to INTELs PC133 specification -8A speedsort removed
Feb. 23, 2000	ICC currents updated in accordance to 128Mbit component datasheets Capacitance values updated according to module C-measurements Block Diagrams corrected, R&L template
10.5.2000	Reference to JEDEC MO-161-BA added
21.8.2000	PC133-222 modules “-7 speed sort” added
06.09.2001	SCR : Absolute Maximum Ratings table added