Data Sheet, Rev. 1.0, Mar. 2004

HYS72D32300GBR–[5/6]–C
HYS72D64300GBR–[5/6]–C
HYS72D64320GBR–[5/6]–C
HYS72D128320GBR–6–C

184-Pin Registered Double Data Rate SDRAM Module

Reg DIMM
DDR SDRAM

Memory Products

Infineon technologies

Never stop thinking.

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Revision History:	**Rev. 1.0**	**2004-03**
Previous Version:	Rev. 0.5	

Page	Subjects (major changes since last revision)
20,21	I_{dd} values updated
8,22	editorial changes
24,27	Changed SPD Code Byte 99 - 127 to FF

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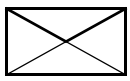

Table of Contents

1 Overview

1.1 Features

- 184-Pin Registered 8-Byte Dual-In-Line
  DDR SDRAM Module for “1U” PC, Workstation and Server main memory applications
- One rank 32 M × 72 and 64M × 72 and two ranks 64 M ×72 and 128 M ×72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM) with a single + 2.5 V (± 0.2 V) power supply and + 2.6 V (± 0.1 V) power supply for DDR400
- Built with 256-Mbit DDR SDRAMs in P-TFBGA-60-1 packages
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Re-drive for all input signals using register and PLL devices.
- Serial Presence Detect with E^2PROM
- Low Profile Modules form factor:
  133.35 mm × 28.58 mm × 4.00 mm / 2.64 mm and for 1GB 133.35 mm × 30.48 mm (1.2”)× 4.00 mm
- JEDEC standard reference layout for one rank 256 MB, 512 MB and two ranks 512 MB, 1 GB:
  PC2700 and PC3200 Registered DIMM Raw Cards A,B,C,D
- Gold plated contacts

Table 1 Performance

Part Number Speed Code			–5	–6	Unit
Speed Grade	Component		DDR400B	DDR333B	—
	Module		PC3200–3033	PC2700–2533	—
max. Clock Frequency	@CL3	f_{CK3}	200	166	MHz
	@CL2.5	$f_{CK2.5}$	166	166	MHz
	@CL2	f_{CK2}	133	133	MHz

1.2 Description

The HYS72D[128/64/32][300/320]GBR–[5/6]–C and HYS72D64320GBR–5–C are low profile versions of the standard Registered DIMM modules suitable for 1U Server Applications. The Low Profile DIMM versions are available as 32 M ×72 (256 MB), 64 M ×72 (512 MB) and 128 M ×72 (1 GB)

The memory array is designed with Double Data Rate Synchronous DRAMs for ECC applications. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Table 2 Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC3200 (CL = 3.0)			
HYS72D32300GBR–5–C	PC3200R–30330–A0	1 Rank 256 MB Registered DIMM ECC	256 Mbit (×8)
HYS72D64300GBR–5–C	PC3200R–30330–C0	1 Rank 512 MB Registered DIMM ECC	256 Mbit (×4)
HYS72D64320GBR–5–C	PC3200R–30330–B0	2 Ranks 512 MB Registered DIMM ECC	256 Mbit (×8)
PC2700 (CL = 2.5, t_{RP} = t_{RCD} = 3 at t_{CK} = 6ns)			
HYS72D32300GBR–6–C	PC2700R–25330–A0	1 Rank 256 MB Registered DIMM ECC	256 Mbit (×8)
HYS72D64300GBR–6–C	PC2700R–25330–C0	1 Rank 512 MB Registered DIMM ECC	256 Mbit (×4)
HYS72D64320GBR–6–C	PC2700R–25330–B0	2 Ranks 512 MB Registered DIMM ECC	256 Mbit (×8)
HYS72D128320GBR–6–C	PC2700R–25330–D0	2 Ranks 1 GB Registered DIMM ECC	256 Mbit (×4)

2 Pin Configuration

The pin configuration of the Registered DDR SDRAM DIMM is listed by function in Table 3 (184 pins). The abbreviations used in columns Pin and Buffer Type are explained in Table 4 and Table 5 respectively. The pin numbering is depicted in Figure 1.

Table 3 Pin Configuration of RDIMM

Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
137	CK0	I	SSTL	**Clock Signal**
138	$\overline{CK0}$	I	SSTL	**Complement Clock**
21	CKE0	I	SSTL	**Clock Enable Rank 0**
111	CKE1	I	SSTL	**Clock Enable Rank 1** *Note: 2-rank module*
	NC	NC	SSTL	*Note:* **1***-rank module*
Control Signals				
157	$\overline{S0}$	I	SSTL	**Chip Select of Rank 0**
158	$\overline{S1}$	I	SSTL	**Chip Select of Rank 1** *Note: 2-ranks module*
	NC	NC	–	*Note: 1-rank module*
154	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
65	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
63	$\overline{WE}$	I	SSTL	**Write Enable**
10	$\overline{RESET}$	I	LV-CMOS	**Register Reset** Forces registered inputs low *Note: For detailed description of the Power Up and Power Management see the Application Note at the end of data sheet*
Address Signals				
59	BA0	I	SSTL	**Bank Address Bus 1:0**
52	BA1	I	SSTL	
48	A0	I	SSTL	**Address Bus 11:0**
43	A1	I	SSTL	
41	A2	I	SSTL	
130	A3	I	SSTL	
37	A4	I	SSTL	
32	A5	I	SSTL	**Address Bus 11:0**
125	A6	I	SSTL	**Address Bus 11:0**
29	A7	I	SSTL	
122	A8	I	SSTL	
27	A9	I	SSTL	
141	A10	I	SSTL	
	AP	I	SSTL	
118	A11	I	SSTL	
115	A12	I	SSTL	**Address Signal 12** *Note: Module based on 256 Mbit or larger dies*
	NC	NC	–	*Note: 128 Mbit based module*
167	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based module*
	NC	NC	–	*Note: Module based on 512 Mbit or smaller dies*

Table 3 Pin Configuration of RDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
Data Signals				
2	DQ0	I/O	SSTL	**Data Bus 63:0**
4	DQ1	I/O	SSTL	
6	DQ2	I/O	SSTL	
8	DQ3	I/O	SSTL	
94	DQ4	I/O	SSTL	
95	DQ5	I/O	SSTL	
98	DQ6	I/O	SSTL	
99	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
19	DQ10	I/O	SSTL	
20	DQ11	I/O	SSTL	
105	DQ12	I/O	SSTL	
106	DQ13	I/O	SSTL	
109	DQ14	I/O	SSTL	
110	DQ15	I/O	SSTL	
23	DQ16	I/O	SSTL	
24	DQ17	I/O	SSTL	
28	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
114	DQ20	I/O	SSTL	
117	DQ21	I/O	SSTL	
121	DQ22	I/O	SSTL	
123	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
35	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
126	DQ28	I/O	SSTL	
127	DQ29	I/O	SSTL	
131	DQ30	I/O	SSTL	
133	DQ31	I/O	SSTL	
53	DQ32	I/O	SSTL	
55	DQ33	I/O	SSTL	
57	DQ34	I/O	SSTL	
60	DQ35	I/O	SSTL	
146	DQ36	I/O	SSTL	
147	DQ37	I/O	SSTL	

Table 3 Pin Configuration of RDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
150	DQ38	I/O	SSTL	**Data Bus 63:0**
151	DQ39	I/O	SSTL	
61	DQ40	I/O	SSTL	
64	DQ41	I/O	SSTL	
68	DQ42	I/O	SSTL	
69	DQ43	I/O	SSTL	
153	DQ44	I/O	SSTL	
155	DQ45	I/O	SSTL	
161	DQ46	I/O	SSTL	
162	DQ47	I/O	SSTL	
72	DQ48	I/O	SSTL	
73	DQ49	I/O	SSTL	
79	DQ50	I/O	SSTL	
80	DQ51	I/O	SSTL	
165	DQ52	I/O	SSTL	
166	DQ53	I/O	SSTL	
170	DQ54	I/O	SSTL	
171	DQ55	I/O	SSTL	
83	DQ56	I/O	SSTL	
84	DQ57	I/O	SSTL	
87	DQ58	I/O	SSTL	
88	DQ59	I/O	SSTL	
174	DQ60	I/O	SSTL	
175	DQ61	I/O	SSTL	
178	DQ62	I/O	SSTL	
179	DQ63	I/O	SSTL	
44	CB0	I/O	SSTL	**Check Bits 7:0**
45	CB1	I/O	SSTL	
49	CB2	I/O	SSTL	
51	CB3	I/O	SSTL	
134	CB4	I/O	SSTL	
135	CB5	I/O	SSTL	
142	CB6	I/O	SSTL	
144	CB7	I/O	SSTL	
5	DQS0	I/O	SSTL	**Data Strobes 8:0**
14	DQS1	I/O	SSTL	*Note: See block diagram for corresponding DQ signals*
25	DQS2	I/O	SSTL	
36	DQS3	I/O	SSTL	
56	DQS4	I/O	SSTL	
67	DQS5	I/O	SSTL	

Table 3 Pin Configuration of RDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
78	DQS6	I/O	SSTL	**Data Strobes 8:0**
86	DQS7	I/O	SSTL	
47	DQS8	I/O	SSTL	
97	DM0	I	SSTL	**Data Mask 0** *Note: ×8 based module*
	DQS9	I/O	SSTL	**Data Strobe 9** *Note: ×4 based module*
107	DM1	I	SSTL	**Data Mask 1** *Note: ×8 based module*
	DQS10	I/O	SSTL	**Data Strobe 10** *Note: ×4 based module*
119	DM2	I	SSTL	**Data Mask 2** *Note: ×8 based module*
	DQS11	I/O	SSTL	**Data Strobe 11** *Note: ×4 based module*
129	DM3	I	SSTL	**Data Mask 3** *Note: ×8 based module*
	DQS12	I/O	SSTL	**Data Strobe 12** *Note: ×4 based module*
149	DM4	I	SSTL	**Data Mask 4** *Note: ×8 based module*
	DQS13	I/O	SSTL	**Data Strobe 13** *Note: ×4 based module*
159	DM5	I	SSTL	**Data Mask 5** *Note: ×8 based module*
	DQS14	I/O	SSTL	**Data Strobe 14** *Note: ×4 based module*
169	DM6	I	SSTL	**Data Mask 6** *Note: ×8 based module*
	DQS15	I/O	SSTL	**Data Strobe 15** *Note: ×4 based module*
177	DM7	I	SSTL	**Data Mask 7** *Note: ×8 based module*
	DQS16	I/O	SSTL	**Data Strobe 16** *Note: ×4 based module*
140	DM8	I	SSTL	**Data Mask 8** *Note: ×8 based module*
	DQS17	I/O	SSTL	**Data Strobe 17** *Note: ×4 based module*

Table 3 Pin Configuration of RDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
EEPROM				
92	SCL	I	CMOS	**Serial Bus Clock**
91	SDA	I/O	OD	**Serial Bus Data**
181	SA0	I	CMOS	**Slave Address Select Bus 2:0**
182	SA1	I	CMOS	
183	SA2	I	CMOS	
Power Supplies				
1	V_{REF}	AI	–	**I/O Reference Voltage**
184	V_{DDSPD}	PWR	–	**EEPROM Power Supply**
15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	V_{DDQ}	PWR	–	**I/O Driver Power Supply**
7, 38, 46, 70, 85, 108, 120, 148, 168	V_{DD}	PWR	–	**Power Supply**

Table 3 Pin Configuration of RDIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	V_{SS}	GND	–	**Ground Plane**
Other Pins				
82	V_{DDID}	O	OD	**V_{DD} Identification** *Note: Pin in tristate, indicating V_{DD} and V_{DDQ} nets connected on PCB*
9, 16, 17, 71, 75, 76, 90, 101, 102, 103, 113, 163, 173	NC	NC	–	**Not connected** Pins not connected on Infineon RDIMM's

Table 4 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 5 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminalted Logic (SSTL2)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

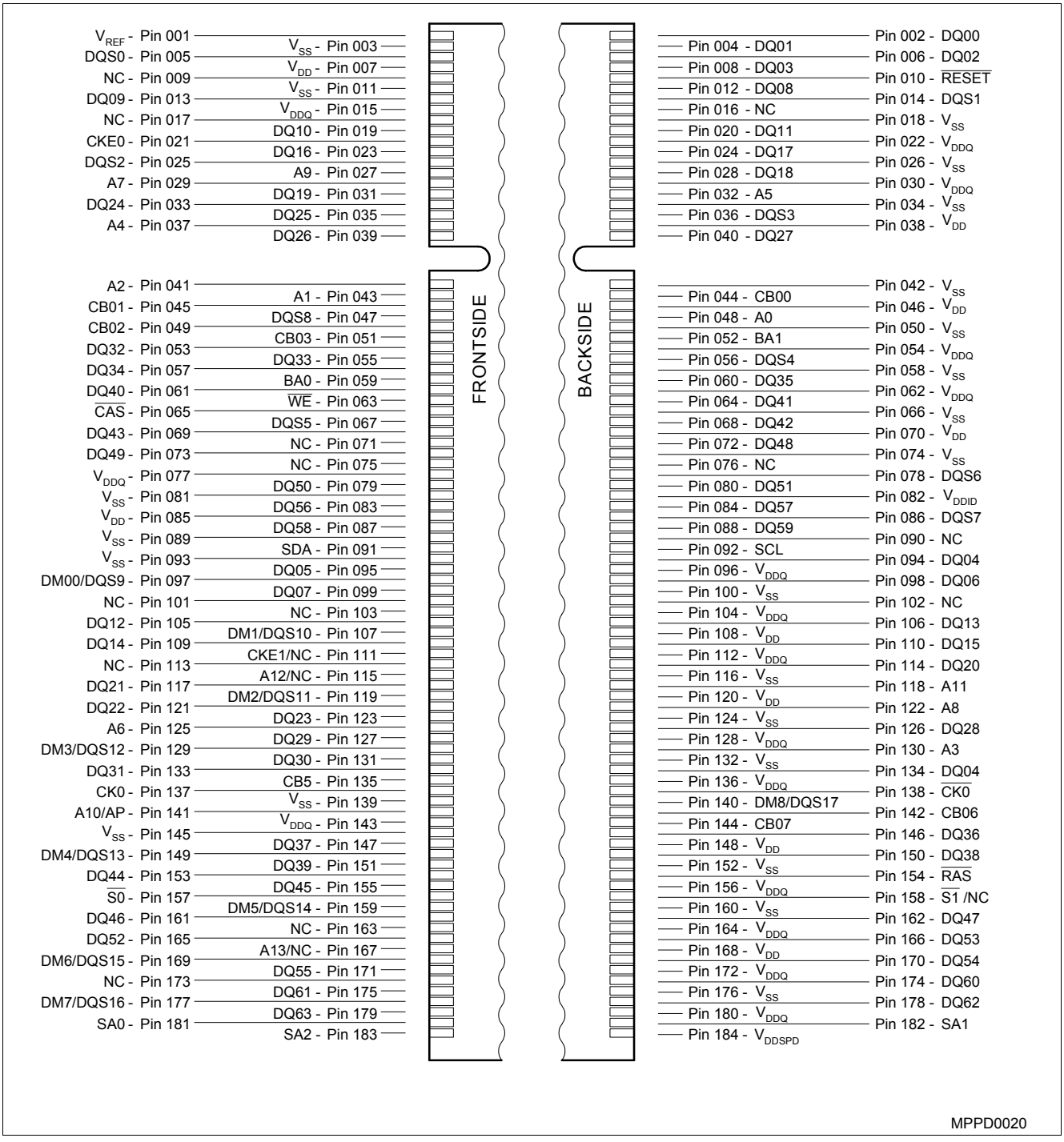

Figure 1 Pin Configuration 184 Pins, Reg

Table 6 Address Table

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/rank/ columns bits	Refresh	Period	Interval
256 MB	32 M ×72	1	32 M ×8	9	13 / 2 / 10	8 K	64 ms	7.8 µs
512 MB	64 M ×72	1	64 M ×4	18	13 / 2 / 11	8 K	64 ms	7.8 µs

Table 6 Address Table

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/rank/ columns bits	Refresh	Period	Interval
512 MB	64 M ×72	2	32 M ×8	18	13 / 2 / 10	8 K	64 ms	7.8 µs
1 GB	128 M ×72	2	64 M ×4	36	13 / 2 / 11	8 K	64 ms	7.8 µs

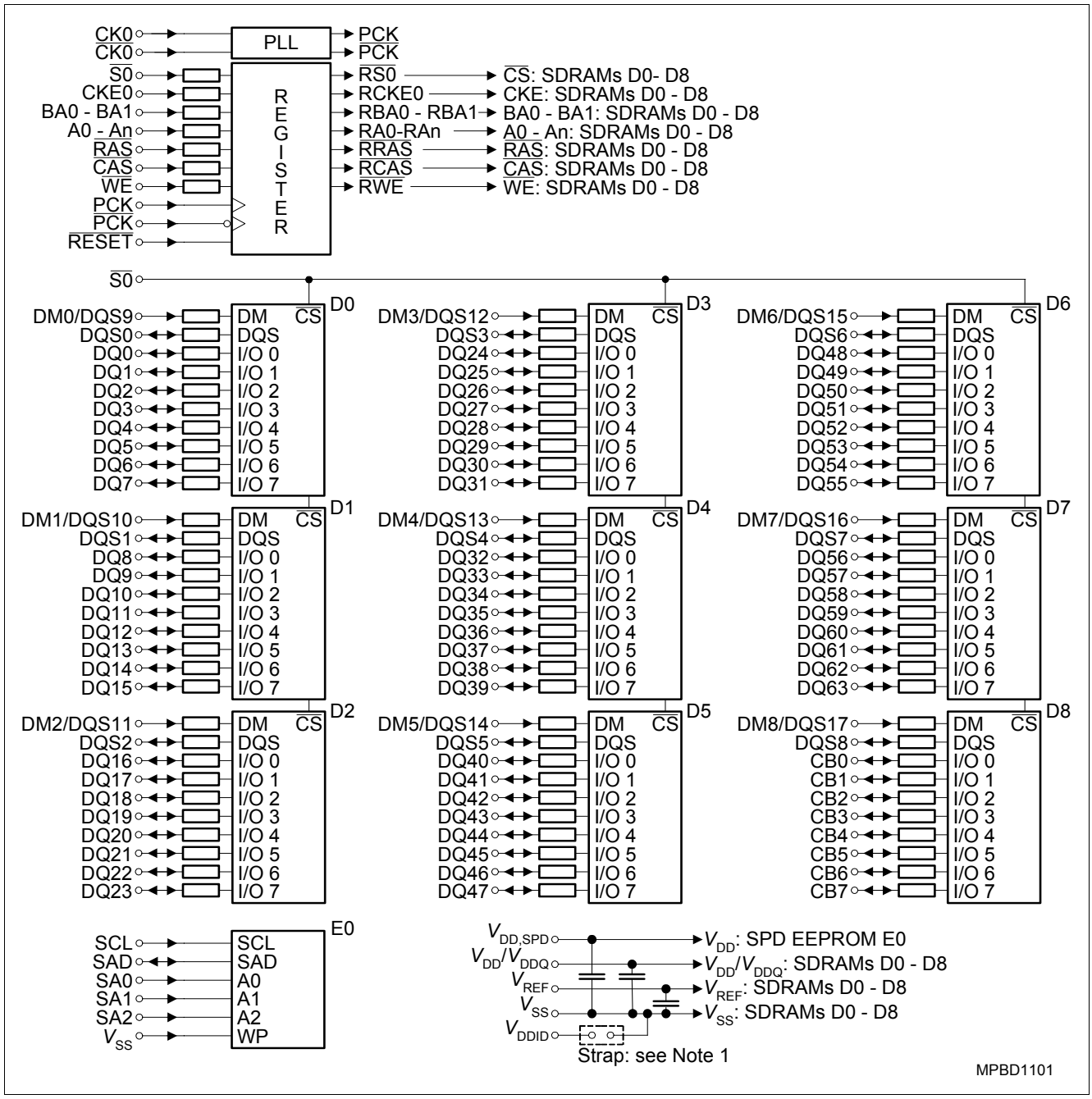

Figure 2 Block Diagram Raw Card A ×72 1 Rank ×8, ECC

Notes

1. *$V_{DD} = V_{DDQ}$, therefore V_{DDID} strap open*
2. *DQ, DQS, DM resistors are 22 ohms ± 5%*
3. *BAn, An, RAS, CAS, WE resistors are 22 ohms ± 5%*

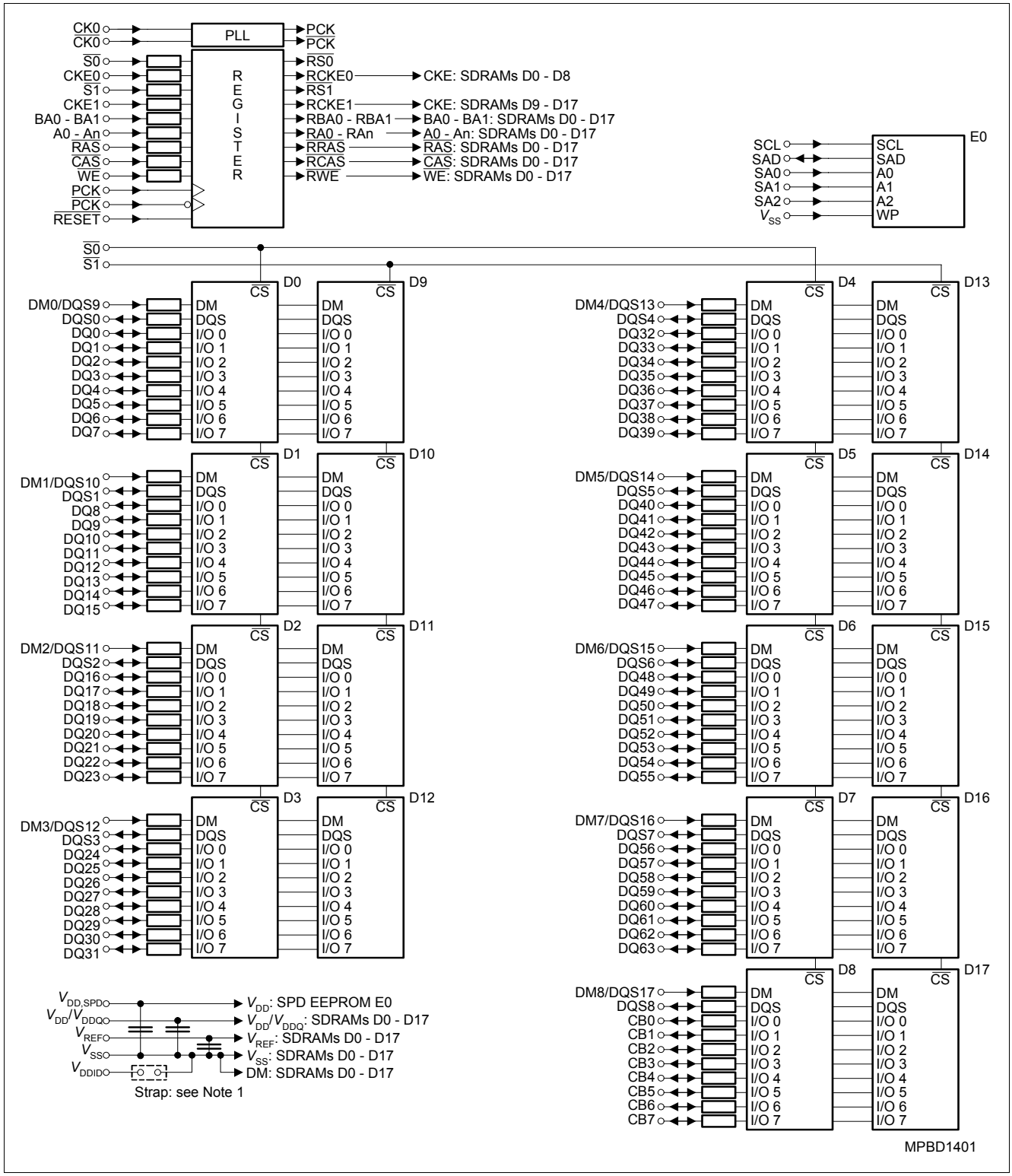

Figure 3 Block Diagram Raw Card B ×72, 2Ranks ×8, ECC

Notes

1. $V_{DD} = V_{DDQ}$, *therefore* V_{DDID} *strap open*
2. *DQ, DQS, DM resistors are 22 ohms ±5%*
3. *BAn, An,* $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ *resistors are 22 ohms ±5%*
4. *For Wire per Clock Loading please see Figure: "Diferential Clock Net Wiring"*

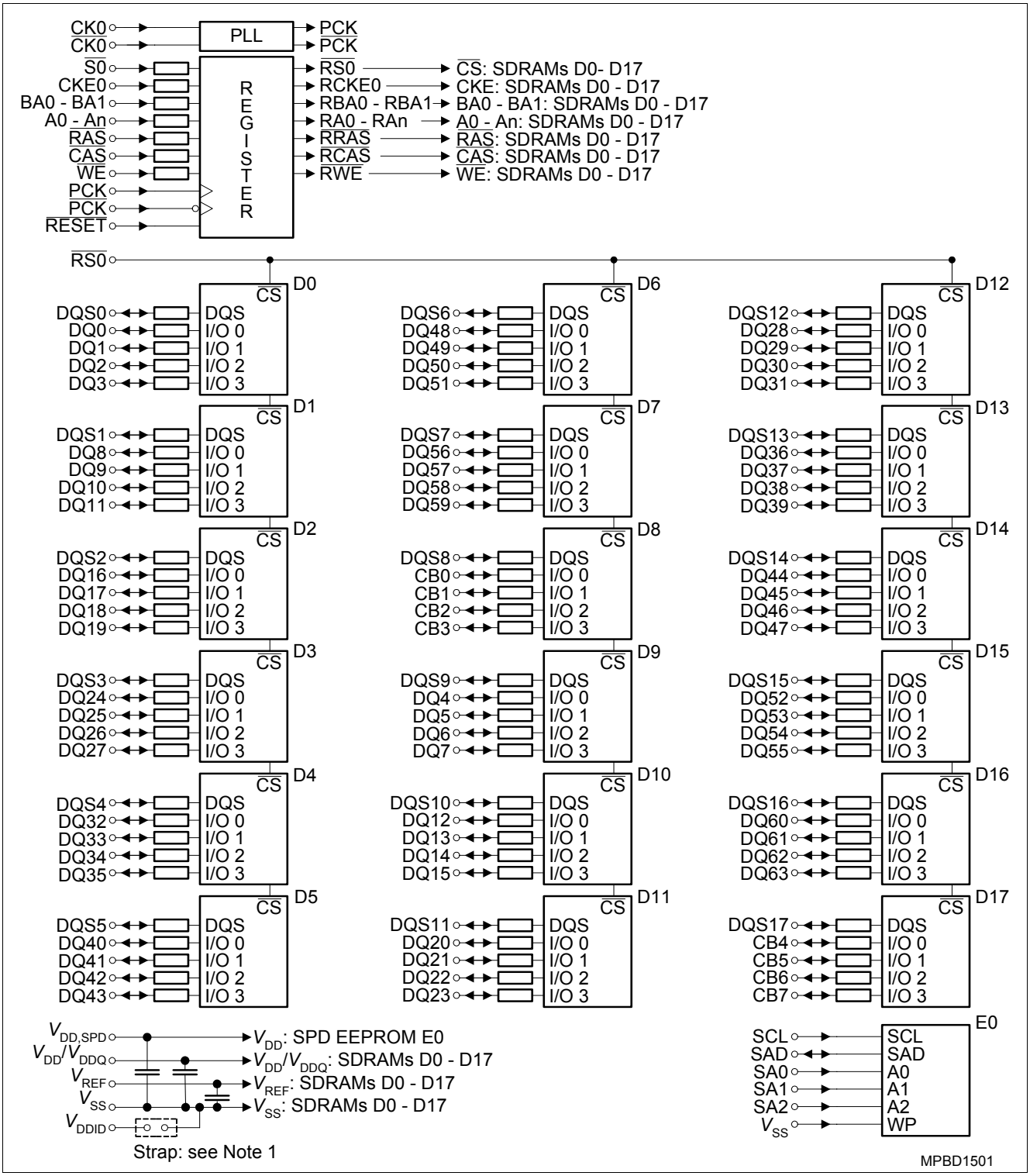

Figure 4 Block Diagram Raw Card C ×72 1 Rank ×4, ECC

Notes

1. *$V_{DD} = V_{DDQ}$, therefore V_{DDID} strap open*
2. *DQ, DQS, DM resistors are 22 ohms ± 5%*
3. *BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 22 ohms ± 5%*

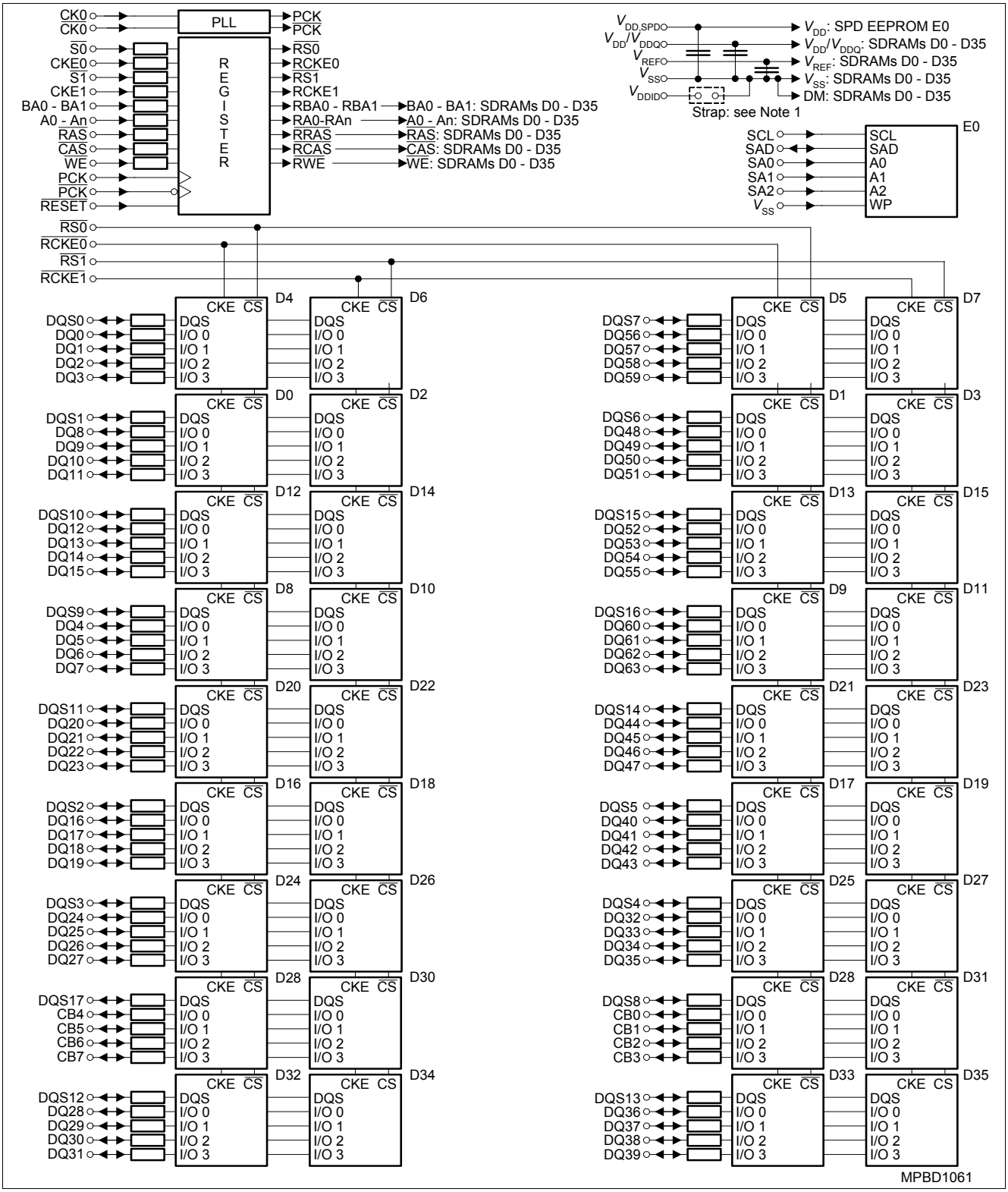

Figure 5 Block Diagram Raw Card D ×72 2 Ranks ×4, ECC

Notes

1. *$V_{DD} = V_{DDQ}$, therefore V_{DDID} strap open*
2. *DQ, DQS, DM resistors are 18 ohms ± 5%*
3. *BAn, An, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors are 22 ohms ± 5%*
4. *For Wire per Clock Loading please see Figure "Differental Clock Net Wiring"*

3 Electrical Characteristics

3.1 Operating Conditions

Table 7 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	–	V_{DDQ} +0.5	V	–
Voltage on inputs relative to V_{SS}	V_{IN}	–1	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	–	+3.6	V	–
Operating temperature (ambient)	T_A	0	–	+70	°C	–
Storage temperature (plastic)	T_{STG}	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	P_D	–	1	–	W	–
Short circuit output current	I_{OUT}	–	50	–	mA	–

Attention: Permanent damage to the device may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.

Table 8 Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	$f_{CK} \leq$ 166 MHz
Device Supply Voltage	V_{DD}	2.5	2.6	2.7	V	f_{CK} > 166 MHz [2]
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	$f_{CK} \leq$ 166 MHz [3]
Output Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V	f_{CK} > 166 MHz [2)3)]
EEPROM supply voltage	V_{DDSPD}	2.3	2.5	3.6	V	—
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0		0	V	—
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	[4]
I/O Termination Voltage (System)	V_{TT}	V_{REF} – 0.04		V_{REF} + 0.04	V	[5]
Input High (Logic1) Voltage	$V_{IH(DC)}$	V_{REF} + 0.15		V_{DDQ} + 0.3	V	[8]
Input Low (Logic0) Voltage	$V_{IL(DC)}$	–0.3		V_{REF} – 0.15	V	[8]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	–0.3		V_{DDQ} + 0.3	V	[8]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		V_{DDQ} + 0.6	V	[8)6)]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71		1.4	—	[7]

Table 8 Electrical Characteristics and DC Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Input Leakage Current	I_I	–2		2	µA	Any input 0 V $\leq V_{IN} \leq V_{DD}$; All other pins not under test = 0 V [8)9)]
Output Leakage Current	I_{OZ}	–5		5	µA	DQs are disabled; 0 V $\leq V_{OUT} \leq V_{DDQ}$
Output High Current, Normal Strength Driver	I_{OH}	—		–16.2	mA	V_{OUT} = 1.95 V
Output Low Current, Normal Strength Driver	I_{OL}	16.2		—	mA	V_{OUT} = 0.35 V

1) 0 °C $\leq T_A \leq$ 70 °C
2) DDR400 conditions apply for all clock frequencies above 166 MHz
3) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
4) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.
5) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
6) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
7) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
8) Inputs are not recognized as valid until V_{REF} stabilizes.
9) Values are shown per DDR SDRAM component

4 Current Specification and Conditions

Table 9 I_{DD} Conditions

Parameter	Symbol
Operating Current 0 one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current 1 one bank; active/read/precharge; Burst Length = 4; see component data sheet.	I_{DD1}
Precharge Power-Down Standby Current all banks idle; power-down mode; CKE ≤ $V_{IL,MAX}$	I_{DD2P}
Precharge Floating Standby Current $\overline{CS}$ ≥ $V_{IH,,MIN}$, all banks idle; CKE ≥ $V_{IH,MIN}$; address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current $\overline{CS}$ ≥ V_{IHMIN}, all banks idle; CKE ≥ $V_{IH,MIN}$; V_{IN} = V_{REF} for DQ, DQS and DM; address and other control inputs stable at ≥ $V_{IH,MIN}$ or ≤ $V_{IL,MAX}$.	I_{DD2Q}
Active Power-Down Standby Current one bank active; power-down mode; CKE ≤ V_{ILMAX}; V_{IN} = V_{REF} for DQ, DQS and DM.	I_{DD3P}
Active Standby Current one bank active; $\overline{CS}$ ≥ $V_{IH,MIN}$; CKE ≥ $V_{IH,MIN}$; t_{RC} = $t_{RAS,MAX}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current Read one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; I_{OUT} = 0 mA	I_{DD4R}
Operating Current Write one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	I_{DD4W}
Auto-Refresh Current t_{RC} = t_{RFCMIN}, burst refresh	I_{DD5}
Self-Refresh Current CKE ≤ 0.2 V; external clock on	I_{DD6}
Operating Current 7 four bank interleaving with Burst Length = 4; see component data sheet.	I_{DD7}

Table 10 I_{DD} Specification for PC3200

Part Number & Organization	HYS72D32300GBR–5–C		HYS72D64300GBR–5–C		HYS72D64320GBR–5–C		Unit	Note/ Test Conditions[1) 2)]
	256 MB		512 MB		512 MB			
	×72		×72		×72			
	1 Rank		1 Rank		2 Ranks			
	–5		–5		–5			
Symbol	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**		
I_{DD0}	1510	1690	2140	2500	1852	2095	mA	3)
I_{DD1}	1600	1780	2320	2680	1942	2185	mA	3)4)
I_{DD2P}	680	689	716	734	788	824	mA	5)
I_{DD2F}	914	968	1184	1292	1184	1292	mA	5)
I_{DD2Q}	824	896	1004	1148	1004	1148	mA	5)
I_{DD3P}	761	806	878	968	878	968	mA	5)
I_{DD3N}	986	1049	1328	1454	1328	1454	mA	5)
I_{DD4R}	1645	1780	2410	2680	1987	2185	mA	3)4)
I_{DD4W}	1690	1825	2500	2770	2032	2230	mA	3)
I_{DD5}	2140	2590	3400	4300	2482	2995	mA	3)
I_{DD6}	657	670	669	694	669	694	mA	5)
I_{DD7}	2770	3130	4660	5380	3112	3535	mA	3)4)

1) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

2) Module I_{DD} is calculated on the basis of component IDD and includes Register an PLL

3) The module I_{DD} values are calculated from the component I_{DD} datasheet values are:
$n * I_{DD}$×[component] for single bank modules (n: number of components per module bank)
$n * I_{DD}$×[component] + $n * I_{DD3N}$[component] for two bank modules (n: number of components per module bank)

4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

5) The module I_{DD} values are calculated from the component I_{DD} datasheet values are:
$n * I_{DD}$×[component] for single bank modules (n: number of components per module bank)
$2 * n * I_{DD}$×[component] for single two bank modules (n: number of components per module bank)

Table 11 I_{DD} Specification for PC2700

Part Number & Organization	HYS72D32300GBR–6–C		HYS72D64300GBR–6–C		HYS72D64320GBR–6–C		HYS72D128320GBR–6–C		Unit	Note/ Test Conditions[1) 2)]
	256 MB		512 MB		512 MB		1 GB			
	×72		×72		×72		×72			
	1 Rank		1 Rank		2 Ranks		2 Ranks			
	–6		–6		–6		–6			
Symbol	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Typ.**	**Max.**		
I_{DD0}	1270	1405	1810	2080	1558	1747	2386	2764	mA	3)
I_{DD1}	1360	1495	1990	2260	1648	1837	2566	2944	mA	3)4)
I_{DD2P}	466	475	502	520	574	610	718	790	mA	5)
I_{DD2F}	655	700	880	970	880	970	1330	1510	mA	5)
I_{DD2Q}	583	646	736	862	736	862	1042	1294	mA	5)
I_{DD3P}	529	565	628	700	628	700	826	970	mA	5)
I_{DD3N}	718	772	1006	1114	1006	1114	1582	1798	mA	5)
I_{DD4R}	1360	1495	1990	2260	1648	1837	2566	2944	mA	3)4)
I_{DD4W}	1405	1540	2080	2350	1693	1882	2656	3034	mA	3)
I_{DD5}	1810	2170	2890	3610	2098	2512	3466	4294	mA	3)
I_{DD6}	443	455	455	480	455	480	480	531	mA	5)
I_{DD7}	2350	2665	3970	4600	2638	3007	4546	5284	mA	3)4)

1) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

2) Module I_{DD} is calculated on the basis of component IDD and includes Register an PLL

3) The module I_{DD} values are calculated from the component I_{DD} datasheet values are:
$n * I_{DD}$×[component] for single bank modules (n: number of components per module bank)
$n * I_{DD}$×[component] + $n * I_{DD3N}$[component] for two bank modules (n: number of components per module bank)

4) DQ I/O (I_{DDQ}) currents are not included into calculations: module I_{DD} values will be measured differently depending on load conditions

5) The module I_{DD} values are calculated from the component I_{DD} datasheet values are:
$n * I_{DD}$×[component] for single bank modules (n: number of components per module bank)
$2 * n * I_{DD}$×[component] for single two bank modules (n: number of components per module bank)

4.1 AC Characteristics

Table 12 AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.5	+0.5	–0.7	+0.7	ns	2)3)4)5)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.6	+0.6	–0.6	+0.6	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Clock cycle time	t_{CK}	5	8	6	12	ns	CL = 3.0 2)3)4)5)
		6	12	6	12	ns	CL = 2.5 2)3)4)5)
		7.5	12	7.5	12	ns	CL = 2.0 2)3)4)5)
DQ and DM input hold time	t_{DH}	0.4	—	0.45	—	ns	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.4	—	0.45	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	t_{IPW}	2.2	—	2.2	—	ns	2)3)4)5)6)
DQ and DM input pulse width (each input)	t_{DIPW}	1.75	—	1.75	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	—	+0.7	–0.7	+0.7	ns	2)3)4)5)7)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.7	+0.7	–0.7	+0.7	ns	2)3)4)5)7)
Write command to 1st DQS latching transition	t_{DQSS}	0.72	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.40	—	+0.40	ns	TFBGA 2)3)4)5)
Data hold skew factor	t_{QHS}	—	+0.50	—	+0.50	ns	TFBGA 2)3)4)5)
DQ/DQS output hold time	t_{QH}	$t_{HP} - t_{QHS}$				ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)8)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)9)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)
Address and control input setup time	t_{IS}	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)10)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)10)
Address and control input hold time	t_{IH}	0.6	—	0.75	—	ns	fast slew rate 3)4)5)6)10)
		0.7	—	0.8	—	ns	slow slew rate 3)4)5)6)10)

Table 12 AC Timing - Absolute Specifications for PC3200 and PC2700

Parameter	Symbol	–5		–6		Unit	Note/ Test Condition [1]
		DDR400B		DDR333			
		Min.	Max.	Min.	Max.		
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	2)3)4)5)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)
Active to Precharge command	t_{RAS}	40	70E+3	42	70E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	55	—	60	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	70	—	72	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	15	—	18	—	ns	2)3)4)5)
Precharge command period	t_{RP}	15	—	18	—	ns	2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	t_{RCD} or t_{RASmin}				ns	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	10	—	12	—	ns	2)3)4)5)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{WR}/t_{CK})+(t_{RP}/t_{CK})$				t_{CK}	2)3)4)5)11)
Internal write to read command delay	t_{WTR}	2	—	1	—	t_{CK}	2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	75	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)12)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V (DDR333); V_{DDQ} = 2.6 V ± 0.1 V, V_{DD} = +2.6 V ± 0.1 V (DDR400)

2) Input slew rate ≥ 1 V/ns for DDR400, DDR333

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate ≥ 1.0 V/ns , slow slew rate ≥ 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{IH(ac)}$ and $V_{IL(ac)}$.

11) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

12) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

5 SPD Contents

Table 13 SPD Codes for HYS72D[128/64/32][300/320]GBR–5–C

	Product Type & Organization	HYS72D64300GBR–5–C	HYS72D64320GBR–5–C	HYS72D32300GBR–5–C
		512 MB	512 MB	256 MB
		×72	×72	×72
		1 Rank	2 Ranks	1 Rank
	Label Code	PC3200R–30331	PC3200R–30331	PC3200R–30331
	Jedec SPD Revision	Rev 1.0	Rev 1.0	Rev 1.0
Byte#	Description	HEX	HEX	HEX
0	Programmed SPD Bytes in E2PROM	80	80	80
1	Total number of Bytes in E2PROM	08	08	08
2	Memory Type (DDR = 07h)	07	07	07
3	Number of Row Addresses	0D	0D	0D
4	Number of Column Addresses	0B	0A	0A
5	Number of DIMM Ranks	01	02	01
6	Data Width (LSB)	48	48	48
7	Data Width (MSB)	00	00	00
8	Interface Voltage Levels	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	50	50	50
10	tAC SDRAM @ CLmax (Byte 18) [ns]	50	50	50
11	Error Correction Support	02	02	02
12	Refresh Rate	82	82	82
13	Primary SDRAM Width	04	08	08
14	Error Checking SDRAM Width	04	08	08
15	tCCD [cycles]	01	01	01
16	Burst Length Supported	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04
18	CAS Latency	1C	1C	1C
19	CS Latency	01	01	01
20	Write Latency	02	02	02
21	DIMM Attributes	26	26	26
22	Component Attributes	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	60	60	60
24	tAC SDRAM @ CLmax -0.5 [ns]	50	50	50
25	tCK @ CLmax -1 (Byte 18) [ns]	75	75	75

Table 13 SPD Codes for HYS72D[128/64/32][300/320]GBR–5–C

	Product Type & Organization	HYS72D64300GBR–5–C	HYS72D64320GBR–5–C	HYS72D32300GBR–5–C
		512 MB	512 MB	256 MB
		×72	×72	×72
		1 Rank	2 Ranks	1 Rank
	Label Code	PC3200R–30331	PC3200R–30331	PC3200R–30331
	Jedec SPD Revision	Rev 1.0	Rev 1.0	Rev 1.0
Byte#	Description	HEX	HEX	HEX
26	tAC SDRAM @ CLmax -1 [ns]	50	50	50
27	tRPmin [ns]	3C	3C	3C
28	tRRDmin [ns]	28	28	28
29	tRCDmin [ns]	3C	3C	3C
30	tRASmin [ns]	28	28	28
31	Module Density per Rank	80	40	40
32	tAS, tCS [ns]	60	60	60
33	tAH, TCH [ns]	60	60	60
34	tDS [ns]	40	40	40
35	tDH [ns]	40	40	40
36 - 40	not used	00	00	00
41	tRCmin [ns]	37	37	37
42	tRFCmin [ns]	41	41	41
43	tCKmax [ns]	28	28	28
44	tDQSQmax [ns]	28	28	28
45	tQHSmax [ns]	50	50	50
46	not used	00	00	00
47	DIMM PCB Height	01	01	01
48 - 61	not used	00	00	00
62	SPD Revision	10	10	10
63	Checksum of Byte 0-62	5F	27	26
64	JEDEC ID Code of Infineon (1)	C1	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00	00
72	Module Manufacturer Location	xx	xx	xx
73	Part Number, Char 1	37	37	37
74	Part Number, Char 2	32	32	32
75	Part Number, Char 3	44	44	44
76	Part Number, Char 4	36	36	33

Table 13 SPD Codes for HYS72D[128/64/32][300/320]GBR–5–C

	Product Type & Organization	HYS72D64300GBR–5–C	HYS72D64320GBR–5–C	HYS72D32300GBR–5–C
		512 MB	512 MB	256 MB
		×72	×72	×72
		1 Rank	2 Ranks	1 Rank
	Label Code	PC3200R–30331	PC3200R–30331	PC3200R–30331
	Jedec SPD Revision	Rev 1.0	Rev 1.0	Rev 1.0
Byte#	**Description**	**HEX**	**HEX**	**HEX**
77	Part Number, Char 5	34	34	32
78	Part Number, Char 6	33	33	33
79	Part Number, Char 7	30	32	30
80	Part Number, Char 8	30	30	30
81	Part Number, Char 9	47	47	47
82	Part Number, Char 10	42	42	42
83	Part Number, Char 11	52	52	52
84	Part Number, Char 12	35	35	35
85	Part Number, Char 13	43	43	43
86	Part Number, Char 14	20	20	20
87	Part Number, Char 15	20	20	20
88	Part Number, Char 16	20	20	20
89	Part Number, Char 17	20	20	20
90	Part Number, Char 18	20	20	20
91	Module Revision Code	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx
95 - 98	Module Serial Number (1 - 4)	xx	xx	xx
99 - 127	Blank	FF	FF	FF

Table 14 SPD Codes for HYS72D[128/64/32][300/320]GBR–6–C

	Product Type & Organization	HYS72D128320GBR–6–C	HYS72D64300GBR–6–C	HYS72D64320GBR–6–C	HYS72D32300GBR–6–C
		1 GByte	512 MB	512 MB	256 MB
		×72	×72	×72	×72
		2 Ranks	1 Rank	2 Ranks	1 Rank
	Label Code	PC2700R–25330	PC2700R–25330	PC2700R–25330	PC2700R–25330
	Jedec SPD Revision	Rev 0.0	Rev 0.0	Rev 0.0	Rev 0.0
Byte#	Description	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in E2PROM	80	80	80	80
1	Total number of Bytes in E2PROM	08	08	08	08
2	Memory Type (DDR = 07h)	07	07	07	07
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0B	0B	0A	0A
5	Number of DIMM Ranks	02	01	02	01
6	Data Width (LSB)	48	48	48	48
7	Data Width (MSB)	00	00	00	00
8	Interface Voltage Levels	04	04	04	04
9	tCK @ CLmax (Byte 18) [ns]	60	60	60	60
10	tAC SDRAM @ CLmax (Byte 18) [ns]	70	70	70	70
11	Error Correction Support	02	02	02	02
12	Refresh Rate	82	82	82	82
13	Primary SDRAM Width	04	04	08	08
14	Error Checking SDRAM Width	04	04	08	08
15	tCCD [cycles]	01	01	01	01
16	Burst Length Supported	0E	0E	0E	0E
17	Number of Banks on SDRAM Device	04	04	04	04
18	CAS Latency	0C	0C	0C	0C
19	CS Latency	01	01	01	01
20	Write Latency	02	02	02	02
21	DIMM Attributes	26	26	26	26
22	Component Attributes	C1	C1	C1	C1
23	tCK @ CLmax -0.5 (Byte 18) [ns]	75	75	75	75
24	tAC SDRAM @ CLmax -0.5 [ns]	70	70	70	70
25	tCK @ CLmax -1 (Byte 18) [ns]	00	00	00	00

Table 14 SPD Codes for HYS72D[128/64/32][300/320]GBR–6–C

	Product Type & Organization	HYS72D128320GBR–6–C	HYS72D64300GBR–6–C	HYS72D64320GBR–6–C	HYS72D32300GBR–6–C
		1 GByte	512 MB	512 MB	256 MB
		×72	×72	×72	×72
		2 Ranks	1 Rank	2 Ranks	1 Rank
	Label Code	**PC2700R–25330**	**PC2700R–25330**	**PC2700R–25330**	**PC2700R–25330**
	Jedec SPD Revision	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**	**Rev 0.0**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
26	tAC SDRAM @ CLmax -1 [ns]	00	00	00	00
27	tRPmin [ns]	48	48	48	48
28	tRRDmin [ns]	30	30	30	30
29	tRCDmin [ns]	48	48	48	48
30	tRASmin [ns]	2A	2A	2A	2A
31	Module Density per Rank	80	80	40	40
32	tAS, tCS [ns]	75	75	75	75
33	tAH, TCH [ns]	75	75	75	75
34	tDS [ns]	45	45	45	45
35	tDH [ns]	45	45	45	45
36 - 40	not used	00	00	00	00
41	tRCmin [ns]	3C	3C	3C	3C
42	tRFCmin [ns]	48	48	48	48
43	tCKmax [ns]	30	30	30	30
44	tDQSQmax [ns]	28	28	28	28
45	tQHSmax [ns]	50	50	50	50
46	not used	00	00	00	00
47	DIMM PCB Height	00	00	00	00
48 - 61	not used	00	00	00	00
62	SPD Revision	00	00	00	00
63	Checksum of Byte 0-62	49	48	10	0F
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1
65 - 71	JEDEC ID Code of Infineon (2 - 8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Part Number, Char 1	37	37	37	37
74	Part Number, Char 2	32	32	32	32
75	Part Number, Char 3	44	44	44	44

Table 14 SPD Codes for HYS72D[128/64/32][300/320]GBR–6–C

	Product Type & Organization	HYS72D128320GBR–6–C	HYS72D64300GBR–6–C	HYS72D64320GBR–6–C	HYS72D32300GBR–6–C
		1 GByte	512 MB	512 MB	256 MB
		×72	×72	×72	×72
		2 Ranks	1 Rank	2 Ranks	1 Rank
	Label Code	PC2700R–25330	PC2700R–25330	PC2700R–25330	PC2700R–25330
	Jedec SPD Revision	Rev 0.0	Rev 0.0	Rev 0.0	Rev 0.0
Byte#	Description	HEX	HEX	HEX	HEX
76	Part Number, Char 4	31	36	36	33
77	Part Number, Char 5	32	34	34	32
78	Part Number, Char 6	38	33	33	33
79	Part Number, Char 7	33	30	32	30
80	Part Number, Char 8	32	30	30	30
81	Part Number, Char 9	30	47	47	47
82	Part Number, Char 10	47	42	42	42
83	Part Number, Char 11	42	52	52	52
84	Part Number, Char 12	52	36	36	36
85	Part Number, Char 13	36	43	43	43
86	Part Number, Char 14	43	20	20	20
87	Part Number, Char 15	20	20	20	20
88	Part Number, Char 16	20	20	20	20
89	Part Number, Char 17	20	20	20	20
90	Part Number, Char 18	20	20	20	20
91	Module Revision Code	xx	xx	xx	xx
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number (1 - 4)	xx	xx	xx	xx
99 -127	Blank	FF	FF	FF0	FF

6 Package Outlines

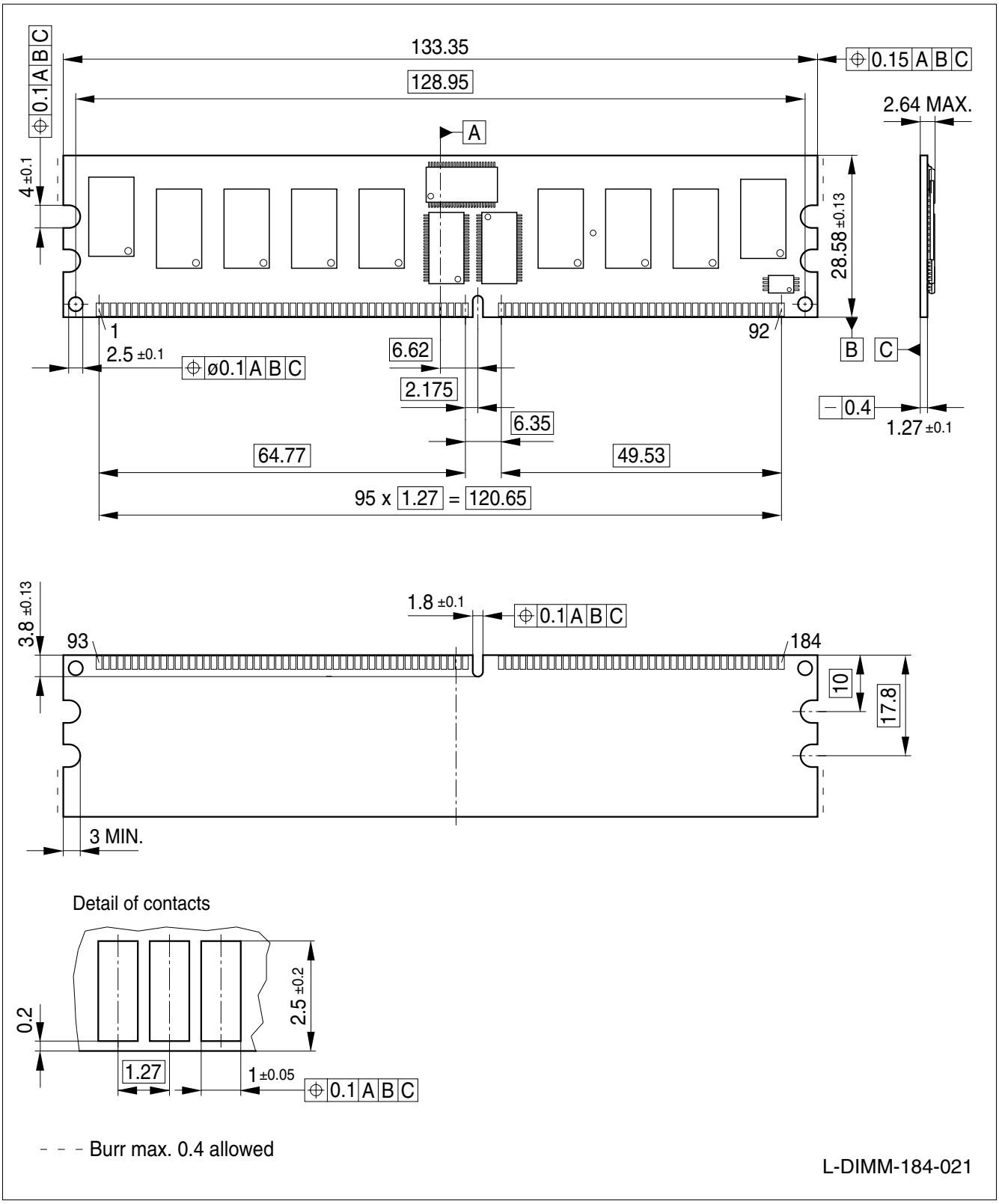

Figure 6 Package Outlines – Raw Card A HYS72D32300GBR–[5/6]–C (1 Rank × 8)

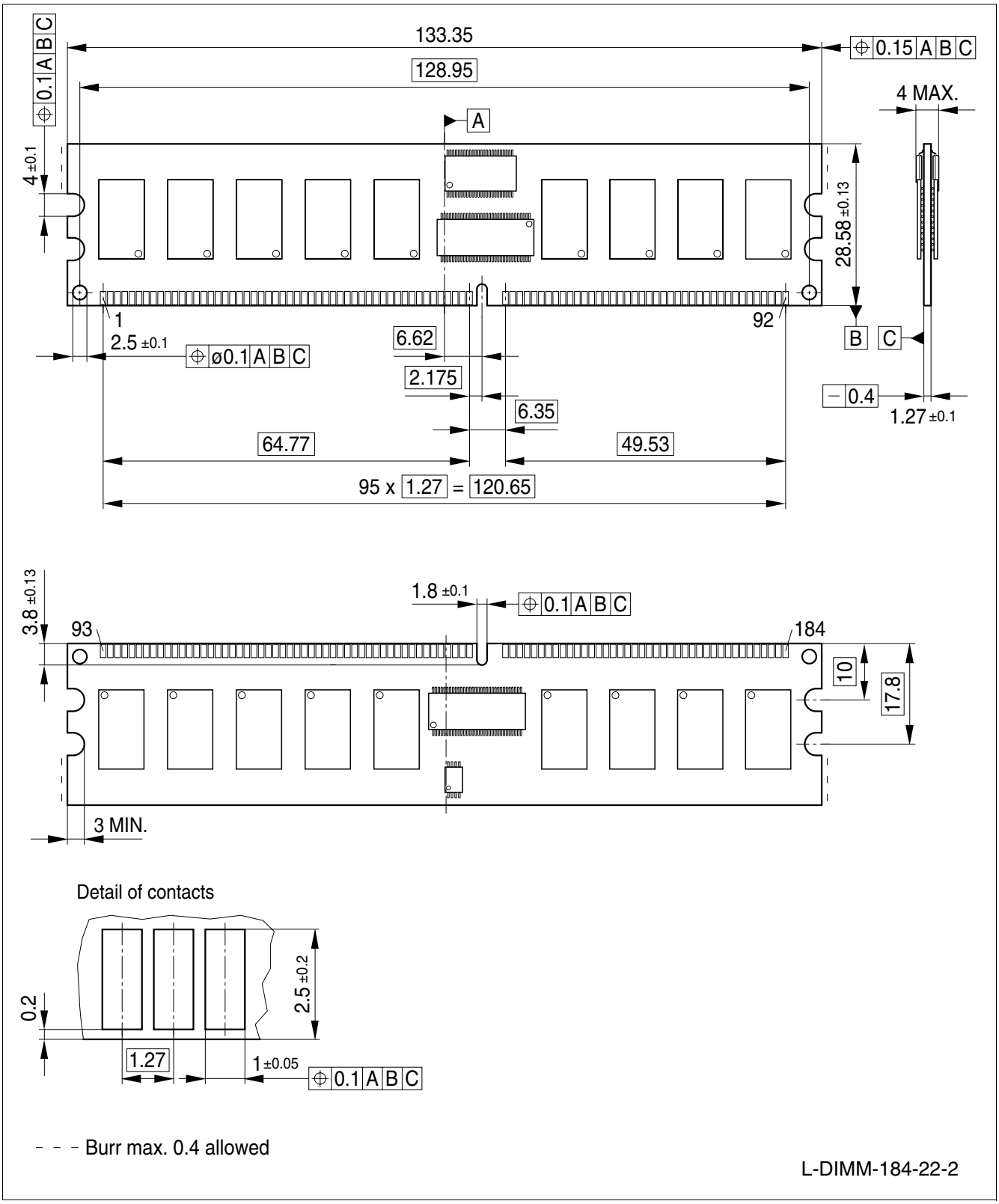

Figure 7 Package Outlines – Raw Card C HYS72D64300GBR–[5/6]–C (1 Rank × 4)

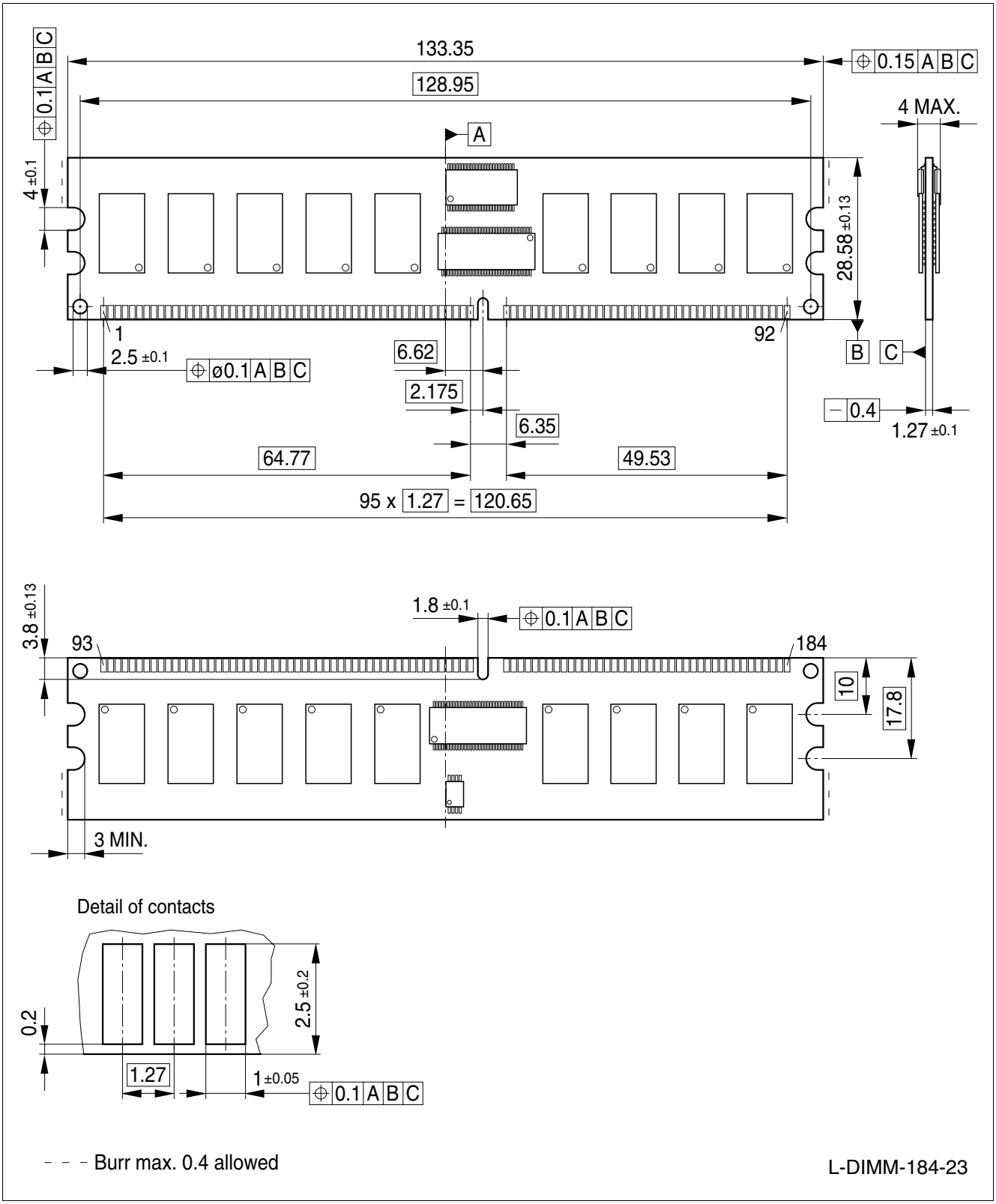

Figure 8 Package Outlines – Raw Card B HYS72D64320GBR–[5/6]–C (2 Ranks ×8)

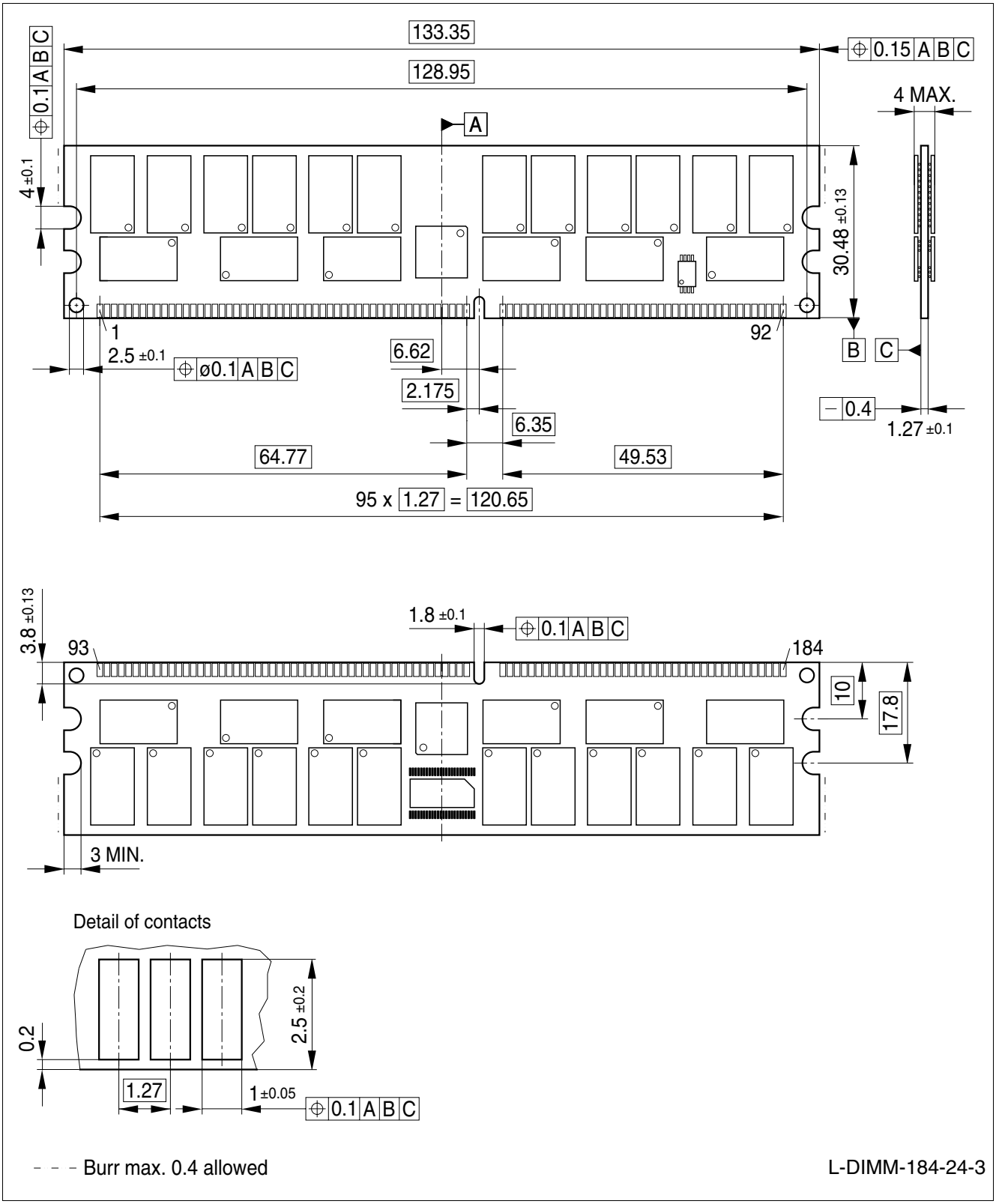

Figure 9 Package Outlines – Raw Card D HYS72D128320GBR–[5/6]–C (2 Ranks ×4)

7 Application Note

Power Up and Power Management on DDR Registered DIMMs (according to JEDEC ballot JC-42.5 Item 1173)

184-pin Double Data Rate (DDR) Registered DIMMs include two new features to facilitate controlled power-up and to minimize power consumption during low power mode. One feature is externally controlled via a system-generated RESET signal; the second is based on module detection of the input clocks. These enhancements permit the modules to power up with SDRAM outputs in a High-Z state (eliminating risk of high current dissipations and/or dotted I/Os), and result in the powering-down of module support devices (registers and Phase-Locked Loop) when the memory is in Self-Refresh mode.

The new RESET pin controls power dissipation on the module's registers and ensures that CKE and other SDRAM inputs are maintained at a valid 'low' level during power-up and self refresh. When RESET is at a low level, all the register outputs are forced to a low level, and all differential register input receivers are powered down, resulting in very low register power consumption. The $\overline{\text{RESET}}$ pin, located on DIMM tab #10, is driven from the system as an asynchronous signal according to the attached details. Using this function also permits the system and DIMM clocks to be stopped during memory Self Refresh operation, while ensuring that the SDRAMs stay in Self Refresh mode.

Table 15 $\overline{\text{RESET}}$ Truth Table

Register Inputs				Register Outputs
$\overline{\text{RESET}}$	CK	$\overline{\text{CK}}$	Data in (D)	Data out (Q)
H	Rising	Falling	H	H
H	Rising	Falling	L	L
H	L or H	L or H	X	Qo
H	High Z	High Z	X	Illegal input conditions
L	X or Hi-Z	X or Hi-Z	X or Hi-Z	L
X: Don't care, Hi-Z: High Impedance, Qo: Data latched at the previous of CK rising and $\overline{\text{CK}}$ falling				

As described in the table above, a low on the $\overline{\text{RESET}}$ input ensures that the Clock Enable (CKE) signal(s) are maintained low at the SDRAM pins (CKE being one of the 'Q' signals at the register output). Holding CKE low maintains a high impedance state on the SDRAM DQ, DQS and DM outputs — where they will remain until activated by a valid 'read' cycle. CKE low also maintains SDRAMs in Self Refresh mode when applicable.

The DDR PLL devices automatically detect clock activity above 20MHz. When an input clock frequency of 20MHz or greater is detected, the PLL begins operation and initiates clock frequency lock (the minimum operating frequency at which all specifications will be met is 95MHz). If the clock input frequency drops below 20MHz (actual detect frequency will vary by vendor), the PLL VCO (Voltage Controlled Oscillator) is stopped, outputs are made High-Z, and the differential inputs are powered down — resulting in a total PLL current consumption of less than 1mA. Use of this low power PLL function makes the use of the PLL $\overline{\text{RESET}}$ (or $\overline{\text{G}}$ pin) unnecessary, and it is tied inactive on the DIMM.

This application note describes the required and optional system sequences associated with the DDR Registered DIMM '$\overline{\text{RESET}}$' function. It is important to note that all references to CKE refer to both CKE0 and CKE1 for a 2-bank DIMM. Because $\overline{\text{RESET}}$ applies to all DIMM register devices, it is therefore not possible to uniquely control CKE to one physical DIMM bank through the use of the $\overline{\text{RESET}}$ pin.

Power-Up Sequence with $\overline{\text{RESET}}$ — Required

1. The system sets $\overline{\text{RESET}}$ at a valid low level.
   This is the preferred default state during power-up. This input condition forces all register outputs to a low state independent of the condition on the register inputs (data and clock), ensuring that CKE is at a stable low-level at the DDR SDRAMs.
2. The power supplies should be initialized according to the JEDEC-approved initialization sequence for DDR SDRAMs.
3. Stabilization of Clocks to the SDRAM
   The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches 20 MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds. When a stable clock is present at the SDRAM input (driven from the PLL), the DDR SDRAM requires 200 µsec prior to SDRAM operation.
4. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector).
   CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM ‘NOP’ command (with CKE low), as this is the first command defined by the JEDEC initialization sequence (ideally this would be a ‘NOP Deselect’ command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.
5. The system switches $\overline{\text{RESET}}$ to a logic ‘high’ level.
   The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, setting the $\overline{\text{RESET}}$ timing in relation to a specific clock edge is not required (during this period, register inputs must remain stable).
6. The system must maintain stable register inputs until normal register operation is attained.
   The registers have an activation time that allows their clock receivers, data input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in step 5. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time (t (ACT)), from asynchronous switching of $\overline{\text{RESET}}$ from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM do-umentation.
7. The system can begin the JEDEC-defined DDR SDRAM power-up sequence (according to the JEDEC-pproved initialization sequence).

Self Refresh Entry ($\overline{\text{RESET}}$ low, clocks powered off) — Optional

Self Refresh can be used to retain data in DDR SDRAM DIMMs even if the rest of the system is powered down and the clocks are off. This mode allows the DDR SDRAMs on the DIMM to retain data without external clocking. Self Refresh mode is an ideal time to utilize the $\overline{\text{RESET}}$ pin, as this can reduce register power consumption ($\overline{\text{RESET}}$ low deactivates register CK and CK, data input receivers, and data output drivers).

1. 1. The system applies Self Refresh entry command.
   (CKE→Low, $\overline{\text{CS}}$→Low, $\overline{\text{RAS}}$ → Low, $\overline{\text{CAS}}$→ Low, $\overline{\text{WE}}$→ High)

Note: Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don’t Cares— with the exception of CKE.

2. The system sets $\overline{\text{RESET}}$ at a valid low level.
   This input condition forces all register outputs to a low state, independent of the condition on the registerm inputs (data and clock), and ensures that CKE, and all other control and address signals, are a stable low-level at the DDR SDRAMs. Since the $\overline{\text{RESET}}$ signal is asynchronous, setting the $\overline{\text{RESET}}$ timing in relation to a specific clock edge is not required.
3. The system turns off clock inputs to the DIMM. (Optional)
   a. In order to reduce DIMM PLL current, the clock inputs to the DIMM are turned off, resulting in High-Z clock

inputs to both the SDRAMs and the registers. This must be done after the $\overline{\text{RESET}}$ deactivate time of the register (t (INACT). The deactivate time defines the time in which the clocks and the control and address signals must maintain valid levels after $\overline{\text{RESET}}$ low has been applied and is specified in the register and DIMM documentation.

b.The system may release DIMM address and control inputs to High-Z.

This can be done after the $\overline{\text{RESET}}$ deactivate time of the register. The deactivate time defines the time in which the clocks and the control and the address signals must maintain valid levels after $\overline{\text{RESET}}$ low has been applied. It is highly recommended that CKE continue to remain low during this operation.

4. The DIMM is in lowest power Self Refresh mode.

Self Refresh Exit ($\overline{\text{RESET}}$ low, clocks powered off) — Optional

1. Stabilization of Clocks to the SDRAM.
   The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches ~20MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds.
2. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector).
   CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM ‘NOP’ command (with CKE low), as this is the first command defined by the JEDEC Self Refresh Exit sequence (ideally this would be a ‘NOP Deselect’ command). A second option is to apply low levels on all of the register inputs, to be consistent with the state of the register outputs.
3. The system switches $\overline{\text{RESET}}$ to a logic ‘high’ level.
   The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, $\overline{\text{RESET}}$ timing relationship to a specific clock edge is not required (during this period, register inputs must remain stable).
4. The system must maintain stable register inputs until normal register operation is attained.
   The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 2. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time (t (ACT)), from asynchronous switching of $\overline{\text{RESET}}$ from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM do-umentation.
5. System can begin the JEDEC-defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry ($\overline{\text{RESET}}$ low, clocks running) — Optional

Although keeping the clocks running increases power consumption from the on-DIMM PLL during self refresh, this is an alternate operating mode for these DIMMs.

1. 1. System enters Self Refresh entry command.
   (CKE→ Low, $\overline{\text{CS}}$→ Low, $\overline{\text{RAS}}$→ Low, $\overline{\text{CAS}}$→ Low, $\overline{\text{WE}}$→ High)

Note: Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don’t Cares — with the exception of CKE.

2. The system sets $\overline{\text{RESET}}$ at a valid low level.
   This input condition forces all register outputs to a low state, independent of the condition on the data and clock register inputs, and ensures that CKE is a stable low-level at the DDR SDRAMs.
3. The system may release DIMM address and control inputs to High-Z.
   This can be done after the $\overline{\text{RESET}}$ deactivate time of the register (t (INACT)). The deactivate time describes the time in which the clocks and the control and the address signals must maintain valid levels after $\overline{\text{RESET}}$ low has been applied. It is highly recommended that CKE continue to remain low during the operation.
4. The DIMM is in a low power, Self Refresh mode.

Self Refresh Exit ($\overline{\text{RESET}}$ low, clocks running) — Optional

1. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector). CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM ‘NOP’ command (with CKE low), as this is the first command defined by the Self Refresh Exit sequence (ideally this would be a ‘NOP Deselect’ command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.
2. The system switches $\overline{\text{RESET}}$ to a logic 'high' level.
   The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, it does not need to be tied to a particular clock edge (during this period, register inputs must continue to remain stable).
3. The system must maintain stable register inputs until normal register operation is attained.
   The registers have an activation time that allows the clock receivers, input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in Step 1. It is also a functional requirement that the registers maintain a low state at the CKE outputs in order to guarantee that the DDR SDRAMs continue to receive a low level on CKE. This activation time, from asynchronous switching of $\overline{\text{RESET}}$ from low to high, until the registers are stable and ready to accept an input signal, is t (ACT) as specified in the register and DIMM documentation.
4. The system can begin JEDEC defined DDR SDRAM Self Refresh Exit Procedure.

Self Refresh Entry/Exit ($\overline{\text{RESET}}$ high, clocks running) — Optional

As this sequence does not involve the use of the $\overline{\text{RESET}}$ function, the JEDEC standard SDRAM specification explains in detail the method for entering and exiting Self Refresh for this case.

Self Refresh Entry ($\overline{\text{RESET}}$ high, clocks powered off) — Not Permissible

In order to maintain a valid low level on the register output, it is required that either the clocks be running and the system drive a low level on CKE, or the clocks are powered off and $\overline{\text{RESET}}$ is asserted low according to the sequence defined in this application note. In the case where $\overline{\text{RESET}}$ remains high and the clocks are powered off, the PLL drives a High-Z clock input into the register clock input. Without the low level on $\overline{\text{RESET}}$ an unknown DIMM state will result.

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