Data Sheet, Rev. 1.04, Jan. 2004

HYS72D16000GR-[7/8]-A
HYS72D32001GR-[7/8]-A

Registered DDR SDRAM-Modules
DDR SDRAM

Memory Products

Infineon technologies

Never stop thinking.

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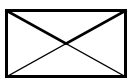

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1 Overview

1.1 Features

- 184-pin Registered 8 Byte Dual-In-Line DDR SDRAM Module for PC and Server main memory applications
- One bank 16M u72 and 32M u72 organization
- JEDEC standard Double Data Rate Synchronous DRAMs (DDR SDRAM) with a single +2.5 V (r 0.2 V) power supply
- Built with 128 Mbit DDR SDRAMs in 66-Lead TSOPII package
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_2 compatible
- Re-drive for all input signals using register and PLL devices.
- Serial Presence Detect with E^2PROM
- JEDEC standard MO-206 form factor:
  133.35 mm (nom.) u43.18 mm (nom.) u4.00 mm (max.)
  (6,80 mm max. with stacked components)
- JEDEC standard reference layout:
  Raw Cards A, B and C
- Gold plated contacts

Table 1 Performance -8/-7

Part Number Speed Code			–7	–8	Unit
Speed Grade	Component		DDR266A	DDR200	—
	Module		PC2100-2033	PC1600-2022	—
max. Clock Frequency	@CL2.5	$f_{CK2.5}$	143	125	MHz
	@CL2	f_{CK2}	133	100	MHz

1.2 Description

The HYS 72D u 0 u0GR are industry standard 184-pin 8 byte Dual in-line Memory Modules (DIMMs) organized as 16M u72 (128 MB) and 32M u72 (256 MB). The memory array is designed with Double Data Rate Synchronous DRAMs for ECC applications. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. A variety of decoupling capacitors are mounted on the PC board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.

Table 2 Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC2100 (CL=2)			
HYS72D16000GR-7-A	PC2100R-20330-A1	one bank 128 MB Reg. DIMM	128 Mbit (x8)
HYS72D32001GR-7-A	PC2100R-20330-B1	one bank 256 MB Reg. DIMM	128 Mbit (x4)
PC1600 (CL=2)			
HYS72D16000GR-8-A	PC1600R-20220-A1	one bank 128 MB Reg. DIMM	128 Mbit (x8)
HYS72D32001GR-8-A	PC1600R-20220-B1	one bank 256 MB Reg. DIMM	128 Mbit (x4)

Note: All part numbers end with a place code (not shown), designating the silicon-die revision. Reference information available on request. Example: HYS72D16000GR-8-A, indicating Rev. A die are used for SDRAM components The Compliance Code is printed on the module labels and describes the speed sort for example “PC2100R”, the latencies (for example “20330” means CAS latency = 2, t_{RCD} latency = 3 and t_{RP} latency = 3) and the Raw Card used for this module.

2 Pin Configuration

Table 3 Pin Definitions and Functions

Symbol	Type	Function
A0 – A11	Input	Address Inputs
BA0, BA1	Input	Rank Selects
DQ0 – DQ63	Input/Output	Data Input/Output
CB0 – CB7	Input/Output	Check Bits (u72 organization only)
$\overline{RAS}$	Input	Row Address Strobe
$\overline{CAS}$	Input	Column Address Strobe
$\overline{WE}$	Input	Read/Write Input
CKE0, CKE1	Input	Clock Enable
DQS0 – DQS8	Input/Output	SDRAM low data strobes
CK0, $\overline{CK0}$	Input	Differential Clock Input
DM0 – DM8	Input	SDRAM low data mask
DQS9 – DQS17	Input/Output	high data strobes
$\overline{CS0}$, $\overline{CS1}$	Input	Chip Selects
V_{DD}	Supply	Power (+2.5 V)
V_{SS}	Supply	Ground
V_{DDQ}	Supply	I/O Driver power supply
V_{DDID}	Output	V_{DD} Indentification flag
V_{DDSPD}	Supply	EEPROM power supply
V_{REF}	Supply	I/O reference supply
SCL	Input	Serial bus clock
SDA	Output	Serial bus data line
SA0 – SA2	Input	slave address select
NC	Input	no connect
DU	Input	don’t use
RESET	Input	Reset pin (forces register inputs low) *)

*) for detailed description of the Power Up and Power Management on DDR Registered DIMMs see the Application Note at the end of this datasheet

Table 4 Address Format

Density	Organization	Memory Ranks	SDRAMs	# of SDRAMs	# of row/rank/ columns bits	Refresh	Period	Interval
128 MB	16M u72	1	16M u8	9	12/2/10	4K	64 ms	15.6 µs
256 MB	32M u72	1	32M u4	18	12/2/11	4K	64 ms	15.6 µs

Table 5 Pin Configuration

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	V_{REF}	48	A0	94	DQ4	141	A10
2	DQ0	49	CB2	95	DQ5	142	CB6
3	V_{SS}	50	V_{SS}	96	V_{DDQ}	143	V_{DDQ}
4	DQ1	51	CB3	97	DM0/DQS9	144	CB7
5	DQS0	52	BA1	98	DQ6	KEY	
6	DQ2	KEY		99	DQ7	145	V_{SS}
7	V_{DD}	53	DQ32	100	V_{SS}	146	DQ36
8	DQ3	54	V_{DDQ}	101	NC	147	DQ37
9	NC	55	DQ33	102	NC	148	V_{DD}
10	$\overline{\text{RESET}}$	56	DQS4	103	NC	149	DM4/DQS13
11	V_{SS}	57	DQ34	104	V_{DDQ}	150	DQ38
12	DQ8	58	V_{SS}	105	DQ12	151	DQ39
13	DQ9	59	BA0	106	DQ13	152	V_{SS}
14	DQS1	60	DQ35	107	DM1/DQS10	153	DQ44
15	V_{DDQ}	61	DQ40	108	V_{DD}	154	$\overline{\text{RAS}}$
16	DU	62	V_{DDQ}	109	DQ14	155	DQ45
17	DU	63	$\overline{\text{WE}}$	110	DQ15	156	V_{DDQ}
18	V_{SS}	64	DQ41	111	CKE1	157	CS0
19	DQ10	65	$\overline{\text{CAS}}$	112	V_{DDQ}	158	CS1
20	DQ11	66	V_{SS}	113	NC	159	DM5/DQS14
21	CKE0	67	DQS5	114	DQ20	160	V_{SS}
22	V_{DDQ}	68	DQ42	115	NC/A12 A12 is used for 256 Mbit and 512 Mbit based modules only	161	DQ46
23	DQ16	69	DQ43	116	V_{SS}	162	DQ47
24	DQ17	70	V_{DD}	117	DQ21	163	NC
25	DQS2	71	NC	118	A11	164	V_{DDQ}
26	V_{SS}	72	DQ48	119	DM2/DQS11	165	DQ52
27	A9	73	DQ49	120	V_{DD}	166	DQ53
28	DQ18	74	V_{SS}	121	DQ22	167	NC
29	A7	75	DU	122	A8	168	V_{DD}
30	V_{DDQ}	76	DU	123	DQ23	169	DM6/DQS15
31	DQ19	77	V_{DDQ}	124	V_{SS}	170	DQ54
32	A5	78	DQS6	125	A6	171	DQ55
33	DQ24	79	DQ50	126	DQ28	172	V_{DDQ}
34	V_{SS}	80	DQ51	127	DQ29	173	NC
35	DQ25	81	V_{SS}	128	V_{DDQ}	174	DQ60
36	DQS3	82	V_{DDID}	129	DM3/DQS12	175	DQ61
37	A4	83	DQ56	130	A3	176	V_{SS}
38	V_{DD}	84	DQ57	131	DQ30	177	DM7/DQS16

Table 5 Pin Configuration (cont'd)

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
39	DQ26	85	V_{DD}	132	V_{SS}	178	DQ62
40	DQ27	86	DQS7	133	DQ31	179	DQ63
41	A2	87	DQ58	134	CB4	180	V_{DDQ}
42	V_{SS}	88	DQ59	135	CB5	181	SA0
43	A1	89	V_{SS}	136	V_{DDQ}	182	SA1
44	CB0	90	NC	137	CK0	183	SA2
45	CB1	91	SDA	138	CK0	184	V_{DDSPD}
46	V_{DD}	92	SCL	139	V_{SS}	185	V_{SS}
47	DQS8	93	V_{SS}	140	DM8/DQS17	–	–

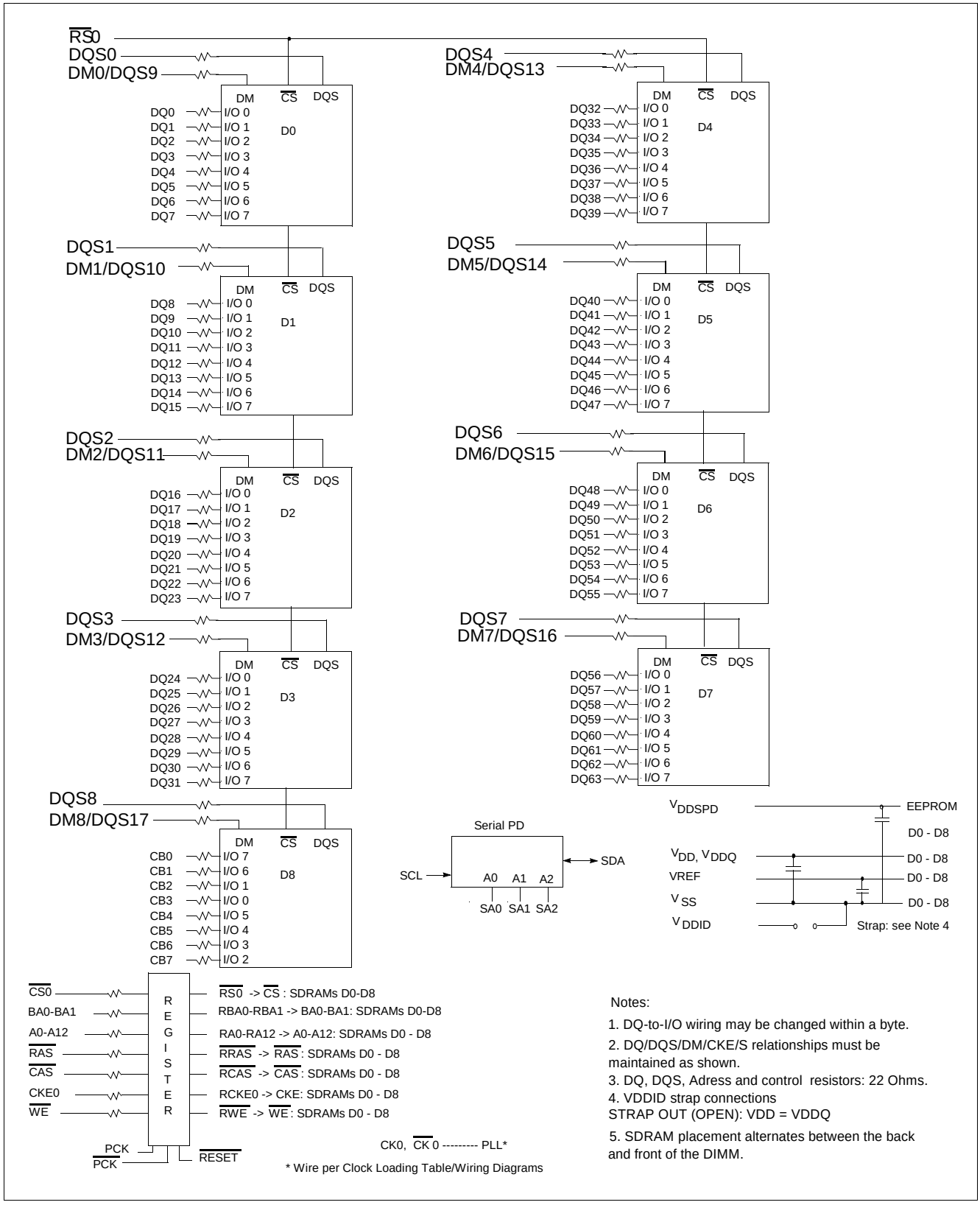
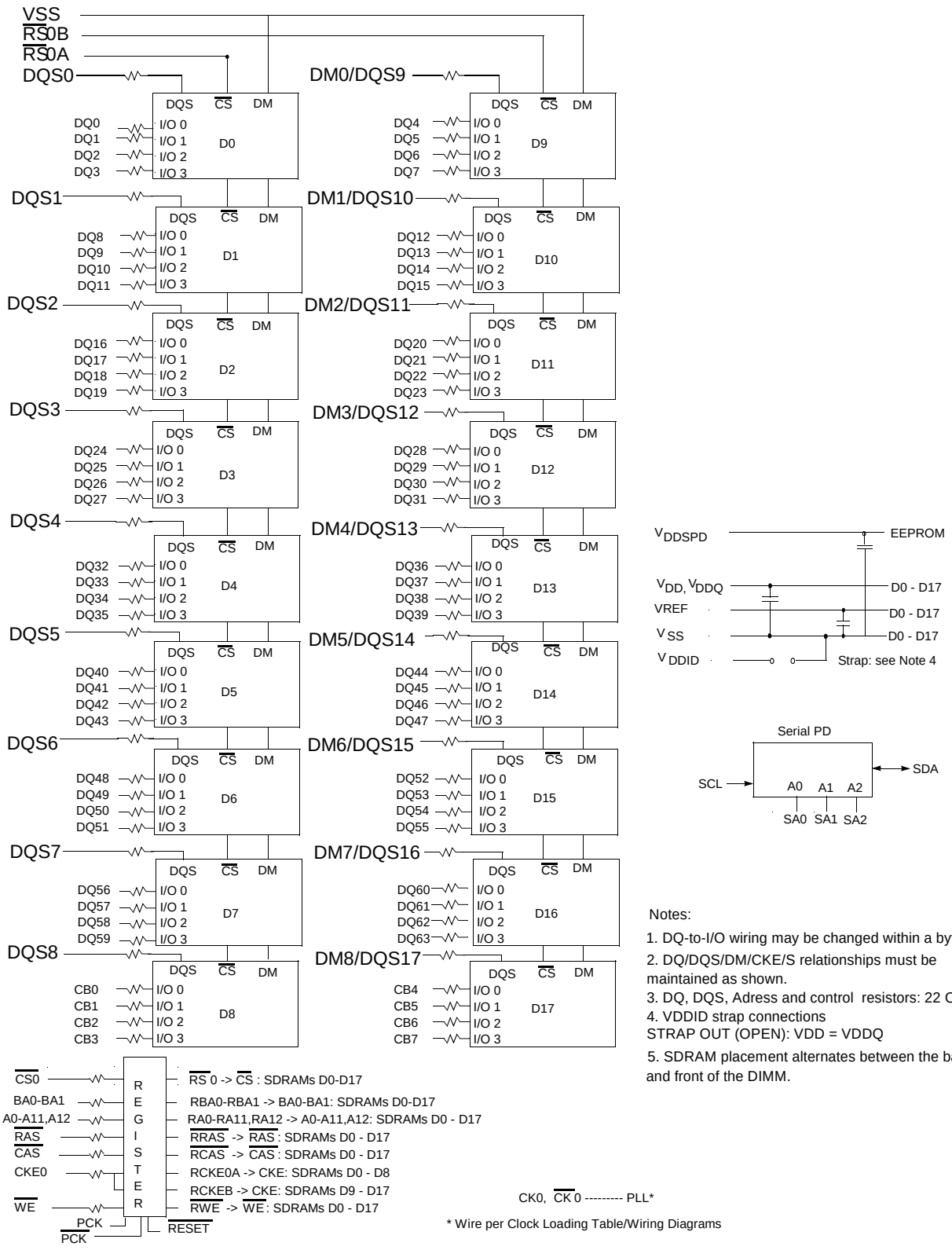


Figure 1 Block Diagram One Rank 16 MB u72 DDR SDRAM DIMM Modules HYS72D16000GR-[7/8]-A using u8 organized SDRAMs on RAW Card Version A



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, Adress and control resistors: 22 Ohms.
4. VDDID strap connections
STRAP OUT (OPEN): VDD = VDDQ
5. SDRAM placement alternates between the back and front of the DIMM.

Figure 2 Block Diagram One Rank 32 MB u72 DDR SDRAM DIMM Modules HYS72D32001GR-[7/8]-A using u4 organized SDRAMs on RAW Card Version B

3 Electrical Characteristics

3.1 Operating Conditions

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	–	V_{DDQ} + 0.5	V	–
Voltage on inputs relative to V_{SS}	V_{IN}	–1	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1	–	+3.6	V	–
Operating temperature (ambient)	T_A	0	–	+70	°C	–
Storage temperature (plastic)	T_{STG}	-55	–	+150	°C	–
Power dissipation (per SDRAM component)	P_D	–	1	–	W	–
Short circuit output current	I_{OUT}	–	50	–	mA	–

Attention: Permanent damage to the device may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only, and functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability and exceeding only one of the values may cause irreversible damage to the integrated circuit.

Table 7 Electrical Characteristics and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note/Test Condition [1]
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
Output Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	[2]
Supply Voltage, I/O Supply Voltage	V_{SS}, V_{SSQ}	0		0	V	—
Input Reference Voltage	V_{REF}	0.49 uV$_{DDQ}$	0.5 uV$_{DDQ}$	0.51 uV$_{DDQ}$	V	[3]
I/O Termination Voltage (System)	V_{TT}	V_{REF} – 0.04		V_{REF} + 0.04	V	[4]
Input High (Logic1) Voltage	$V_{IH(DC)}$	V_{REF} + 0.15		V_{DDQ} + 0.3	V	[7]
Input Low (Logic0) Voltage	$V_{IL(DC)}$	–0.3		V_{REF} – 0.15	V	[7]
Input Voltage Level, CK and $\overline{CK}$ Inputs	$V_{IN(DC)}$	–0.3		V_{DDQ} + 0.3	V	[7]
Input Differential Voltage, CK and $\overline{CK}$ Inputs	$V_{ID(DC)}$	0.36		V_{DDQ} + 0.6	V	[7][5]
VI-Matching Pull-up Current to Pull-down Current	VI_{Ratio}	0.71		1.4	—	[6]
Input Leakage Current	I_I	–2		2	µA	Any input 0 V dV$_{IN}$ dV$_{DD}$; All other pins not under test = 0 V [7][8]
Output Leakage Current	I_{OZ}	–5		5	µA	DQs are disabled; 0 V dV$_{OUT}$ dV$_{DDQ}$ [7]
Output High Current, Normal Strength Driver	I_{OH}	—		–16.2	mA	V_{OUT} = 1.95 V [7]
Output Low Current, Normal Strength Driver	I_{OL}	16.2		—	mA	V_{OUT} = 0.35 V [7]

1) 0 °C dT$_A$ d70 °C

2) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

3) Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.

4) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.

5) V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

6) The ratio of the pull-up current to the pull-down current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltage from 0.25 to 1.0 V. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

7) Inputs are not recognized as valid until V_{REF} stabilizes.

8) Values are shown per component

Table 8 I_{DD} Conditions

Parameter	Symbol
Operating Current 0 one bank; active/ precharge; DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles.	I_{DD0}
Operating Current 1 one bank; active/read/precharge; Burst Length = 4; see component data sheet.	I_{DD1}
Precharge Power-Down Standby Current all banks idle; power-down mode; CKE dV$_{IL,MAX}$	I_{DD2P}
Precharge Floating Standby Current $\overline{CS}$ t V$_{IH,,MIN}$, all banks idle; CKE t V$_{IH,MIN}$; address and other control inputs changing once per clock cycle; V$_{IN}$ = V$_{REF}$ for DQ, DQS and DM.	I_{DD2F}
Precharge Quiet Standby Current $\overline{CS}$ t V$_{IHMIN}$, all banks idle; CKE t V$_{IH,MIN}$; V$_{IN}$ = V$_{REF}$ for DQ, DQS and DM; address and other control inputs stable at t V$_{IH,MIN}$ or dV$_{IL,MAX}$.	I_{DD2Q}
Active Power-Down Standby Current one bank active; power-down mode; CKE dV$_{ILMAX}$; V$_{IN}$ = V$_{REF}$ for DQ, DQS and DM.	I_{DD3P}
Active Standby Current one bank active; $\overline{CS}$ t V$_{IH,MIN}$; CKE t V$_{IH,MIN}$; t$_{RC}$ = t$_{RAS,MAX}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle.	I_{DD3N}
Operating Current Read one bank active; Burst Length = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B; I$_{OUT}$ = 0 mA	I_{DD4R}
Operating Current Write one bank active; Burst Length = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR266(A), CL = 3 for DDR333 and DDR400B	I_{DD4W}
Auto-Refresh Current t$_{RC}$ = t$_{RFCMIN}$, burst refresh	I_{DD5}
Self-Refresh Current CKE d0.2 V; external clock on	I_{DD6}
Operating Current 7 four bank interleaving with Burst Length = 4; see component data sheet.	I_{DD7}

Table 9 I_{DD} Specification and Conditions

Part Number & Organization	HYS72D16000GR-7-A	HYS72D32001GR-7-A	HYS72D16000GR-8-A	HYS72D16000GR-8-A	Unit	Note 1)2)
	128MB	256MB	128MB	256MB		
	x72	x72	x72	x72		
	1 Rank	1 Rank	1 Rank	1 Rank		
	–7	–7	–8	–8		
Symbol	max.	max.	max.	max.		
I_{DD0}	810	1620	765	1530	mA	3)
I_{DD1}	990	1980	900	1800	mA	3)4)
I_{DD2P}	45	90	40.5	81	mA	5)
I_{DD2F}	405	810	315	630	mA	5)
I_{DD2Q}	405	810	315	630	mA	5)
I_{DD3P}	135	270	135	270	mA	5)
I_{DD3N}	405	810	315	630	mA	5)
I_{DD4R}	990	1980	810	1620	mA	3)4)
I_{DD4W}	990	1980	855	1710	mA	3)
I_{DD5}	1710	3420	1620	3240	mA	3)
I_{DD6}	22.5	45	22.5	45	mA	5)
I_{DD7}	2520	5040	2430	4860	mA	3)4)

1) Module I_{DD} values are calculated on the basis of component I_{DD} and can be measured differently according to DQ loading capacity.

2) Test condition for maximum values: V_{DD} = 2.7 V, T_A = 10 °C

3) The module I_{DDx} values are calculated from the I_{DDx} values of the component data sheet as follows:
m uI_{DDx}[component] + n uI_{DD3N}[component] with m and n number of components of rank 1 and 2; n=0 for 1 rank modules

4) DQ I/O (I_{DDQ}) currents are not included in the calculations (see note 1)

5) The module I_{DDx} values are calculated from the corrponent I_{DDx} data sheet values as: (m + n) uI_{DDx}[component]

3.2 Current Specifi cation and Conditions

3.3 AC Characteristics

Table 10 AC Timing - Absolute Specifications –8/–7

Parameter	Symbol	–8		–7		Unit	Note/ Test Condition [1]
		DDR200		DDR266A			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	–0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)
CK high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
CK low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	2)3)4)5)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		ns	2)3)4)5)
Clock cycle time	$t_{CK2.5}$	8	12	7	12	ns	CL = 2.5 2)3)4)5)
	t_{CK2}	10	12	7.5	12	ns	CL = 2.0 2)3)4)5)
	$t_{CK1.5}$	10	12	—	—	ns	CL = 1.5 2)3)4)5)
DQ and DM input hold time	t_{DH}	0.6	—	0.5	—	ns	2)3)4)5)
DQ and DM input setup time	t_{DS}	0.6	—	0.5	—	ns	2)3)4)5)
Control and Addr. input pulse width (each input)	t_{IPW}	2.5	—	2.2	—	ns	2)3)4)5)6)
DQ and DM input pulse width (each input)	t_{DIPW}	2.0	—	1.75	—	ns	2)3)4)5)6)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	–0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)7)
Data-out low-impedance time from CK/$\overline{CK}$	t_{LZ}	–0.8	+0.8	–0.75	+0.75	ns	2)3)4)5)7)
Write command to 1st DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	2)3)4)5)
DQS-DQ skew (DQS and associated DQ signals)	t_{DQSQ}	—	+0.6	—	+0.5	ns	2)3)4)5)
Data hold skew factor	t_{QHS}	—	1.0	—	0.75	ns	2)3)4)5)
DQ/DQS output hold time	t_{QH}	t_{HP} – t_{QHS}	—	t_{HP} – t_{QHS}	—	ns	2)3)4)5)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	2)3)4)5)
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	2)3)4)5)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	2)3)4)5)
Write preamble setup time	t_{WPRES}	0	—	0	—	ns	2)3)4)5)8)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)9)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	2)3)4)5)

Table 10 AC Timing - Absolute Specifications –8/–7

Parameter	Symbol	–8		–7		Unit	Note/ Test Condition [1]
		DDR200		DDR266A			
		Min.	Max.	Min.	Max.		
Address and control input setup time	t_{IS}	1.1	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		1.1	—	1.0	—	ns	slow slew rate 3)4)5)6)10)
Address and control input hold time	t_{IH}	1.1	—	0.9	—	ns	fast slew rate 3)4)5)6)10)
		1.1	—	1.0	—	ns	slow slew rate 3)4)5)6)10)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	CL > 1.5 2)3)4)5)
	$t_{RPRE1.5}$	0.9	1.1	NA		t_{CK}	CL = 1.5 2)3)4)5)11)
Read preamble setup time	t_{RPRES}	1.5	—	NA		ns	2)3)4)5)12)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	2)3)4)5)
Active to Precharge command	t_{RAS}	50	120E+3	45	120E+3	ns	2)3)4)5)
Active to Active/Auto-refresh command period	t_{RC}	70	—	65	—	ns	2)3)4)5)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	80	—	75	—	ns	2)3)4)5)
Active to Read or Write delay	t_{RCD}	20	—	20	—	ns	2)3)4)5)
Precharge command period	t_{RP}	20	—	20	—	ns	2)3)4)5)
Active to Autoprecharge delay	t_{RAP}	20	—	20	—	ns	2)3)4)5)
Active bank A to Active bank B command	t_{RRD}	15	—	15	—	ns	2)3)4)5)
Write recovery time	t_{WR}	15	—	15	—	ns	2)3)4)5)
Auto precharge write recovery + precharge time	t_{DAL}	$(t_{wr}/t_{CK}) + (t_{rp}/t_{CK})$				t_{CK}	2)3)4)5)13)
Internal write to read command delay	t_{WTR}	1	—	1	—	t_{CK}	CL > 1.5 2)3)4)5)
	$t_{WTR1.5}$	2	—	—	—	t_{CK}	CL = 1.5 2)3)4)5)
Exit self-refresh to non-read command	t_{XSNR}	80	—	75	—	ns	2)3)4)5)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	2)3)4)5)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	2)3)4)5)14)

1) 0 °C ≤ T_A ≤ 70 °C; V_{DDQ} = 2.5 V ± 0.2 V, V_{DD} = +2.5 V ± 0.2 V

2) Input slew rate ≥ 1 V/ns for DDR266, and = 1 V/ns for DDR200

3) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$, is V_{REF}. CK/$\overline{CK}$ slew rate are ≥ 1.0 V/ns.

4) Inputs are not recognized as valid until V_{REF} stabilizes.

5) The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (note 3) is V_{TT}.

6) These parameters guarantee device timing, but they are not necessarily tested on each device.

7) t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

8) The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.

9) The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.

10) Fast slew rate t 1.0 V/ns , slow slew rate t 0.5 V/ns and < 1 V/ns for command/address and CK & $\overline{CK}$ slew rate > 1.0 V/ns, measured between $V_{OH(ac)}$ and $V_{OL(ac)}$.

11) CAS Latency 1.5 operation is supported on DDR200 devices only

12) t_{RPRES} is defined for CL = 1.5 operation only

13) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} is equal to the actual system clock cycle time.

14) A maximum of eight Autorefresh commands can be posted to any given DDR SDRAM device.

4 SPD Contents

Table 11 SPD Codes

Byte#	Description		128MB x72 1rank –7	128MB x72 1rank –8	256MB x72 1rank –7	256MB x72 1rank –8
			HEX.	HEX.	HEX.	HEX.
0	Number of SPD Bytes	128	80	80	80	80
1	Total Bytes in Serial PD	256	08	08	08	08
2	Memory Type	DDR-SDRAM	07	07	07	07
3	Number of Row Addresses	12	0C	0C	0C	0C
4	Number of Column Addresses	10/11	0A	0A	0B	0B
5	Number of DIMM Banks	1	01	01	01	01
6	Module Data Width	x72	48	48	48	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	SSTL_2.5	04	04	04	04
9	SDRAM Cycle Time at CL = 2.5	7 ns/8 ns	70	80	70	80
10	Access Time from Clock at CL = 2.5	0.75 ns/0.8 ns	75	80	75	80
11	DIMM config	ECC	02	02	02	02
12	Refresh Rate/Type	Self-Refresh 15.6 ms	80	80	80	80
13	SDRAM Width, Primary	x8/ x4	08	08	04	04
14	Error Checking SDRAM Data Witdh	na	08	08	04	04
15	Minimum Clock Delay for Back-to-Back Random Column Address	t_{CCD} = 1 CLK	01	01	01	01
16	Burst Length Supported	2, 4 & 8	0E	0E	0E	0E
17	Number of SDRAM Banks	4	04	04	04	04
18	Supported CAS Latencies	CAS latency = 2 & 2.5	0C	0C	0C	0C
19	CS Latencies	CS latency = 0	01	01	01	01
20	WE Latencies	Write latency = 1	02	02	02	02
21	SDRAM DIMM Module Attributes	registered	26	26	26	26
22	SDRAM Device Attributes: General	Concurrent Auto Precharge	C0	C0	C0	C0
23	Min. Clock Cycle Time at CAS Latency = 2	7.5 ns/10 ns	75	A0	75	A0
24	Access Time from Clock for CL = 2	0.75 ns/0.8 ns	75	80	75	80
25	Minimum Clock Cycle Time for CL = 1.5	not supported	00	00	00	00
26	Access Time from Clock at CL = 1.5	not supported	00	00	00	00

Table 11 SPD Codes (cont'd)

Byte#	Description		128MB x72 1rank –7	128MB x72 1rank –8	256MB x72 1rank –7	256MB x72 1rank –8
			HEX.	HEX.	HEX.	HEX.
27	Minimum Row Precharge Time	20 ns	50	50	50	50
28	Minimum Row Act. to Row Act. Delay t_{RRD}	15 ns	3C	3C	3C	3C
29	Minimum RAS to CAS Delay t_{RCD}	20 ns	50	50	50	50
30	Minimum RAS Pulse Width t_{RAS}	45 ns/50 ns	2D	32	2D	32
31	Module Bank Density (per Bank)	128 MByte/256 Mbyte	20	20	40	40
32	Addr. and Command Setup Time	0.9 ns/1.1 ns	90	B0	90	B0
33	Addr. and Command Hold Time	0.9 ns/1.1 ns	90	B0	90	B0
34	Data Input Setup Time	0.5 ns/0.6 ns	50	60	50	60
35	Data Input Hold Time	0.5 ns/0.6 ns	50	60	50	60
36 to 40	Superset Information	–	00	00	00	00
41	Minimum Core Cycle Time t_{RC}	65 ns/70 ns	41	46	41	46
42	Min. Auto Refresh Cmd Cycle Time t_{FRC}	75 ns/80 ns	4B	50	4B	50
43	Maximum Clock Cycle Time t_{CK}	12 ns	0C	0C	0C	0C
44	Max. DQS-DQ Skew tDQSQ	0.5 ns/0.6 ns	32	3C	32	3C
45	X-Factor tQHS	0.75 ns/1.0 ns	75	A0	75	A0
46 to 61	Superset Information	–	00	00	00	00
62	SPD Revision	Revision 0.0	00	00	00	00
63	Checksum for Bytes 0 - 62	–	A7	9C	C0	B5
64	Manufactures JEDEC ID Codes	–	C1	C1	C1	C1
65 to 71	Manufactures	–	Infineon	Infineon	Infineon	Infineon
72	Module Assembly Location	–	–	–	–	–
73 to 90	Module Part Number	–	–	–	–	–
91 to 92	Module Revision Code	–	–	–	–	–
93 to 94	Module Manufacturing Date	–	–	–	–	–
95 to 98	Module Serial Number	–	–	–	–	–
99 to 127	–	–	–	–	–	–
128 to 255	open for Customer use	–	–	–	–	–

5 Package Outlines

Module Package
DDR Registered DIMM Modules Raw Card A, 128 MB Module
(one physical bank, 9 components)

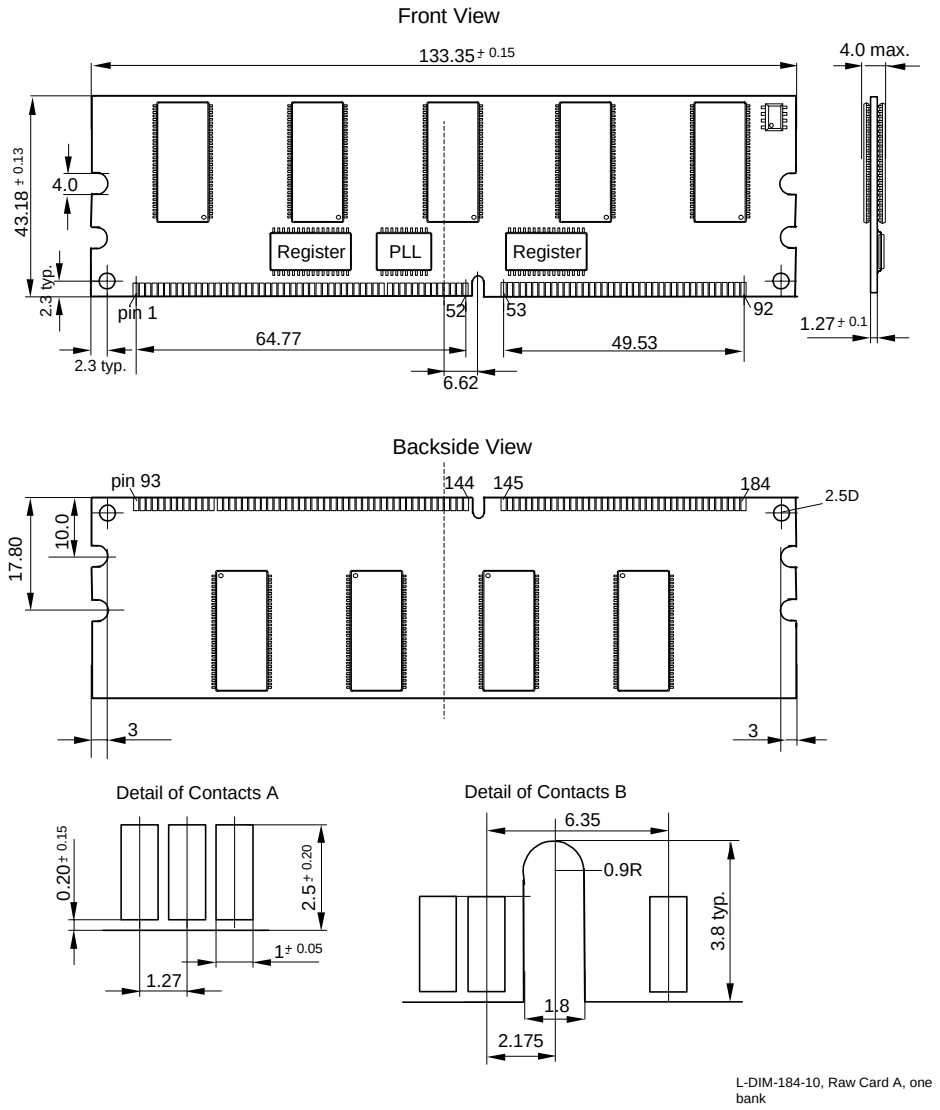


Figure 3 Package Outlines Raw Card A

Module Package
DDR Registered DIMM Modules Raw Card B, 256 MB Module
(one physical bank, 18 components)

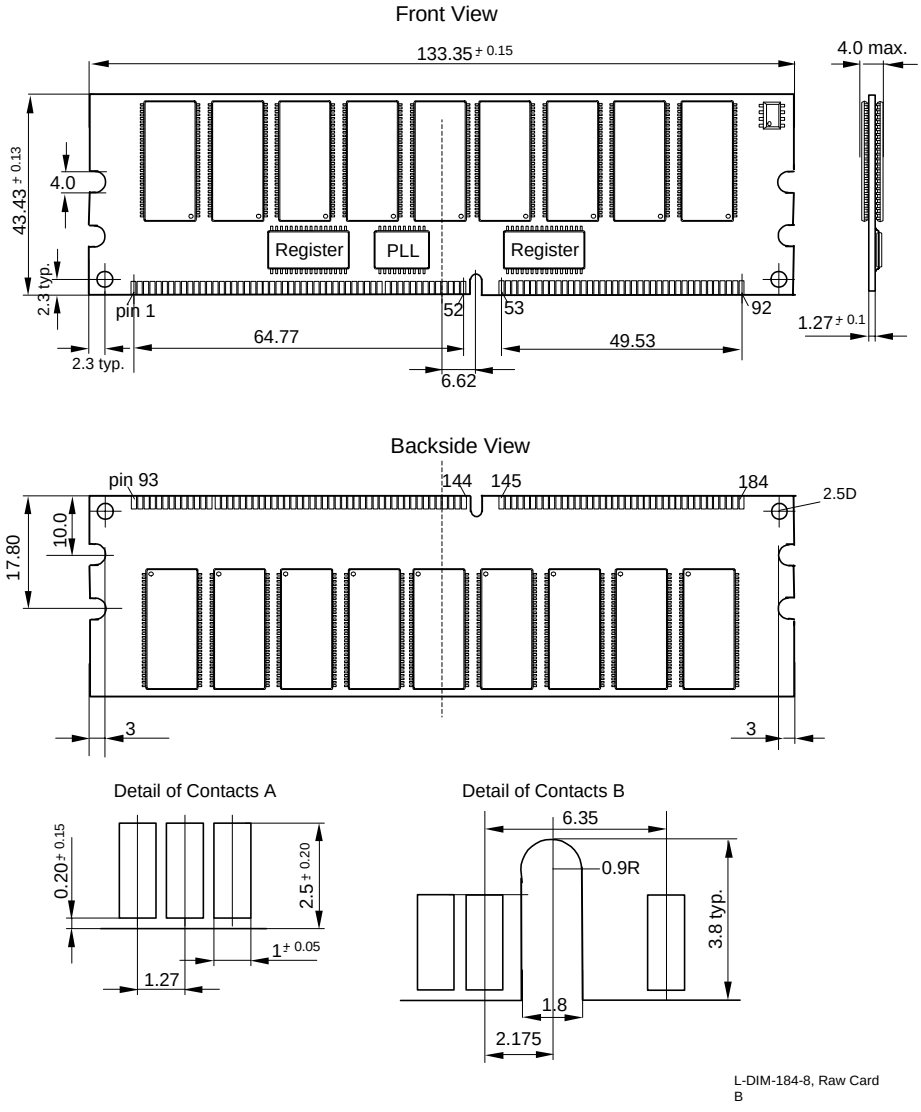


Figure 4 Package Outlines Raw Card B

6 Application Note

Power Up and Power Management on DDR Registered DIMMs (according to JEDEC ballot JC-42.5 Item 1173)

184-pin Double Data Rate (DDR) Registered DIMMs include two new features to facilitate controlled power-up and to minimize power consumption during low power mode. One feature is externally controlled via a system-generated $\overline{\text{RESET}}$ signal; the second is based on module detection of the input clocks. These enhancements permit the modules to power up with SDRAM outputs in a High-Z state (eliminating risk of high current dissipations and/or dotted I/Os), and result in the powering-down of module support devices (registers and Phase-Locked Loop) when the memory is in Self-Refresh mode.

The new $\overline{\text{RESET}}$ pin controls power dissipation on the module's registers and ensures that CKE and other SDRAM inputs are maintained at a valid 'low' level during power-up and self refresh. When $\overline{\text{RESET}}$ is at a low level, all the register outputs are forced to a low level, and all differential register input receivers are powered down, resulting in very low register power consumption. The $\overline{\text{RESET}}$ pin, located on DIMM tab #10, is driven from the system as an asynchronous signal according to the attached details. Using this function also permits the system and DIMM clocks to be stopped during memory Self Refresh operation, while ensuring that the SDRAMs stay in Self Refresh mode.

Table 12 $\overline{\text{RESET}}$ Truth Table

Register Inputs				Register Outputs
$\overline{\text{RESET}}$	CK	$\overline{\text{CK}}$	Data in (D)	Data out (Q)
H	Rising	Falling	H	H
H	Rising	Falling	L	L
H	L or H	L or H	X	Qo
H	High Z	High Z	X	Illegal input conditions
L	X or Hi-Z	X or Hi-Z	X or Hi-Z	L
X: Don't care, Hi-Z: High Impedance, Qo: Data latched at the previous of CK rising and $\overline{\text{CK}}$ falling				

As described in the table above, a low on the $\overline{\text{RESET}}$ input ensures that the Clock Enable (CKE) signal(s) are maintained low at the SDRAM pins (CKE being one of the 'Q' signals at the register output). Holding CKE low maintains a high impedance state on the SDRAM DQ, DQS and DM outputs — where they will remain until activated by a valid 'read' cycle. CKE low also maintains SDRAMs in Self Refresh mode when applicable.

The DDR PLL devices automatically detect clock activity above 20 MHz. When an input clock frequency of 20 MHz or greater is detected, the PLL begins operation and initiates clock frequency lock (the minimum operating frequency at which all specifications will be met is 95 MHz). If the clock input frequency drops below 20 MHz (actual detect frequency will vary by vendor), the PLL VCO (Voltage Controlled Oscillator) is stopped, outputs are made High-Z, and the differential inputs are powered down — resulting in a total PLL current consumption of less than 1 mA. Use of this low power PLL function makes the use of the PLL $\overline{\text{RESET}}$ (or $\overline{\text{G}}$ pin) unnecessary, and it is tied inactive on the DIMM. This application note describes the required and optional system sequences associated with the DDR Registered DIMM '$\overline{\text{RESET}}$' function. It is important to note that all references to CKE refer to both CKE0 and CKE1 for a 2-bank DIMM. Because $\overline{\text{RESET}}$ applies to all DIMM register devices, it is therefore not possible to uniquely control CKE to one physical DIMM bank through the use of the $\overline{\text{RESET}}$ pin.

Power-Up Sequence with $\overline{\text{RESET}}$ — Required

1. The system sets $\overline{\text{RESET}}$ at a valid low level.
   This is the preferred default state during power-up. This input condition forces all register outputs to a low state independent of the condition on the register inputs (data and clock), ensuring that CKE is at a stable low-level at the DDR SDRAMs.

2. The power supplies should be initialized according to the JEDEC-approved initialization sequence for DDR SDRAMs.
3. Stabilization of Clocks to the SDRAM
   The system must drive clocks to the application frequency (PLL operation is not assured until the input clock reaches 20 MHz). Stability of clocks at the SDRAMs will be affected by all applicable system clock devices, and time must be allotted to permit all clock devices to settle. Once a stable clock is received at the DIMM PLL, the required PLL stabilization time (assuming power to the DIMM is stable) is 100 microseconds. When a stable clock is present at the SDRAM input (driven from the PLL), the DDR SDRAM requires 200 µsec prior to SDRAM operation.
4. The system applies valid logic levels to the data inputs of the register (address and controls at the DIMM connector).
   CKE must be maintained low and all other inputs should be driven to a known state. In general these commands can be determined by the system designer. One option is to apply an SDRAM 'NOP' command (with CKE low), as this is the first command defined by the JEDEC initialization sequence (ideally this would be a 'NOP Deselect' command). A second option is to apply low levels on all of the register inputs to be consistent with the state of the register outputs.
5. The system switches $\overline{\text{RESET}}$ to a logic 'high' level.
   The SDRAM is now functional and prepared to receive commands. Since the $\overline{\text{RESET}}$ signal is asynchronous, setting the $\overline{\text{RESET}}$ timing in relation to a specific clock edge is not required (during this period, register inputs must remain stable).
6. The system must maintain stable register inputs until normal register operation is attained.
   The registers have an activation time that allows their clock receivers, data input receivers, and output drivers sufficient time to be turned on and become stable. During this time the system must maintain the valid logic levels described in step 5. It is also a functional requirement that the registers maintain a low state at the CKE outputs to guarantee that the DDR SDRAMs continue to receive a low level on CKE. Register activation time (t (ACT)), from asynchronous switching of $\overline{\text{RESET}}$ from low to high until the registers are stable and ready to accept an input signal, is specified in the register and DIMM do-umentation.
7. The system can begin the JEDEC-defined DDR SDRAM power-up sequence (according to the JEDEC-pproved initialization sequence).

Self Refresh Entry ($\overline{\text{RESET}}$ low, clocks powered off) — Optional

Self Refresh can be used to retain data in DDR SDRAM DIMMs even if the rest of the system is powered down and the clocks are off. This mode allows the DDR SDRAMs on the DIMM to retain data without external clocking. Self Refresh mode is an ideal time to utilize the $\overline{\text{RESET}}$ pin, as this can reduce register power consumption ($\overline{\text{RESET}}$ low deactivates register CK and CK, data input receivers, and data output drivers).

1. The system applies Self Refresh entry command.
   (CKE o Low, $\overline{\text{CS}}$ o Low, $\overline{\text{RAS}}$ o Low, $\overline{\text{CAS}}$ o Low, $\overline{\text{WE}}$ o High)

Note: The commands reach the DDR SDRAM one clock later due to the additional register pipelining on a Registered DIMM. After this command is issued to the SDRAM, all of the address and control and clock input conditions to the SDRAM are Don't Cares— with the exception of CKE.The system sets $\overline{\text{RESET}}$ at a valid low level.
This input condition forces all register outputs to a low state, independent of the condition on the registerm inputs (data and clock), and ensures that CKE, and all other control and address signals, are a stable low-level at the DDR SDRAMs. Since the $\overline{\text{RESET}}$ signal is asynchronous, setting the $\overline{\text{RESET}}$ timing in relation to a specific clock edge is not required.

2. The system turns off clock inputs to the DIMM. (Optional)
   a. In order to reduce DIMM PLL current, the clock inputs to the DIMM are turned off, resulting in High-Z clock inputs to both the SDRAMs and the registers. This must be done after the $\overline{\text{RESET}}$ deactivate time of the register (t (INACT)). The deactivate time defines the time in which the clocks and the control and address signals must maintain valid levels after $\overline{\text{RESET}}$ low has been applied and is specified in the register and DIMM documentation.
   b. The system may release DIMM address and control inputs to High-Z.
   This can be done after the $\overline{\text{RESET}}$ deactivate time of the register. The deactivate time defines the time in which