HYS72T64000HF[A/N]–[3.7/3S]–A
HYS72T128020HF[A/N]–[3.7/3S]–A
HYS72T256020HF[A/N]–[3.7/3S]–A

240-Pin Fully-Buffered DDR2 SDRAM Modules

DDR2 SDRAM
FB-DIMM SDRAM
RoHS Compliant Products
Green Product
High-Speed Differential Point-to-Point Link Interface at 1.5 V

Memory Products

infineon

Never stop thinking.

Edition 2006-01

**Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
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Revision History: 2006-01, **Rev. 1.41**

Previous Version: 1.40

Page	Subjects (major changes since last revision)
75	Add note to **Figure 16 “Package Outline L-DIM-240-21” on Page 74**
76	Add note to **Figure 17 “Package Outline L-DIM-240-22” on Page 75**
77	Add note to **Figure 18 “Package Outline L-DIM-240-25” on Page 76**

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1 Overview

This chapter describes the main characteristics of the 240-Pin Fully-Buffered DDR2 SDRAM Modules product family.

1.1 Features

- 240-pin Fully-Buffered ECC Dual-In-Line DDR2 SDRAM Module for PC, Workstation and Server main memory applications.
- Module organisation one rank 64M x 72, one rank 128M x 72, two ranks 128M x 72, two ranks 256M x 72
- JEDEC Standard Double Data Rate 2 Synchronous DRAMs (DDR2 SDRAMs) with 1.8 V (± 0.1 V) power supply.
- Built with 512Mb DDR2 SDRAMs in 60-ball FBGA Chipsize Packages.
- Re-drive and re-sync of all address, command, clock and data signals using AMB (Advanced Memory Buffer).
- High-Speed Differential Point-to-Point Link Interface at 1.5 V (Jedec standard pending).
- Host Interface and AMB component industry standard compliant.
- Supports SMBus protocol interface for access to the AMB configuration registers.
- Detects errors on the channel and reports them to the host memory controller.
- Automatic DDR2 DRAM Bus Calibration.
- Automatic Channel Calibration.
- Full Host Control of the DDR2 DRAMs.
- Over-Temperature Detection and Alert.
- Hot Add-on and Hot Remove Capability.
- MBIST and IBIST Test Functions.
- Transparent Mode for DRAM Test Support.
- Low profile: 133.35mm x 30,35mm
- 240 Pin gold plated card connector with 1.00mm contact centers (JEDEC standard pending).
- Based on JEDEC standard reference card designs (Jedec standard pending).
- SPD (Serial Presence Detect) with 256 Byte serial E^2PROM.Performance:
- RoHS Compliant Products[1)]

Table 1 Performance for DDR2–533 and DDR2–667

Product Type Speed Code			–3S	–3.7	Unit
Speed Grade			**PC2–5300 5–5–5**	**PC2–4200 4–4–4**	**—**
max. Clock Frequency	@CL5	f_{CK5}	333	266	MHz
	@CL4	f_{CK4}	266	266	MHz
	@CL3	f_{CK3}	200	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	15	ns
min. Row Precharge Time		t_{RP}	15	15	ns
min. Row Active Time		t_{RAS}	45	45	ns
min. Row Cycle Time		t_{RC}	60	60	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

1.2 Description

This document describes the electrical and mechanical features of Infineon's 240-pin, PC2-4200F, PC2-5300F ECC type, Fully Buffered Double-Data-Rate Two Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM FB-DIMMs). Fully Buffered DIMMs use commodity DRAMs isolated from the memory channel behind a buffer on the DIMM. They are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200, PC2-5300 refers to the DIMM naming convention indicating the DDR2 SDRAMs running at 266, 333 MHz clock speed and offering 4200, 5300 MB/s peak bandwidth. FB-DIMM features a novel architecture including the Advanced Memory Buffer. This single chip component, located in the center of each DIMM, acts as a repeater and buffer for all signals and commands which are exchanged between the host controller and the DDR2 SDRAMs including data in- and output. The AMB communicates with the host controller and / or the adjacent DIMMs on a system board using an Industry Standard High-Speed Differential Point-to-Point Link Interface at 1.5 V.

The Advanced Memory Buffer also allows buffering of memory traffic to support large memory capacities. All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The Advanced Memory Buffer interface is responsible for handling channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the memory channel. Fully Buffered DIMM provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. The maximum memory capacity is 288 DDR2 SDRAM devices per channel or 8 DIMMs.

Table 2 Ordering Information (Pb-free components and assembly)

green Product

Type & Partnumber[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC2-4200F (DDR2-533):			
HYS72T64000HFA–3.7–A	PC2–4200F–444–10–A	one rank 512 MB FB-DIMM	512 Mbit (x8)
HYS72T64000HFN–3.7–A	PC2–4200F–444–10–A	one rank 512 MB FB-DIMM	512 Mbit (x8)
HYS72T128020HFA–3.7–A	PC2–4200F–444–10–B	two ranks 1 GB FB-DIMM	512 Mbit (x8)
HYS72T128020HFN–3.7–A	PC2–4200F–444–10–B	two ranks 1 GB FB-DIMM	512 Mbit (x8)
HYS72T256020HFA–3.7–A	PC2–4200F–444–10–H	two ranks 2 GB FB-DIMM	512 Mbit (x4)
HYS72T256020HFN–3.7–A	PC2–4200F–444–10–H	two ranks 2 GB FB-DIMM	512 Mbit (x4)
PC2-5300F (DDR2-667):			
HYS72T64000HFA–3S–A	PC2–4200F–444–10–A	one rank 512 MB FB-DIMM	512 Mbit (x8)
HYS72T64000HFN–3S–A	PC2–4200F–444–10–A	one rank 512 MB FB-DIMM	512 Mbit (x8)
HYS72T128020HFA–3S–A	PC2–4200F–444–10–B	two ranks 1 GB FB-DIMM	512 Mbit (x8)
HYS72T128020HFN–3S–A	PC2–4200F–444–10–B	two ranks 1 GB FB-DIMM	512 Mbit (x8)
HYS72T256020HFA–3S–A	PC2–4200F–444–10–H	two ranks 2 GB FB-DIMM	512 Mbit (x4)
HYS72T256020HFN–3S–A	PC2–4200F–444–10–H	two ranks 2 GB FB-DIMM	512 Mbit (x4)

1) All product types end with a place code, designating the silicon die revision. Example: HYS 72T64000HFA-3.7-A, indicating Rev. A dice are used for DDR2 SDRAM components. To learn more on INFINEON DDR2 module and component nomenclature see section 8 of this datasheet.

2) The Compliance Code is printed on the module label and describes the speed grade, e.g. "PC2-4200F-444-10-A", where 4200F means Fully Buffered DIMM with 4.26 GB/sec Module Bandwidth and "444-10" means CAS latency = 4, t_{rcd} latency = 4 and t_{rp} latency = 4 using JEDEC SPD Revision 1.0 and assembled on Raw Card "A".

Table 3 Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/columns bits	Raw Card
512 MB	64M ×72	1	ECC	9	13/2/10	A
1 GB	128M ×72	2	ECC	18	13/2/10	B
2 GB	256M ×72	2	ECC	36	13/2/11	H

Table 4 Components on Modules[1)]

Product Type	DRAM components[2)]	DRAM Density	DRAM Organisation
HYS72T64000HF	HYB18T512800AF	512 Mbit	64M ×8
HYS72T128020HF	HYB18T512800AF	512 Mbit	64M ×8
HYS72T256020HF	HYB18T512400AF	512 Mbit	128M ×4

1) For a detailed description of all functionalities of the DRAM components on these modules see the component datasheet.
2) Green Product

2 Pin Configuration

The pin configuration of the DDR2 SDRAM DIMM is listed by function in **Table 5** (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 7** and **Table 6** respectively. The pin numbering is depicted in **Figure 1**.

Table 5 Pin Configuration of FB-DIMM

Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
228	SCK	I	HSDL_15	**System Clock Input, positive line**
229	$\overline{\text{SCK}}$	I	HSDL_15	**System Clock Input, negative line**
Control Signals				
17	RESET	I	LV-CMOS	**AMB reset signal**
Northbound				
22	PN0	O	HSDL_15	**Primary Northbound Data, positive lines**
25	PN1	O	HSDL_15	
28	PN2	O	HSDL_15	
31	PN3	O	HSDL_15	
34	PN4	O	HSDL_15	
37	PN5	O	HSDL_15	
51	PN6	O	HSDL_15	
54	PN7	O	HSDL_15	
57	PN8	O	HSDL_15	
60	PN9	O	HSDL_15	
63	PN10	O	HSDL_15	
66	PN11	O	HSDL_15	
48	PN12	O	HSDL_15	
40	PN13	O	HSDL_15	
23	$\overline{\text{PN0}}$	O	HSDL_15	**Primary Northbound Data, negative lines**
26	$\overline{\text{PN1}}$	O	HSDL_15	
29	$\overline{\text{PN2}}$	O	HSDL_15	
32	$\overline{\text{PN3}}$	O	HSDL_15	
35	$\overline{\text{PN4}}$	O	HSDL_15	
38	$\overline{\text{PN5}}$	O	HSDL_15	
52	$\overline{\text{PN6}}$	O	HSDL_15	
55	$\overline{\text{PN7}}$	O	HSDL_15	
58	$\overline{\text{PN8}}$	O	HSDL_15	
61	$\overline{\text{PN9}}$	O	HSDL_15	
64	$\overline{\text{PN10}}$	O	HSDL_15	
67	$\overline{\text{PN11}}$	O	HSDL_15	
49	$\overline{\text{PN12}}$	O	HSDL_15	
41	$\overline{\text{PN13}}$	O	HSDL_15	

Table 5 Pin Configuration of FB-DIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
142	SN0	I	HSDL_15	**Secondary Northbound Data, positive lines**
145	SN1	I	HSDL_15	
148	SN2	I	HSDL_15	
151	SN3	I	HSDL_15	
154	SN4	I	HSDL_15	
157	SN5	I	HSDL_15	
171	SN6	I	HSDL_15	
174	SN7	I	HSDL_15	**Secondary Northbound Data, positive lines**
177	SN8	I	HSDL_15	
180	SN9	I	HSDL_15	
183	SN10	I	HSDL_15	
186	SN11	I	HSDL_15	
168	SN12	I	HSDL_15	
160	SN13	I	HSDL_15	
143	$\overline{\text{SN0}}$	I	HSDL_15	**Secondary Northbound Data, negative lines**
146	$\overline{\text{SN1}}$	I	HSDL_15	
149	$\overline{\text{SN2}}$	I	HSDL_15	
152	$\overline{\text{SN3}}$	I	HSDL_15	
155	$\overline{\text{SN4}}$	I	HSDL_15	
158	$\overline{\text{SN5}}$	I	HSDL_15	
172	$\overline{\text{SN6}}$	I	HSDL_15	
175	$\overline{\text{SN7}}$	I	HSDL_15	
178	$\overline{\text{SN8}}$	I	HSDL_15	
181	$\overline{\text{SN9}}$	I	HSDL_15	
184	$\overline{\text{SN10}}$	I	HSDL_15	
187	$\overline{\text{SN11}}$	I	HSDL_15	
169	$\overline{\text{SN12}}$	I	HSDL_15	
161	$\overline{\text{SN13}}$	I	HSDL_15	
Southbound				
70	PS0	I	HSDL_15	**Primary Southbound Data, positive lines**
73	PS1	I	HSDL_15	
76	PS2	I	HSDL_15	
79	PS3	I	HSDL_15	
82	PS4	I	HSDL_15	
93	PS5	I	HSDL_15	
96	PS6	I	HSDL_15	
99	PS7	I	HSDL_15	
102	PS8	I	HSDL_15	
90	PS9	I	HSDL_15	

Table 5 Pin Configuration of FB-DIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
71	$\overline{PS0}$	I	HSDL_15	**Primary Southbound Data, negative lines**
74	$\overline{PS1}$	I	HSDL_15	
77	$\overline{PS2}$	I	HSDL_15	
80	$\overline{PS3}$	I	HSDL_15	
83	$\overline{PS4}$	I	HSDL_15	
94	$\overline{PS5}$	I	HSDL_15	
97	$\overline{PS6}$	I	HSDL_15	
100	$\overline{PS7}$	I	HSDL_15	
103	$\overline{PS8}$	I	HSDL_15	
91	$\overline{PS9}$	I	HSDL_15	
190	SS0	O	HSDL_15	**Secondary Southbound data, positive lines**
193	SS1	O	HSDL_15	
196	SS2	O	HSDL_15	
199	SS3	O	HSDL_15	
202	SS4	O	HSDL_15	
213	SS5	O	HSDL_15	**Secondary Southbound data, positive lines**
216	SS6	O	HSDL_15	
219	SS7	O	HSDL_15	
222	SS8	O	HSDL_15	
210	SS9	O	HSDL_15	
191	$\overline{SS0}$	O	HSDL_15	**Secondary Southbound data, negative lines**
194	$\overline{SS1}$	O	HSDL_15	
197	$\overline{SS2}$	O	HSDL_15	
200	$\overline{SS3}$	O	HSDL_15	
203	$\overline{SS4}$	O	HSDL_15	
214	$\overline{SS5}$	O	HSDL_15	
217	$\overline{SS6}$	O	HSDL_15	
220	$\overline{SS7}$	O	HSDL_15	
223	$\overline{SS8}$	O	HSDL_15	
211	$\overline{SS9}$	O	HSDL_15	
EEPROM				
120	SCL	I	CMOS	**Serial Bus Clock**
119	SDA	I/O	OD	**Serial Bus Data**
239	SA0	I	CMOS	**Serial Address Select Bus 2:0**
240	SA1	I	CMOS	
118	SA2	I	CMOS	
Power Supplies				
238	V_{DDSPD}	PWR	–	**EEPROM Power Supply**
9,10,12,13,129,130,132,133	V_{CC}	PWR	–	**AMB Core Power / Channel Interface Power**

Table 5 Pin Configuration of FB-DIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
15,117,135,237	V_{TT}	PWR	–	**Address/Command/Clock Termination Power**
1,2,3,5,6,7,108,109,111,112,113, 115,116,121,122,123,125,126, 127,231,232,233,235,236	V_{DD}	PWR	–	**Power Supply**
4,8,11,14,18,21,24,27,30,33,36, 39,42,43,46,47,50,53,56,59,62, 65,68,69,72,75,78,81,84,85,88, 89,92,95,98,101,104,107,110, 114,124,128,131,134,138,141, 144,147,150,153,156,159,162, 163,166,167,170,173,176,179, 182,185,188,189,192,195,198, 201,204,205,208,209,212,215, 218,221,224,227,230,234	V_{SS}	GND	–	**Ground Plane**
Other Pins				
19,20,44,45,86,87,105,106,139, 140,164,165,206,207,225,226	NC	NC	–	**Not connected** Pins not connected on Infineon FB-DIMM's
136	VID0	–	–	**Voltage ID** *Note: These Pins must be unconnected for DDR2-based Fully Buffered DIMMs VID[0] is V_{DD} value: OPEN = 1.8 V, GND = 1.5 V; VID[1] is V_{CC} value: OPEN = 1.5 V, GND = 1.2 V*
16	VID1	–	–	
137	Test	AI	–	**VREF** *Note: Pin must be unconnected for normal operation*

Table 6 Abbreviations for Buffer Type

Abbreviation	Description
HSDL_15	High-Speed Differential Point-to-Point Link Interface at 1.5 V
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

Table 7 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable
NC	Not Connected

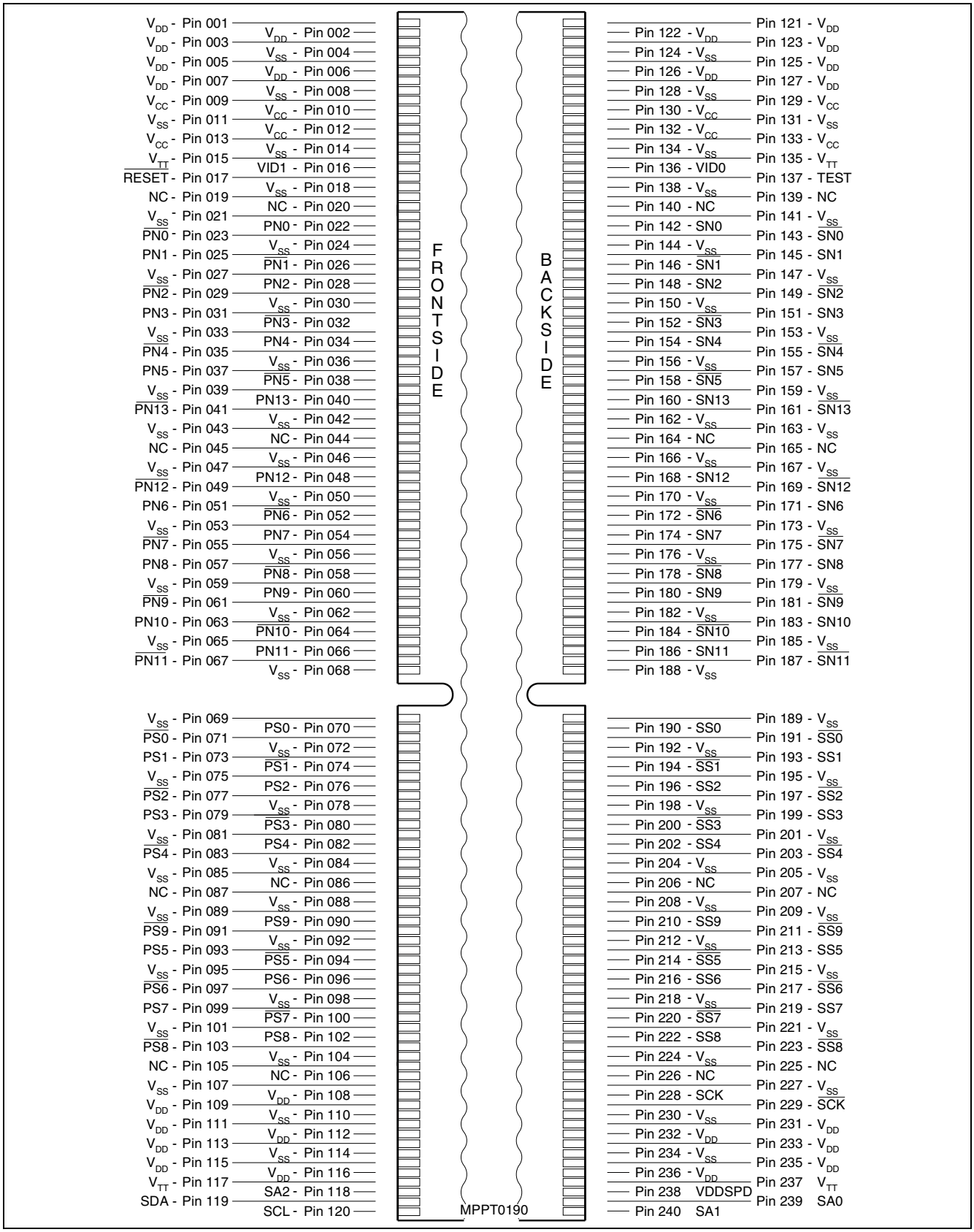

Figure 1 Pin Configuration for FB-DIMM (240 pin)

3 FB-DIMM Input/Output Functional Description

Table 8 FB-DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
Channel Signals			
SCK, $\overline{\text{SCK}}$	Input	Differential	System Clock Input
PN[13:0], $\overline{\text{PN[13:0]}}$	Output	Differential	Primary Northbound Data
PS[9:0], $\overline{\text{PS[9:0]}}$	Input	Differential	Primary Southbound Data
SN[13:0], $\overline{\text{SN[13:0]}}$	Input	Differential	Secondary Northbound Data
SS[9:0], $\overline{\text{SS[9:0]}}$	Output	Differential	Secondary Southbound Data
SMB Bus Signals			
SA[2:0]	Input	—	SPD Address, also used to select the DIMM number in the AMB
SDA	I/O	—	SPD Data. A resistor must be connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up.
SCL	Input	—	SPD Clock
Miscellaneous Signals			
$\overline{\text{RESET}}$	Input	Active Low	AMB Reset Signal
VID[1:0]	Input	—	Voltage ID. Both pins shall be NC in case of V_{DD} = 1.8 V, V_{CC} = 1.5 V
TEST	Analog	+ 0.9 V	DRAM V_{REF} Margin Test. Do not connect on the system planar.
Power / Ground			
V_{DD}	Supply	+ 1.8 V	DDR2 DRAM Power
V_{CC}	Supply	+ 1.5 V	AMB Core Power
V_{DDSPD}	Supply	+ 3.3 V	SPD Power

4 Block Diagrams

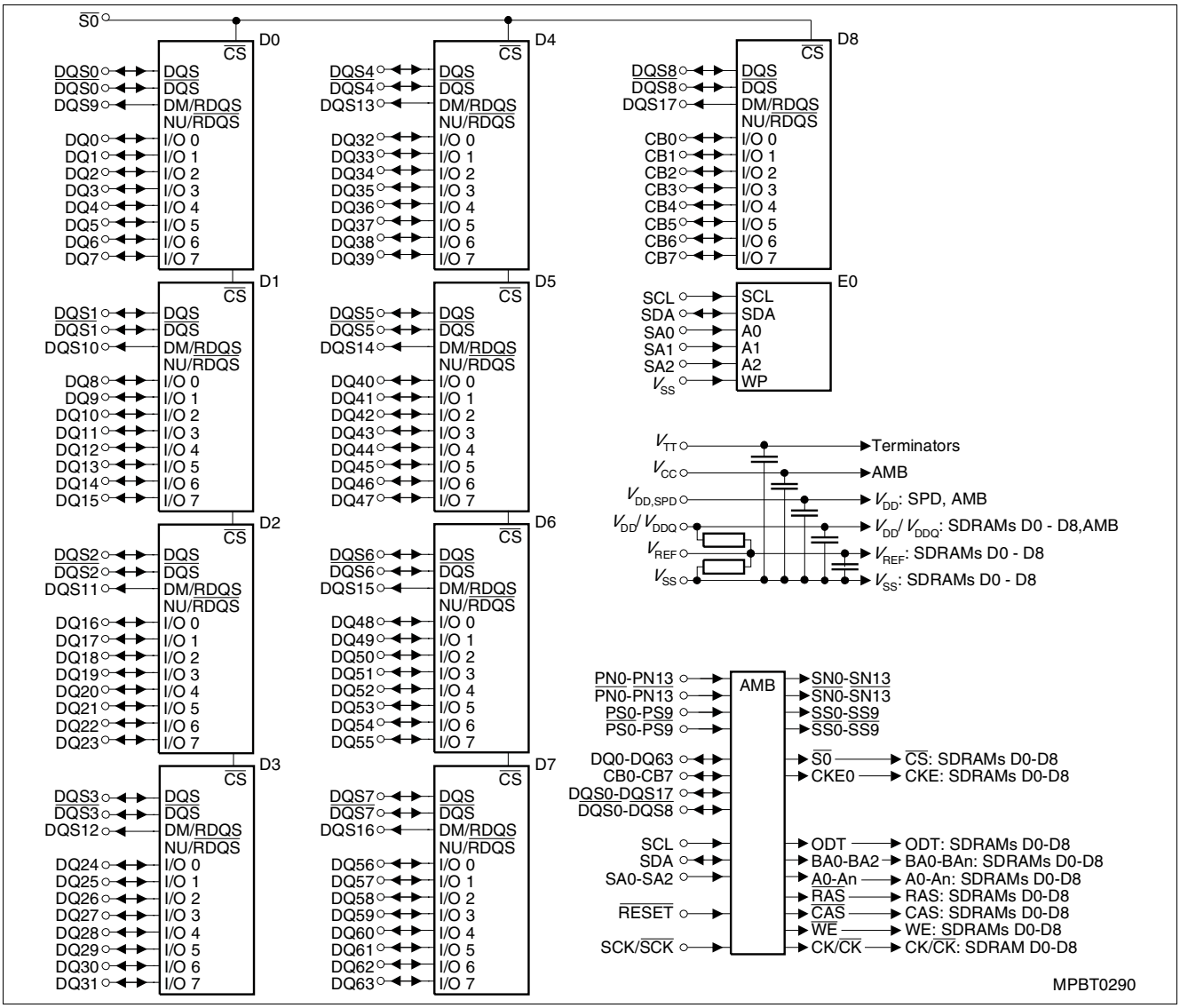

Figure 2 Block Diagram Raw Card A FB-DIMM ECC (x72, 1Rank, x8)

Notes

1. *DQ to I/O wiring may be changed within a byte*
2. *There are two physical copies of each address, command, control, clock*
3. *All address, command, control, clock have termination resitors to V_{TT}*

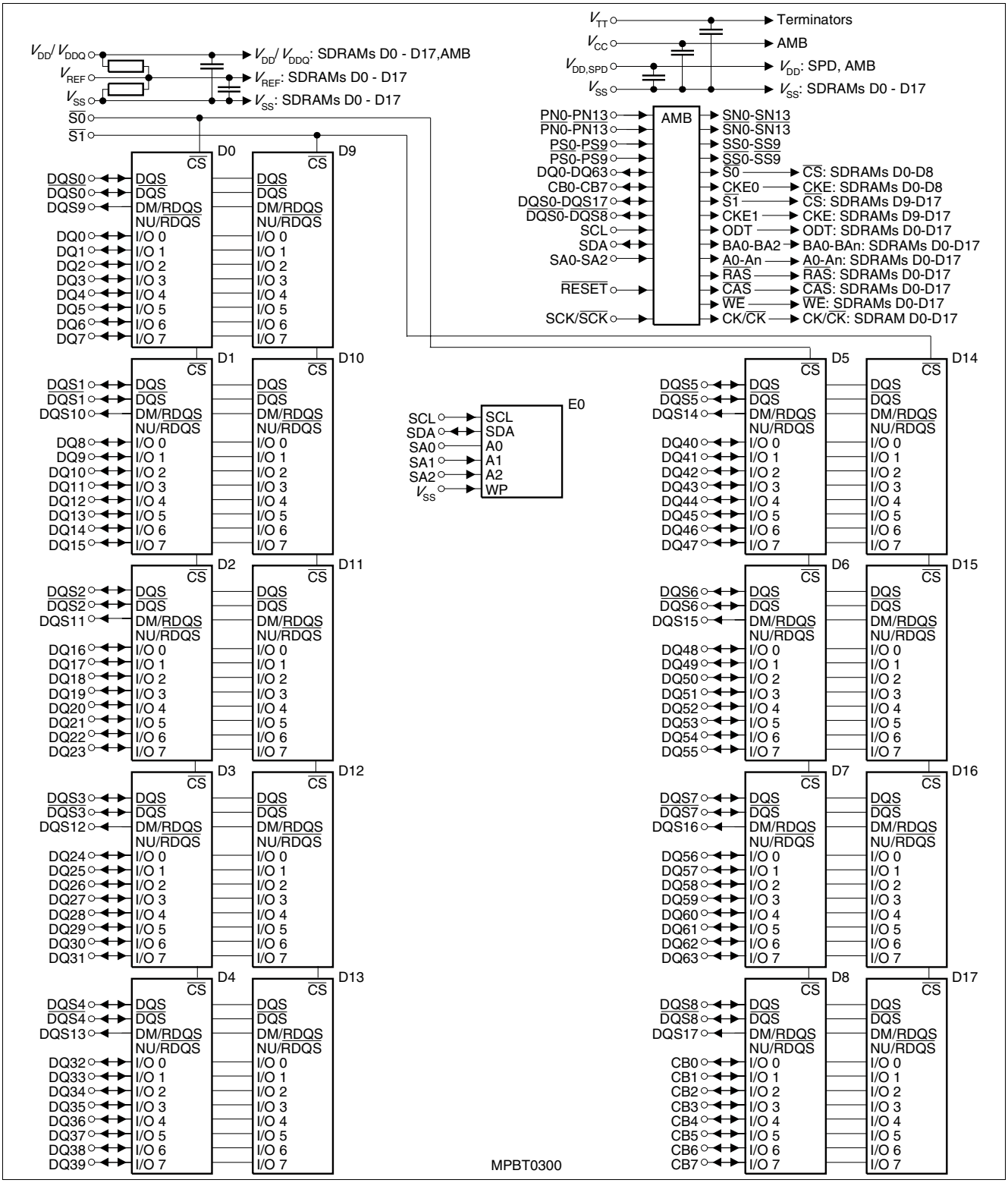

Figure 3 Block Diagram Raw Card B FB-DIMM ECC (x72, 2Ranks, x8)

Notes

1. *DQ to I/O wiring may be changed within a byte*
2. *There are two physical copies of each address, command, control and clock*
3. *All address, command, control, clock have termination resitors to V_{TT}*

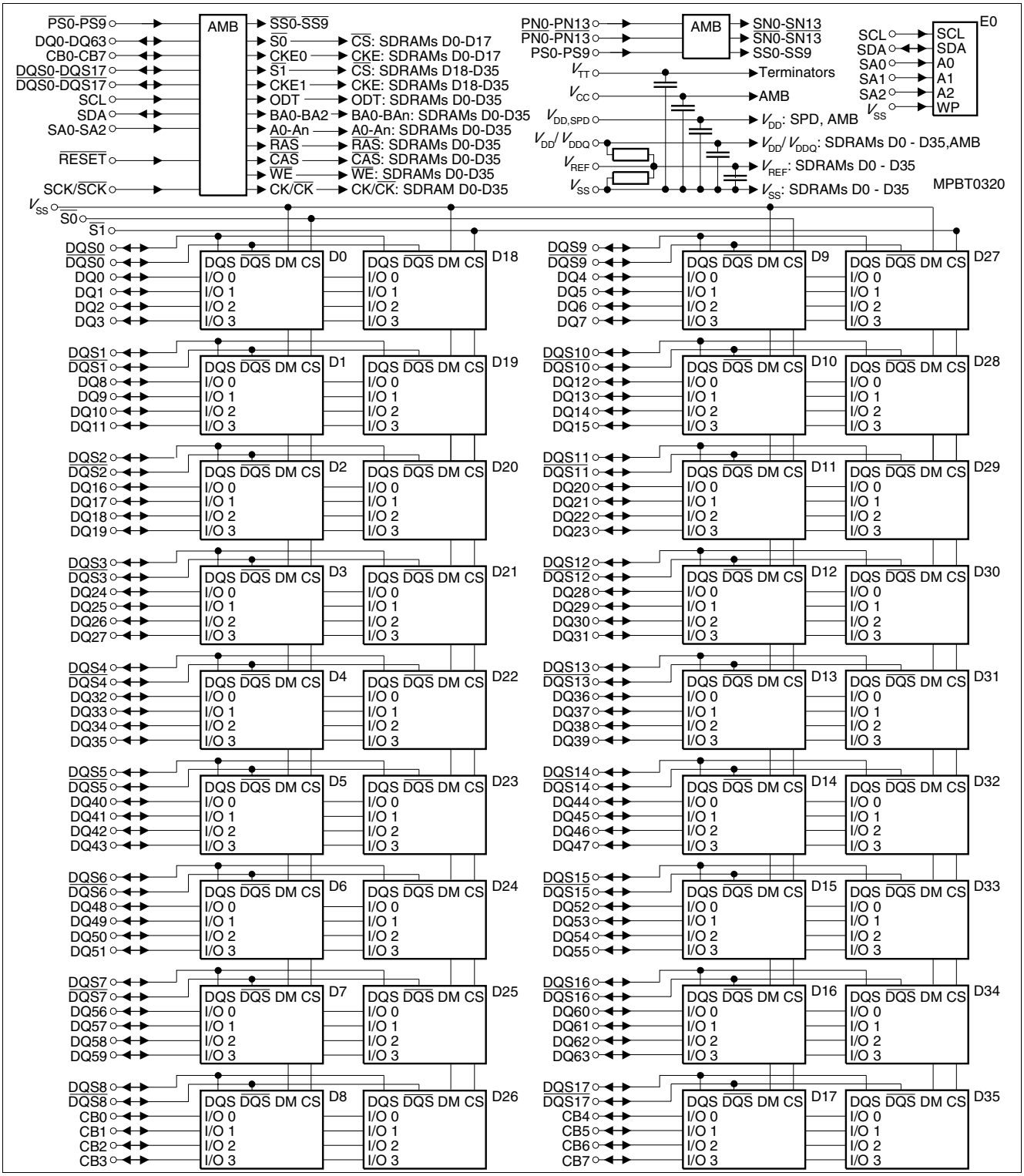

Figure 4 Block Diagram Raw Card H FB-DIMM ECC (×72, 2Ranks, ×4)

Notes

1. *DQ to I/O wiring may be changed within a nibble*
2. *Two physical copies of each address, command, control and four physical copies of each clock*
3. *All address, command, control, clock have termination resitors to V_{TT}*

5 Basic Functionality

5.1 Advanced Memory Buffer Overview

The Advanced Memory Buffer (AMB) reference design complies with the FB-DIMM Architecture and Protocol Specification.The AMB block diagram is depicted in **Figure 5**.

5.2 Advanced Memory Buffer Functionality

The Advanced Memory Buffer will perform the following FB-DIMM channel functions:

- Supports channel initialization procedures as defined in the initialization chapter of the FB-DIMM Architecture and Protocol Specification to align the clocks and the frame boundaries, verify channel connectivity, and identify AMB DIMM position.
- Supports the forwarding of southbound and northbound frames, servicing requests directed to a specific AMB or DIMM, as defined in the protocol chapter, and merging the return data into the northbound frames.
- If the AMB resides on the last DIMM in the channel, the AMB initializes northbound frames.
- Detects errors on the channel and reports them to the host memory controller.
- Support the FB-DIMM configuration register set as defined in the register chapters.
- Acts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM.
- Provides a read buffer FIFO and a write buffer FIFO.
- Supports an SMBus protocol interface for access to the AMB configuration registers.
- Provides logic to support MEMBIST and IBIST Design for Test functions.
- Provides a register interface for the thermal sensor and status indicator.
- Functions as a repeater to extend the maximum length of FB-DIMM Links.

Transparent Mode for DRAM Test Support

In this mode, the Advanced Memory Buffer will provide lower speed tester access to DRAM pins through the FB-DIMM I/O pins. This allows the tester to send an arbitrary test pattern to the DRAMs. Transparent mode only supports a maximum DRAM frequency equivalent to DDR2 400. Transparent mode functionality:

- Reconfigures FB-DIMM inputs from differential high speed link receivers to two single ended lower speed receivers (~200 MHz)
- These inputs directly control DDR2 Command/Address and input data that is replicated to all DRAMs
- Uses low speed direct drive FB-DIMM outputs to bypass high speed Parallel/Serial circuitry and provide test results back to tester

DDR2 SDRAM Interface

- Supports DDR2 at speeds of 533, 667MT/s
- Supports 256Mb, 512Mb and 1Gb devices in x4 and x8 configurations
- 72-bit DDR2 SDRAM memory array

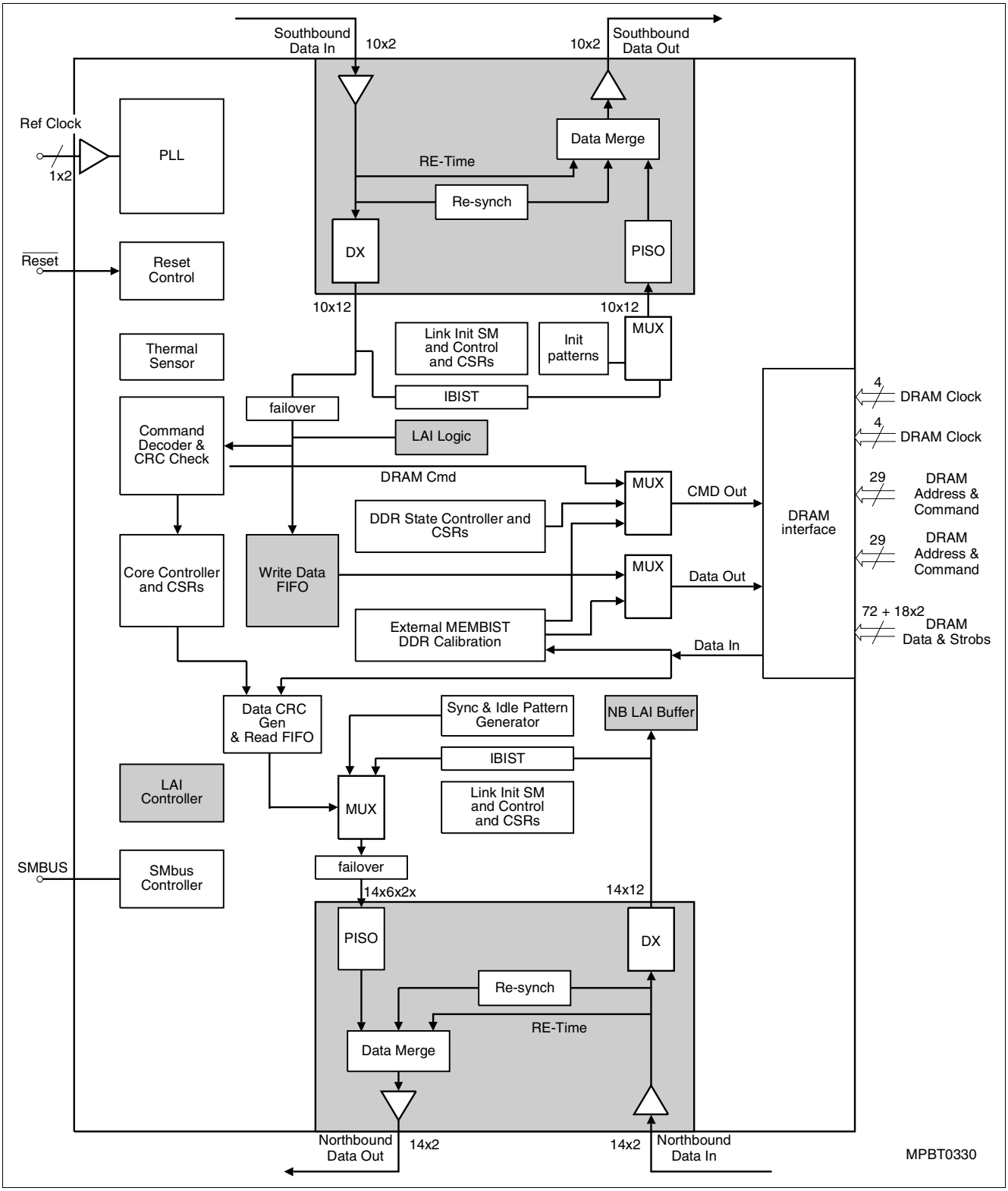

Figure 5 Block Diagram Advanced Memory Buffer FB–DIMM ECC

Note: Figure is a conceptual Block Diagram of the Advanced Memory Bufferis data flow and clock domains.

5.3 Interfaces

Figure 6 illustrates the Advanced Memory Buffer and all of its interfaces. They consist of two FB-DIMM links, one DDR2 channel and an SMBus interface. Each FB-DIMM link connects the Advanced Memory Buffer to a host memory controller or an adjacent FB-DIMM. The DDR2 channel supports direct connection to the DDR2 SDRAMs on a Fully Buffered DIMM.

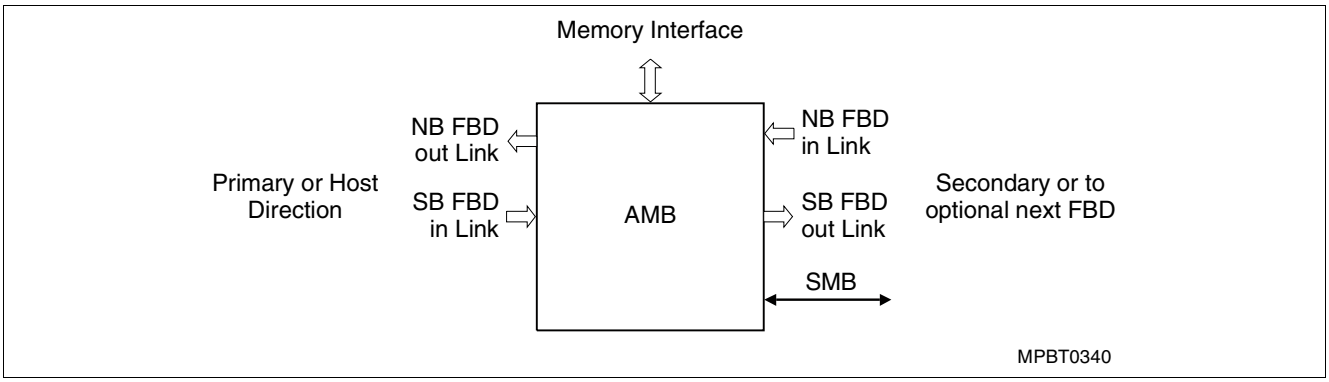

Figure 6 Block Diagram Advanced Memory Buffer Interface

Interface Topology

The FB-DIMM channel uses a daisy-chain topology to provide expansion from a single DIMM per channel to up to 8 DIMMs per channel. The host sends data on the southbound link to the first DIMM where it is received and redriven to the second DIMM. On the southbound data path each DIMM receives the data and again re-drives the data to the next DIMM until the last DIMM receives the data. The last DIMM in the chain initiates the transmission of data in the direction of the host (a.k.a. northbound). On the northbound data path each DIMM receives the data and re-drives the data to the next DIMM until the host is reached.

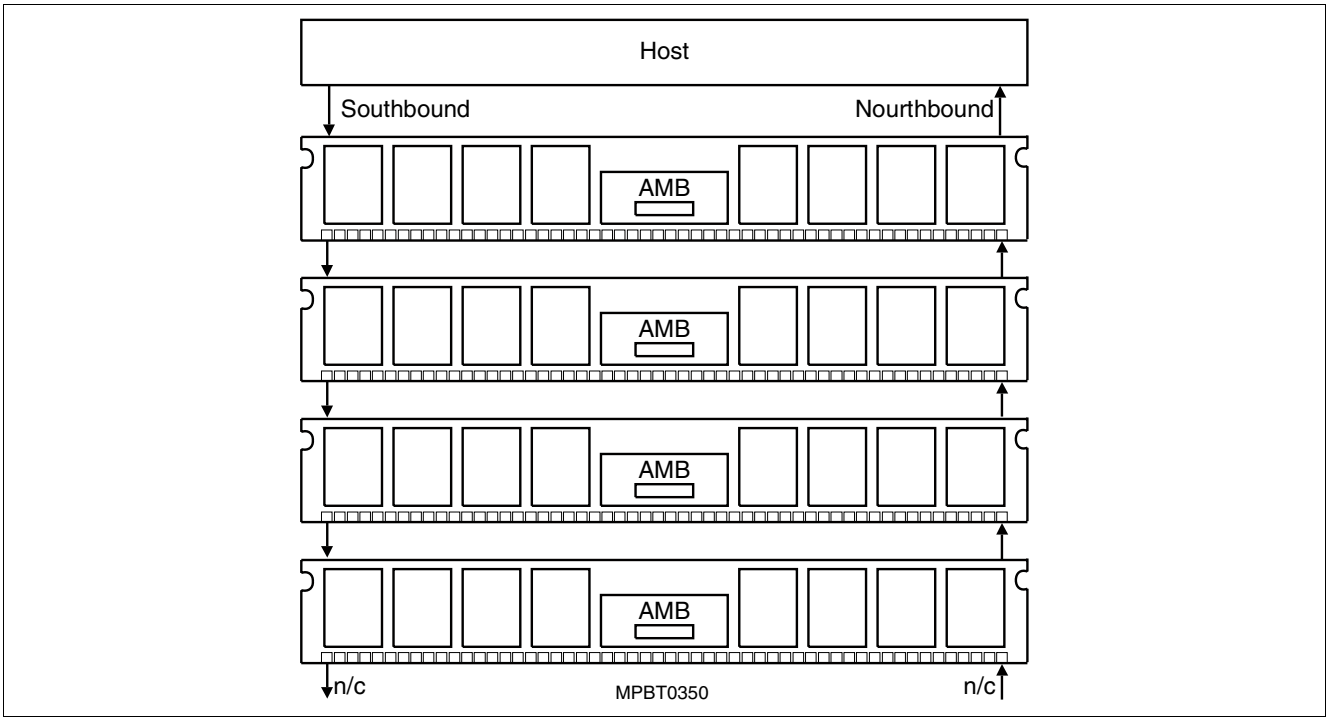

Figure 7 Block Diagram FB–DIMM Channel Soutbound and Northbound Paths

5.4 High-Speed Differential Point-to-Point Link (at 1.5 V) Interfaces

The Advanced Memory Buffer supports one FB-DIMM Channel consisting of two bidirectional link interfaces using highspeed differential point-to-point electrical signaling. The southbound input link is 10 lanes wide and carries commands and write data from the host memory controller or the adjacent DIMM in the host direction. The southbound output link forwards this same data to the next FB-DIMM. The northbound input link is 14 lanes wide and carries read return data or status information from the next FB-DIMM in the chain back towards the host. The northbound output link forwards this information back towards the host and multiplexes in any read return data or status information that is generated internally. Data and commands sent to the DRAMs travel southbound on 10 primary differential signal line pairs. Data received from the DRAMs and status information travel northbound on 14 primary differential pairs. Data and commands sent to the adjacent DIMM upstream are repeated and travel further southbound on 10 secondary differential pairs. Data and status information received from the adjacent DIMM upstream travel further northbound on 14 secondary differential pairs.

5.4.1 DDR2 Channel

The DDR2 channel on the Advanced Memory Buffer supports direct connection to DDR2 SDRAMs. The DDR2 channel supports two ranks of eight banks with 16 row/column request, 64 data, and eight check-bit signals. There are two copies of address and command signals to support DIMM routing and electrical requirements. Four transfer bursts are driven on the data and check-bit lines at 800 MHz. Propagation delays between read data/check-bit strobe lanes on a given channel can differ. Each strobe can be calibrated by hardware state machines using write/read trial and error. Hardware aligns the read data and check-bits to a single core clock. The Advanced Memory Buffer provides four copies of the command clock phase references (CLK[3:0]) and write data/check-bit strobes (DQSs) for each DRAM nibble.

5.4.2 SMBus Slave Interface

The Advanced Memory Buffer supports an SMBus interface to allow system access to configuration registers independent of the FB-DIMM link. The Advanced Memory Buffer will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100 kHz. SMBus access to the Advanced Memory Buffer may be a requirement to boot and to set link strength, frequency and other parameters needed to insure robust configurations. It is also required for diagnostic support when the link is down. The SMBus address straps located on the DIMM connector are used by the unique ID.

5.4.3 Channel Latency

FB-DIMM channel latency is measured from the time a read request is driven on the FB-DIMM channel pins to the time when the first 16 bytes (2nd chunk) of read completion data is sampled by the memory controller. When not using the Variable Read Latency capability, the latency for a specific DIMM on a channel is always equal to the latency for any other DIMM on that channel. However, the latency for each DIMM in a specific configuration with some number of DIMMs installed may not be equal to the latency for each FB-DIMM in a configuration with some different number of DIMMs installed. As more DIMMs are added to the channel, additional latency is required to read from each DIMM on the channel. Because the channel is based on the point-to-point interconnection of buffer components between DIMMs, memory requests are required to travel through N-1 buffers before reaching the Nth buffer. The result is that a 4 DIMM channel configuration will have greater idle read latency compared to a 1 DIMM channel configuration. The Variable Read Latency capability can be used to reduce latency for DIMMs closer to the host. The idle latencies listed in this section are representative of what might be achieved in typical AMB designs. Actual implementations with latencies less than the values listed will have higher application performance and vice versa.

5.4.4 Peak Theoretical Channel Throughput

An FB-DIMM channel transfers read completion data on the Northbound data connection. 144 bits of data are transferred for every Northbound data frame. This matches the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 from a single channel or a DRAM burst of four from two lockstepped channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC). The FB-DIMM frame rate matches the DRAM command clock because of the fixed 6:1 ratio of the FB-DIMM channel clock to the DRAM command clock. Therefore, the Northbound data connection will exhibit the same peak theoretical throughput as a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Northbound data connection is 4.267 GB/sec. Write data is transferred on the Southbound command and data connection, via Command+Wdata frames. 72 bits of data are transferred for every Command+Wdata frame. Two Command+Wdata frames match the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 transfers from a single channel, or a burst of 4 from two lock-step channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC). When the frame rate matches the DRAM command clock, the Southbound command and data connection will exhibit one half the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Southbound command and data connection is 2.133 GB/sec. The total peak theoretical throughput for a single FB-DIMM channel is defined as the sum of the peak theoretical throughput of the Northbound data connection and the Southbound command and data connection. When the frame rate matches the DRAM command clock, this is equal to 1.5 times the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical throughput of a single DDR2-533 channel would be 4.267 GB/sec, while the peak theoretical throughput of the entire FB-DIMM PC4200F channel would be 6.4GB/sec.

5.5 Hot-add

The FB-DIMM channel does not provide a mechanism to automatically detect and report the addition of a new DIMM south of the currently active last DIMM. It is assumed the system will be notified through some means of the addition of one or more new DIMMs so that specific commands can be sent to the host controller to initialize the newly added DIMM(s) and perform a Hot-Add Reset to bring them into the channel timing domain. It should be noted that the power to the DIMM socket must be removed before a “hot-add” DIMM is inserted or removed. Applying or removing the power to a DIMM socket is a system platform function.

5.6 Hot-remove

In order to accomplish removal of DIMMs the host must perform a Fast Reset sequence targeted at the last DIMM that will be retained on the channel. The Fast Reset re-establish the appropriate last DIMM so that the Southbound Tx outputs of the last active DIMM and the Southbound and Northbound outputs of the DIMMs beyond the last active DIMM are disabled. Once the appropriate outputs are disabled the system can coordinate the procedure to remove power in preparation for physical removal of the DIMM if needed. It should be noted that the power to the DIMM socket must be removed before a “hot-add” DIMM is inserted or removed. Applying or removing the power to a DIMM socket is a system platform function.

5.7 Hot-replace

Hot replace of DIMM is accomplished through combining the Hot-Remove and Hot-Add process.

6 Electrical Characteristics

6.1 Operating Conditions

Table 9 Absolute Maximum Ratings

Symbol	Parameter	Values		Unit	Note
		Min.	Max.		
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.3	1.75	V	1)
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}	–0,3	1.75	V	1)
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–0.5	2.3	V	1)
V_{TT}	Voltage on V_{TT} pin relative to V_{SS}	–0.5	2.3	V	1)
T_{STG}	Storage Temperature	–55	+100	°C	1)

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 10 Operating Temperature Range

Symbol	Parameter	Values		Unit	Note
		Min.	Max.		
T_{CASE}	DRAM Component Case Temperature Range	0	+95	°C	1)2)3)4)
T_{CASE}	AMB Component Case Temperature Range	0	+110	°C	1)

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) Within the DRAM Component Case Temperature range all DRAM specification will be supported.

3) Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85C case temperature before initiating self-refresh operation.

4) Above 85C DRAM case temperature the Auto-Refresh command interval has to be reduced to tREFI = 3.9 µs.

Table 11 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Nom.	Max.		
AMB Supply Voltage	V_{CC}	1.455	1.5	1.575	V	–
DRAM Supply Voltage	V_{DD}	1.7	1.8	1.9	V	–
Termination Voltage	V_{TT}	0.48 ×V_{DD}	0.50 ×V_{DD}	0.52 ×V_{DD}	V	–
EEPROM Supply Voltage	V_{DDSPD}	3.0	3.3	3.6	V	–
DC Input Logic High(SPD)	$V_{IH(DC)}$	2.1	—	V_{DDSPD}	V	1)
DC Input Logic Low(SPD)	$V_{IL(DC)}$	—	—	0.8	V	1)
DC Input Logic High(RESET)	$V_{IH(DC)}$	1.0	—	—	V	2)
DC Input Logic Low(RESET)	$V_{IL(DC)}$	—	—	+0.5	V	1)

Table 11 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Nom.	Max.		
Leakage Current (RESET)	I_L	–90	—	+90	µA	2)
Leakage Current (Link)	I_L	–5	—	+5	µA	3)

1) applies for SMB and SPD Bus Signals
2) applies for AMB CMOS Signal RESET
3) for all other AMB related DC parameters, please refer to the High Speed Differential Link Interface Specifications

Table 12 Timing Parameters

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
EI Assertion Pass-Thru Timing	$t_{EI\ Propagate}t$	—	—	4	clks	—
EI Deassertion Pass-Thru Timing	t_{EID}	—	—	Bitlock	clks	2
EI Assertion Duration	t_{EI}	100	—	—	clks	1)2)
FBD Cmd to DDR Clk out that latches Cmd	—	—	8.1	—	ns	3)
FBD Cmd to DDR Write	—	—	TBD	—	ns	
DDR Read to FBD (last DIMM)	—	—	5.0	—	ns	4)
Resample Pass-Thru time	—	—	1.075	—	ns	
ResynchPass-Thru time	—	—	2.075	—	ns	
Bit Lock Interval	$t_{BitLock}$	—	—	119	frames	1)
Frame Lock Interval	$t_{FrameLock}$	—	—	154	frames	1)

1) Defined in FB-DIMM Architecture and Protocol Spec
2) Clocks defined as core clocks = 2x SCK input
3) @ DDR2-667 - measured from beginning of frame at southbound input to DDR clock output that latches the first command of a frame to the DRAMs
4) @ DDR2-667 - measured from latest DQS input to AMB to start of matching data frame at northbound FB-DIMM outputs

Table 13 Environmental Parameters

Parameter	Symbol	Rating	Units	Notes
Operating Temperature	T_{OPR}	See Note		1)
Operating Humidity (relative)	H_{OPR}	10 to 90	%	2)
Storage Temperature	T_{STG}	-50 to +100	°C	2)
Storage Humidity (without condensation)	H_{STG}	5 to 95	%	2)
Barometric pressure (operating)	P_{BAR}	3050	m	2)
Barometric pressure (storage)	P_{BAR}	14240	m	2)

1) The designer must meet the case temperature specifications for individual module components.
2) Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and the device funcional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

7 High-Speed Differential Point-to-Point Link Interface

The following specifications define the High-Speed Differential Point-to-Point Signaling Link for FB-DIMMD, operating at the AMB supply voltage of 1.5 V that is provided at the DIMM connector. The link consists of a transmitter and a receiver and the interconnect in between them. The transmitter sends serialized bits into a lane and the receiver accepts the electrical signals of the serialized bits and transforms them into a serialized bit-stream. This FB-DIMM link is being specified to operate from 3.2 to 4.8 Gb/s. The specifications are defined for three distinct bit-rates of operation: 3.2 Gb/s (PC2-4200F), 4.0 Gb/s (PC2-5300F) and 4.8 Gb/s (PC2-6400F). The link utilizes a derived clock approach and transmitter de-emphasis to compensate for channel loss characteristics.

7.1 Differential Signaling

A Differential Signal is defined by taking the voltage difference between two conductors. In this specification, a differential signal or differential pair is comprised of a voltage on a positive conductor, VD+, and a negative conductor, VD-. The differential voltage (VDIFF) is defined as the difference of the positive conductor voltage and the negative conductor voltage (VDIFF = VD+ - VD-). The Common Mode Voltage (VCM) is defined as the average or mean voltage present on the same differential pair (VCM = [VD++ VD-]/2). This documentís electrical specifications often refer to peak-to-peak measurements or peak measurements, which are defined by the following 5 equations:

1. $V_{DIFFp-p}$ = (2*max|VD+ - VD-|) (This applies to a symmetric differential swing)
2. $V_{DIFFp-p}$ = (max|VD+ - VD-| {VD+ > VD-} + max|VD+ - VD-| {VD+ < VD-}) (This applies to an asymmetric differential swing.)
3. V_{DIFFp} = (max|VD+ - VD-|) (This applies to a symmetric differential swing)
4. V_{DIFFp} = (max|VD+ - VD-| {VD+ > VD-}) or (max|VD+ - VD-| {VD+ < VD-}) which ever is greater (This applies to an asymmetric differential swing.)
5. V_{CMp} = (max|VD+ + VD-|/2)

Note: The maximum value is calculated on a per unit interval evaluation. The maximum function as described is implicit for all peak-to-peak and peak equations throughout the rest of this chapter, and thus a max function will not appear in any following representations of these equations. In this section, DC is defined as all frequency components below Fdc = 30 kHz. AC is defined as all frequency components at or above Fdc = 30 kHz. These definitions pertain to all voltage and current specifications. An example waveform is shown in Figure 1-2. In this waveform the differential peak-peak signal is approximately 0.6 V, the differential peak signal is approximately 0.3 V and the common mode is approximately 0.25 V.

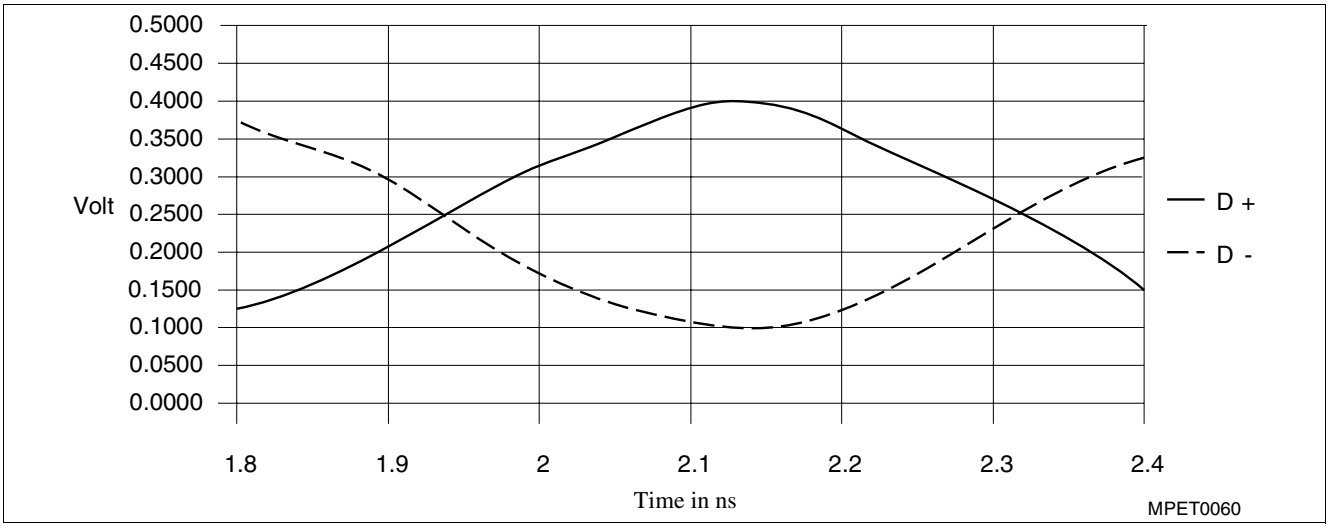

Figure 8 Sample Differental Signal FB-DIMMUnit Interval (UI)

Average time interval between voltage transitions of a signal. This is the same as the period of the FB-DIMM link bit-rate clock. Given a <...1010...> between voltage transitions, over a time interval long enough to make all intentional frequency modulation of the source clock negligible. The UI will be different depending on the data rate of operation. UI=312.5ps (PC2-4200F), UI=250ps (PC2-5300F), UI=208ps (PC2-6400F).

7.1.1 Transition Density in Transmitted Signals

The FB-DIMM link doesn't prescribe encoding. However the link bit stream needs to maintain a minimum transition density. The transition density is defined as the number of transitions that occurs either from 0 to 1 or from 1 to 0 within any bit stream of a prescribed length. The minimum prescribed Transition-Density_min is: 6 transitions per 512 bits: FB-DIMM at 3.2 Gb/s, 4.0 Gb/s and 4.8 Gb/s. The prescribed minimum is required to enable phase tracking of the received data by the receiver while at the same time minimize the overhead requirements.

7.1.2 Jitter and Bit Error Rate

Jitter is defined as the deviation in the edges of a sequence of data bits from their ideal timing positions. This deviation can be in phase, period or duty cycle. Jitter is further categorized into random jitter and deterministic jitter. The total jitter is the convolution of the probability density for all the independent jitter sources. The random jitter magnitude can be approximated as Gaussian and can be used to estimate the bit error rate (BER) of the link. In this document the allocation to random jitter and deterministic jitter has not been separately specified. The total jitter must support a maximum BER of 10 -16. The methods for measuring BER compliance are still being evaluated.

7.1.3 De-Emphasis

De-emphasis is the engineering term used to describe the technique of utilizing a voltage swing reduction of non-transition bits. Figure 1-3 shows an example of a de-emphasized differential signal. De-emphasis is different from pre-emphasis in that non-transition bits are reduced in voltage as opposed to an increase in voltage swing for transition bits with pre-emphasis. De-emphasis is included to minimize Inter-symbol interference (ISI) due to the difference in loss across the frequency band where the main energy of the transmitted bit patterns is located. De-emphasis must be implemented when multiple bits of the same polarity are output in succession. Subsequent bits are driven at a differential voltage level below the first bit and individual bits are always driven at the full voltage level, for normal operation.

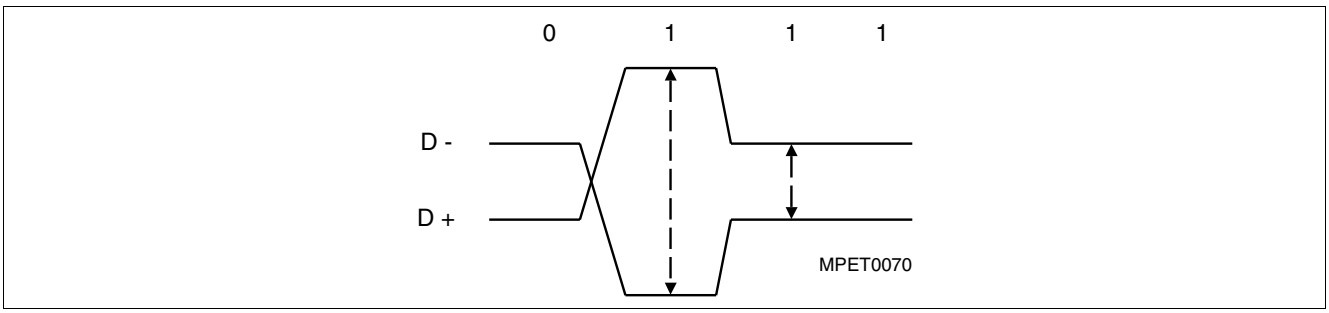

Figure 9 De-Emphasis

7.1.4 Electrical Idle (EI)

The condition when both conductors of a differential pair are at 0 volt (grounded) level. Electrical idle is primarily used in power saving and inactive states (i.e. DISABLE).

7.1.5 Reference Clock

The reference clock network consists of the clock generator and the clock buffer that drives the PLL of any front-end transmitter or receiver. The same reference clock shall be transmitted to the front-end of the chips at both ends of the link. The reference clock signal meets the High-Speed Current Steering Logic (HCSL) specification.

7.2 High Speed Serial Link Reference Clocks (SCK, SCK)

To reduce jitter and allow for future silicon fabrication process changes, HCSL (High-Speed Current Steering Logic) clocks are used. The nominal single-ended swing for each clock is 0 to 0.7 V.

The reference clock frequency is 1/24 of the link data rate, e.g. 166.67 MHz for a data rate of 4.0Gb/s. The reference clock pair is routed point-to-point to each DIMM on the system board. The FB-DIMM channel utilizes mesochronous clocking, i.e. the phase relationship between TX reference clock and RX reference clock is unspecified. However, in order to limit the jitter difference between TX and RX there is an upper limit for the phase difference between data and reference clock at the RX, called the transport delay, T1).

7.3 Spread Spectrum Clocking (SSC)

Spread Spectrum Clock (SSC) with up to -0.5% down spread in frequency shall be supported. The frequency of the clock and therefore bit rate can be modulated from 0% to -0.5% of the nominal data rate/frequency, at a modulation rate in the range between 30 kHz and 33 kHz. The modulation profile of SSC shall be able to provide optimal or close to optimal EMI reduction. Typical profiles include Triangular or Hershey profile.

7.4 Reference Clock Input Specifications

Table 14 Reference Clock Input Specifications

Parameter	Symbol	Values		Unit	Notes
		Min.	Max.		
Reference clock frequency	f_{SCK}	133.33	200.00	MHz	1)2)
Rise time, Fall time	$T_{sck\text{-}rise}$ $T_{sck\text{-}fall}$	175	700	psec	3)
Voltage high	$V_{SCK\text{-}high}$	660	850	mV	
Voltage low	$V_{SCK\text{-}low}$	-150		mV	
Absolute crossing point	$V_{Cross\text{-}abs}$	250	550	mV	4)
Relative crossing point	$V_{Cross\text{-}rel}$	Calculated	Calculated		5)4)
% mismatch between rise and fall times	$T_{SCK\text{-}Rise\text{-}Fall\text{-}Match}$	-	10	%	
Duty cycle of referance clock	$T_{SCK\text{-}Dutycycle}$	40	60	%	
Clock leakage current	I_{I_CK}	-10	10	uA	6)7)
Clock input capacitance	C_{I_CK}	0.5	2	pF	7)
Clock input capacitance delta	$C_{I\_CK(D)}$	-0.25	0.25	pF	8)
Transport delay	T1		5	ns	9)10)
Phase Jitter Sample Size	NSAMPLE	10^{16}		Periods	11)
Reference clock jitter, filtered	$T_{REF\text{-}JITTER}$		40	ps	12)13)
Reference clock deterministic jitter	$T_{REF\text{-}DJ}$		TBD	ps	

1) 133MHz for PC2-4200, 166MHz for PC2-5300 and 200MHz for PC2-6400.
2) Measured with SSC disabled.
3) Measured differentially through the range of 0.175V to 0.525V.
4) The crossing point must meet the absolute and relative crossing point specification simultaneously.
5) $V_{Cross\_rel\_(min)}$ and $V_{Cross\_rel\_(max)}$ are derived using the following calculation: Min = 0.5 (V_{havg} - 0.710) + 0.250; and Max = 0.5 (V_{havg} - 0.710) + 0.550, where V_{havg} is the average of $V_{SCK\text{-}highm}$
6) Measured with a single-ended input voltage of 1V.
7) Applies to Reference Clocks SCK and $\overline{SCK}$.
8) Differance between SCK and $\overline{SCK}$ input
9) T1 = |Tdatapath - Tclockpath| (excluding PLL loop delays). This parameter is not a direct clock output parameter but it indirectly determines the clock output parameter TREF-JITTER.
10) The net transport delay is the difference in time of flight between associated data and clock paths. The data path is defined from the reference clock source, through the TX, to data arrival at the data sampling point in the RX. The clock path is defined from the reference clock source to clock arrival at the same sampling point. See Figure 3-3. The path delays are caused by copper trace routes, on-chip routing, on-chip buffering, etc. They include the time-of-flight of interpolators or other clock adjustment mechanisms. They do *not* include the phase delays caused by finite PLL loop bandwidth because these delays are modeled by the PLL transfer functions.
11) Direct measurement of phase jitter records over 1016 periods is impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and the total jitter at 1016 samples extrapolated from an estimate of the sigma of the random jitter components.
12) Measured with SSC enabled on reference clock generator.
13) As measured after the phase jitter filter. This number is separate from the receiver jitter budget that is defined by the TRX-Total-MIN parameters.

7.5 Differential Transmitter Output Specifications

This specification defines a differential current mode driver with a three different TX voltage swing modes (large, regular and small). The AMBs supports all three voltage swing modes. The specification defines several de-emphasis settings for each voltage swing. Each setting is defined as a separate differential eye diagram that must be met for the transmitter. Figure 3-4 defines the eye heights for the large, regular and small voltage swing. The no de-emphasis voltages are for a transition bit while the other voltages are for a de-emphasized bit. All eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. All eyes must meet the minimum timing requirement of $T_{TX\text{-}Total\text{-}Min}$(specified later). The eye diagrams must be valid for at least $N_{MIN\text{-}UI\text{-}TX}$ consecutive UIs (specified in Table 3-3). An appropriate average transmitter UI must be used as the interval for measuring the eye diagram. The eye diagram is created using all edges of the $N_{MIN\text{-}UI\text{-}TX}$ consecutive UIs. The eye diagrams shall be measured by observing a continuous TBD pattern at the pin of the device for the non de-emphasized eye and by observing a continuous TBD pattern at the pin of the device for the deemphasized eye. The transmitter output eye is referenced to V_{SS} and all transmitter terminations must be referenced to V_{SS} .

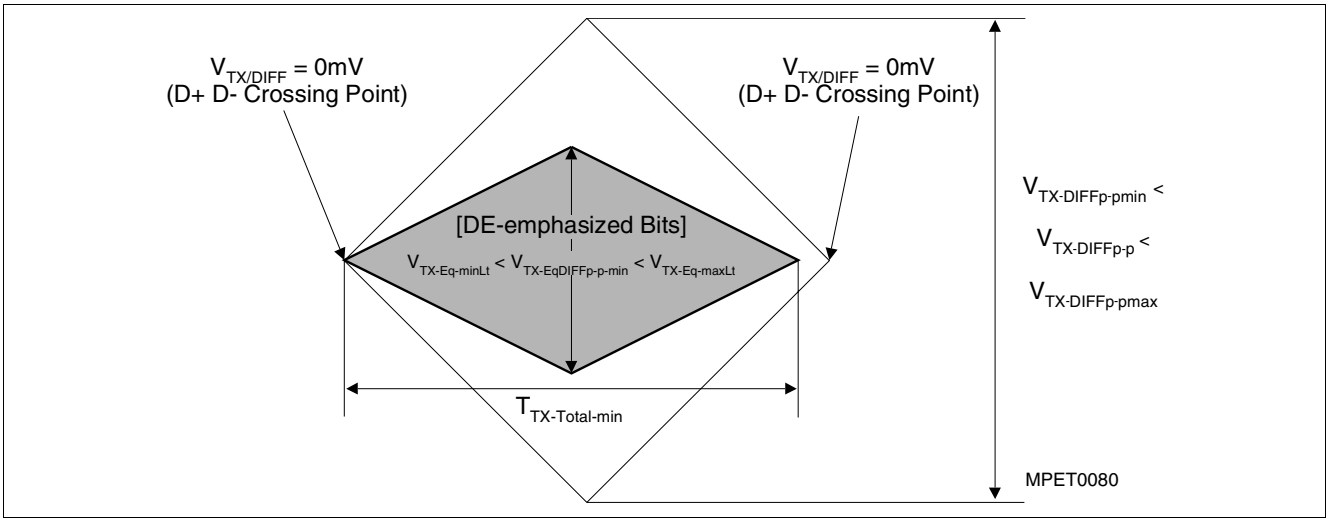

Figure 10 Differential requirement minimum transmitter output eye specifications

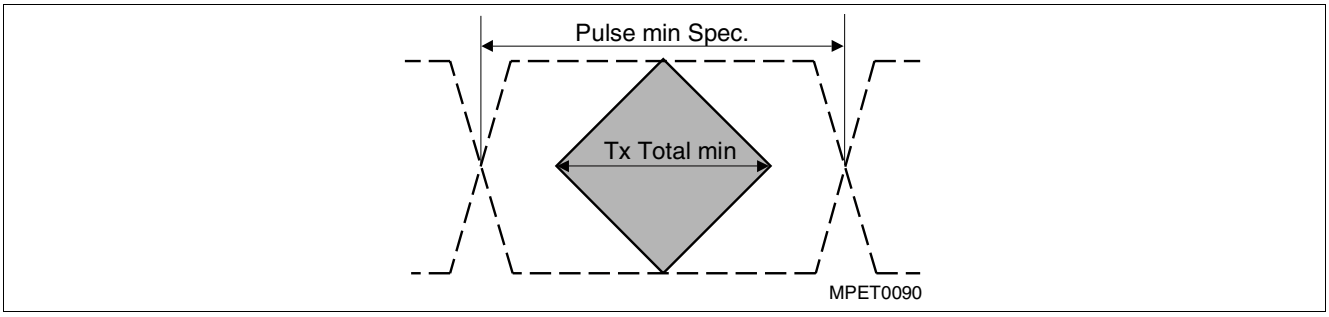

Figure 11 Illustrates the transmitter timing specifications

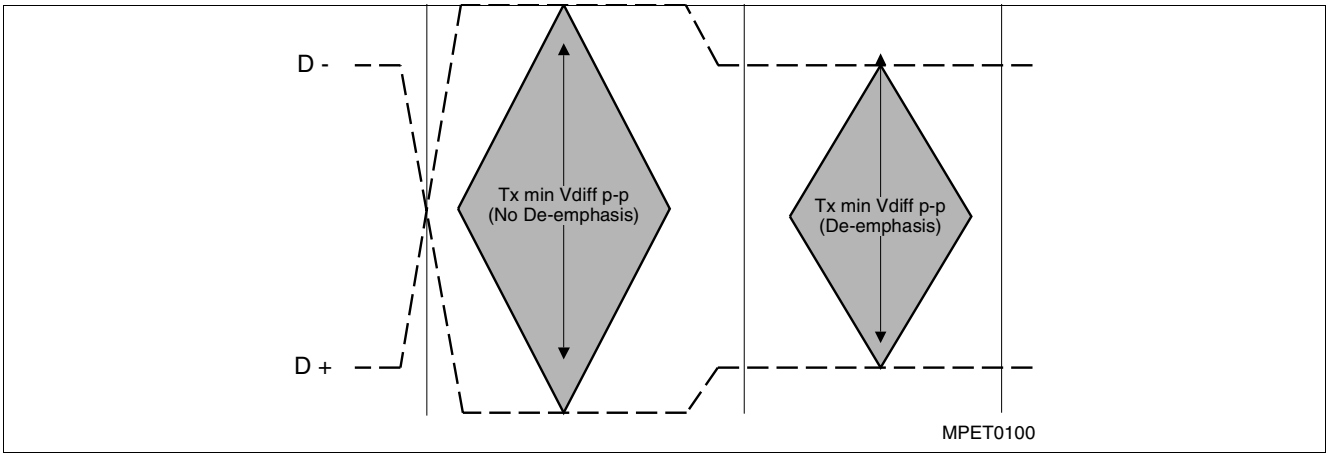

Figure 12 Illustrates the de-emphasized string of patterns at the output of a transmitter

Table 15 Differential Transmitter Output Specifications

Parameter	Symbol	Values		Unit	Comments
		Min.	Max.		
Differential peak-to-peak output voltage for large voltage swing	$V_{TX-DIFFp-p\_L}$	900	1300	mV	see **Equation (1)** Measured as Note[1)]
Differential peak-to-peak output voltage for regular voltage swing	$V_{TX-DIFFp-p\_R}$	800		mV	see **Equation (1)** Measured as Note[1)]

Table 15 Differential Transmitter Output Specifications (cont'd)

Parameter	Symbol	Values		Unit	Comments
		Min.	Max.		
Differential peak-to-peak output voltage for small voltage swing	$V_{TX-DIFFp-p\_S}$	520		mV	see **Equation (1)** Measured as Note[1)]
DC common code output voltage for large voltage swing	V_{TX-CM_L}		375	mV	see **Equation (2)** Measured as Note[1)]
DC common code output voltage for small voltage swing	V_{TX-CM_S}	135	280	mV	see **Equation (2)** Measured as Note[1)] See also Note[2)]
De-emphasized differential output voltage ratio for -3.5 dB de-emphasis	$V_{TX-DE-3.5-Ratio}$	-3.0	-4.0	dB	[1)3)4)]
De-emphasized differential output voltage ratio for -6.0 dB de-emphasis	$V_{TX-DE-6.0-Ratio}$	-5.0	-7.0	dB	[1)2)3)]
AC peak-to-peak common mode output voltage for large swing	$V_{TX-CM-ACp-p-L}$		90	mV	see **Equation (7)** Measured as Note[1)] See also Note[5)]
AC peak-to-peak common mode output voltage for regular swing	$V_{TX-CM-ACp-p-R}$		80	mV	see **Equation (7)** Measured as Note[1)] See also Note[5)]
AC peak-to-peak common mode output voltage for small swing	$V_{TX-CM-ACp-p-S}$		70	mV	see **Equation (7)** Measured as Note[1)] See also Note[5)]
Maximum single-ended voltage in EI condition DC + AC	$V_{TX-IDLE-SE}$		50	mV	[6)]
Maximum single-ended voltage in EI condition DC + AC	$V_{TX-IDLE-SE-DC}$		20	mV	[6)]
Maximum peak-to-peak differential voltage in EI condition	$V_{TX-IDLE-DIFFp-p}$		40	mV	
Single-ended voltage (w.r.t. VSS) on D+/D-	V_{TX-SE}	-75	750	mV	[1)7)]
Mimimum TX eye width, 3.2 and 4.0Gb/s	$T_{TX-Eye-MIN}$	0.7		UI	[1)8)]
Mimimum TX eye width 4.8Gb/s	$T_{TX-Eye-MIN4.8}$	TBD		UI	[1)8)]
Maximum TX deterministic jitter,3.2 and 4.8 Gb/s	$T_{TX-DJ-DD}$		0.2	UI	[1)8)9)]
Maximum TX deterministic jitter, 4.8 Gb/s	$T_{TX-DJ-DD-4.8}$		TBD	UI	[1)8)9)]
Instantaneous puls width	$T_{TX\ -PULSE}$	0.85		UI	[10)]
Differential TX outout rise/fall time	$T_{TX-RISE}$ $T_{TX-FALL}$	30	90	ps	Given by 20 % - 80 % voltage levels. Measured as Note[1)]
Mismatch between rise and fall times	$T_{TX-RF-MISMATCH}$		20	ps	
Differential return loss	$RL_{TX-DIFF}$	8		dB	Measured over 0.1 GHz to 2.4 GHz. See also Note[11)]
Common mode return loss	RL_{TX-CM}	6		dB	Measured over 0.1 GHz to 2.4 GHz. See also Note[11)]

Table 15 Differential Transmitter Output Specifications (cont'd)

Parameter	Symbol	Values		Unit	Comments
		Min.	Max.		
Transmitter termination impender	R_{TX}	41	55		12)
D+/D- TX Impedance difference	$R_{TX\text{-}MATCH\text{-}DC}$		4%		see **Equation (4)** Bounda are applied separately to high and low output voltages states
Lane-to lane skew at TX	$L_{TX\text{-}SKEW\ 1}$		100+ 3UI	ps	13)15)
Lane-to lane skew at TX	$L_{TX\text{-}SKEW\ 2}$		100+ 2UI	ps	14)15)
Maximum TX Drift (resync mode)	$T_{TX\text{-}Drift\text{-}RESYNC}$		240	ps	16)
Maximum TX Drift (resample mode only)	$T_{TX\text{-}Drift\text{-}RESAMPLE}$		120	ps	16)
BER	Bir Error Ratio	10^{-12}			17)

1) Specified at the package pins into a timing and voltage compliance test load as shown in Figure 4-2 and in steps outlined in 4.1.2.1. Common-mode measurements to be performed using a 101010 pattern.
2) The transmitter designer should not artifically elevate the common mode in order to meet this specification.
3) This is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
4) De-emphasis shall be disabled in the calibration state.
5) Includes all sources of AC common mode noise
6) Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition.
7) The maximum value is specified to be at least ($V_{TX\text{-}DIFFp\text{-}pL/4}$) + $V_{TX\text{-}CML}$ + ($V_{TX\text{-}CM\text{-}ACp\text{-}p/2}$).
8) This number does not include the effects of SSC or reference clock jitter.
9) Defined as the expected maximum jitter for the given probability as measured in the system (TJ), les the unbounded jitter.
10) Puls width measure at 0V differential.
11) One of the components that contribute to the deterioration of the return loss is the ESD structure wich needs to be carefully designed
12) The termination small signal resistance; tolerance across voltages from 100 mV to 400 mV shall not exceed +/- 5 W with regard to the average of the values measured at 100 mV and 400 mV for that pin.
13) Lane to Lane skew at the Transmitter pins for an end component.
14) Lane to Lane skew at the Transmitter pins for an intermediate component (assuming zero Lane to Lane skew at the Receiver pins of the incoming PORT).
15) This is a static skew. An FB-DIMM component is not allowed to change its lane to lane phase relationship after initialization.
16) Measured from the reference clock edge to the center of the output eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate change is significantly below the tracking capability of the reciver.
17) BER per differential lane.

$$V_{TX-DIFFp-p} = 2 \times |V_{TX-D+} - V_{TX-D-}| \quad (1)$$

$$V_{TX-CM} = DC_{(avg)}\text{of}\ (|V_{TX-D+} + V_{TX-D-}|/2) \quad (2)$$

$$V_{TX-CM-AC} = ((\text{Max}\ |V_{TX-D+} + V_{TX-D-}|)/2) - ((\text{Min}\ |V_{TX-D+} + V_{TX-D-}|)/2) \quad (3)$$

$$R_{TX-Match-DC} = 2 \times \frac{|R_{TX\text{-}D+} - R_{TX\text{-}D-}|}{R_{TX\text{-}D+} + R_{TX\text{-}D-}} \quad (4)$$

7.6 Differential Receiver Input Specifications

The receiver definition starts from the input pin of the receiver end package and therefore includes the package and the receiver end chip.

7.6.1 Receiver Input Compliance Eye Specification

Following the specification of the transmitter, the receiver is specified in terms of the minimum input eye that must be maintained at the input to the receiver, and under which the receiver must function at the specified data rates. The receiver eye is referenced to VSS and all input terminations at receiver must be referenced to VSS. This input eye must be maintained for at least NMIN-UI-RX consecutive UIs. An appropriate average transmitter UI must be used as the interval for measuring the eye diagram. The eye diagram is created using all edges of the NMIN-UI-TX consecutive UIs. The eye diagrams shall be measured by observing a continuous TBD pattern at the pin of the device.

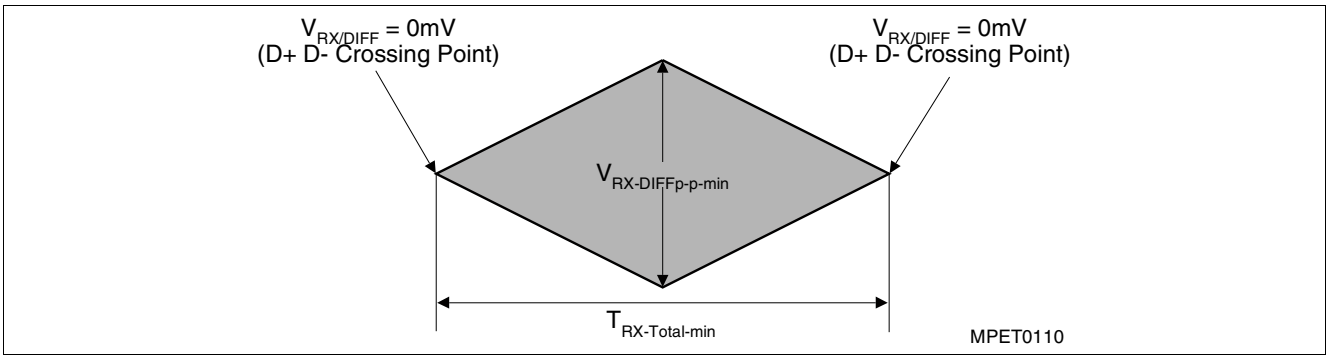

Figure 13 Required receiver input eye (differential) showing minimum voltage and timing Spec.

Table 16 Revision History

Filename	Date	Initials	Comment	Conditional Tags	R/SC Number
mpit2113	2005-11-21	msc	new template_321		
mpit2112					
mpit2111					
mpit2110			Initial document		

Table 17 Differential Receiver Input Specifications

Parameter	Symbol	Values		Unit	Comments
		Min.	Max.		
Differential peak-to-peak input voltage	$V_{RX-DIFFp-p}$	170	TBD	mV	see **Equation (5)** Measured as Note[1)]
Maximum single-ended voltage for EI condition	$V_{RX-IDLE\_SE}$		75	mV	[2)3)]
Maximum single-ended voltage for EI condition(DC only)	$V_{RX-IDLE\_SE\_DC}$		50	mV	[2)3)]
Maximum peak-to-peak differental voltage for EI condition	$V_{RX-IDLE-DIFFp-p}$		65	mV	[3)]
Single ended voltage (w.r.t. VSS) on D+/D-	V_{RX-SE}	-300	900	mV	[4)]
Single-pulse peak differential input voltage	$V_{RX-DIFF-PULSE}$	85		mV	[4)5)]

Table 17 Differential Receiver Input Specifications

Parameter	Symbol	Values		Unit	Comments
		Min.	Max.		
Amplitude ratio between adjacent symbols	$V_{RX-DIFF-ADJ-Ratio}$		TBD		4)6)
Maximum RX inherent timing error, 3.2 and 4.0 Gb/s	$T_{RX-TJ-MAX}$		0.4	UI	4)7)8)
Maximum RX inherent timing error, 4.8Gb/s	$T_{RX-TJ-MAX4.8}$		TBD	UI	4)7)8)
Maximum RX inherent deterministic timing error, 3.2 and 4.0 Gb/s	$V_{RX-DJ-DD}$		0.3	UI	4)7)8)9)
Maximum RX inherent deterministic timing error, 4.8 Gb/s	$V_{RX-DJ-DD-4.8}$		TBD	UI	4)7)8)9)
Single-puls width at zero-voltage crossing	$T_{RX-PW-ZC}$	0.55		UI	4)5)
Single-puls width at minimum-level crossing	$T_{RX-PW-ML}$	0.2		UI	4)5)
Differential RX input rise/fall time	$T_{RX-RISE}$, $T_{RX-FALL}$,	50		ps	Given by 20 % - 80 % voltage levels.
Common mode of the input voltage	V_{RX-CM}	120	400	mV	see **Equation (6)** Measure as Note[1)], See also Note[10)]
AC peak-to-peak common mode of input voltage	$V_{RX-CM-ACp-p}$		270	mV	see **Equation (7)** Note[1)]
Ratio of $V_{RX-CM-ACp-p}$ to minimum $V_{RX-DIFFp-p}$	$V_{RX-CM-EH-Ratop}$		45	%	11)
Differential return loss	$RL_{RX-DIFF}$	9		dB	Measured over 0.1 GHz to 2.4 GHz. See also Note[12)]
Common mode return loss	R_{RX-CM}	6		dB	Measured over 0.1 GHz to 2.4 GHz. See also Note [12)]
RX termination impendance	R_{RX}	41	55	Ω	13)
D+/D- RX impendance difference	$R_{RX-Match-DC}$		4	%	see **Equation (8)**
Lane-to-lane PCB skew at Rx	$L_{RX-PCB-SKEW}$		6	UI	Lane to Lane skew at the Receiver that must be tolerated. See also Note[14)]
Minimum RX Drift Tolerance	$T_{RX-DRIFT}$	400		ps	15)
Minimum data tracking 3 dB bandwidth	F_{TRK}	0.2		MHz	16)
Electrical idle entry datect time	$T_{EI-ENTRY-DETECT}$		60	ns	17)
Electrical idle exit datect time	$T_{EI-ENTRY-DETECT}$		30	ns	
Bit Error Ratio	BER		10^{-12}		18)

1) Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.

2) Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition. Worst-case margins are determined for the case with transmitter using small voltage swing.
3) Multiple lanes need to detect the EI condition before the device can act upon the EI detection.
4) Specified at the package pins into a timing and voltage compliance test setup.
5) See Figure 3-8 and Figure 3-9. The single-pulse mask provides sufficient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eyemask.
6) See Figure 3-10. The relative amplitude ratio limit between adjacent symbols prevents excessive intersymbol interference in the Rx. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.
7) This number does not include the effects of SSC or reference clock jitter.
8) This number includes setup and hold of the RX sampling flop.
9) Defined as the dual-dirac deterministic timing error.
10) Allows for 15 mV DC offset between transmit and receive devices.
11) The received differential signal must satisfy both this ratio as well as the absolute maximum AC peaktopeak common mode specification. For example, if $V_{RX\text{-}DIFFp\text{-}p}$ is 200 mV, the maximum AC peak-to peak common mode is the lesser of (200 mV * 0.45 = 90 mV) and $V_{RX\text{-}CM\text{-}AC\text{-}p\text{-}p}$.
12) One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.
13) The termination small signal resistance; tolerance across voltages from 100 mV to 400 mV shall not exceed +/- 5 W with regard to the average of the values measured at 100 mV and at 400 mV for that pin.
14) This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component driving the signal to the receiver. This is one component of the end-to-end channel skew in the AMB specification.
15) Measured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.
16) This bandwidth number assumes the specified minimum data transition density. Maximum jitter at 0.2 MHz is 0.05 UI, see Section 4 for full jitter tolerance mask.
17) The specified time includes the time required to forward the EI entry condition.
18) BER per differential lane. Refer to Section 4 for a complete definition of Bit Error Ratio.

$$V_{RX-DIFFp-p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}| \quad (5)$$

$$(V_{RX-CM} = DC_{(avg)} \text{of} |V_{RX-D+} + V_{RX-D\text{-}}|)/2 \quad (6)$$

$$V_{RX-CM-AC} = ((\text{Max} |V_{RX-D+} + V_{RX-D\text{-}}|)/2)((\text{Min} |V_{RX-D+} + V_{RX-D\text{-}}|)/2) \quad (7)$$

$$R_{RX-Match-DC} = 2 \times \frac{|R_{RX\text{-}D+} - R_{RX\text{-}D\text{-}}|}{R_{RX\text{-}D+} + R_{RX\text{-}D\text{-}}} \quad (8)$$

8 Channel Initialization

The FB-DIMM channel initialization process generally follows the top to bottom sequence of state transitions shown in the high level AMB Initialization Flow diagram in Figure 3-4. The host must sequence the AMB devices through the Disable, Calibrate, (back to Disable), Training, Testing, and Polling states in order to transition the AMBs into the active channel L0 state. The value in parenthesis in each state bubble indicates the condition/activity of the links during these states.

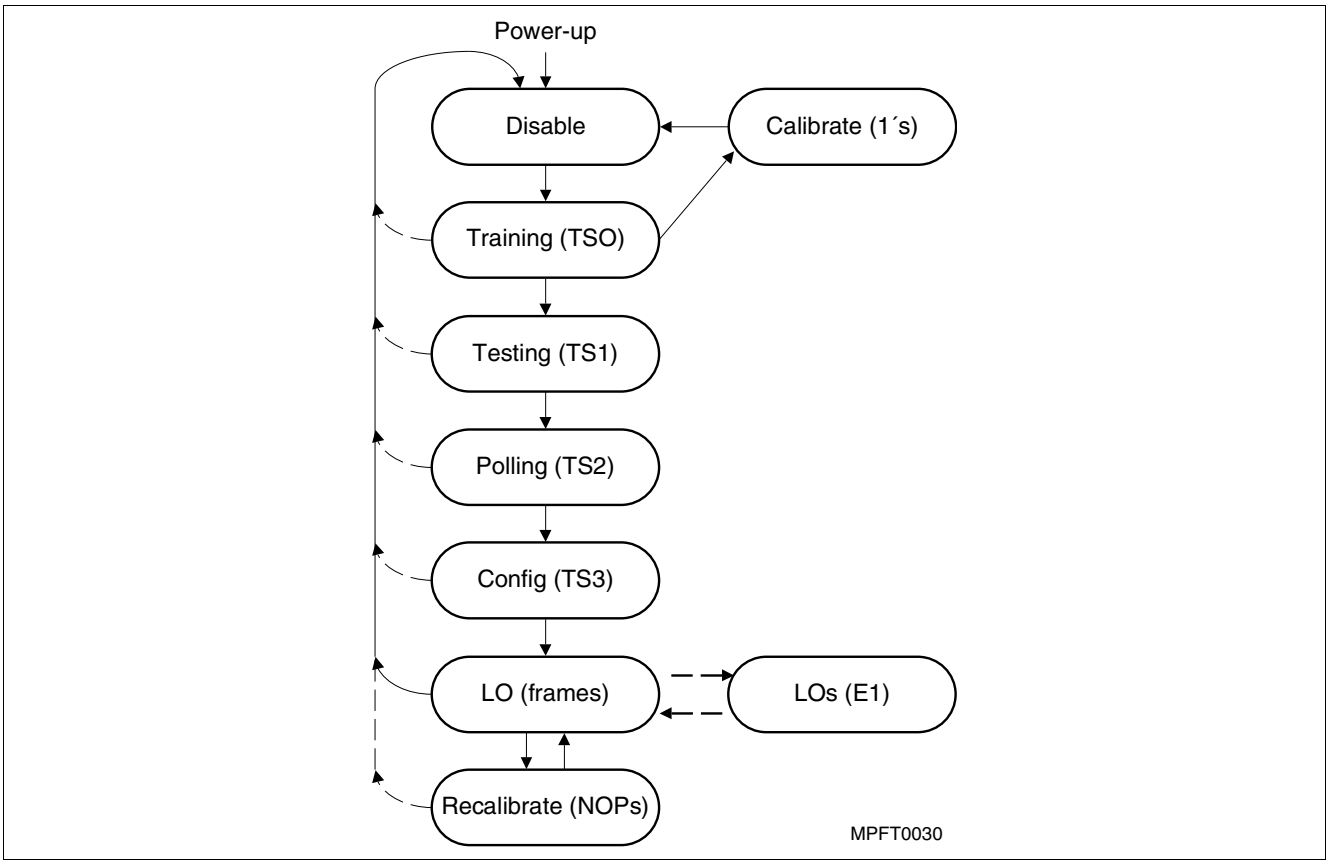

Figure 14 Flow Chart AMB Initialization

8.1 RESET Signal

The RESET signal acts as a hardware reset and immediately puts the AMB into a known state. The AMB Initialization FSM is put into the Disable state and the NB Tx outputs are put into Electrical Idle regardless of the state of the NB Rx inputs. All 'sticky' bits are set to their default values. The CKE signals to the DRAM devices are driven inactive to turn off the DRAM output drivers. DRAM specific mechanisms in the AMB may generate additional signal transitions to the DRAM devices to make sure that they do not hang in an unknown state. The AMB specification for each DRAM technology defines any DRAM specific mechanisms. If the DRAMs were in self refresh prior to RESET being asserted, they will remain in self refresh through the hardware reset. The host must wait until the power and the reference clock to the AMBs have been stable for greater than or equal to 1ms before transitioning the channel out of the Disable state. The relationship between supply voltage, reference clock and the RESET signal is defined in the AMB Buffer Specification

8.1.1 Inband Control 'Signals'

There are no dedicated control signals implemented on an FB-DIMM channel. Two different channel characteristics are exploited to deliver inband control information on the FB-DIMM channel wires when no

clock timing has been established between the host and the AMBs: Electrical Idle (EI): During normal channel operation the Tx outputs are enabled and a differential voltage is present on each bit lane. In Electrical Idle the Tx outputs source insignificant current and the termination resistors at the receiver pull both signals of the differential pair to ground. The Rx inputs can detect if both differential inputs are near ground to receive inband control information. Clock Training Violation: During normal channel operation the southbound bit lanes contain a minimum number of transitions every tClkTrain frames to keep the clock tracking circuits on each bit lane locked to the data stream. It is the absence of these periodic bit lane transitions that is used by the host to communicate control information..

8.2 Channel Initialization Sequence

The host controller sequences the FB-DIMM channel through the initialization sequence. The AMB devices on each DIMM monitor in-band signals from the host and use events and patterns on these signals to transition from one state to another. If the channel fails to initialize properly the host may transition the channel back to the Disable state and try again a number of times before reporting a failure to the system. It is undesirable to continuously drive high frequency signals into un-terminated transmission lines because of the EMI that is generated and the power that is wasted. To avoid this the host must return to the Disable state if the channel does not properly initialize.

8.2.1 Firmware Transition Control

The channel initialization and configuration sequence may be controlled by a hardware state machine or directed by firmware. To provide a flexible mechanism for dealing with a variety of FB-DIMM channel failure conditions it is recommended that the channel initialization and configuration process be controlled by firmware. It is recommended that implementation specific control registers be included in the host to allow firmware to step through the initialization steps and perform the following functions:

- Put the SB Tx outputs into Electrical Idle.
- Drive SB Tx outputs to all ones.
- Detect if the NB port is receiving Electrical Idle.
- Drive TS0 patterns with an arbitrary AMB_ID value.
- Receive TS0 patterns and read the returned AMB_ID value
- Drive TS1 patterns with an arbitrary AMB_ID value and with a sequence of electrical stress test patterns on each bit lane. Registers to hold an arbitrary 24 bits of Test Parameter values are recommended.
- Receive TS1 electrical stress test patterns and check the patterns.
- Test the NB bit lanes and report NB test results.
- Drive TS2 patterns.
- Receive TS2 patterns and determine the round trip channel delay.
- Drive TS3 patterns with channel configuration values.
- Receive TS3 patterns and check the returned values.
- Set the Last_AMB_ID value.
- Set the Hot_Add_AMB_ID value
- Set the Fast_Reset_Flag value.
- Set the Recalibrate_Duration value.
- Set the L0s_Duration value.
- Transition the channel to the L0 state and send the first Sync command.

8.2.2 AMB Internal State Variables

A number of internal flags and timers are referenced in the following sections. These flags and timers are implementation specific and included in the state tables to describe internal AMB state that may or may not be visible in defined AMB registers. These flags and timers include:

- Last_AMB_Flag - set in the last AMB to enable unique properties of the AMB in this position.

- First_Sync_Received_Flag - set to disable further initialization of the Idle/Alert Frame LFSR.
- Idle/Alert Frame LFSR - a counter in each AMB used to generate Idle and Alert frames on the NB channel.
- Alert_Flag - a flag that indicated that this AMB detected an error and is or was generating NB Alert frames.
- Recalibrate_Timer - a timer that keeps track of how long the AMB has been in the Recalibrate state.
- L0s_Timer - a timer that keeps track of how long the AMB has been in the L0s state.

8.2.3 Disable State

The channel is forced into the Disable state during hardware reset. The host may put the channel into the Disable state at any time and from any other state other than L0s by putting the three least significant Tx outputs into Electrical Idle. The host must not put the channel into the Disable state from the L0 state until any DRAM write operations have had time to complete. Channel initialization always starts in the Disable state.

8.2.4 Training State

The host drives a repetitive series of TS0 patterns to transition the AMBs from the Disable state to the Training state and to perform initial link training. The host may detect that the last AMB has acquired frame lock when TS0 patterns are received on the required number of inputs. Bit patterns in TS0 are used to perform bit lock and frame lock. The pattern is mostly filled with an alternating 1010 pattern to align the clock trackers with the incoming data stream. The sequence generally has logic zeroes in the even bit positions and logic ones in the odd bit positions. The beginning of the sequence is identified by the header pattern shown in the table below and is used to establish the alignment of the serial data onto frame boundaries.

8.2.5 Testing State

The host drives a TS1 pattern to transition the AMBs from the Training state to the Testing state and may send an arbitrary number of TS1 patterns to test the channel.

8.2.6 Polling State

The host drives a TS2 pattern to transition the AMBs from the Testing state to the Polling state. The host sends a continuous stream of TS2 patterns to the last AMB to determine the round trip latency of the channel. The host may subsequently and optionally send a TS2 pattern to each intermediate AMB to test if it has aligned its northbound merge data timing to the timing of the last AMB and can properly merge its data into the northbound data stream.

8.2.7 Config State

The TS3 training sequence is used to communicate the channel configuration to the AMBs in the Config state. On exit transitions to L0 state if 4 consecutive NOP frames are received.

9 Channel Protocol

The host performs all of the scheduling of the southbound and northbound data paths. The FB DIMMs do not initiate any northbound traffic but instead respond to commands provided by the host. This protocol style results in a memory channel that has deterministic behavior (in the absence of error events) and facilitates the use of two or more FB-DIMM channels in lock stepped configurations. The host sends commands and data to the DIMMs in 120-bit southbound frames. Similarly the DIMMs return data to the host in 168-bit northbound frames.

9.1 Southbound Frames

After initialization the host communicates with the AMBs on the channel using southbound frames of information containing commands and data. There are two modes of operation of the southbound channel, normal and fail-over. In normal mode the southbound link is full width and has a stronger CRC code. In fail-over mode the southbound link is reduced in width by one bit and uses a weaker CRC code.

9.1.1 Normal Southbound Frames

Normal southbound frames consist of 12 transfers of data delivered on 10 southbound bit lanes. Each frame contains 72-bits of data, 24-bits of command, 2-bits of command type and is protected by 22-bits of CRC information.

9.1.2 Fail-over Southbound Frames

Fail-over southbound frames consist of 12 transfers of data delivered on 9 southbound bit lanes. The most significant bit lane is not available to carry CRC bits in fail-over mode and the CRC code size is reduced in this mode.

9.1.3 Command Frame Format

The Command frame contains up to three independent commands that can be executed in parallel by separate DIMMs and in some cases by the same DIMM. Bits in each command specify which DIMM should execute the command.

9.1.3.1 Command Frame with Data Format

Specific commands, such as configuration register write commands, may need to deliver data to the AMB devices. The Command frame is used by these commands to deliver a data payload with information that cannot be encoded in the command itself.

9.1.3.2 Command+Wdata Frame Format

The Command+Wdata frame is used to deliver write data to write FIFO structures on each DIMM for future transfer to the DRAM devices. The content of the data payload is not examined by the AMB. The write data is loaded into the write FIFO on the DIMM from 3 consecutive Command+Wdata frames.

9.1.4 Southbound Commands

There are two categories of southbound commands. DRAM commands and channel commands.

9.1.4.1 DRAM Commands

DRAM commands are generated by the host to access the DRAM devices behind each AMB buffer. The host has access to the DRAM devices as if the devices were directly connected to the host. The AMB decodes the

DRAM commands and generates the control signals to the DRAM devices. The command delivery on the DRAM address and control signals (excluding CKE) use 1n command timing. 1n command timing means that the commands are present on the DRAM pins for a single clock cycle. DRAM Read and Write commands always transfer complete bursts of data determined by the Burst Length field programmed into the DRAM MRS registers. A burst length of 4 will transfer 36 bytes and a burst length of 8 will transfer 72 bytes to/from each ECC DIMM. Non-ECC memory DIMMs support the Data Mask function. Write accesses transfer the data from the write data FIFO located inside the AMB device on the DIMM. A register instructs the AMB when to drive the data after the Write command. The DDR2 specific Off-Chip Driver (OCD) impedance Adjust command also transfers data from the write data FIFO to the DRAM devices. The host is responsible for memory ordering, FB-DIMM channel scheduling, and error handling.

Available DRAM Commands

- Activate
- Write
- Read
- Precharge All
- Precharge Single
- Auto Refresh
- Enter Self Refresh
- Enter Power Down
- Exit Self Refresh and Exit Power Down

9.1.4.2 Channel Commands

Channel commands include the Sync command, miscellaneous DRAM commands, configuration register read and write commands, and miscellaneous maintenance commands.

Available Channel Commands

- Channel NOP
- Sync
- Soft Channel Reset
- Write Config Register
- Read Config Register
- DRAM CKE per DIMM
- DRAM CKE per Rank
- Debug

9.1.4.3 CKE Control Commands

Two versions of the CKE control command allows for individual rank control, where up to 4 DIMMs may be targeted at once, or per DIMM control, where all 8 DIMMs can be accessed from a single command. The CKE control commands will affect the CKE pins for the addressed DIMM(s) with the same timing as a DRAM command, based on slot location. Multiple CKE commands may be included in one frame as long as no more than one of the commands targets any one DIMM on the same DRAM clock. The Host Controller is responsible for CKE timing with respect to the DRAM protocol, including the explicit Self Refresh command. The AMB will not do any protocol checking. The Per DIMM CKE command allows all 8 DIMMs to be targeted by a single command. The Per Rank CKE command allows for individual Rank CKE control.

9.1.4.4 Soft Channel Reset Command

The Soft Channel Reset command may be used to attempt to recover from a transient bit failure on the channel. In the case of a minor transient bit error a single or a small group of commands may be corrupted.

The AMB will detect the corruption as a CRC error and will ignore the corrupted commands and report the error to the host with Alert frames. The host may issue a Soft Channel Reset command to acknowledge the receipt of the Alert frames and reset the command state of the AMBs. The Soft Channel Reset command must be preceded by at least 1 NOP frame and followed by at least 4 NOP frames. The AMB recognizes the Soft Channel Reset command while ignoring all others and resets its internal command state.

The following actions are performed by the AMB:

- Discontinue Alert frame generation and generate Idle frames or forward NB traffic in the frame that a Status return would be located if the Soft Channel Reset command was a Sync command.
- Discard all data content in the Write FIFO
- Reset the DIMM target Write FIFO state machine

The host may follow the Soft Channel Reset command (and the 4 NOP frames) with a sequence of DRAM commands to clear the command state of the DRAM devices. The sequence may look something like this:

1. Assert CKE to all ranks
2. Wait the appropriate number of clocks
3. Issue a Precharge All command to all ranks If the Soft Channel Reset itself is corrupted the stream of Alert frames will continue and the host may perform a Fast Reset to reinitialize the channel.

9.1.4.5 Sync Command

The FB-DIMM channel periodically requires a minimum number of transitions on each bit lane to maintain clock recovery synchronization. The host must periodically send a Sync command on the channel to maintain the required transition density. The maximum interval between sync frames is 42 frames, in order to maintain clock recovery synchronization. The host controller must adhere to a minimum interval between sync frames to guarantee that the AMB clock recovery circuits will be adjusted. This allows the AMB to save power by switching off internal circuits between sync commands. The AMB contains a register in which the host controller programs the minimum interval between syncs which it will send. The host controller may then send syncs at any interval between the programmed interval and 42. For example, if the host controller design can send syncs in the range of 38 to 42 frames apart, the register would be programmed to 38. The best power management for the AMB can be achieved by the host controller being as consistent as possible in its sync generation. Power Management within the AMB can have an impact on bandwidth capabilities in some platforms. The AMB specification provides information on the programming of this register as well as the default and minimum values. Following a reset, the host may ignore the minimum sync interval up until the 4th sync.

9.1.4.6 NOP Frame

The NOP frame contains three NOP commands and is sent on the southbound link when there are no other commands to send on the channel. The frame is a normal Command frame format.

9.1.4.7 Command Delivery Timing

DRAM access latency is minimized by allowing the command to be delivered to the DRAM immediately after the first 4 transfers of the frame have been received.

9.1.4.8 Concurrent Command Delivery Rules

Commands may be issued in any combination, as long as they do not collide on any DRAM pin or FB-DIMM data slot, and follow a few additional rules below.

DRAM Command and Address Pins

Only one of the following commands may target a particular DIMM in the same DRAM clock due to collisions on the DRAM command and address pins. Multiple commands within this list may be issued if each targets a different DIMM, as long as there is no collision on the FB-DIMM channel northbound data bus:

Activate, Write, Read, Precharge Single, Precharge All, Auto Refresh, and Enter Self Refresh.

DRAM CKE Pins

Only one of the following commands may target a particular DIMM in the same DRAM clock due to collisions on the CKE pins: Enter Self Refresh, Exit Self Refresh, DRAM CKE per DIMM, DRAM CKE per Rank, and Enter Power Down. Note that DRAM CKE commands may target a single DIMM, or 4 or 8 DIMMs at once. When multiple DIMMs are targeted by a command, no other command affecting the CKE pins may be issued to any of the targeted DIMMs.

DRAM Data and Strobe Pins

Commands cannot be issued to a DIMM that would cause collisions on the DRAM data and strobe pins within a DIMM. In addition, all turnaround times for the DRAM data and strobe pins must be observed.

Northbound Data Bus

Commands cannot be issued on the channel that would cause collisions on the Northbound data bus. Commands that generate data on the northbound data bus are: Read, Read Config Reg, and Sync. The order of responses must be preserved. Commands issued following a Sync command with SD > 0 must not return data before or on top of the Sync status return.

Other Restrictions

Only one outstanding configuration read or write register transaction is allowed on the channel. A configuration register read begins with the command and ends with the data being returned to the host. A configuration write begins with the command and ends when the read data would have been returned if the command were a Read Config Reg. This is the same point that an Alert Frame would be generated if there were a CRC error on the Write Config Reg command. Allowing only one outstanding configuration transaction on the bus allows for proper replay of the Write Config Reg command following an Alert Frame. A Soft Channel Reset requires NOP commands in all other command slots in the previous DRAM clock, the current DRAM clock, and the next 4 DRAM clocks. Only one In-band Debug event may be sent within a DRAM clock. The host controller is responsible for state and timing of the CKE pins vs. DRAM commands based on the DRAM specifications. A DRAM command and CKE command may target the same DIMM on the same DRAM clock provided that the DRAM specifications are met.

9.1.4.9 Command Encoding

Commands are encoded into the 24 bit of Command frames. For detailed command bit maps please refer to the AMB Buffer Specification.

9.2 Northbound CRC Modes

FB-DIMM supports three northbound CRC modes to support applications that require different levels of error detection. The frames contain two 72-bit or 64-bit data payloads. Each data payload is protected by either a 12-bit CRC or a 6-bit CRC. The three supported northbound CRC modes are: 14 bit lanes: 12-bit CRC over 72-bit data payload, fail-over to 6-bit CRC 13 bit lanes: 6-bit CRC over 72-bit data payload, fail-over to ECC coverage only 12 bit lanes: 6-bit CRC over 64-bit data payload, no fail-over The selection on the mode of operation is controlled by the host and communicated during the initialization process. Northbound CRC is only computed for Data frames. The Idle, Alert, and Status frame types drive the upper bit lanes with a known data pattern. During fail-over the host simply ignores the missing bit lanes.

9.2.1 Northbound Idle Frame

Each Idle frame contains a permuting data pattern. The last DIMM on the channel sends this permuting data pattern when not sending requested data from the DIMM. The content of the frame is designed to intentionally generate CRC errors if not in fail-over mode so that the host can easily detect when an expected Northbound Data frame with good CRC is missing. The host does not log the CRC errors generated by the Idle frames. Host hardware will issue a Sync command on the channel immediately following entry into the L0 state to reset the permuting data pattern of the Idle and Alert frames to their initial value. The first Idle frame follows immediately after the Status frame returned for the first Sync command. The permuting data pattern is generated by a 12-bit linear-feedback shift register (LFSR) with a polynomial of x12 +x7 + x4 + x3 + 1. The LFSR counter cycles through 212-1 states (4095 frames) before the pattern is repeated. Each bit of the counter is mapped onto a corresponding northbound bit lane. The LFSR does not generate an all zero data payload.

9.2.2 Northbound Alert Frame

AMBs report detection of errors on the channel using the Northbound Alert frame. The Northbound Alert frame contains the inverse of the Idle frame data pattern. The host may use detection of this permuting data pattern to indicate that an error has occurred. An AMB on the channel will send this permuting data pattern after it has detected a CRC error in any southbound command frame. The AMB will continue to generate Northbound Alert frames until it receives a Soft Channel Reset command or a channel reset.

9.2.3 Northbound Data Frames

This section defines the format of the Northbound Data frames. Each frame contains either two 72-bit data payloads or two 64-bit data payloads. A CRC code is computed across each of the 72-bit data payloads and is sent on the 12th, 13th, or 13th & 14th bit lanes if not in fail-over mode. Each data payload has its own CRC code to minimize the latency to deliver the first data payload to the host.

9.2.3.1 14-bit Lane Northbound Data Frame

This is the highest RAS mode of operation for the northbound channel. In this mode a 12-bit CRC is delivered during the transfer of each 72-bit data payload. For the mapping of the data from each of the DRAM devices into the Northbound Data frame please refer to the AMB Buffer Specification.

9.2.3.2 13-bit Lane Fail-over Northbound Data Frame

When the 14 lane mode has failed over to 13 lanes, the northbound data frame is identical to the 13 bit lane frame below.

9.2.3.3 13-bit Lane Northbound Data Frame

This is the medium RAS mode of operation for the northbound channel. In this mode a 6-bit CRC is delivered during the transfer of each 72-bit data payload. For the mapping of the data from each of the DRAM devices into the Northbound Data frame please refer to the AMB Buffer Specification.

9.2.3.4 13-bit Lane Fail-Over Northbound Data Frame

When 13-bit lane mode has failed over and is operating on 12 lanes, each transfer consists of only the 72 bit payload with no CRC. The ECC implemented by the host is the only error detection available. Note that this frame format is NOT the same as the 12-bit Lane frame format.

9.2.3.5 12-bit Lane Northbound Data Frame (Non-ECC Mode)

This is the lowest RAS mode of operation for the northbound channel. In this mode a 6-bit CRC is delivered during the transfer of each 64-bit data payload. The data payload does not contain ECC bits and the CRC code is the only form of protection. For the mapping of the data from each of the DRAM devices into the Northbound Data frame please refer to the AMB Buffer Specification.

9.2.3.6 Northbound Register Data Frame

The NB Register Data frame is used to return data in response to a Read Configuration command. The frame always returns 32-bits of register data. The host must select the appropriate bytes from the four data bytes delivered if fewer than four bytes are needed.

9.2.3.7 Northbound Status Frame

The Status frame is returned to the host in response to a Sync command from the host. The status returned in the Status frame corresponds to the status of the AMB to commands before the Sync command. Errors that are generated by commands after the Sync command are reported in subsequent Status frames. In other words the Sync command provides a fence for status reporting. Each AMB will merge its status into the northbound bit stream on the appropriate bit lane. The northbound Status frame contains a group of status bits from each AMB. The status bits are protected by an odd parity bit DnSP that covers the status bits from each AMB individually. This is necessary because the status from each AMB is merged ìon-the-flyî into the Status Frame by each AMB and a CRC that covers all of the status bits could not be calculated within this mechanism. Each AMB drives all 12 bits delivered in the frame for its assigned bit lane, including the alternating one/zero pattern. The AMB in the last DIMM position of the daisy chain initiates the northbound Status frame and fills the bit lane corresponding to its DIMM position with its status information and fills the remainder of the bit lanes with a zero status code and an invalid zero parity value. This is done so that the host may detect a missing status response if an AMB misinterprets the Sync command. The host is expected (but not required) to detect the status response error and reissue the Sync command to request the status again. The CRC bit lanes are filled with the same fixed pattern because the CRC is not valid in this frame type.

9.3 DRAM Memory Timing

The host accesses the DRAM devices on an FB-DIMM DIMM as if they were directly connected to the host but with a few differences. First there is generally a longer than usual delay in the return data path between the DRAM and the host,and second there is a FIFO mechanism in the write data path between the host and the DRAM. The host sends ‘RAS’ and ‘CAS’ style commands directly to the DRAM devices. The commands on the FB-DIMM channel are delivered to the DRAM devices with a fixed delay. The host controller must deliver commands onto the FB-DIMM channel exactly as the host intends the commands to be delivered to the DRAM devices. This section illustrates the DRAM timing on the channel. The command delivery on the DRAM address and control pins use 1n command timing. 1n command timing means that the commands are present on the DRAM pins for a single clock cycle. This allows the commands present on the channel to be forwarded to the DRAM channel without timing modification.

9.3.1 Read Timing

The command timing of the DRAM devices on an FB-DIMM is identical to the timing of an individual DRAM device. The RAS latency, CAS latency, etc. are controlled by the MRS values loaded into the DRAM devices. Figure 4-15 illustrates an example DRAM Read operation. The data returned to the host is delayed for an interval of time determined by the propagation delay characteristics of the channel. For single DIMM configurations the timing behaves similar to a Registered SDRAM DIMM. As DIMMs are added to the channel the accumulated delay due to PCB flight time and delay through intermediate AMB components increases the delay in the return data path.

Back-to-back reads from different DIMMs is illustrated in Figure 4-16. Unlike DDR2, the data from the separateDIMMs can be returned without a dead clock between the data bursts.

Figure 15

9.3.2 Write Timing

The write command timing of a DRAM device on an FB-DIMM is identical to the timing of an individual DRAM device. The Write latency is controlled by the MRS values loaded into the DRAM devices. Figure 4-17 illustrates an example DRAM Write operation. The host transfers the data to be written into a write FIFO in the AMB preceding the DRAM write transfer. The write FIFO is used to accumulate write data in the AMB so that the data can be transferred to the DRAM devices at full burst rate during the write operation. The host must be aware of the DRAM Write latency value in order to make sure that the write data is available in the Write FIFO early enough to be delivered to the DRAMs when expected. The AMB must be aware of the DRAM Write latency value in order to deliver the write data to the DRAMs when expected. Note that the Write command may be issued before the frame holding the last payload of data. The figure shows the shortest time between the last frame of data is driven on the southbound channel and when the data can be driven onto the DRAM data pins. The data can be loaded into the FIFO earlier than what is shown but will occupy an entry in the FIFO until used. The fixed fall through time shown defines the just-in-time arrival of the data to meet delivery to the DRAM. This just-in-time arrival time allows the controller to deliver a burst of 64 transfers to the DRAM using the 35 deep FIFO in the AMB. Writes may be followed by a Sync command that returns status information to indicate to the host that no errors are associated with the write operation(s). The figure shows the earliest the Sync command can be issued and report completion of the write operations. If there are errors with the write command or the write data the AMB will report the error by sending Alert frames. Following error detection, the host may issue the Soft Channel Reset command to discard any data in the write FIFO. This would empty the write FIFO and put the write FIFO state machines into a known state.

9.3.2.1 Write Data FIFO

The Write Data FIFO is a data structure that is used to accumulate write data in the AMB in preparation for bursting the data to the DRAM devices. The FIFO can be filled at a maximum of half of the DRAM burst rate but is emptied at the full DRAM burst data rate. The Command+Wdata frames contain a data payload of 72-bits that is loaded into the designated write FIFO. The Command+Wdata frames are not required to be contiguous and may be separated by an arbitrary number of intervening frames. The write FIFO on each DIMM can hold thirty-five (35) 72-bit data payloads. Multiple bursts of data can be accumulated in the FIFO to amortize the read-write-read DRAM data bus turnaround penalty over a number of write operations. The DRAM Write command pulls the data from the head of the FIFO and delivers it to the DRAM devices in the clock cycle determined by register settings in the AMB. Additional data can be loaded into the FIFO while data is being delivered to the DRAM. The depth of the FIFO supports a continuous burst of 64 transfers to the DRAM devices.

9.3.3 Simultaneous Read and Write Data Transfers

The FB-DIMM channel provides separate data path for read completion data and write request data. Because each FB-DIMM contains an isolated DRAM channel behind the AMB component, read data from the DRAM devices on one FB-DIMM can be read at the same time that write data is being written to the DRAM devices on another FB-DIMM.

9.3.4 DRAM Bus Segment Restrictions

Either one or two ranks of DRAM devices may be located behind the AMB on an FB-DIMM. These devices sit on a DRAM bus segment and must observe the restrictions on the usage of the bus segment. The DDR2 SDRAM data sheets should be referenced for details of the restrictions. A dead time is required between read operations for DDR2 devices from the two separate ranks to avoid electrical conflict on the DQS and $\overline{\text{DQS}}$ signals. The turnaround times for dead times such as read-to-read, read-to-write, and write-to-read are DIMM layout specific and are captured in the SPD EEPROM on the DIMM. These parameters are readable by firmware to direct the appropriate behavior of the host controller.

10 Reliability, Availability and Serviceability

10.1 Overview

The FB-DIMM channel specification provides comprehensive RAS support including, error detection and frame transmission retry, error logging, error injection, host add/remove of DIMMs, and the mechanisms for in-operation test and fault recovery using the Fast Reset capability of the channel. The philosophy for FB-DIMM channel reliability is to provide strong error detection of channel transaction errors, and the ability to retry the transactions after automatic hardware recovery. Both the northbound and southbound links include fail-over mechanisms that can keep the links running after any one wire fails with enough fault detection to maintain reliable operation until repair. The FB-DIMM channel protects data from errors using CRC codes generated by both the host and the AMB. FB-DIMM provides error detection and retry mechanisms for commands and data. It further provides an Alert frame reporting mechanism whereby the host is made aware of errors found by an AMB in the command or (write) data. A Status response mechanism is provided to return to the host quick abbreviated status information from all of the AMBs simultaneously. An AMB will discard any commands or data received with a CRC error. For reads, the read data that is returned to the host with correct ECC and/or CRC is the positive acknowledgement that all has transpired without error. If the host does not receive a read return when scheduled, or if the read return contains an error, the host may reissue the read command or the entire read sequence, and/or send a sync command to acquire error status from the AMBs. Error free writes are silently accepted by the AMB with no response returned to the host. Write data or any commands that are received by the AMB in error will cause the AMB to notify the host through Alert frames. Alert frames are continuously sent until acknowledged by the host with a Soft Channel Reset command or a channel reset.

10.2 Example Error Flows

This section gives an informal overview of error handling by walking through example write and read flows. Precise details follow in subsequent sections.

10.2.1 Command Error Flow

The AMB checks for errors in all commands but cannot discriminate one failed type of command from any other type of command. All command errors are reported to the host and all subsequent commands except Soft Channel Reset are ignored. Command errors are reported to the host by a stream of Alert frames in place of normally returned frames. Upon receiving an Alert response indicating that there was a command error, the host may issue a Soft Channel Reset command or a Fast Reset to attempt to recover from the error. The AMB will close all DRAM pages and place the DRAM devices into self-refresh upon detection of the Fast Reset. Following the Fast Reset the host may reissue all read and write transactions since the previous verified transaction completion and continue normal operation.

10.2.2 Write Data Error Flow

The AMB checks for errors in the write data by computing a 22-bit CRC covering the write data frame. When in wire fail-over mode a 10-bit CRC is available to check for link transmission errors in the write data. CRC errors detected in the write data are reported to the host the same as command errors.

10.2.3 Read Error Flow

A read differs from a write primarily in that the AMB provides a positive acknowledgement that there were no errors with the read command through the delivery of the read data in the specified northbound data frame. If the AMB detects an error in a read command, the AMB discards the command and Alert frames will be

returned. Upon receiving a read return, the host verifies that it has received the correct amount of data at the scheduled time, and checks the correctness of the data. If any of these are in error the read command may either be retried or the host may attempt to correct the [data] error. Section 5.7 describes the algorithm in more detail.

10.3 Overview of Error Protection, Detection, Correction, and Logging

FB-DIMM uses several different mechanisms for error protection, detection, correction, and error logging. Error handling elements are made up of the following:

Southbound Commands and Data$_B$

a) The host computes check bits for commands -14-bit CRC on a per command basis. Reduced to 10-bit CRC in fail-over mode.
b) The host computes check bits for (write) data - 22-bit CRC on a per 72-bit write burst basis. Reduced to 10-bit CRC in fail-over mode.
c) The AMB detects CRC errors in southbound commands or (write) data, and logs information on the errors detected - Command or write data errors once observed prevent the AMB from decoding any commands except the
d) Soft Channel Reset command or until the channel is reset by the host - The AMB does not evaluate any ECC information sent with the (DRAM) write or attempt to correct any errors
e) The AMB returns error status on detected errors - CRC errors are reported on the northbound link by inserting Alert frames in place of other content. - Alerts continue to be sent until a Soft Channel Reset command is received or the channel is reset.

Northbound Read Data $_B$

FB-DIMM supports three northbound CRC modes to support applications that require different levels of error detection and cost. The frames contain two 72-bit or 64-bit data payloads. Each data payload is protected by either a 12-bit CRC or a 6-bit CRC, with reduced protection during fail-over. The three supported northbound
CRC modes are:
14 bit lanes: 12-bit CRC over 72-bit data payload, fail-over to 6-bit CRC
13 bit lanes: 6-bit CRC over 72-bit data payload, fail-over to ECC coverage only
12 bit lanes: 6-bit CRC over 64-bit data payload, no fail-over
The selection on the mode of operation is controlled by the host and communicated during the initialization process as defined in the Initialization chapter. Northbound CRC is only computed for Data frames. The Idle, Alert, and Status frame types drive the upper bit lanes with a known data pattern. During fail-over the host ignores the missing bit lanes and operates with reduced CRC coverage.
a) The host detects an error in the data through CRC (added by the AMB when not in fail-over mode) or by ECC provided with the data when read from DRAM (provided by the host with the data when written to DRAM)
- The host logs the information on errors detected
- The host corrects the data if possible using the ECC included within the data
- The host takes whatever other steps deemed prudent (such as reissuing the command to see if the data error was transient or scrubbing the DRAM location if it were a correctable error)

Northbound Status$_B$

a) The AMB computes a parity bit over its own status information
b) The host detects an error in the northbound status return
- The host logs the information on errors detected
- The host takes whatever other steps deemed prudent (such as issuing another sync command ñ up to a limit)
- If there were no errors in the status return itself then the host would log any error information reported through the status return and take whatever other steps deemed prudent. As noted above, the host is the only agent that corrects errors in system data. However, to provide enhanced data integrity, the host may first retry a read request upon detecting a data error before

attempting to correct the error. Furthermore, the host may choose to patrol memory, reading memory locations and writing back corrected data for any errors detected. Such patrol 'scrubbing' is orthogonal to the FB-DIMM error handling specification. It is left to the host designers to determine their own memory scrub methodology. The error logging done by the AMB(s) and the host are designed to permit isolation of the error source.

10.4 Error Protection and Detection Methods

10.4.1 CRC Logic Used on Normal Southbound Frames

See the AMB Buffer Specification for details.

10.4.2 Fail-over Southbound Frames

Fail-over southbound frames consist of 12 transfers of data delivered on the 9 southbound bit lanes. Bit lane 9 is not available to carry CRC bits in fail-over mode, and the CRC code size is reduced in this mode.

10.4.3 Write and Read Data ECC Error Protection

FB-DIMM makes provision for both read and write data to be protected with system defined ECC check bits per data block by supporting 8 check bits per 64 data bits in 14 and 13 lane northbound frames. The host generates the ECC code and passes it along with the write data to the AMB. The AMB will store the ECC along with the data in the DRAM memory. The AMB will not check the ECC code for errors and the host may use whatever algorithm it chooses. This allows the host to use various complex ECC algorithms, possibly spread across multiple channels. The mapping of the data and ECC bits to the DRAM components and channel bit lanes can enhance the protection provided by the ECC code to cover DRAM device failures and channel bit lane failures. Refer to the Southbound Command+Wdata frame format and Northbound Data frame definitions for details.

10.5 Southbound Error Handling at the AMB

Errors in southbound frames are handled using the following method:

a) Check for CRC errors in the command. If the AMB detects an error in the command then discard the entire frame, and marks as faulted the commands or data from the previous frame. Process as command error. Log the error. The first CRC error latches the error data contents. The AMB will save the 72-bits plus CRC bits from the previous frame and the command plus CRC from the current frame. Enter Command Error state: The AMB is forced to discard [all] subsequent commands until the channel is reset. Indicate error by returning Alert frames.

b) Determine if the frame is a Command, or Command+Wdata frame; evaluate each command within a frame separately.

c) Check if the command is a Sync command. If Sync then respond with Status.

d) Check if the command is targeted for this AMB then process command. If the command is an unrecognizable command then ignore the command. The AMB is not expected to do DRAM protocol checking (e.g., looking for command conflicts such as a write interrupting a read, etc.)

e) Process the next command in the command frame if any are left.

f) Process next frame.

10.5.1 Exiting Command Error State

Once an AMB has entered the Command Error state it will no longer process commands other than the Soft Channel Reset command. Indication that the AMB is in the Command Error state is made manifest by the hardware setting of the appropriate configuration register bit and returning Alert frames. The AMB will continue to operate in this mode until a Soft Channel

Reset command is received or the host resets the channel.

10.6 Northbound Error Handling at the AMB

The AMB does not evaluate the data and/or ECC information provided to it by the DRAM in response to a read command; it will forward the information supplied by the DRAM unchanged with a CRC for link error detection. An AMB does not evaluate the data and/or ECC or CRC information passing through it from AMBs further south than it.

10.7 Error Logging

Refer to the AMB Buffer Specification

10.8 Fail-over Mode Operation

During channel initialization each bit lane is tested to determine if it is functioning properly. If one of the southbound bit lanes, northbound bit lanes, or one bit lane in both directions is non-functional, the redundant bit lane(s) may be used to map out the bad bit lane. Operation with the redundant bit lane used to map out a bad bit lane is described as ‘fail-over mode.’

10.8.1 Fail-over Mode Operation on Southbound Lanes

Without the redundant bit lane used for CRC protection on the southbound lanes, commands continue to be protected by the 10-bit compound checksum CRC included with each command, DRAM write data continues to be protected by system level ECC data within the write data payload and the optional 12-bit CRC across each 72-bit data block, and the configuration register write data (within a Command+Data frame) continues to be protected by a 10-bit compound checksum CRC.

10.8.2 Fail-over Mode Operation on Northbound Lanes

The 14-lane northbound frame provides a 12-bit CRC over 72-bits of data in normal operation, and a 6- bit CRC over 72-bits of data in fail-over mode. The 13-lane frames are without the redundant bit lane used for CRC protection. The read data continues to be protected by system level ECC data within the read data payload, and the status response continues to be covered by its 10-bit compound checksum CRC.

10.9 AMB Pass-through Functionality

As noted earlier much of the discussion regarding AMB behavior was from the viewpoint of having only a single AMB on the channel. FB-DIMM supports from one to eight DIMMs and several additional AMB components per channel. As outlined in the protocol chapter, in terms of data movement an AMB is responsible for:

- Receiving southbound frames from the host or another AMB and in general re-driving those frames to a more southerly AMB.
- Evaluating southbound frames for commands or data targeted to that AMB and for checking all commands and data for errors.
- Receiving northbound frames from another AMB (generally) and re-driving those frames to another northerly AMB or to the host.
- Supplying frame content for read and status responses. Each AMB must maintain the compound checksums used on the southbound channel. As can be seen from the four simple steps above an AMB does not check [for errors in] frames moving north that have been forwarded by another AMB, the frames are either discarded and replaced by frames from this AMB (if it is responsible for providing a read response), selectively overwritten by this AMB (if this AMB is providing a status response), or simply forwarded on to the next AMB or host. Because an AMB component does not evaluate data passing northbound through it, a read response or Idle frame being delivered by a more southerly AMB at the same time as this AMB is simply discarded without error notification. If a given AMB is the last AMB (southern most AMB) it does not receive frames from the south and thus does not forward such

frames in the northerly direction. It is responsible, however, for always generating Idle frames whenever it is not providing a read response or status response frame in response to a command from the host. These frames enable easy error detection by the host whenever a read return or status return is not provided by an AMB as scheduled by the host. Particular attention is paid to the reliability of the pass-through logic. The logic is isolated from the rest of the internal AMB functions to ensure that the pass-through mechanism is functional even if other AMB functions have failed. This improves the reliability of the channel by minimizing the amount of logic that could result in a single point of failure.

10.10 Memory Initialization

The AMB contains a memory built-in self-test (MEMBIST) engine that is used to test the DRAM devices on the DIMM and initialize the contents of the DRAM devices to a known state. Refer to the FBD DFx specification for details.

10.11 Thermal Trip Sensor

The AMB is outfitted with a thermal sensor that measures the temperature of the AMB die. A DAC and comparator mechanism driven from a Finite State Machine in the AMB periodically adjusts its value to indicate the temperature of the die. The temperature of the AMB die can be read at any time in the Thermal Sensor register. The Thermal Trip registers can be set to signal thermal warnings whenever the value of the Thermal Sensor register is higher than the Thermal Trip register trip points. The AMB provides the warning via bits in the status response that indicates if the thermal condition has been exceeded. Refer to the AMB Buffer Specification for details. Serial Presence Detect Codes for FB-DIMM Modules

11 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

Table 18 PC2–4200F–444

Product Type		HYS72T64000HFN–3.7–A	HYS72T128020HFN–3.7–A	HYS72T256020HFN–3.7–A
Organization		512MB	1 GByte	2 GByte
		×72	×72	×72
		1 Rank (×8)	2 Ranks (×8)	2 Ranks (×4)
Label Code		PC2–4200F–444	PC2–4200F–444	PC2–4200F–444
JEDEC SPD Revision		Rev. 1	Rev. 1	Rev. 1
Byte#	Description	HEX	HEX	HEX
0	SPD Size CRC / Total / Used	92	92	92
1	SPD Revision	10	10	10
2	Key Byte / DRAM Device Type	09	09	09
3	Voltage Level of this Assembly	12	12	12
4	SDRAM Addressing	44	44	48
5	Module Physical Attributes	23	23	23
6	Module Type	07	07	07
7	Module Organization	09	11	10
8	Fine Timebase (FTB) Dividend and Divisor	00	00	00
9	Medium Timebase (MTB) Dividend	01	01	01
10	Medium Timebase (MTB) Divisor	04	04	04
11	$t_{CK.MIN}$ (min. SDRAM Cycle Time)	0F	0F	0F
12	$t_{CK.MAX}$ (max. SDRAM Cycle Time)	20	20	20
13	CAS Latencies Supported	33	33	33
14	$t_{CAS.MIN}$ (min. CAS Latency Time)	3C	3C	3C
15	Write Recovery Values Supported (WR)	32	32	32

Table 18 PC2–4200F–444 (cont'd)

Product Type		**HYS72T64000HFN–3.7–A**	**HYS72T128020HFN–3.7–A**	**HYS72T256020HFN–3.7–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200F–444**	**PC2–4200F–444**	**PC2–4200F–444**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
16	$t_{WR.MIN}$ (Write Recovery Time)	3C	3C	3C
17	Write Latency Times Supported	42	42	42
18	Additive Latency Times Supported	40	40	40
19	$t_{RCD.MIN}$ (min. RAS# to CAS# Delay)	3C	3C	3C
20	$t_{RRD.MIN}$ (min. Row Active to Row Active Delay)	1E	1E	1E
21	$t_{RP.MIN}$ (min. Row Precharge Time)	3C	3C	3C
22	t_{RAS} and t_{RC} Extension	00	00	00
23	$t_{RAS.MIN}$ (min. Active to Precharge Time)	B4	B4	B4
24	$t_{RC.MIN}$ (min. Active to Active / Refresh Time)	F0	F0	F0
25	$t_{RFC.MIN}$ LSB (min. Refresh Recovery Time Delay)	A4	A4	A4
26	$t_{RFC.MIN}$ MSB (min. Refresh Recovery Time Delay)	01	01	01
27	$t_{WTR.MIN}$ (min. Internal Write to Read Cmd Delay)	1E	1E	1E
28	$t_{RTP.MIN}$ (min. Internal Read to Precharge Cmd Delay)	1E	1E	1E
29	Burst Lengths Supported	03	03	03
30	Terminations Supported	07	07	07
31	Drive Strength Supported	01	01	01
32	t_{REFI} (avg. SDRAM Refresh Period)	C2	C2	C2
33	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	51	51	51
34	Psi(T-A) DRAM	78	78	78
35	ΔT_0 (DT0) DRAM	3C	3C	3C
36	ΔT_{2Q} (DT2Q) DRAM	22	22	22
37	ΔT_{2P} (DT2P) DRAM	1E	1E	1E
38	ΔT_{3N} (DT3N) DRAM	1E	1E	1E
39	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W) DRAM	34	34	34
40	ΔT_{5B} (DT5B) DRAM	1E	1E	1E

Table 18 PC2–4200F–444 (cont'd)

Product Type		**HYS72T64000HFN–3.7–A**	**HYS72T128020HFN–3.7–A**	**HYS72T256020HFN–3.7–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200F–444**	**PC2–4200F–444**	**PC2–4200F–444**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
41	ΔT_7 (DT7) DRAM	20	20	20
42 - 78	Not used	00	00	00
79	FBDIMM ODT Values	01	22	22
80	Not used	00	00	00
81	Channel Protocols Supported LSB	02	02	02
82	Channel Protocols Supported MSB	00	00	00
83	Back-to-Back Access Turnaround Time	10	10	10
84	AMB Read Access Delay for DDR2-800	56	56	58
85	AMB Read Access Delay for DDR2-667	40	40	42
86	AMB Read Access Delay for DDR2-533	36	36	38
87	Psi(T-A) AMB	30	30	30
88	ΔT_{Idle_0} (DT Idle_0) AMB	54	54	62
89	ΔT_{Idle_1} (DT Idle_1) AMB	6E	6E	7A
90	ΔT_{Idle_2} (DT Idle_2) AMB	60	60	65
91	ΔT_{Active_1} (DT Active_1) AMB	9A	9A	AA
92	ΔT_{Active_2} (DT Active_2) AMB	78	78	89
93	ΔT_{L0s} (DT L0s) AMB	00	00	00
94 - 97	Not used	00	00	00
98	AMB Junction Temperature Maximum (T_{jmax})	00	00	00
99	Category Byte	49	49	49
100	Not used	00	00	00
101	AMB Personality Bytes: Pre-initialization (1)	80	80	80
102	AMB Personality Bytes: Pre-initialization (2)	20	20	20
103	AMB Personality Bytes: Pre-initialization (3)	00	00	00
104	AMB Personality Bytes: Pre-initialization (4)	44	44	44
105	AMB Personality Bytes: Pre-initialization (5)	00	00	00
106	AMB Personality Bytes: Pre-initialization (6)	80	80	80

Table 18 PC2–4200F–444 (cont'd)

Product Type		**HYS72T64000HFN–3.7–A**	**HYS72T128020HFN–3.7–A**	**HYS72T256020HFN–3.7–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200F–444**	**PC2–4200F–444**	**PC2–4200F–444**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
107	AMB Personality Bytes: Post-initialization (1)	40	40	40
108	AMB Personality Bytes: Post-initialization (2)	53	53	53
109	AMB Personality Bytes: Post-initialization (3)	00	00	00
110	AMB Personality Bytes: Post-initialization (4)	00	00	00
111	AMB Personality Bytes: Post-initialization (5)	65	65	65
112	AMB Personality Bytes: Post-initialization (6)	4C	4C	4C
113	AMB Personality Bytes: Post-initialization (7)	00	00	00
114	AMB Personality Bytes: Post-initialization (8)	05	05	05
115	AMB Manufacturers JEDEC ID Code LSB	80	80	80
116	AMB Manufacturers JEDEC ID Code MSB	89	89	89
117	DIMM Manufacturers JEDEC ID Code LSB	80	80	80
118	DIMM Manufacturers JEDEC ID Code MSB	C1	C1	C1
119	Module Manufacturing Location	xx	xx	xx
120	Module Manufacturing Date Year	xx	xx	xx
121	Module Manufacturing Date Week	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx
126	Cyclical Redundancy Code LSB	94	A8	4E
127	Cyclical Redundancy Code MSB	95	9D	A4
128	Module Product Type, Char #1	37	37	37
129	Module Product Type, Char #2	32	32	32
130	Module Product Type, Char #3	54	54	54
131	Module Product Type, Char #4	36	31	32
132	Module Product Type, Char #5	34	32	35
133	Module Product Type, Char #6	30	38	36
134	Module Product Type, Char #7	30	30	30
135	Module Product Type, Char #8	30	32	32

Table 18 PC2–4200F–444 (cont'd)

Product Type		**HYS72T64000HFN–3.7–A**	**HYS72T128020HFN–3.7–A**	**HYS72T256020HFN–3.7–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200F–444**	**PC2–4200F–444**	**PC2–4200F–444**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
136	Module Product Type, Char #9	48	30	30
137	Module Product Type, Char #10	46	48	48
138	Module Product Type, Char #11	4E	46	46
139	Module Product Type, Char #12	33	4E	4E
140	Module Product Type, Char #13	2E	33	33
141	Module Product Type, Char #14	37	2E	2E
142	Module Product Type, Char #15	41	37	37
143	Module Product Type, Char #16	20	41	41
144	Module Product Type, Char #17	20	20	20
145	Module Product Type, Char #18	20	20	20
146	Module Revision Code	3x	3x	3x
147	Test Program Revision Code	xx	xx	xx
148	DRAM Manufacturers JEDEC ID Code LSB	80	80	80
149	DRAM Manufacturers JEDEC ID Code MSB	C1	C1	C1
150	informal AMB content revision tag (MSB)	00	00	00
151	informal AMB content revision tag (LSB)	08	08	08
152 - 175	Not used	00	00	00
176 - 255	Blank for customer use	FF	FF	FF

Table 19 PC2–4200F–444

Product Type		HYS72T64000HFA–3.7–A	HYS72T128020HFA–3.7–A	HYS72T256020HFA–3.7–A
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200F–444**	**PC2–4200F–444**	**PC2–4200F–444**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	SPD Size CRC / Total / Used	92	92	92
1	SPD Revision	10	10	10
2	Key Byte / DRAM Device Type	09	09	09
3	Voltage Level of this Assembly	12	12	12
4	SDRAM Addressing	44	44	48
5	Module Physical Attributes	23	23	23
6	Module Type	07	07	07
7	Module Organization	09	11	10
8	Fine Timebase (FTB) Dividend and Divisor	00	00	00
9	Medium Timebase (MTB) Dividend	01	01	01
10	Medium Timebase (MTB) Divisor	04	04	04
11	$t_{CK.MIN}$ (min. SDRAM Cycle Time)	0F	0F	0F
12	$t_{CK.MAX}$ (max. SDRAM Cycle Time)	20	20	20
13	CAS Latencies Supported	33	33	33
14	$t_{CAS.MIN}$ (min. CAS Latency Time)	3C	3C	3C
15	Write Recovery Values Supported (WR)	32	32	32
16	$t_{WR.MIN}$ (Write Recovery Time)	3C	3C	3C
17	Write Latency Times Supported	42	42	42
18	Additive Latency Times Supported	40	40	40
19	$t_{RCD.MIN}$ (min. RAS# to CAS# Delay)	3C	3C	3C
20	$t_{RRD.MIN}$ (min. Row Active to Row Active Delay)	1E	1E	1E
21	$t_{RP.MIN}$ (min. Row Precharge Time)	3C	3C	3C
22	t_{RAS} and t_{RC} Extension	00	00	00
23	$t_{RAS.MIN}$ (min. Active to Precharge Time)	B4	B4	B4
24	$t_{RC.MIN}$ (min. Active to Active / Refresh Time)	F0	F0	F0
25	$t_{RFC.MIN}$ LSB (min. Refresh Recovery Time Delay)	A4	A4	A4

Table 19 PC2–4200F–444 (cont'd)

Product Type		**HYS72T64000HFA–3.7–A**	**HYS72T128020HFA–3.7–A**	**HYS72T256020HFA–3.7–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200F–444**	**PC2–4200F–444**	**PC2–4200F–444**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
26	$t_{RFC.MIN}$ MSB (min. Refresh Recovery Time Delay)	01	01	01
27	$t_{WTR.MIN}$ (min. Internal Write to Read Cmd Delay)	1E	1E	1E
28	$t_{RTP.MIN}$ (min. Internal Read to Precharge Cmd Delay)	1E	1E	1E
29	Burst Lengths Supported	03	03	03
30	Terminations Supported	07	07	07
31	Drive Strength Supported	01	01	01
32	t_{REFI} (avg. SDRAM Refresh Period)	C2	C2	C2
33	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	51	51	51
34	Psi(T-A) DRAM	78	78	78
35	ΔT_0 (DT0) DRAM	3C	3C	3C
36	ΔT_{2Q} (DT2Q) DRAM	22	22	22
37	ΔT_{2P} (DT2P) DRAM	1E	1E	1E
38	ΔT_{3N} (DT3N) DRAM	1E	1E	1E
39	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W) DRAM	34	34	34
40	ΔT_{5B} (DT5B) DRAM	1E	1E	1E
41	ΔT_7 (DT7) DRAM	20	20	20
42 - 78	Not used	00	00	00
79	FBDIMM ODT Values	01	22	22
80	Not used	00	00	00
81	Channel Protocols Supported LSB	02	02	02
82	Channel Protocols Supported MSB	00	00	00
83	Back-to-Back Access Turnaround Time	20	18	18
84	AMB Read Access Delay for DDR2-800	74	74	74
85	AMB Read Access Delay for DDR2-667	62	62	62
86	AMB Read Access Delay for DDR2-533	56	56	56

Table 19 PC2–4200F–444 (cont'd)

Product Type		**HYS72T64000HFA–3.7–A**	**HYS72T128020HFA–3.7–A**	**HYS72T256020HFA–3.7–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200F–444**	**PC2–4200F–444**	**PC2–4200F–444**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
87	Psi(T-A) AMB	26	26	26
88	ΔT_{Idle_0} (DT Idle_0) AMB	3F	3F	3F
89	ΔT_{Idle_1} (DT Idle_1) AMB	50	50	50
90	ΔT_{Idle_2} (DT Idle_2) AMB	54	54	54
91	ΔT_{Active_1} (DT Active_1) AMB	57	57	57
92	ΔT_{Active_2} (DT Active_2) AMB	53	53	53
93	ΔT_{L0s} (DT L0s) AMB	00	00	00
94 - 97	Not used	00	00	00
98	AMB Junction Temperature Maximum (T_{jmax})	15	15	15
99	Category Byte	49	49	49
100	Not used	00	00	00
101	AMB Personality Bytes: Pre-initialization (1)	15	15	15
102	AMB Personality Bytes: Pre-initialization (2)	00	00	00
103	AMB Personality Bytes: Pre-initialization (3)	03	03	03
104	AMB Personality Bytes: Pre-initialization (4)	00	00	00
105	AMB Personality Bytes: Pre-initialization (5)	00	00	00
106	AMB Personality Bytes: Pre-initialization (6)	00	00	00
107	AMB Personality Bytes: Post-initialization (1)	00	00	00
108	AMB Personality Bytes: Post-initialization (2)	00	00	00
109	AMB Personality Bytes: Post-initialization (3)	00	00	00
110	AMB Personality Bytes: Post-initialization (4)	C0	C0	C0
111	AMB Personality Bytes: Post-initialization (5)	FF	FF	FF
112	AMB Personality Bytes: Post-initialization (6)	FF	FF	FF
113	AMB Personality Bytes: Post-initialization (7)	FF	FF	FF
114	AMB Personality Bytes: Post-initialization (8)	01	01	01
115	AMB Manufacturers JEDEC ID Code LSB	80	80	80
116	AMB Manufacturers JEDEC ID Code MSB	C1	C1	C1

Table 19 PC2–4200F–444 (cont'd)

Product Type		**HYS72T64000HFA–3.7–A**	**HYS72T128020HFA–3.7–A**	**HYS72T256020HFA–3.7–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200F–444**	**PC2–4200F–444**	**PC2–4200F–444**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
117	DIMM Manufacturers JEDEC ID Code LSB	80	80	80
118	DIMM Manufacturers JEDEC ID Code MSB	C1	C1	C1
119	Module Manufacturing Location	xx	xx	xx
120	Module Manufacturing Date Year	xx	xx	xx
121	Module Manufacturing Date Week	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx
126	Cyclical Redundancy Code LSB	95	8E	5E
127	Cyclical Redundancy Code MSB	F6	AA	EE
128	Module Product Type, Char #1	37	37	37
129	Module Product Type, Char #2	32	32	32
130	Module Product Type, Char #3	54	54	54
131	Module Product Type, Char #4	36	31	32
132	Module Product Type, Char #5	34	32	35
133	Module Product Type, Char #6	30	38	36
134	Module Product Type, Char #7	30	30	30
135	Module Product Type, Char #8	30	32	32
136	Module Product Type, Char #9	48	30	30
137	Module Product Type, Char #10	46	48	48
138	Module Product Type, Char #11	41	46	46
139	Module Product Type, Char #12	33	41	41
140	Module Product Type, Char #13	2E	33	33
141	Module Product Type, Char #14	37	2E	2E
142	Module Product Type, Char #15	41	37	37
143	Module Product Type, Char #16	20	41	41
144	Module Product Type, Char #17	20	20	20
145	Module Product Type, Char #18	20	20	20

Table 19 PC2–4200F–444 (cont'd)

Product Type		**HYS72T64000HFA–3.7–A**	**HYS72T128020HFA–3.7–A**	**HYS72T256020HFA–3.7–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–4200F–444**	**PC2–4200F–444**	**PC2–4200F–444**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
146	Module Revision Code	3x	4x	4x
147	Test Program Revision Code	xx	xx	xx
148	DRAM Manufacturers JEDEC ID Code LSB	80	80	80
149	DRAM Manufacturers JEDEC ID Code MSB	C1	C1	C1
150	informal AMB content revision tag (MSB)	00	00	00
151	informal AMB content revision tag (LSB)	10	10	10
152 - 175	Not used	00	00	00
176 - 255	Blank for customer use	FF	FF	FF

Table 20 PC2–5300F–555

Product Type		HYS72T64000HFN–3S–A	HYS72T128020HFN–3S–A	HYS72T256020HFN–3S–A
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300F–555**	**PC2–5300F–555**	**PC2–5300F–555**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	SPD Size CRC / Total / Used	92	92	92
1	SPD Revision	10	10	10
2	Key Byte / DRAM Device Type	09	09	09
3	Voltage Level of this Assembly	12	12	12
4	SDRAM Addressing	44	44	48
5	Module Physical Attributes	23	23	23
6	Module Type	07	07	07
7	Module Organization	09	11	10
8	Fine Timebase (FTB) Dividend and Divisor	00	00	00
9	Medium Timebase (MTB) Dividend	01	01	01
10	Medium Timebase (MTB) Divisor	04	04	04
11	$t_{CK.MIN}$ (min. SDRAM Cycle Time)	0C	0C	0C
12	$t_{CK.MAX}$ (max. SDRAM Cycle Time)	20	20	20
13	CAS Latencies Supported	33	33	33
14	$t_{CAS.MIN}$ (min. CAS Latency Time)	3C	3C	3C
15	Write Recovery Values Supported (WR)	42	42	42
16	$t_{WR.MIN}$ (Write Recovery Time)	3C	3C	3C
17	Write Latency Times Supported	42	42	42
18	Additive Latency Times Supported	40	40	40
19	$t_{RCD.MIN}$ (min. RAS# to CAS# Delay)	3C	3C	3C
20	$t_{RRD.MIN}$ (min. Row Active to Row Active Delay)	1E	1E	1E
21	$t_{RP.MIN}$ (min. Row Precharge Time)	3C	3C	3C
22	t_{RAS} and t_{RC} Extension	00	00	00
23	$t_{RAS.MIN}$ (min. Active to Precharge Time)	B4	B4	B4
24	$t_{RC.MIN}$ (min. Active to Active / Refresh Time)	E4	E4	E4
25	$t_{RFC.MIN}$ LSB (min. Refresh Recovery Time Delay)	A4	A4	A4

Table 20 PC2–5300F–555 (cont'd)

Product Type		**HYS72T64000HFN–3S–A**	**HYS72T128020HFN–3S–A**	**HYS72T256020HFN–3S–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300F–555**	**PC2–5300F–555**	**PC2–5300F–555**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
26	$t_{RFC.MIN}$ MSB (min. Refresh Recovery Time Delay)	01	01	01
27	$t_{WTR.MIN}$ (min. Internal Write to Read Cmd Delay)	1E	1E	1E
28	$t_{RTP.MIN}$ (min. Internal Read to Precharge Cmd Delay)	1E	1E	1E
29	Burst Lengths Supported	03	03	03
30	Terminations Supported	07	07	07
31	Drive Strength Supported	01	01	01
32	t_{REFI} (avg. SDRAM Refresh Period)	C2	C2	C2
33	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	53	53	53
34	Psi(T-A) DRAM	78	78	78
35	ΔT_0 (DT0) DRAM	48	48	48
36	ΔT_{2Q} (DT2Q) DRAM	2E	2E	2E
37	ΔT_{2P} (DT2P) DRAM	26	26	26
38	ΔT_{3N} (DT3N) DRAM	26	26	26
39	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W) DRAM	4A	4A	4A
40	ΔT_{5B} (DT5B) DRAM	20	20	20
41	ΔT_7 (DT7) DRAM	22	22	22
42 - 78	Not used	00	00	00
79	FBDIMM ODT Values	01	22	22
80	Not used	00	00	00
81	Channel Protocols Supported LSB	02	02	02
82	Channel Protocols Supported MSB	00	00	00
83	Back-to-Back Access Turnaround Time	10	10	10
84	AMB Read Access Delay for DDR2-800	56	56	58
85	AMB Read Access Delay for DDR2-667	40	40	42
86	AMB Read Access Delay for DDR2-533	36	36	38

Table 20 PC2–5300F–555 (cont'd)

Product Type		**HYS72T64000HFN–3S–A**	**HYS72T128020HFN–3S–A**	**HYS72T256020HFN–3S–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300F–555**	**PC2–5300F–555**	**PC2–5300F–555**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
87	Psi(T-A) AMB	30	30	30
88	ΔT_{Idle_0} (DT Idle_0) AMB	67	67	76
89	ΔT_{Idle_1} (DT Idle_1) AMB	7F	7F	8E
90	ΔT_{Idle_2} (DT Idle_2) AMB	6E	6E	73
91	ΔT_{Active_1} (DT Active_1) AMB	AA	AA	BB
92	ΔT_{Active_2} (DT Active_2) AMB	86	86	97
93	ΔT_{L0s} (DT L0s) AMB	00	00	00
94 - 97	Not used	00	00	00
98	AMB Junction Temperature Maximum (T_{jmax})	00	00	00
99	Category Byte	49	49	49
100	Not used	00	00	00
101	AMB Personality Bytes: Pre-initialization (1)	80	80	80
102	AMB Personality Bytes: Pre-initialization (2)	20	20	20
103	AMB Personality Bytes: Pre-initialization (3)	00	00	00
104	AMB Personality Bytes: Pre-initialization (4)	44	44	44
105	AMB Personality Bytes: Pre-initialization (5)	00	00	00
106	AMB Personality Bytes: Pre-initialization (6)	80	80	80
107	AMB Personality Bytes: Post-initialization (1)	40	40	40
108	AMB Personality Bytes: Post-initialization (2)	53	53	53
109	AMB Personality Bytes: Post-initialization (3)	00	00	00
110	AMB Personality Bytes: Post-initialization (4)	00	00	00
111	AMB Personality Bytes: Post-initialization (5)	65	65	65
112	AMB Personality Bytes: Post-initialization (6)	4C	4C	4C
113	AMB Personality Bytes: Post-initialization (7)	00	00	00
114	AMB Personality Bytes: Post-initialization (8)	05	05	05
115	AMB Manufacturers JEDEC ID Code LSB	80	80	80
116	AMB Manufacturers JEDEC ID Code MSB	89	89	89

Table 20 PC2–5300F–555 (cont'd)

Product Type		**HYS72T64000HFN–3S–A**	**HYS72T128020HFN–3S–A**	**HYS72T256020HFN–3S–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300F–555**	**PC2–5300F–555**	**PC2–5300F–555**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
117	DIMM Manufacturers JEDEC ID Code LSB	80	80	80
118	DIMM Manufacturers JEDEC ID Code MSB	C1	C1	C1
119	Module Manufacturing Location	xx	xx	xx
120	Module Manufacturing Date Year	xx	xx	xx
121	Module Manufacturing Date Week	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx
126	Cyclical Redundancy Code LSB	6D	51	FE
127	Cyclical Redundancy Code MSB	A6	AE	2B
128	Module Product Type, Char #1	37	37	37
129	Module Product Type, Char #2	32	32	32
130	Module Product Type, Char #3	54	54	54
131	Module Product Type, Char #4	36	31	32
132	Module Product Type, Char #5	34	32	35
133	Module Product Type, Char #6	30	38	36
134	Module Product Type, Char #7	30	30	30
135	Module Product Type, Char #8	30	32	32
136	Module Product Type, Char #9	48	30	30
137	Module Product Type, Char #10	46	48	48
138	Module Product Type, Char #11	4E	46	46
139	Module Product Type, Char #12	33	4E	4E
140	Module Product Type, Char #13	53	33	33
141	Module Product Type, Char #14	41	53	53
142	Module Product Type, Char #15	20	41	41
143	Module Product Type, Char #16	20	20	20
144	Module Product Type, Char #17	20	20	20
145	Module Product Type, Char #18	20	20	20

Table 20 PC2–5300F–555 (cont'd)

Product Type		**HYS72T64000HFN–3S–A**	**HYS72T128020HFN–3S–A**	**HYS72T256020HFN–3S–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300F–555**	**PC2–5300F–555**	**PC2–5300F–555**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
146	Module Revision Code	4x	4x	4x
147	Test Program Revision Code	xx	xx	xx
148	DRAM Manufacturers JEDEC ID Code LSB	80	80	80
149	DRAM Manufacturers JEDEC ID Code MSB	C1	C1	C1
150	informal AMB content revision tag (MSB)	00	00	00
151	informal AMB content revision tag (LSB)	08	08	08
152 - 175	Not used	00	00	00
176 - 255	Blank for customer use	FF	FF	FF

Table 21 PC2–5300F–555

Product Type		HYS72T64000HFA–3S–A	HYS72T128020HFA–3S–A	HYS72T256020HFA–3S–A
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300F–555**	**PC2–5300F–555**	**PC2–5300F–555**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
0	SPD Size CRC / Total / Used	92	92	92
1	SPD Revision	10	10	10
2	Key Byte / DRAM Device Type	09	09	09
3	Voltage Level of this Assembly	12	12	12
4	SDRAM Addressing	44	44	48
5	Module Physical Attributes	23	23	23
6	Module Type	07	07	07
7	Module Organization	09	11	10
8	Fine Timebase (FTB) Dividend and Divisor	00	00	00
9	Medium Timebase (MTB) Dividend	01	01	01
10	Medium Timebase (MTB) Divisor	04	04	04
11	$t_{CK.MIN}$ (min. SDRAM Cycle Time)	0C	0C	0C
12	$t_{CK.MAX}$ (max. SDRAM Cycle Time)	20	20	20
13	CAS Latencies Supported	33	33	33
14	$t_{CAS.MIN}$ (min. CAS Latency Time)	3C	3C	3C
15	Write Recovery Values Supported (WR)	42	42	42
16	$t_{WR.MIN}$ (Write Recovery Time)	3C	3C	3C
17	Write Latency Times Supported	42	42	42
18	Additive Latency Times Supported	40	40	40
19	$t_{RCD.MIN}$ (min. RAS# to CAS# Delay)	3C	3C	3C
20	$t_{RRD.MIN}$ (min. Row Active to Row Active Delay)	1E	1E	1E
21	$t_{RP.MIN}$ (min. Row Precharge Time)	3C	3C	3C
22	t_{RAS} and t_{RC} Extension	00	00	00
23	$t_{RAS.MIN}$ (min. Active to Precharge Time)	B4	B4	B4
24	$t_{RC.MIN}$ (min. Active to Active / Refresh Time)	F0	F0	F0
25	$t_{RFC.MIN}$ LSB (min. Refresh Recovery Time Delay)	A4	A4	A4

Table 21 PC2–5300F–555 (cont'd)

Product Type		**HYS72T64000HFA–3S–A**	**HYS72T128020HFA–3S–A**	**HYS72T256020HFA–3S–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300F–555**	**PC2–5300F–555**	**PC2–5300F–555**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
26	$t_{RFC.MIN}$ MSB (min. Refresh Recovery Time Delay)	01	01	01
27	$t_{WTR.MIN}$ (min. Internal Write to Read Cmd Delay)	1E	1E	1E
28	$t_{RTP.MIN}$ (min. Internal Read to Precharge Cmd Delay)	1E	1E	1E
29	Burst Lengths Supported	03	03	03
30	Terminations Supported	07	07	07
31	Drive Strength Supported	01	01	01
32	t_{REFI} (avg. SDRAM Refresh Period)	C2	C2	C2
33	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	53	53	53
34	Psi(T-A) DRAM	78	78	78
35	ΔT_0 (DT0) DRAM	48	48	48
36	ΔT_{2Q} (DT2Q) DRAM	2E	2E	2E
37	ΔT_{2P} (DT2P) DRAM	26	26	26
38	ΔT_{3N} (DT3N) DRAM	26	26	26
39	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W) DRAM	4A	4A	4A
40	ΔT_{5B} (DT5B) DRAM	20	20	20
41	ΔT_7 (DT7) DRAM	22	22	22
42 - 78	Not used	00	00	00
79	FBDIMM ODT Values	01	22	22
80	Not used	00	00	00
81	Channel Protocols Supported LSB	02	02	02
82	Channel Protocols Supported MSB	00	00	00
83	Back-to-Back Access Turnaround Time	20	28	28
84	AMB Read Access Delay for DDR2-800	74	74	74
85	AMB Read Access Delay for DDR2-667	62	62	62
86	AMB Read Access Delay for DDR2-533	56	56	56

Table 21 PC2–5300F–555 (cont'd)

Product Type		**HYS72T64000HFA–3S–A**	**HYS72T128020HFA–3S–A**	**HYS72T256020HFA–3S–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300F–555**	**PC2–5300F–555**	**PC2–5300F–555**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
87	Psi(T-A) AMB	26	26	26
88	ΔT_{Idle_0} (DT Idle_0) AMB	3F	3F	3F
89	ΔT_{Idle_1} (DT Idle_1) AMB	50	50	50
90	ΔT_{Idle_2} (DT Idle_2) AMB	54	54	54
91	ΔT_{Active_1} (DT Active_1) AMB	57	57	57
92	ΔT_{Active_2} (DT Active_2) AMB	53	53	53
93	ΔT_{L0s} (DT L0s) AMB	00	00	00
94 - 97	Not used	00	00	00
98	AMB Junction Temperature Maximum (T_{jmax})	15	15	15
99	Category Byte	49	49	49
100	Not used	00	00	00
101	AMB Personality Bytes: Pre-initialization (1)	15	15	15
102	AMB Personality Bytes: Pre-initialization (2)	00	00	00
103	AMB Personality Bytes: Pre-initialization (3)	03	03	03
104	AMB Personality Bytes: Pre-initialization (4)	00	00	00
105	AMB Personality Bytes: Pre-initialization (5)	00	00	00
106	AMB Personality Bytes: Pre-initialization (6)	00	00	00
107	AMB Personality Bytes: Post-initialization (1)	00	00	00
108	AMB Personality Bytes: Post-initialization (2)	00	00	00
109	AMB Personality Bytes: Post-initialization (3)	00	00	00
110	AMB Personality Bytes: Post-initialization (4)	C0	C0	C0
111	AMB Personality Bytes: Post-initialization (5)	FF	FF	FF
112	AMB Personality Bytes: Post-initialization (6)	FF	FF	FF
113	AMB Personality Bytes: Post-initialization (7)	FF	FF	FF
114	AMB Personality Bytes: Post-initialization (8)	01	01	01
115	AMB Manufacturers JEDEC ID Code LSB	80	80	80
116	AMB Manufacturers JEDEC ID Code MSB	C1	C1	C1

Table 21 PC2–5300F–555 (cont'd)

Product Type		**HYS72T64000HFA–3S–A**	**HYS72T128020HFA–3S–A**	**HYS72T256020HFA–3S–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300F–555**	**PC2–5300F–555**	**PC2–5300F–555**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
117	DIMM Manufacturers JEDEC ID Code LSB	80	80	80
118	DIMM Manufacturers JEDEC ID Code MSB	C1	C1	C1
119	Module Manufacturing Location	xx	xx	xx
120	Module Manufacturing Date Year	xx	xx	xx
121	Module Manufacturing Date Week	xx	xx	xx
122 - 125	Module Serial Number	xx	xx	xx
126	Cyclical Redundancy Code LSB	E6	76	A6
127	Cyclical Redundancy Code MSB	A2	0B	4F
128	Module Product Type, Char #1	37	37	37
129	Module Product Type, Char #2	32	32	32
130	Module Product Type, Char #3	54	54	54
131	Module Product Type, Char #4	36	31	32
132	Module Product Type, Char #5	34	32	35
133	Module Product Type, Char #6	30	38	36
134	Module Product Type, Char #7	30	30	30
135	Module Product Type, Char #8	30	32	32
136	Module Product Type, Char #9	48	30	30
137	Module Product Type, Char #10	46	48	48
138	Module Product Type, Char #11	41	46	46
139	Module Product Type, Char #12	33	41	41
140	Module Product Type, Char #13	53	33	33
141	Module Product Type, Char #14	41	53	53
142	Module Product Type, Char #15	20	41	41
143	Module Product Type, Char #16	20	20	20
144	Module Product Type, Char #17	20	20	20
145	Module Product Type, Char #18	20	20	20

Table 21 PC2–5300F–555 (cont'd)

Product Type		**HYS72T64000HFA–3S–A**	**HYS72T128020HFA–3S–A**	**HYS72T256020HFA–3S–A**
Organization		**512MB**	**1 GByte**	**2 GByte**
		×72	**×72**	**×72**
		1 Rank (×8)	**2 Ranks (×8)**	**2 Ranks (×4)**
Label Code		**PC2–5300F–555**	**PC2–5300F–555**	**PC2–5300F–555**
JEDEC SPD Revision		**Rev. 1**	**Rev. 1**	**Rev. 1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**
146	Module Revision Code	5x	5x	5x
147	Test Program Revision Code	xx	xx	xx
148	DRAM Manufacturers JEDEC ID Code LSB	80	80	80
149	DRAM Manufacturers JEDEC ID Code MSB	C1	C1	C1
150	informal AMB content revision tag (MSB)	00	00	00
151	informal AMB content revision tag (LSB)	10	10	10
152 - 175	Not used	00	00	00
176 - 255	Blank for customer use	FF	FF	FF

12 Package Outline

All Components are surface mounted on one or both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR2 SDRAM signals. Bypass capacitors for DDR2 SDRAM devices are located near the device power pins. The AMB device in the center of the DIMM has a metal Heat Sink. The FB-DIMM mechanical outlines are consistent with JEDEC MO-256.

Table 22 Raw Card Reference

JEDEC Raw Card	Infineon PCB		Dimensions			
			Width [mm]	Height [mm]	Thickness [mm]	Notes
R/C A	L-DIM-240-21	Figure 16	133.35	30.35	7.1	1)
R/C B	L-DIM-240-22	Figure 17	133.35	30.35	7.1	1)
R/C H	L-DIM-240-25	Figure 18	133.35	30.35	7.1	1)

1) Thickness includes Infineon Heat Sink. Some early production modules with Jedec Heatspreader may be thicker up to 8.2mm.

Attention: Heat Sink heat up during operation. When unplugging a DIMM from a system direct skin contact should be avoided until the Heat Sink has reached room temperature.

Attention: The Heat Sink is mechanically loaded. Do not remove. Removal of the clip may cause injuries.

Attention: Any mechanical stress on the Heat Sink should be avoided. Touching the Heat Sink while plugging or unplugging the module may permanently damage the DIMM.

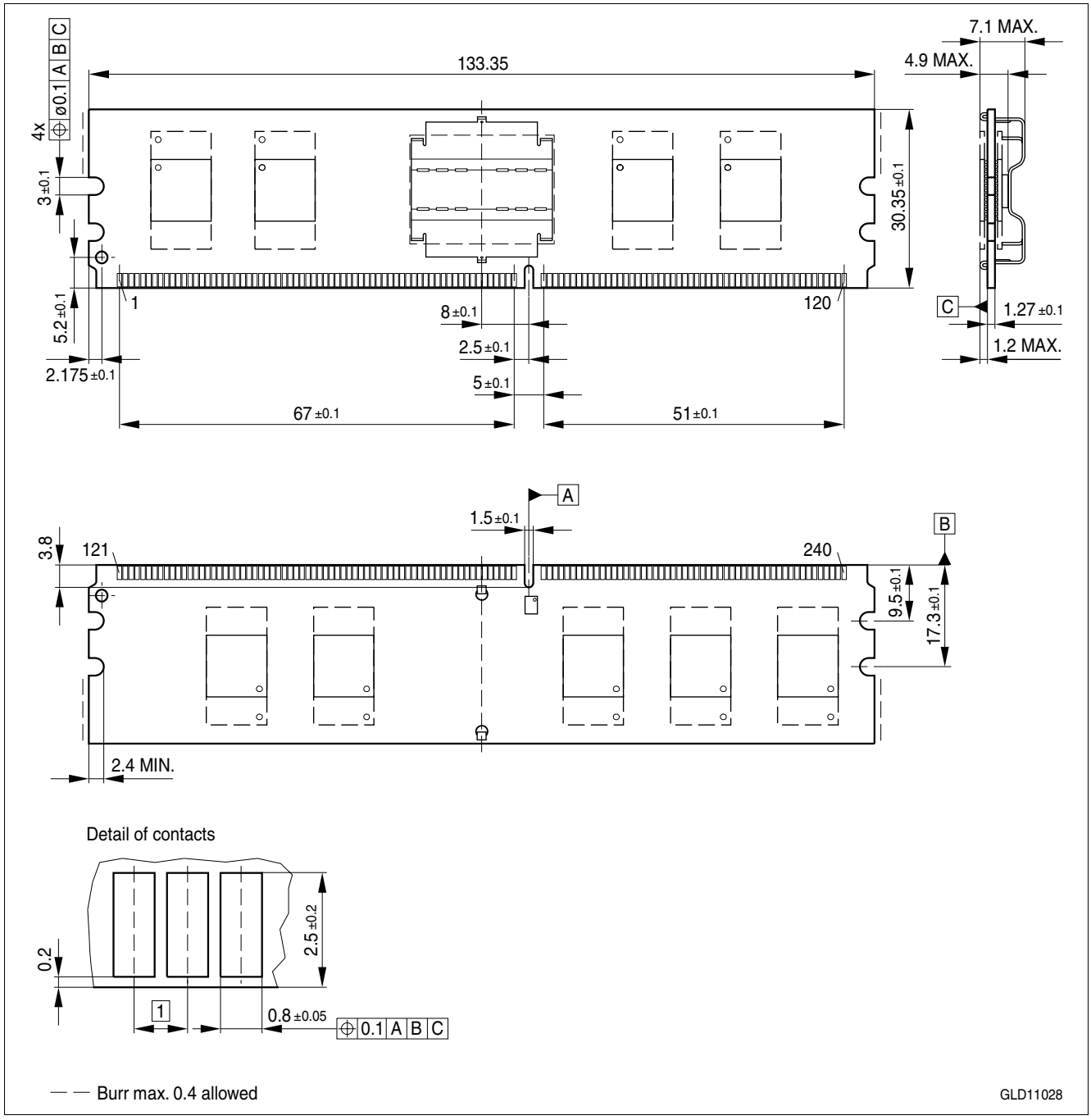

Figure 16 Package Outline L-DIM-240-21

Note: Please contact your sales or marketing representative for more details on package dimensions.

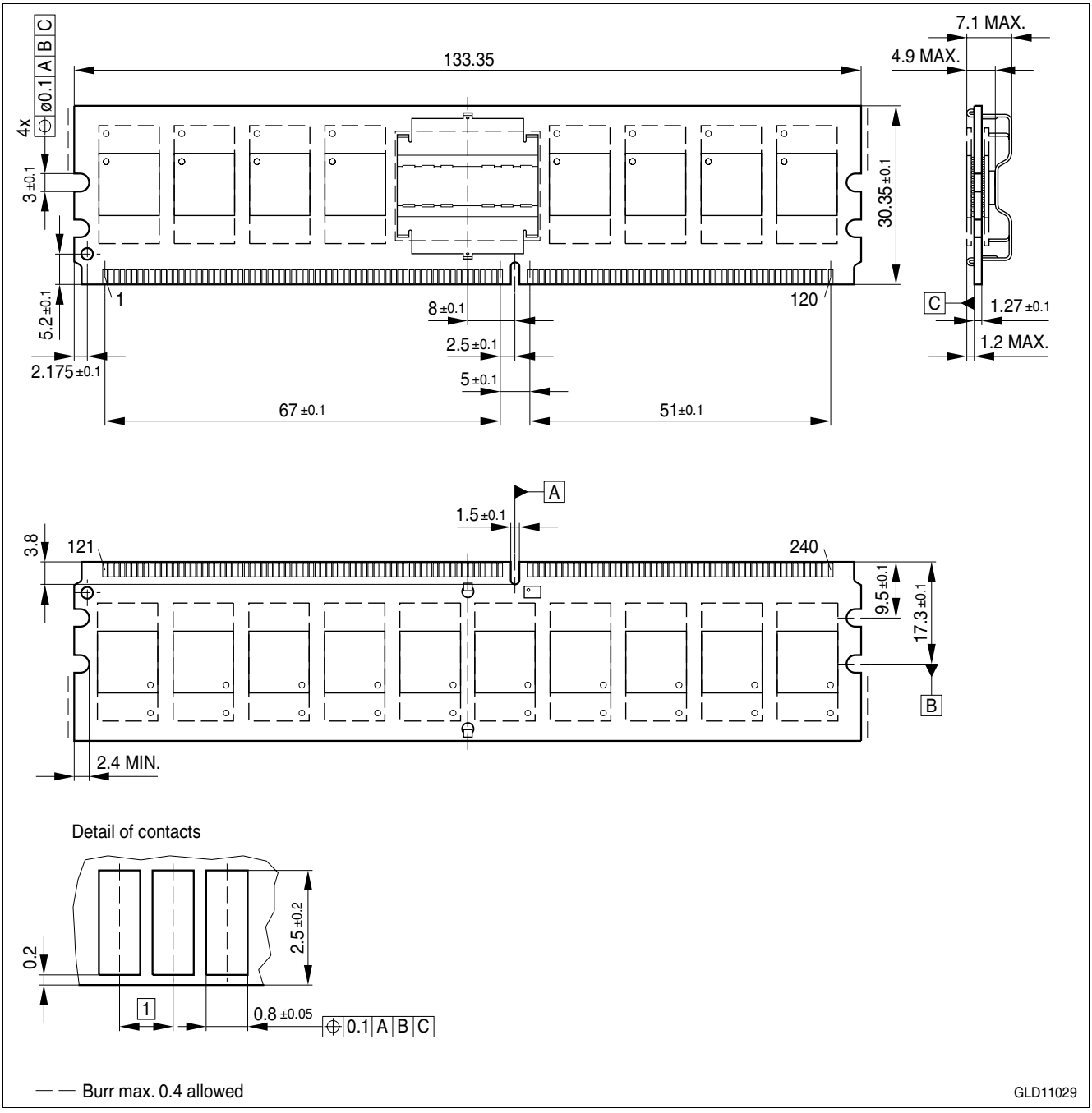

Figure 17 Package Outline L-DIM-240-22

Note: Please contact your sales or marketing representative for more details on package dimensions.

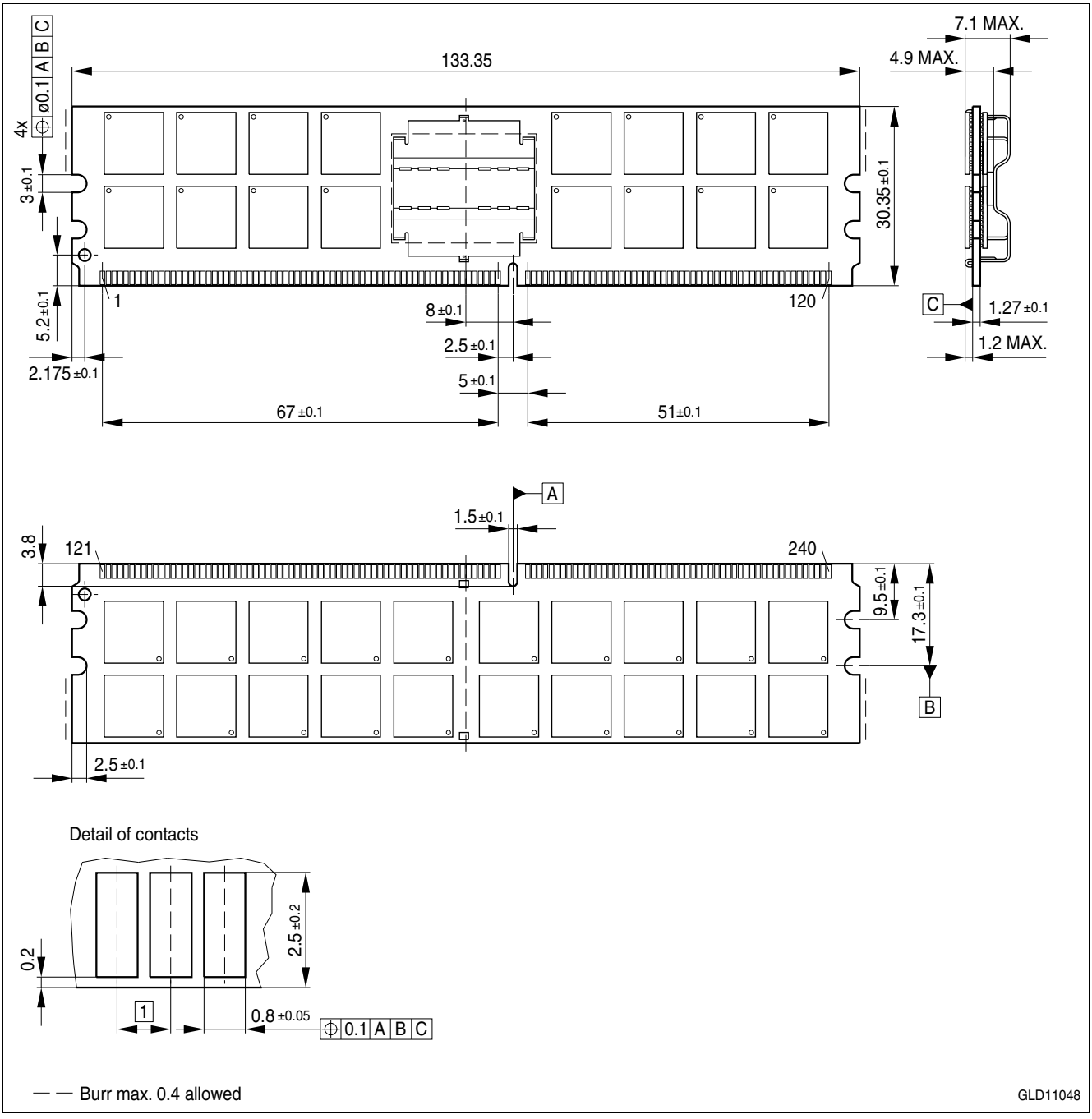

Figure 18 Package Outline L-DIM-240-25

Note: Please contact your sales or marketing representative for more details on package dimensions.

13 DDR2 Nomencature

Table 23 Nomenclature Fields and Examples

Example for	Field Number										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Micro-DIMM	HYS	64	T	64	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512	16		0	A	C	–5	

Table 24 DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
		F	**F**ully Buffered
10	Speed Grade	–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

Table 25 DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–2.5	DDR2-800 6-6-6
		–3	DDR2-667 4-4-4
		–3S	DDR2-667 5-5-5
		–3.7	DDR2-533 4-4-4
		–5	DDR2-400 3-3-3

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