ILLUMINANT 北極光企業有限公司

PRODUCT SPECIFICATION FOR LCM

CUSTOMER:	
MODEL NO:	I2420-6OMN4823A
ACCEPTED BY:	

APPROVED BY:	CHECKED BY:	ORGANIZED BY:
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■Approval for Specifications Only

□Approval for Specifications and Sample

Note: 1. Version of Specifications : 1

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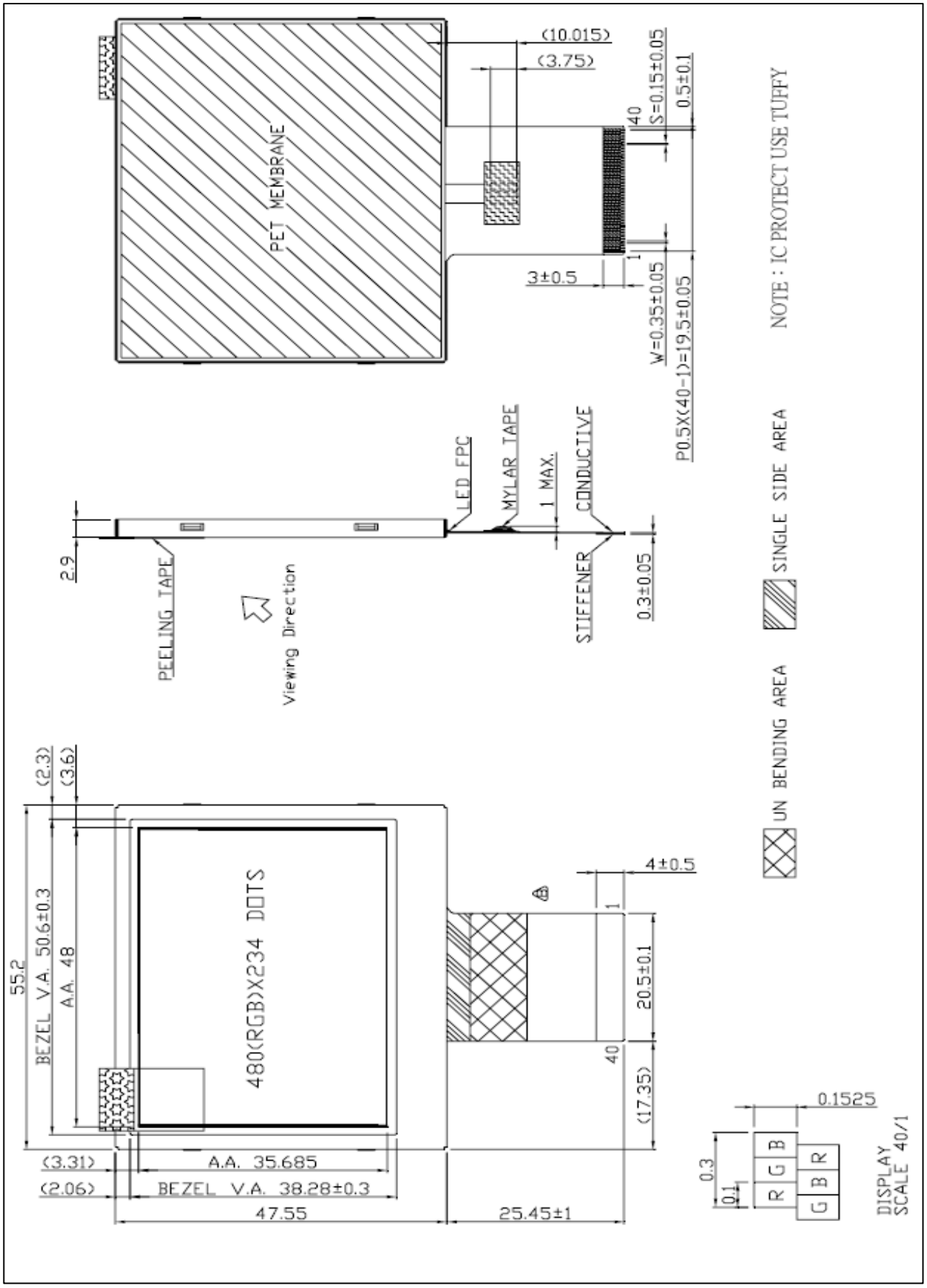
Version	Date	Contents
1	08/08/25	Initial Release

CONTENTS

1. Mechanical Specification

Item	Standard Value	Unit
Display Size	2.36	inch
Module Dimension	55.20(W)*47.55(H)*2.90(D)	mm
Active Area	48.0(W)*35.69(H)	mm
Number of Dots	480(RGB)*234 Delta Type	Dot
Pixel Pitch	0.1(W)mm*0.1525(H)	mm
LCD Type	Normal White	-
Viewing Direction	6H	-
Approx. Weight	TBD	g
Various Color Display	16.7M	
Brightness	250	cd/m2
Backlight Type	1-LED parallel	
Backlight Color	White	



2. Absolute Maximum Ratings

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Logic	V_{DD}	-0.5		+7.0	V	
Input Voltage	Vin	-0.3		V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	-	+60	℃	-
Storage Temperature	T_{ST}	-25	-	+80	℃	-

*NOTE: Based on Vss=0V.

3. Electrical Characteristics

Item		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
Supply Voltage		VDD	3.0	3.3	3.6	V	
		VDDIO	3.0	3.3	3.6		Note 3-1
Supply Voltage for Gate Driver	H Level	VGH	17	18.5	19.5	V	Note 3-1
	L Level	VGL	-7.5	-6	-4.5	V	
Digital Input Voltage	H Level	V_{IH}	VDDIO-0.4-	-	VDDIO	V	
	L Level	V_{IL}	0	-	VDDIO+0.4	V	
Digital Output Voltage	H Level	V_{OH}	0.7VDDIO	-	VDDIO	V	
	L Level	V_{OL}	0	-	0.3VDDIO	V	
VCOM		V_{LCOMAC}	-	+4.5	+5.0	Vp-p	AC Component of VCOM
		V_{LCOMDC}	-	0.72	-	V	Note 3-2

Note 3-1 : VGH and VGL supplied by internal setup circuit.
Note 3-2 : Adjust VCDC to make the flicker level be minimum. Suggest R5 setting data 0x7d.

Current Consumption

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current	IDD	VDD=+3.3V	9	13.2	mA	-

4. Optical Characteristics

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note1,2,3.

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
Response Time		T_R	$\theta = 0$	-	6	12	ms	Note 4,6
		T_F		-	15	30	ms	
Contrast Ratio		CR	At optimized viewing angle	-	400	-	-	Note 5,6
Viewing Angle	Hor.	θ_R	CR≧10	40	45	-	Degree	Note 6,7
		θ_L		40	45	-		
	Ver.	φ_H		10	15	-		
		φ_L		30	35	-		
Transmission		Y_L	$\theta = 0$	-	6.5	-	%	Note 8
White Chromaticity Shift		X	$\theta = 0$	0.26	0.31	0.36	-	
		Y		0.28	0.33	0.38		
Brightness			$\theta = 0$	200	250	-	Cd/m^2	

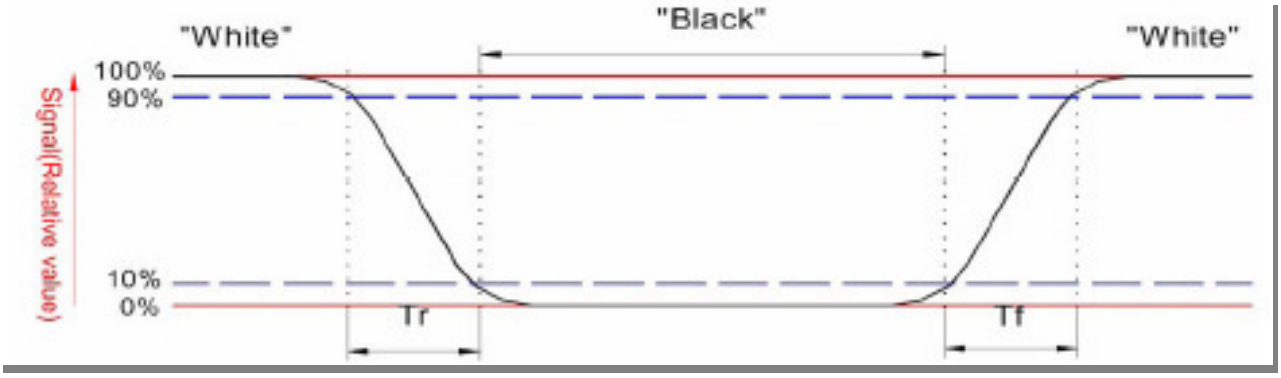
Note 1 : Ambient temperature =25℃

Note 2 : To be measured in the dark room.

Note 3 : To be measured on the center area of panel with a field angle of 1℃ by Topcon luminance meter BM-7, after 10minutes operation.

Note 4 : Definition of Response time

The output signals of photo detector are measured when the input signals are changed from " black" to "white" (falling time) and from "white" to "black" (rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5 : Definition of Contrast Ratio

Contrast Ratio is calculated with the following formula.

$$\text{Contrast Ratio (CR)} = \frac{\text{Brightness measured when LCD is at “white state”}}{\text{Brightness measured when LCD is at “black state”}}$$

Note 6 : White Vi=Viso -/+1.5V

Black Vi=Viso ± 2.0V

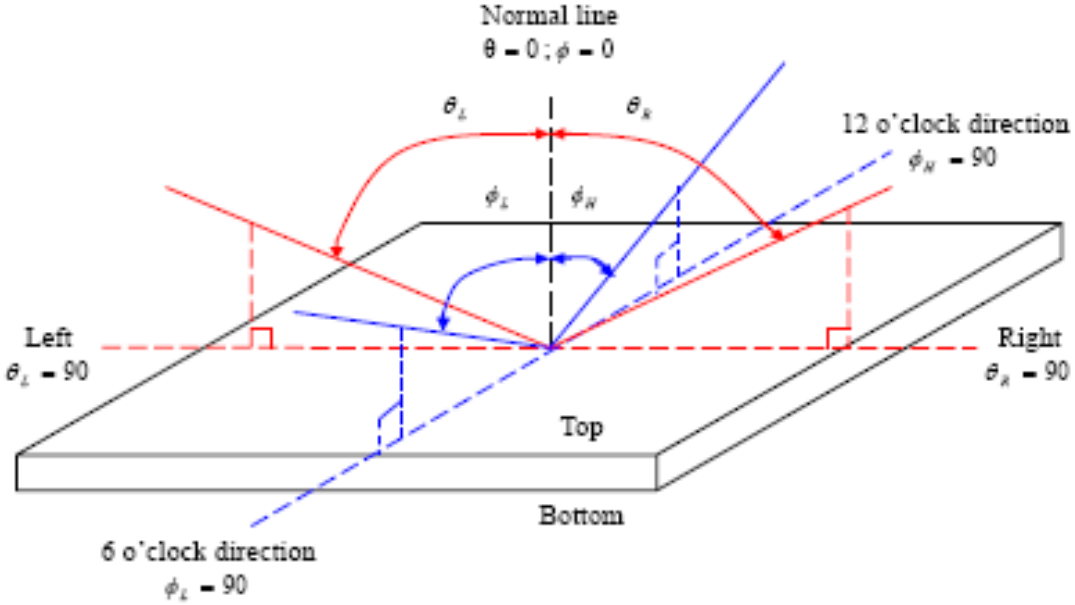
“±”means that the analog input signal swings in phase with COM signal.

“-/+” means that the analog input signal swings out of phase with COM signal.

Vsio : The analog input voltage when transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7 : Definition of Viewing Angle

Refer to the figure as below.



Note 8 : Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

5. Interface

Pin	Symbol	I/O	Function	Remark
1	VCOM	I	Common Electrode Driving Voltage	Note 5-1
2	NC	--	-	
3	VGL	O	Power Supply for Gate off Voltage	Note 5-2
4	C4P	C	Pins to Connect Capacitance for Power Circuitry	
5	C4N	C	Pins to Connect Capacitance for Power Circuitry	
6	VGH	O	Power Supply for Gate on Voltage	
7	FRP	O	Frame Polarity Output for VCOM	
8	VCAC	O	Define the Amplitude of the VCOM swing	
9	VDD_25V	O	Intermediate Voltage for Charge Pump. Please Connect the Capacitor between VDD_25V and VSS	
10	C3P	C	Pins to Connect Capacitance for Power Circuitry	
11	C3N	C	Pins to Connect Capacitance for Power Circuitry	
12	VDD3	O	Charge-pump Circuit Reference Voltage. Please connect the Capacitor between VCIOUT and VSS	
13	C2P	C	Pins to Connect Capacitance for Power Circuitry	
14	C2N	C	Pins to Connect Capacitance for Power Circuitry	
15	VDDA	O	Power Supply Voltage of Source Driver Liquid Crystal Drive Circuit. Please Connect the Capacitor between DDVDH and VSS.	
16	C1P	C	Pins to Connect Capacitance for Power Circuitry	
17	C1N	C	Pins to Connect Capacitance for Power Circuitry	

18	GND	P	Charge Pump Power GND	
19	VDD	P	Charge Pump Power VDD	Note 5-3
20	DRV	O	Gate Signal for the Power Transistor of the Boost Converter	Note 5-4
21	VLED	P	Supply Voltage for LED Backlight	
22	NC	--	Dummy	
23	FB	I	Main Boost Regulator Feedback Input	Note 5-5
24	NC	--	Dummy	
25	AGND	P	Ground Terminal in the Logic Circuit	
26	VDDIO	P	Power Supply Terminal in the Logic Circuit	Note 5-3
27	CSB	I	Serial Communication Chip Select	
28	SDA	I/O	Serial Communication Data Input	
29	SCL	I	Serial Communication Clock Input	
30	HSYNC	I	Horizontal Sync Input	Note 5-6
31	VSYNC	I	Vertical Sync Input	Note 5-7
32	DCLK	I	Clock Input	Note 5-8
33	D7	I	Data Input : MSB	
34	D6	I	Data Input	
35	D5	I	Data Input	
36	D4	I	Data Input	
37	D3	I	Data Input	
38	D2	I	Data Input	
39	D1	I	Data Input	
40	D0	I	Data Input	

***I** : Input **O**: Output **P** : Power **I/O** : Serial Communication Data Input/Output **C** : Capacitor*

Note 5-1 : VCOM=+5.0 Vp-p.(Typ.)
Note 5-2 : The external capacitor is required on those pins as following.

Symbol	Part Standard		Notes
	Capacitance	Voltage	
VDD3	1 to 2.2uF	16V over	
VDDA	1 to 2.2uF	16V over	
VGH	1 to 2.2uF	25V over	
VGL	1 to 2.2uF	25V over	
VCAC	1 to 2.2uF	16V over	
C1P, C1N	1 to 4.7uF	16V over	
C2P, C2N	1 to 4.7uF	16V over	
C3P, C3N	1 to 4.7uF	16V over	
C4P, C4N	1 to 4.7uF	16V over	
FRP	1 to 2.2uF	16V over	
VDD_25V	1 to 2.2uF	16V over	

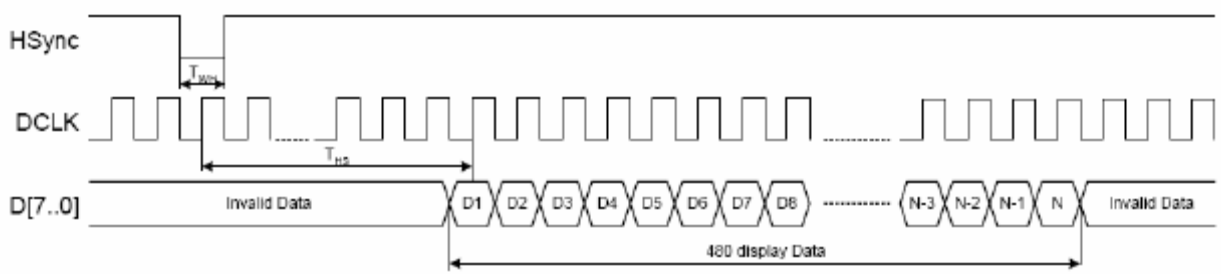
Note 5-3 : VDD, VDDIO=+3.3V(Typ.)
Note 5-4 : Outputs the control signal of switching regulator for LED, Duty cycle varies according to FB input voltage.
Note 5-5 : Feedback signal of switching for LED, It controls DRV output duty cycle with 0.6V input level sense.
Note 5-6 : Horizontal sync signal, it is a “L” active signal.
Note 5-7 : Vertical Sync signal, it is a “Low” active signal.
Note 5-8 : Dot clock signal for RGB interface, timing for data loading defined at rising edge.

6. AC Characteristics

AC Characteristics (VDD=3.3V, AND=GND=0V, TOPR=-30℃ to =85℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK pulse duty	T_{CW}		40	50	60	%
Delay between Hsync and DCLK	Thc		-	-	1.0	DCLK
Hsync width	Twh		1.0	-	-	DCLK
Hsync period	Th		60	63.56	67	us
Vsync setup time	Tvst		12	-	-	ns
Vsync hold time	Tvhd		12	-	-	ns
Hsync set-up time	Thst		12	-	-	ns
Hsync hold time	Thhd		12	-	-	ns
Data set-up time	Tdsu	D00~D07 to DCLK	12	-	-	ns
Data hold time	Tdhd	D00~D07 to DCLK	12	-	-	ns
Vsync to 1st gate output	Tstv	Sel≠"111";By HDL[3..0] settings	6	13	21	Th
CCIR V to 1st gate output	Tstv	Sel="111" NTCS (PAL=0); By HDL[3..0] settings	14	21	29	Th
CCIR V to 1st gate output	Tstv	Sel="111" PAL=1; By HDL[3..0] settings	20	27	35	Th
SD output stable time	Tst	30mV precision; CL=6.75pF, R=3.62K	-	25	30	us
GD output delay time	Tgd	CL=17.6pF, R=1.29K	-	900	1500	ns
GD output rise and fall time	Tgst	CL=17.6pF, R=1.29K 10% to 90%	-	900	1500	ns
Serial communication						
Serial clock period	Tsck		320	-	-	ns
Serial clock duty cycle	Tscw		40	50	60	%
Serial clock width low/high	Tssw		120			ns
Serial data setup time	Tist		120			ns
Serial data hold time	Tihd		120			ns
CSB setup time	Tcst		120			ns
CSB data hold time	Tchd		120			ns
Chip select distinguish	Tcd		1			us
Delay between CSB and Vsync	Tcv		1			us

6.1. Raw Data Mode

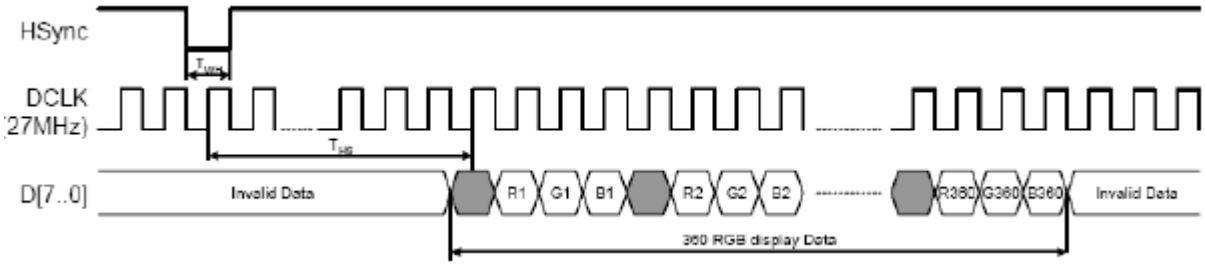


(VDDIO=1.8V~VDD, VDD=+3.0 to +3.6V, VSS=0V)

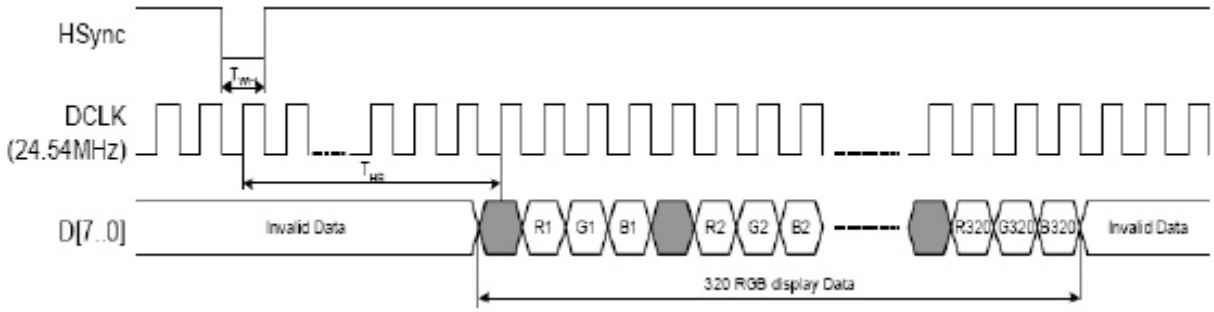
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DCLK frequency	Fclk		-	9.7	-	MHz
DCLK period	Tcph		-	103	-	Ns
Delay from Hsync to Source Output	Thso		-	56	-	DCLK
Delay from Hsync to Gate Output	Thgo		-	45	-	DCLK
Delay from Hsync to Gate Output off	Thgz		-	19	-	DCLK
Delay from Hsync to Q1H	Thq		-	39	-	DCLK
Delay from Hsync to FRP	Thf			59	-	DCLK
Delay from Hsync to 1st data input	Ths	Function of DDL[5..0] settings	68	100	131	DCLK
DC converter osc. Frequency	Fosc	Fclk/32	-	303.1	-	KHz

6.2. Serial RGB Mode

A. 360 Mode (27Mhz) Time Specifications



B. 320 Mode (24.545Mhz) Time Specifications

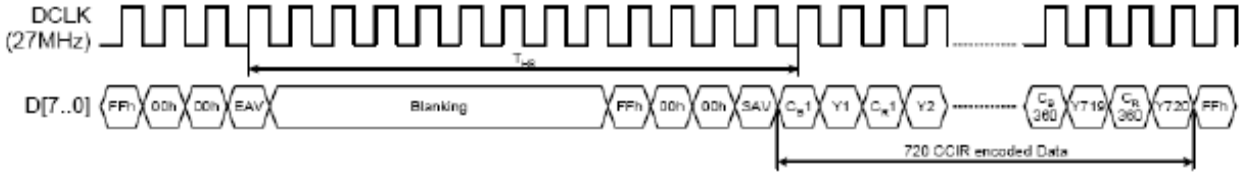


(VDDIO=1.8V~VDD, VDD=+3.0 to +3.6V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DCLK frequency	Fclk		-	24.54/ 27	-	MHz
DCLK cycle time	Tcph		-	40/37	-	ns
Delay from Hsync to Source Output	Thso		-	143	-	DCLK
Delay from Hsync to Gate Output	Thgo		-	113	-	DCLK
Delay from Hsync to Gate Output off	Thgz		-	48	-	DCLK
Delay from Hsync to Q1H	Thq		-	100	-	DCLK
Delay from Hsync to FRP	Thf			143		DCLK
Delay from Hsync to 1st data input	Ths	Function of DDL[5..0] settings	220	252	283	DCLK
DC converter osc. Frequency	Fosc	Fclk/64=383.4kHz /421.9kHz		383.4/ 421.9		KHz

6.3 CCIR Mode (CCIR 656)

Timing Characteristic



(VDDIO=1.8V~VDD, VDD=+3.0 to +3.6V, VSS=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DCLK frequency	Fclk		-	27	-	MHz
DCLK cycle time	Tcph		-	37	-	ns
CLK pulse duty	Tcw		40	50	60	%
Delay from EAV to Source Output	Thso		-	143	-	DCLK
Delay from EAV to Gate Output	Thgo		-	113	-	DCLK
Delay from EAV to Gate Output off	Thgz		-	48	-	DCLK
Delay from EAV to Q1H	Thq		-	100	-	DCLK
Delay from EAV to FRP	Thf			143		DCLK
Delay from EAV to 1st data input	Ths	Function of DDL[5..0] settings	241	273	304	DCLK
DC converter osc. Frequency	Fosc	Fclk/64		421.9		KHz

6.4 Internal Register Description

There is a total of 16 registers each containing several parameters. For a detailed description of the parameters refer the Register summary.

The serial register has read (1) / write (0) function. D [15:12] are the register address, D [11] defined the read or write mode and D [10:0] are the data. Register 14 is a read only register and is used for chip identification. At power-on, the default values specified for each parameter (in Register summary) are taken. All data, except S0 D[3:2], are validated on the negative edge of Vsync. In 3-wire register, GRB clear registers to default value except GRB value. If less than 16-bit data are read during the CS low time period the data is cancelled.

Register Summary

Table 1: Serial register table

Reg	ADRESS				CONTENT											
N°	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
S0	0	0	0	0	R/W	-	-	-	-				GRB (1)	STB (1)	SHDB (0)	SHCB (1)
S1	0	0	0	1	R/W	-	-	-	GAMAH (000)			PDTY (00)		FBV (100)		
S2	0	0	1	0	R/W	-	-			000				DITHB (0)	PFON (0)	1
S3	0	0	1	1	R/W	-	-	-	-	0	0	0	CONST (1000)			
S4	0	1	0	0	R/W	-	-	-	-	-			FPOL (0)	0	UD (1)	SHL (1)
S5	0	1	0	1	R/W	-			VDC EN(0)	VCOMDC (100000)						
S6	0	1	1	0	R/W	-	-	-	-	-		PALM (0)	PAL (0)	SEL (000)		
S7	0	1	1	1	R/W	-	-	-	-	BRADJ (1000000)						
S8	1	0	0	0	R/W	-	-					DDL (00000)				
S10	1	0	1	0	R/W	-	-	-	-	-		FRAD (00)	HDL (0000)			
S12	1	1	0	0	R/W	-	-	-	-					VCSL (110)		
S14	1	1	1	0	R/W	-	-	-				GAMSEL(0)	0	0	1	1

Register Description

S0 Settings

R0: System settings

Adress	Bit	Description		Default
0000	[3:0]	Bit3(GRB)	Global reset	xxxx_1101b
		Bit2(STB)	Standby mode setting	
		Bit1(SHDB)	DC-DC converter shutdown setting	
		Bit0(SHCB)	Charge Pump shutdown setting	

Bit3	GRB Function
0	The controller is resets, the charge pump and DC-DC is off. Reset all register to default value.
1	Normal operation. (Default)
Bit2	**STB Function**
0	T-CON, source driver and DC-DC converter are off. All outputs are High-Z.
1	Normal operation. (Default)
Bit1	**SHDB Function**
0	DC-DC converter is off. (Default)
1	DC-DC converter is on. DC-DC controls by STB and power on/off sequence.
Bit0	**SHCB Function**
0	Charge Pump converter is off.
1	Charge Pump converter is on. (Default) Charge Pump controls by STB and power on/off sequence.

S1 Settings

Adress	Bit	Description		Default
0001	[7:0]	Bit[7:5](GAMAH)	Internal GAMAH voltage generator setting for Gamma	0110_0100b
		Bit[4:3](PDTY)	PWM1 duty control for DC2DC converter	
		Bit[2:0](FBV)	FB1 reference level adjustment for DC2DC converter	

Bit[7:5]	GAMAH Level	Unit
000	4.5	V
001	4.6	
010	4.7	
011	4.8	
100	4.9	
101	5.0	
110	5.1	
111	5.2	

Bit[4:3]	PTDY Duty	Unit
00	75	%
01	55	
10	60	
11	65	

Bit[2:0]	FB Vref Level	Unit
000	0.4	V
001	0.45	
010	0.5	
011	0.55	
100	0.6	
101	0.65	
110	0.7	
111	0.75	

S2 Settings

Adress	Bit	Description		Default
0010	[5:0]	Bit2(DITH)	Dithering algorithm selection	xx00_0001b

Bit2	DITHB Function
0	Dithering on. 8-bit resolution. (Default)
1	Dithering off. 6-bit resolution (last 2bits of input data truncated)
Bit1	**PFON Function**
0	PFON=”L”, Pre-filter off
1	PFON=”H”, Pre-filter on Remark : Disable this function In RAW DATA MODE mode

S3 Settings

Adress	Bit	Description		Default
0011	[3:0]	Bit[3:0](CONST)	RGB constant level adjustment (0.125/Step)	x000_1000b

Bit[3:0]	RGB constrast
0x0	0
0x8	1.00
0xF	1.875

S4 Settings

Adress	Bit	Description		Default
0011	[3:0]	Bit3(FPOL)	FRP source driver polarity inversion polarity inversion selection	xxxx_0011b
		Bit1(UD)	Vertical shift direction selection	
		Bit0(SHL)	Horizontal shift direction selection	

Bit3	FPOL Function
0	FRP=0 when positive polarity FRP=1 when negative polarity (Default)
1	FRP=0 when positive polarity FRP=1 when negative polarity
Bit1	**UD Function**
0	Scan down : First line=G241=>G240=>…=>G1=>Last line=G0
1	Scan up : First line=G0=>G1=>…=>G240=>Last line=G241 (Default)
Bit0	**SHL Function**
0	Shift left; First data=S480=>S479=>…=>S2=>Last data=S1
1	Shift right; First data=S1=>S2=>…=>S479=>Last data=S480 (Default)

S5 Settings

Adress	Bit	Description		Default
0101	[6:0]	Bit6(VDCEN)	Setting FRP output to add DC level	x010_0000b
		Bit[5:0](VCOMDC)	VCOM DC Level adjustment	

Bit6	VDCEN Function
0	VDCEN=”L”, without VCOM DC Level
1	VDCEN=”H”, with VCOM DC Level

Bit[5:0]	VCOMDC Setting Table	Unit
0x0	0.192	V
0x20	0.704	
0x3F	1.2	

Note : S5 setting step must be enter the test mode, then start set the S5 register and data.

Interval VCOMDC voltage can adjust by the S5 data.

S6 Settings

Adress	Bit	Description		Default
0110	[4:0]	Bit4(PALM)	Select skip method in PAL mode interface	xxx0_0000b
		Bit3(PAL)	PAL/NTSC selection	
		Bit[2:0] (SEL)	Select Raw data/SERIAL RGB MODE path and input data format When SEL[2:0] select different, AC timing also different.	

Bit4	PALM Function
0	PAL 280 active lines. (Default)
1	PAL 280 active lines.

Bit3	PAL Function
0	NTSC Input format (240 active line). (Default)
1	PAL Input format.

Bit[2:0]	SEL Function	Operating Frequency
000	Select RAW DATA MODE path, special data format(DDX) input	9.7MHz
001	Select SERIAL MODE path, normal data format(DIN) input	24.54MHz
010	Select SERIAL MODE path, normal data format(DIN) input	27MHz
111	Select CCIR_656 path, format(YcbCr) input.	27MHz

S7 Settings

Adress	Bit	Description		Default
0111	[6:0]	Bit[6:0](BRADJ)	Brightness Level Adjustment	x100_0000b

Bit[6:0]	Brightness Level
0x00	-256
0x40	0
0x7F	+256

S8 Settings

Adress	Bit	Description		Default
1000	[4:0]	Bit[4:0](DDL)	Horizontal Data start delay selection	xxx0_0000b

Bit[4:0]	DDL Function	
	No.	Unit
00000	0	DCLK
00001	+1	
00010	+2	
00011	+3	
00100	+4	
00101	+5	
00110	+6	
00111	+7	
01000	+8	
01001	+9	
01010	+10	
01011	+11	
01100	+12	
01101	+13	
01110	+14	
01111	+15	
10000	-1	
10001	-2	
10010	-3	
10011	-4	

10100	-5	
10101	-6	
10110	-7	
10111	-8	
11000	-9	
11001	-10	
11010	-11	
11011	-12	
11100	-13	
11101	-14	
11110	-15	
11111	-16	

S10 Settings

Adress	Bit	Description		Default
1010	[5:0]	Bit[5:4](FRAD)	Odd frame or Even frame advance select	xx00_0000b
		Bit[3:0](HDL)	Select the Data delay timing	

Bit[5:4]	FRAD Function
00	Odd/Even frame Tstv are the same
01	Even frame Tstv=HDL setting+1, unit=H
10	Odd frame Tstv=HDL setting+1, unit=H Remark: This function is enable in SEL[2:0]=”111”mode

S12 Settings

Adress	Bit	Description		Default
1100	[2:0]	Bit[2:0](VCSL)	VCAC Level Selection	xxxx_x101b

Bit[2:0]	VCAC Level	Unit
000	4.5	V
001	4.6	
010	4.7	
011	4.8	
100	4.9	
101	5.0	
110	5.1	
111	5.2	

S14 Settings

Adress	Bit	Description		Default
1110	[4:0]	Bit4(GAMSEL)	Gamma R Table selection	xxx0_0011b

Bit4	GAMSEL Function
0	GAMSEL=”L” select GAM1 value
1	GAMSEL=”H” select GAM2 value

6.5 CPU Serial Transfer Timing Wave Form :

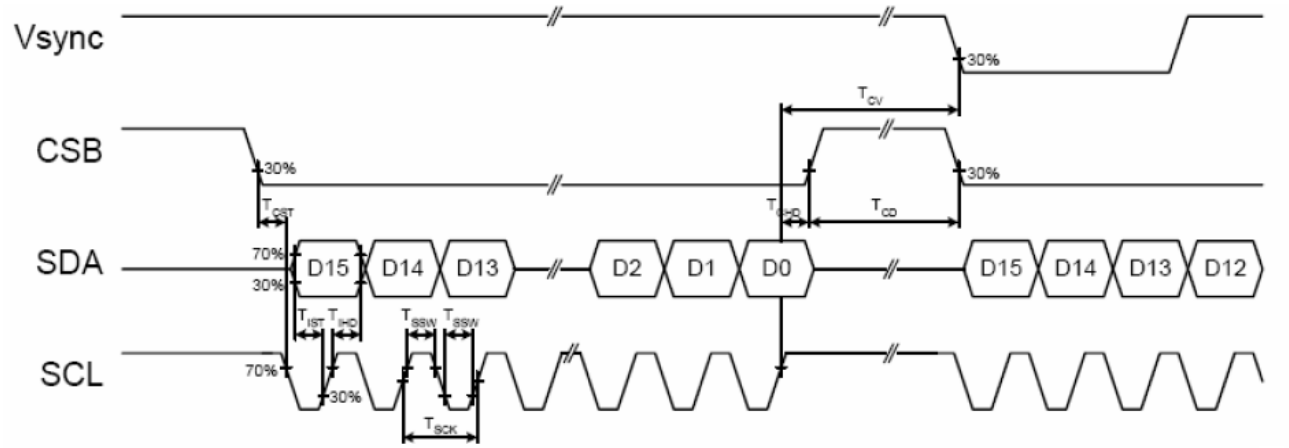
The register setting is done by 3-interface of chip select signal (CS_X), serial clock signal (SCL), and data input signal (SDA) from CPU etc.

When CS_X=L, it is recognized forwarding to this chip, and takes the SDA signal by rising edge about the SCL signal. The forwarding ends with CS_X=H and only the data of the register corresponding to LSI holds. The forwarding bits is 16-bits and 3bits of the head becomes an address cord and 13 bits after those becomes register setting data. It is forwarded to the turn of LSB from MSB.

If less than 16-bits of SCL are input while CS_X=L, the transferred data is ignored.

If 16-bits or more of SCL are input while CS_X=L, the first 16-bits of transferred data before the rising edge of CS_X pulse are valid data.

After power-on reset is released, the command of the initial operation setting etc. can be forwarded. The register setting can be received in the standby mode.



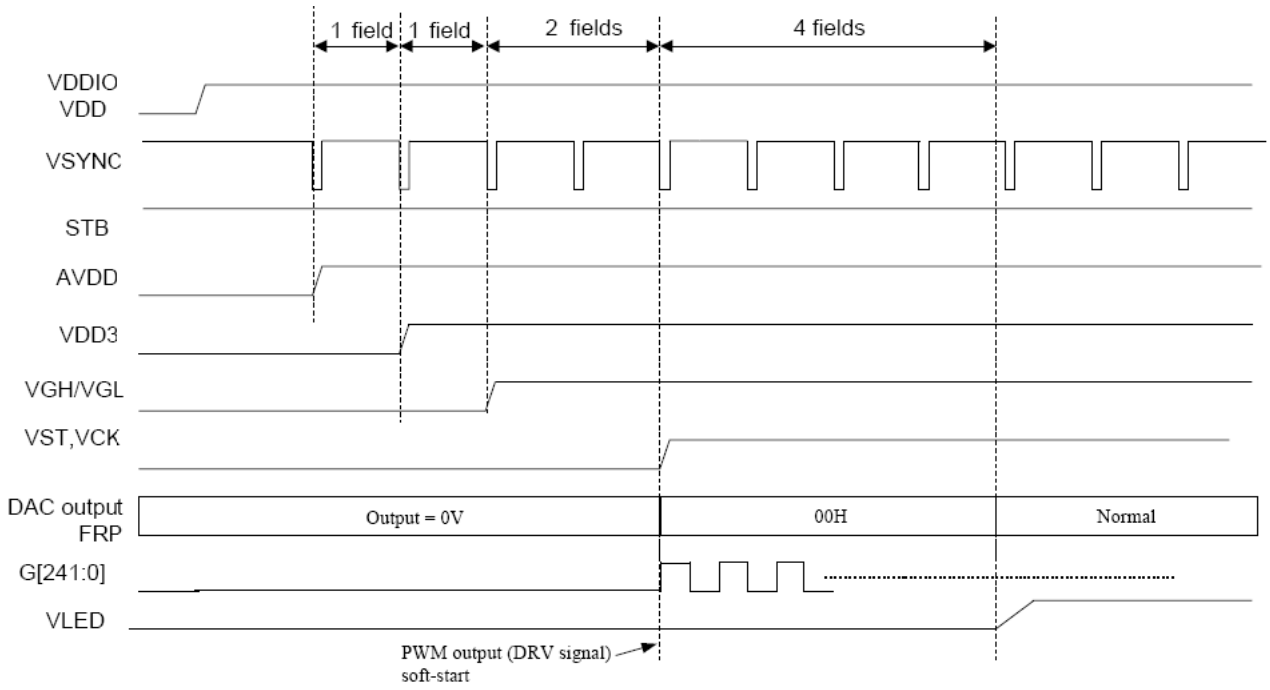
(VDD=+3.0 to +3.6V, VSS=0V)

Serial Communication						
Serial clock period	Tsck		320	-	-	ns
Serial clock duty cycle	Tscw		40	50	60	%
Serial clock width low/high	Tssw		120			ns
Serial data setup time	Tist		120			ns
Serial data hold time	Tihd		120			ns
CSB setup time	Tcst		120			ns
CSB data hold time	Tchd		120			ns
Chip select distinguish	Tcd		1			us
Delay between CSB and Vsync	Tcv		1			us

7. Power On/Off Sequence

Special care should be taken that the large current may cause a permanent damage to the LSI when voltage is applied to the LCD drive power supply terminals in the condition that the logic power supply terminals are floating.

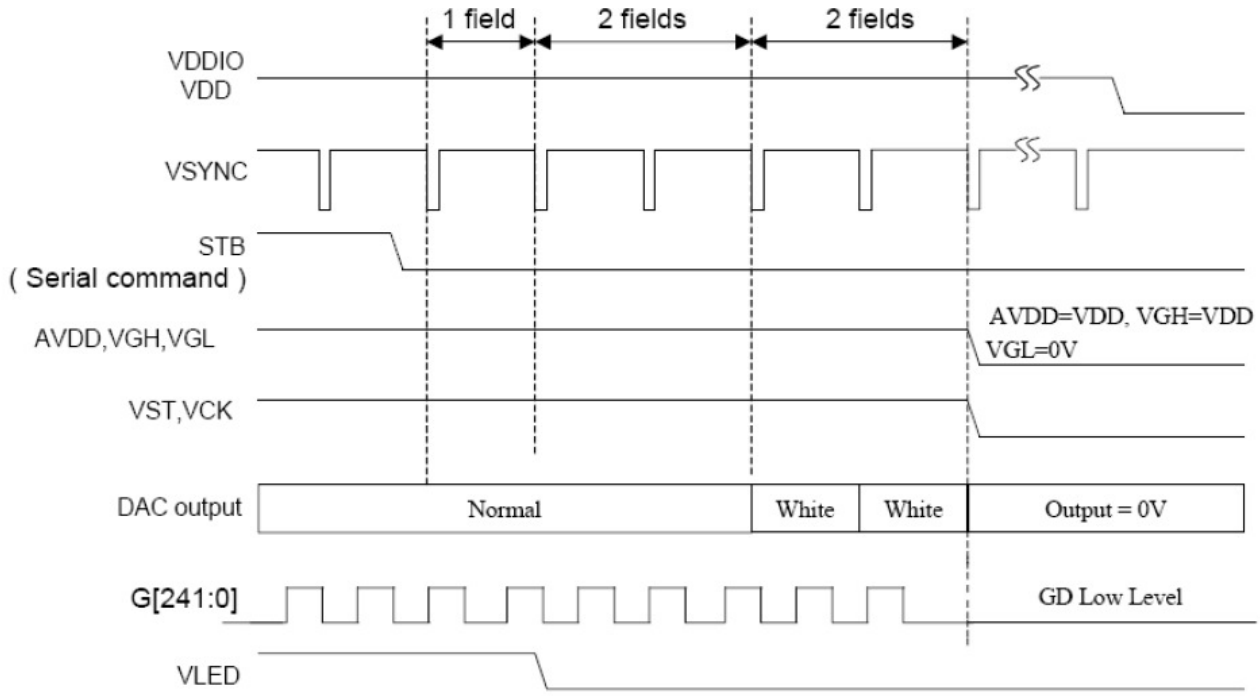
The following sequences are recommended from the power supply ON to the image display.



Note

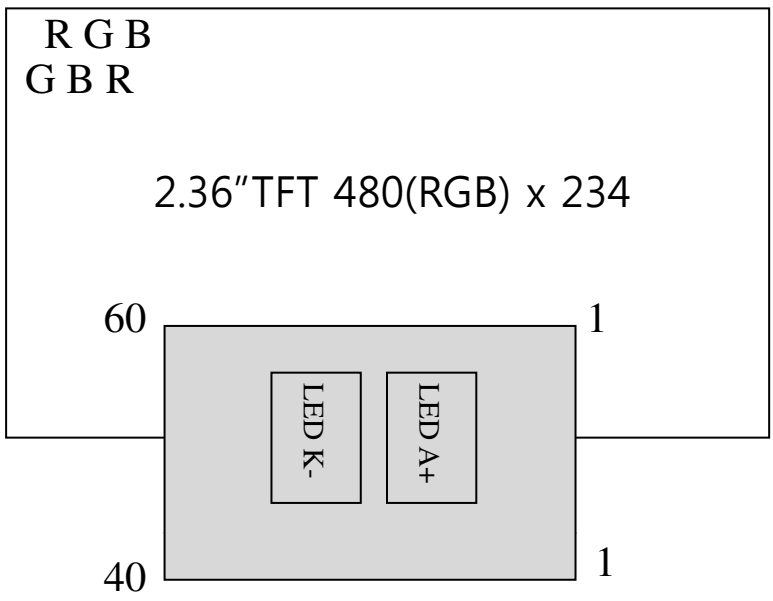
1. The software reset command by the GRB register is not cared about even if it doesn't send it because the initialization operation is done with LSI internal power-on reset circuit when the power supply is turned on.
2. The setting of SHDB register and GRB register is sent at the same time and not cared about. However, LED is lighted after the image data over 3 frames is received.

The following sequences are recommended from the image display to the power supply OFF.



Note

If the SHDB register is not set as 0 before stopping image data (DOTCLK), since the transistor of an external backlight LED control circuit may become being in ON state with as and may generate heat, please be sure to set SHDB as 0.

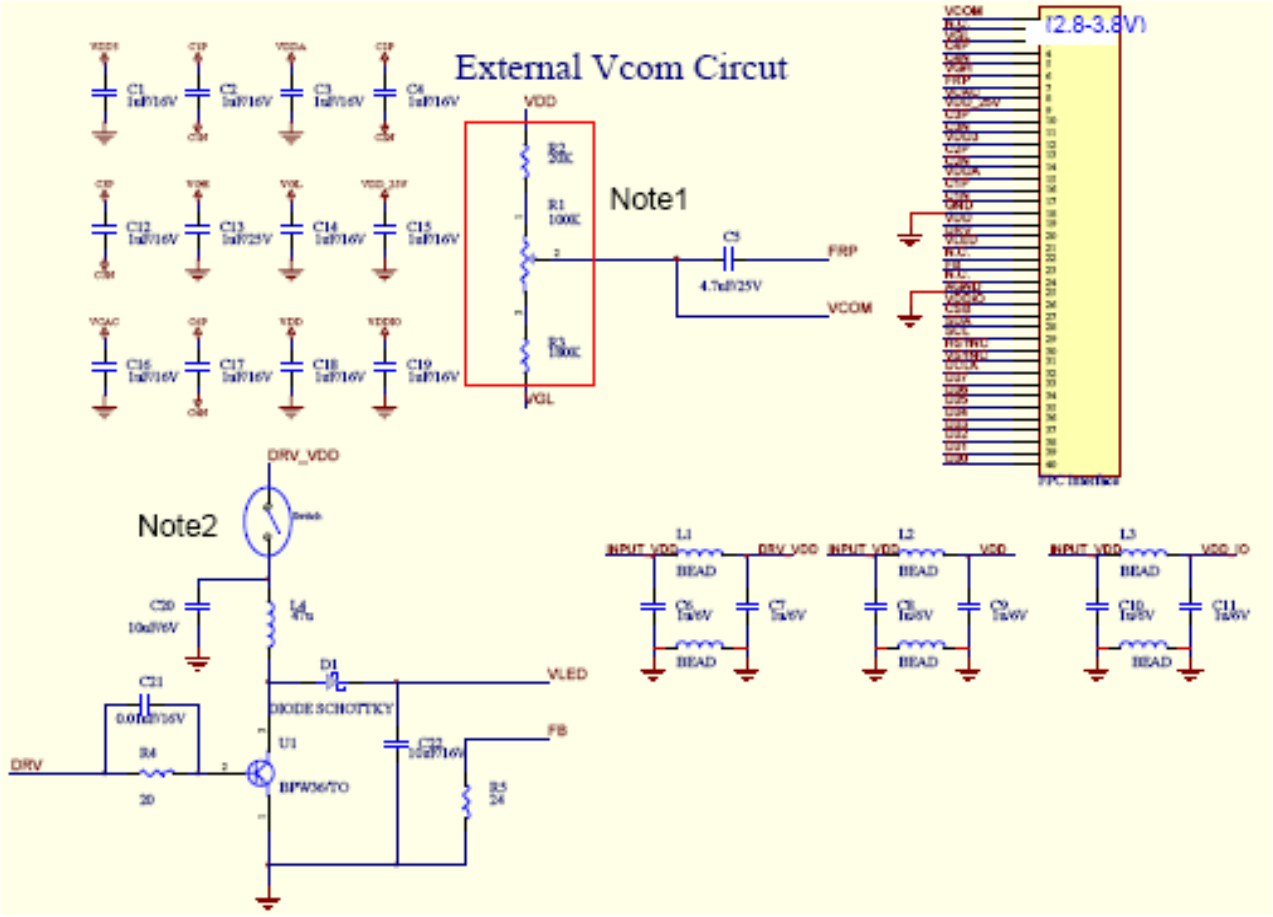


8. Block Diagram

8.1 Display Color and Gray Scale Reference

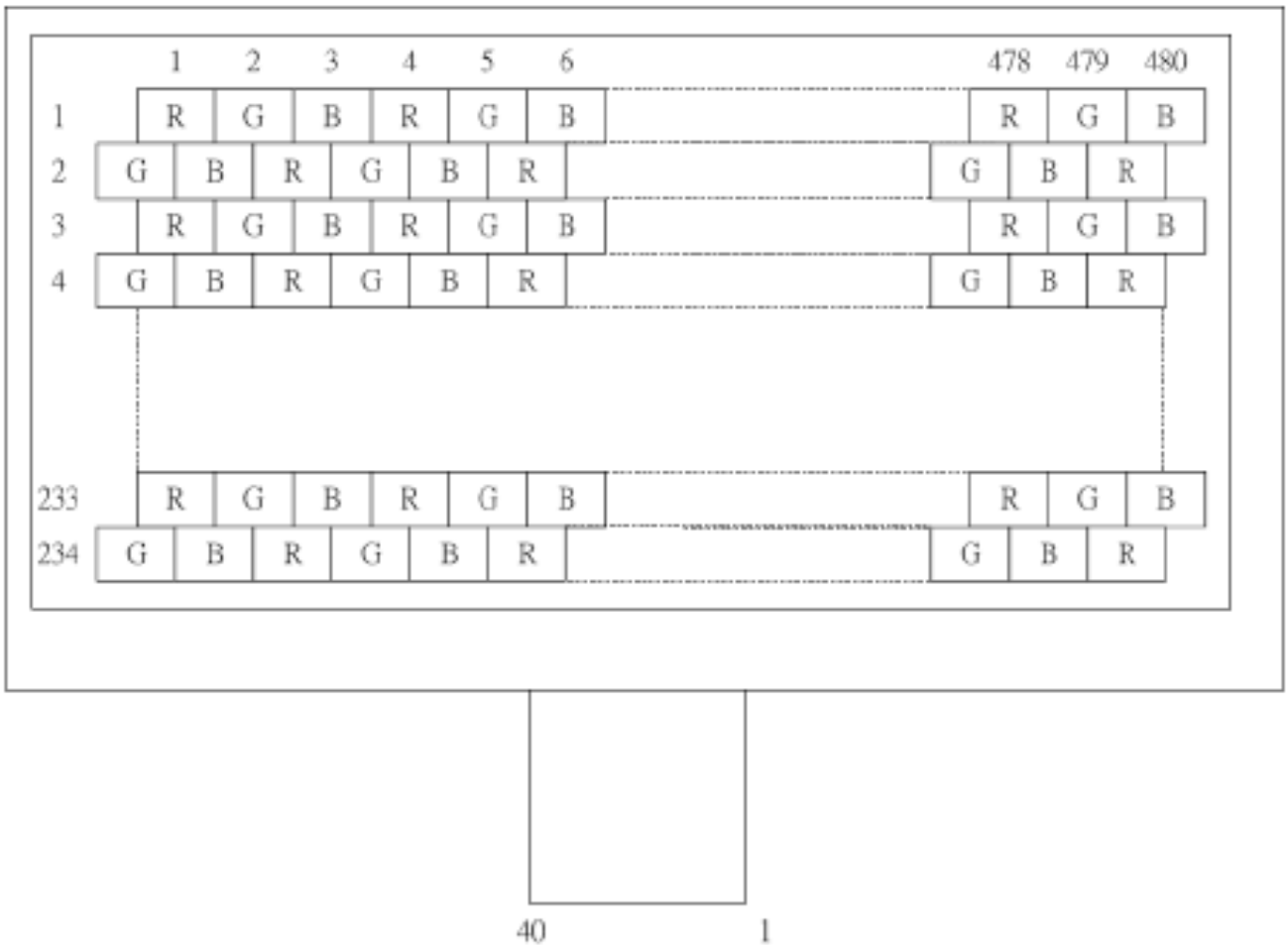
Color		Input Color Data																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

8.2 Reference Application Note



Note
1. When use the internal VcomDC adjust, the resistors R1’R2’R3 must be open.
2. When backlight is turn off, the power supply for backlight driver must be open.

8.3 Pixel Arrangement and Input Pin Connector No.



9. Backlight

9.1 Standard Lamp Styles (Edge Lighting Type):

The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:

9.2 The Main Advantages of the LED Backlight are as Following:

The brightness of the backlight can simply be adjusted.
By a resistor or a potentiometer.

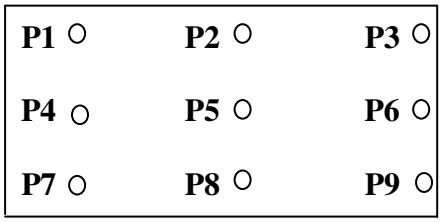
9.3 Data About LED Backlight:

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power Consumption	VLED	2.8	-	3.8	V	
LED Current	I_F	-	25	-	mA	
LCM Brightness		200	250	-	Cd/m^2	

NOTE:

1.Test Instrument : BM-7 (Distance=500mm ; Field =1°)
2.Light Source : LED * 1(White)
3.Conditions : I_F=25mA, VLED(Typ.)=3.3V
4.Uniformity : (Min. Brightness / Max. Brightness) *100%
5.Uniformity ≧ 70%

9.4 Measured Method:



(Effective spatial Distribution)
Hole Diameter±1ø ; 1 to 9per Position Measured Luminous

10. Reliability

10.1 MTTF

The LCD module shall be designed to meet a minimum MTTF value of 50,000 hours with normal condition. (25°C in the room without sunlight; not include lifetime of backlight).

10.2 Tests

No.	Item	Condition	Criterion
1	High Temperature Operating	+60°C 240hrs	。No defect of operational function in room temperature are allowable(23±5°C). 。Leakage current should be below double of initial value.
2	Low Temperature Operating	0°C 240hrs	
3	High Temperature Non-Operating	+80°C 240hrs	
4	Low Temperature Non-Operating	-25°C 240hrs	
5	High Temperature / Humidity Non-Operating	60°C ; 90%RH ; 240hrs	
6	Temperature Shock Operating	-30°C ←→ 80°C (30min) (5min) (30min) 100 Cycles	
7	Electro-Static Discharge	HBM : ±2kv	

Note 1: Test after 24 hours in room temperature(23±5°C).

Note 2: The sampling above is individually for each reliability testing condition.

Note 3: The color fading of polarizing filter should not care.

Note 4: All of the reliability testing chamber above, is using D.I. water.(Min value:1.0 MΩ-cm)

Note 5: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.