ILLUMINANT 北極光企業有限公司

PRODUCT SPECIFICATION FOR LCM

CUSTOMER:	
MODEL NO:	I2501-6IGN9624B
ACCEPTED BY:	

APPROVED BY:	CHECKED BY:	ORGANIZED BY:
LCM產品部 2009.01.25 Long	LCM產品部 2009.01.25 Vicky	LCM產品部 2009.01.25 Vicky

■ **Approval for Specifications Only**

□ **Approval for Specifications and Sample**

Note: 1. Version of Specifications : 1

2. Others: Rohs Compliment

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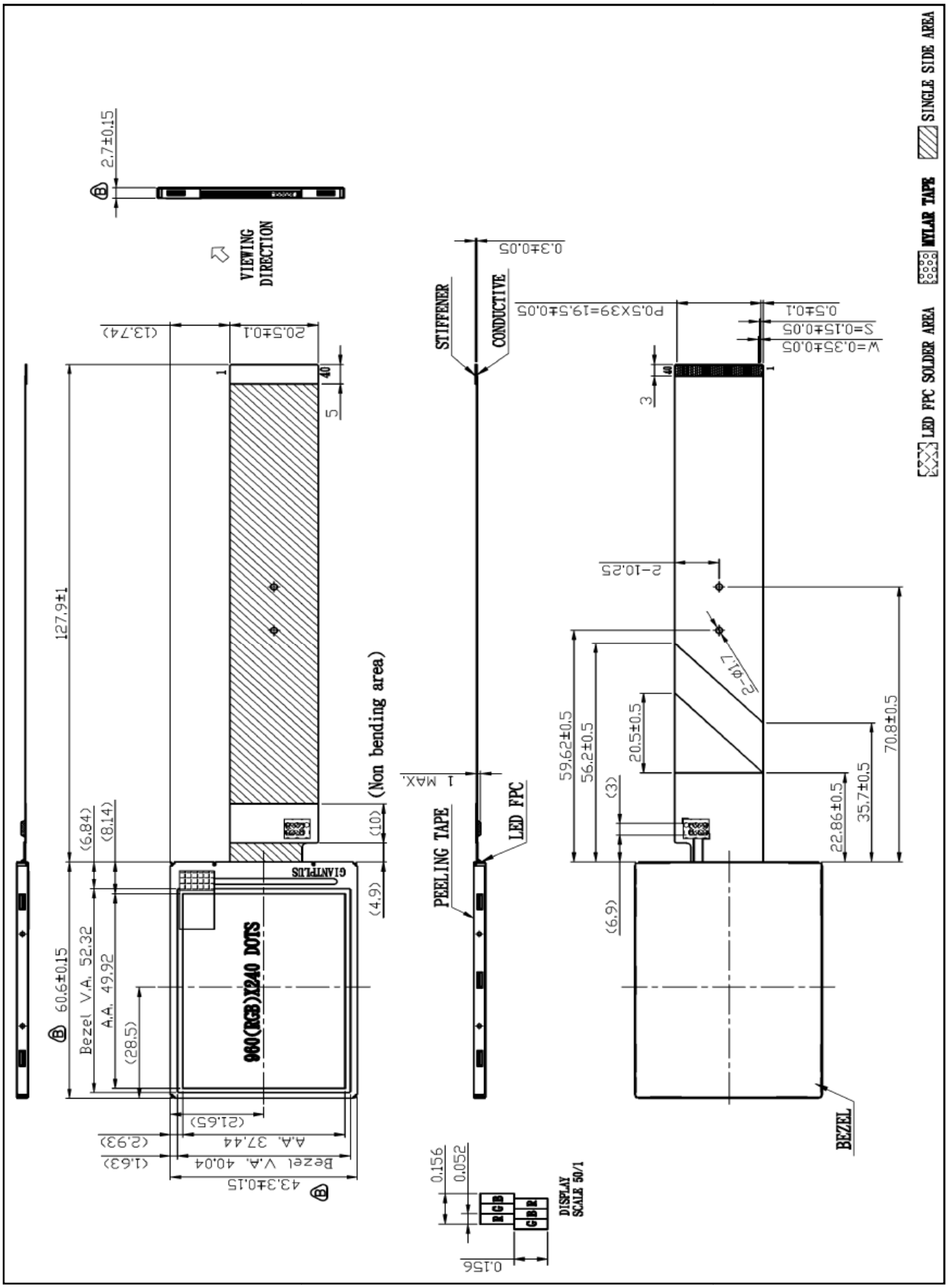
Version	Date	Contents
1	09/01/25	Initial Release

CONTENTS

1. Mechanical Specification

Item	Standard Value	Unit
Display Size	2.5	inch
Module Dimension	43.3(W)*60.6(H)*2.70(D)	mm
Active Area	37.44(W)*49.92(H)	mm
Number of Dots	960(RGB)*240 Delta Type	Dot
Surface Treatment	Clear	-
Display Mode	Transmissive Type, Positive Mode	-
Viewing Direction	6H	-
Approx. Weight	TBD	g
Various Color Display	16.7M Color	-
Brightness	250	cd/m^2
Backlight Type	2-LED Serial	
Backlight Color	White	



2. Maximum Ratings

If the operating condition exceeds the following absolute maximum ratings, the TFT LCD module may be damaged permanently. PGND=VSS=0V, Ta=25℃

Item	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Voltage	VDD	-0.5	3.6	V	
	PVDD	-0.5	3.6	V	
Input Signal Voltage	VCOM	-2.9	5.2	V	
Digital Input Voltage	V_{IN}	-0.3	VDD+0.3	V	
Storage Temperature	T_{ST}	-25	80	℃	
Operating Temperature	T_{OP}	0	60	℃	
Maximum Clock Frequency	Fmax	--	30	MH_Z	
Humidity	-	-	90	%RH	Note1

Note1 : T_A≤40℃ without dewing

3. Electrical Characteristics

a. Typical Operating Conditions

Item		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
Supply Voltage for Source Driver		VDD	3.0	3.3	3.6	V	
Supply Voltage for Gate Driver		PVDD	3.0	3.3	3.6		
	H Level	VGH	14	16	19.5	V	Note3-1
	L Level	VGL	-7.5	-6	-4	V	Note3-1
Digital Input Voltage	H Level	V_{IH}	VDD-0.4	-	VDD	V	
	L Level	V_{IL}	0	-	VDD+0.4	V	
Digital Output Voltage	H Level	VOH	0.7VDD	-	VDD	V	
	L Level	VOL	0	-	0.3VDD	V	
VCOM		V_{COMAC}	-	+4.5	+4.8	Vp-p	AC Component of VCOM
		V_{COMDC}	-	0.24	-	V	

Note 3-1 : VGH and VGL supplied by internal setup circuit.

b. Current Consumption

Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Current for FOG	IDD	VDD=+3.3V	6.2	12.4	mA	Note1
Current for LCM	PIDD	PVDD1=+3.3V	35.0	70.0	mA	Note2

Note 1: FOG means LCM without B/L unit
Note 2: The test conditions is by reference application note as below

4. Optical Characteristics

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note1,2,3.

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
Response Time		T_R	θ =0	-	20	30	ms	Note 4,6
		T_F		-	10	15	ms	
Contrast Ratio		CR	At optimized viewing angle	200	300	-	-	Note 5,6
Viewing Angle	Hor.	Top	CR≧10	40	45	-	Degree	Note 6,7
		Bottom		20	55	-		
	Ver.	Left		45	65	-		
		Right		45	65	-		
White Chromaticity Shift		X	θ =0	(0.26)	(0.31)	(0.36)	-	
		Y		(0.28)	(0.33)	(0.38)		
Brightness			θ =0	200	250	-	Cd/m^2	

Note 1 : Ambient temperature =25℃

Note 2 : To be measured in the dark room.

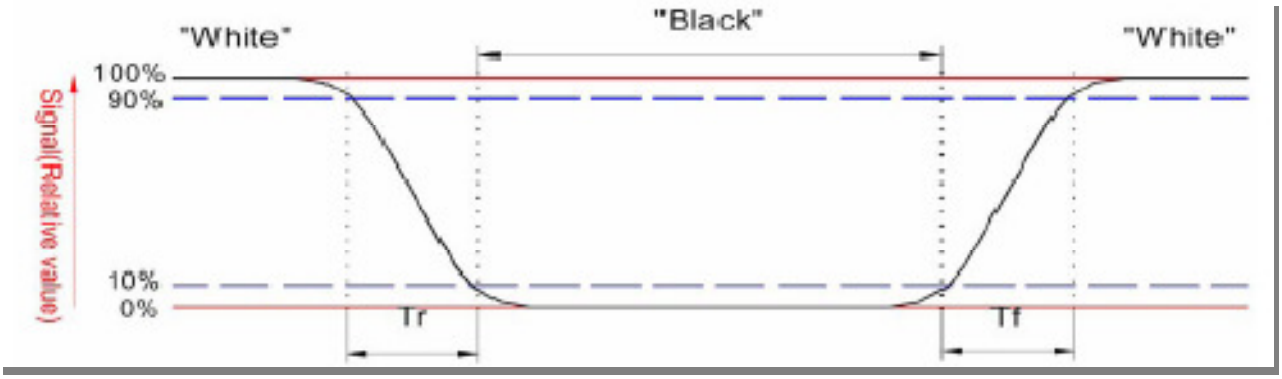
Note 3 : To be measured on the center area of panel with a field angle of 1℃

by Topcon luminance meter BM-7, after 10minutes operation.

Note 4 : Definition of Response time

The output signals of photo detector are measured when the input signals are changed from " black" to "white" (falling time) and from "white" to "black" (rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5 : Definition of Contrast Ratio

Contrast Ratio is calculated with the following formula.

$$\text{Contrast Ratio (CR)} = \frac{\text{Brightness measured when LCD is at "white state"}}{\text{Brightness measured when LCD is at "black state"}}$$

Note 6 : White $Vi=Vi_{50}$ +1.5V

Black $Vi=Vi_{50}$ ± 2.0V

"±"means that the analog input signal swings in phase with COM signal.

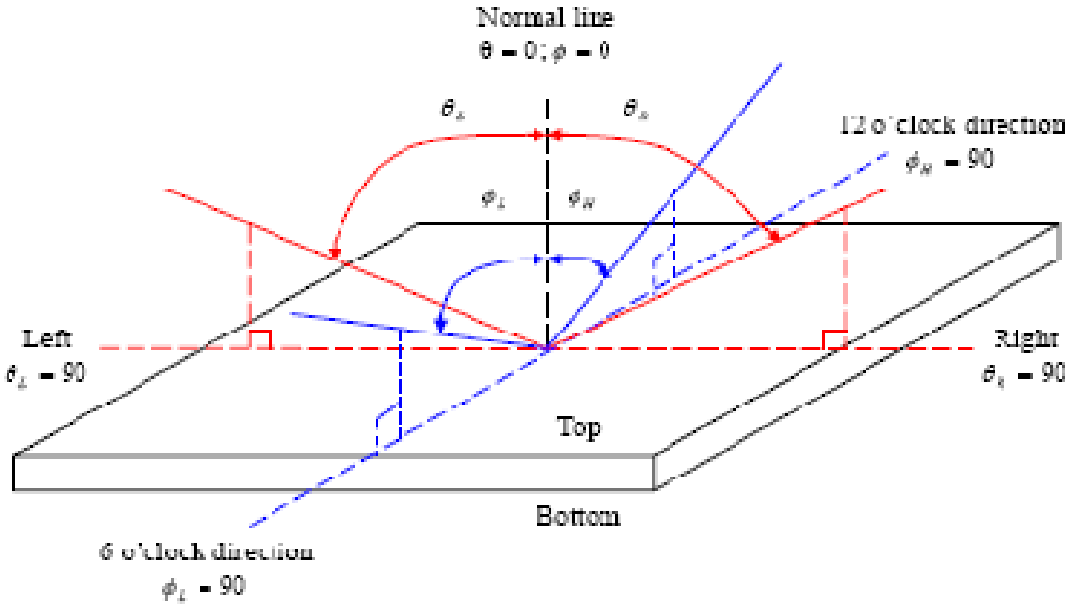
"+" means that the analog input signal swings out of phase with COM signal.

Vi_{50} : The analog input voltage when transmission is 50%.

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7 : Definition of Viewing Angle

Refer to the figure as below.



5. Interface

Pin	Symbol	I/O	Function	Remark
1	VCOM	I	Common Electrode Driving Voltage	Note5-1
2	CS	I	Serial Command Enable	
3	SDA	I	Serial Command Data Input	
4	SCL	I	Serial Command Clock Input	
5	HSYNC	I	Horizontal Sync Input	Note5-6
6	VSYNC	I	Vertical Sync Input	Note5-7
7	DCLK	I	Data Clock Input	Note5-8
8	D7	I	Data Input : MSB	
9	D6	I	Data Input	
10	D5	I	Data Input	
11	D4	I	Data Input	
12	D3	I	Data Input	
13	D2	I	Data Input	
14	D1	I	Data Input	
15	D0	I	Data Input	
16	DGND	P	Ground Terminal in the Logic Circuit	
17	VDD	P	System Power	Note5-3
18	VDDIO	P	Digital Voltage Input	
19	DVDD	C	Charge Pump Power GND	Note5-2
20	V1	C	Charge Pump Power GND	
21	V2	C	Charge Pump Power GND	
22	V3	C	Charge Pump Power GND	

23	V4	C	Charge Pump Power GND	Note5-2
24	VDD2	C	Charge Pump Power GND	
25	V5	C	Charge Pump Power GND	
26	V6	C	Charge Pump Power GND	
27	VDD3	C	Charge Pump Power GND	
28	VDD5	C	Charge Pump Power GND	Note5-2
29	V7	C	Charge Pump Power GND	
30	V8	C	Charge Pump Power GND	
31	VGH	C	Serial Communication Clock Input	
32	VGL	C	Horizontal Sync Input	
33	AGND	P	Ground Terminal in the Analog Circuit	
34	FRP	O	Frame Polarity Output for VCOM	
35	COMDC	O	VCOM DC Voltage Output Pin	
36	VCAC	C	Power Setting	Note5-2
37	DRV	O	VLED Boost Transistor for VCOM AC	Note5-4
38	VLED	P	LED Power Anode	
39	FB	P	LED Power Cathode	Note5-5
40	VCOM	I	Common Electrode Driving Voltage	Note5-1

***I** : Input **O**: Output **P** : Power **I/O** : Serial Communication Data Input/Output **C** : Capacitor*

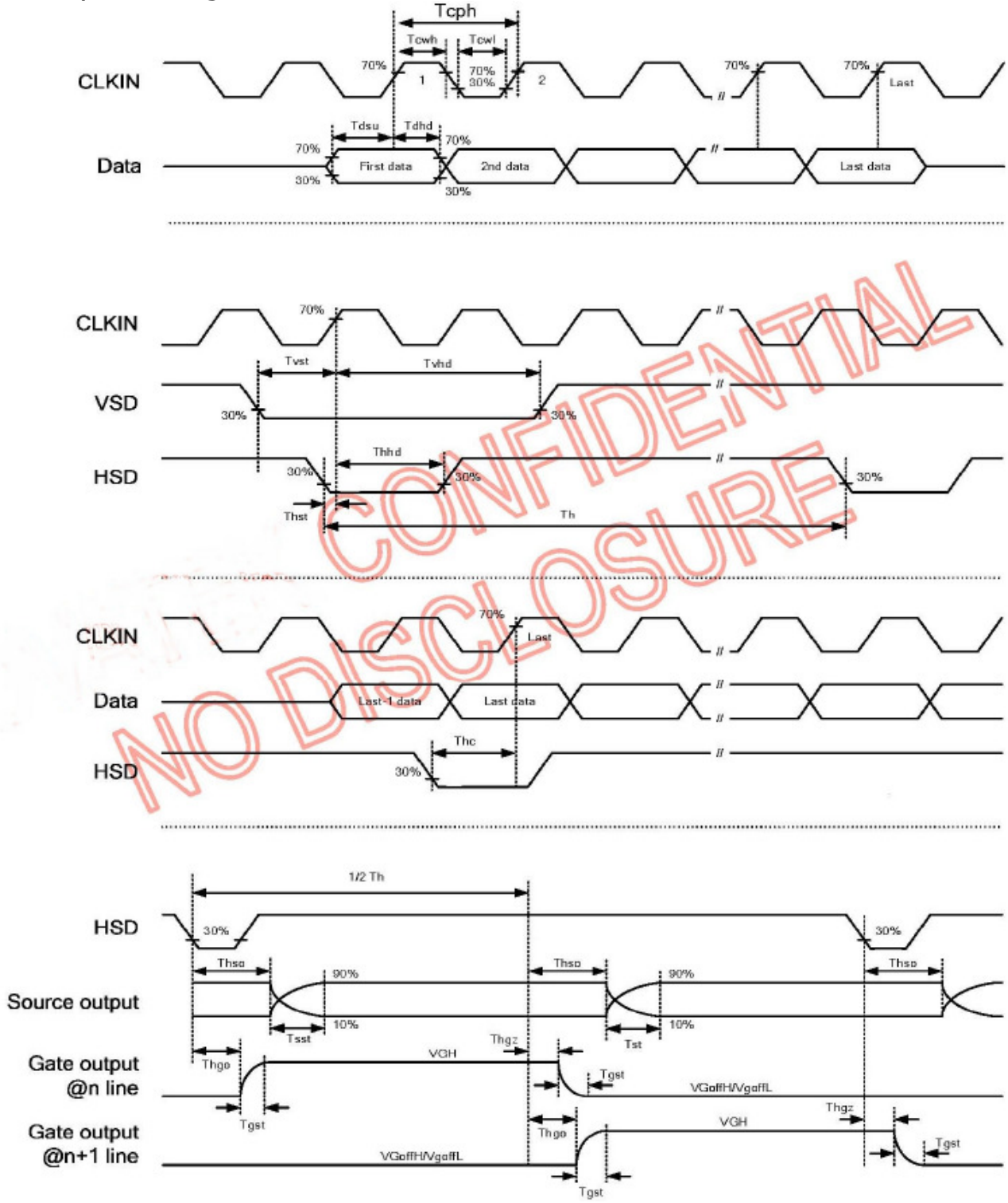
Note 5-1:VCOM=+4.8 Vp-p.(Typ.)
Note 5-2: The external capacitor is required on those pins as following.

Symbol	Capacitor No.	Part Standard		Notes
		Capacitance	Voltage	
VGH	C11	≥4.7uF	25V over	
VGL	C12	≥4.7uF	16V over	
VCAC	C10	≥4.7uF	10V over	
DVDD	C6	≥4.7uF	6.3V over	
VDD/AVDD	C5	≥4.7uF	6.3V over	
C1P C1M	C1	≥2.2uF	10V over	
C2P C2M	C2	≥2.2uF	10V over	
C3P C3M	C3	≥2.2uF	16V over	
C4P C4M	C4	≥2.2uF	16V over	
VINT1	C7	≥4.7uF	10V over	
VINT2	C8	≥4.7uF	16V over	
VINT3	C9	≥4.7uF	25V over	
FRP/VCOMDC	C13	≥4.7uF	10V over	

Note 5-3: VDD, VDDIO=+3.3V (Typ.)
Note 5-4: Outputs the control signal of switching regulator for LED.
Duty cycle varies according to FB input voltage
Note 5-5: Feedback signal of switching signal for LED.
It controls DRV output duty cycle with 0.6V input level sense.
Note 5-6: Horizontal sync signal, it is a "Low "active signal.
Note 5-7: Vertical sync signal, it is a "Low "active signal.
Note 5-8: Dot clock signal for RGB interface, timing for data loading defined at rising edge.

6. Timing Characteristics

6.1. Input Timing AC Characteristics

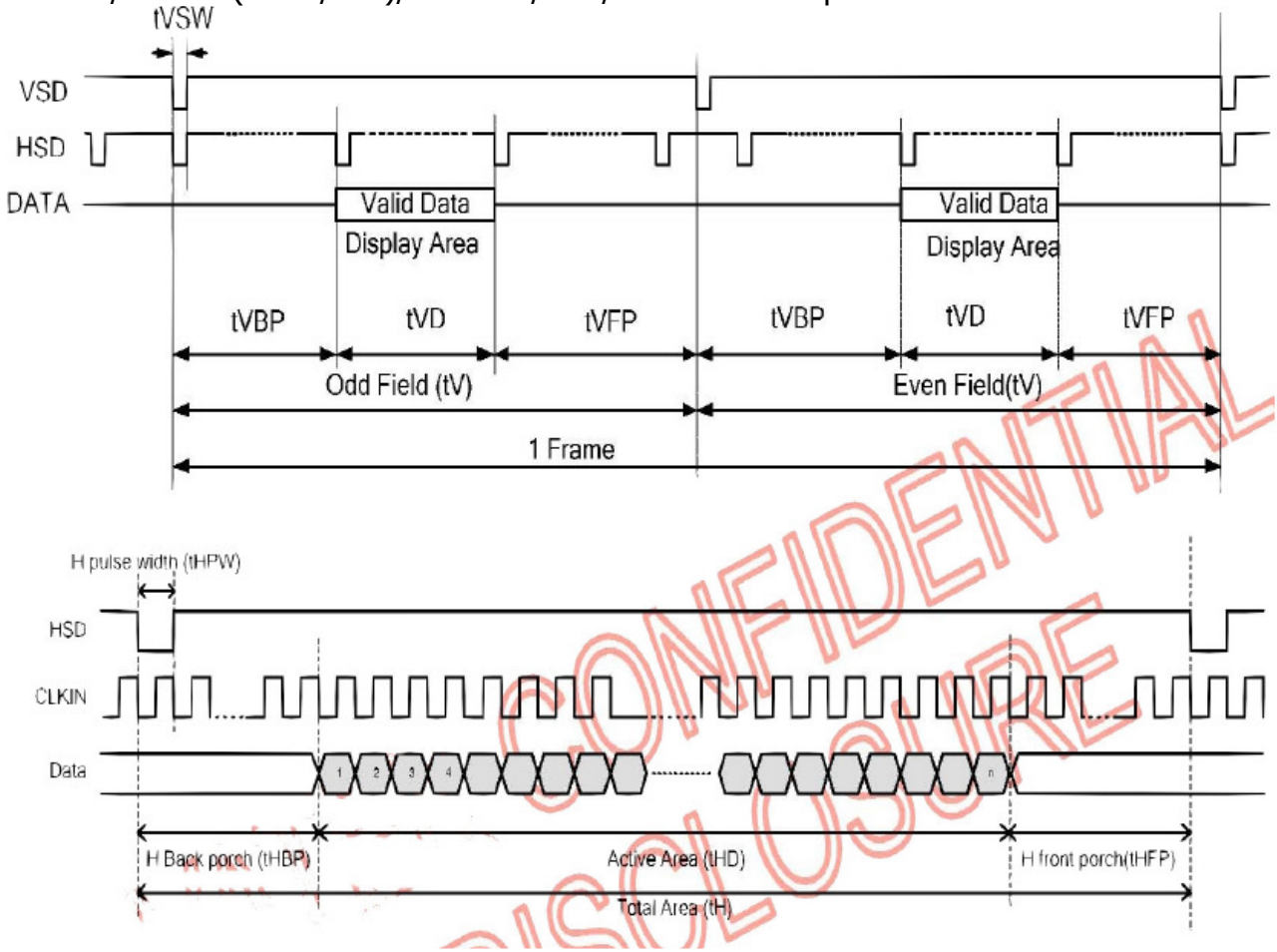


Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Time that the HSD to CLKIN	Thc	-	-	1	CLKIN	
HSD period time	Th	60	63.56	67	us	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
Data setup time	Tdsu	12	-	-	ns	DR0~DR7, DG0~DG7, DB0~DB7 to CLKIN
Data hold time	Tdhd	12	-	-	ns	DR0~DR7, DG0~DG7, DB0~DB7 to CLKIN
Time that VSD to 1st Gate output	Tstv	0	21	31	H	@ 8-bit RGB, 8-bit Dummy RGB NTSC, and Parallel RGB, Delay by VBLK setting.
Time that CCIR_V to 1st Gate output	Tstv	0	22	31	H	@CCIR656 NTSC, Delay by VBLK setting.
Time that CCIR_V to 1st Gate output	Tstv	3	24	34	H	@8-bit Dummy RGB & CCIR656 PAL, Delay by VBLK setting.
Source output setting time (*1)	Tst	-	-	8	us	R= TBD Kohm , C= TBD pF 10% 90%
Gate output setting time (*1)	Tstg	-	0.5	1	us	R= TBD Kohm , C= TBD pF 10% 90%
VCOM setting time (*1)	Tst,vcom	-	-	9	us	R= TBD Kohm , C= TBD nF 10% 90%
Time that HSD width	Twh	1	-	-	CLKIN	

Ps. (*1) Test Condition:
When the tested signal is changed from Vo, min to Vo, max, the time that is from the start of change to the time that the swing voltage at point B is less than +/- 20 mV is called the setting time of the tested signal.

6.2. Input Timing Format

UPS051/UPS052(NTSC/PAL)/CCIR656/YUV/Parallel RGB Input time chart



6.3. UPS051 Interface Timing Characteristic

(VDD=+3.0 to +3.6V, VSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
CLKIN Frequency		fCLKIN	12.5	27	27.19	MH_Z
HSD Period		tH	1024	1716	1728	CLKIN
HSD Display Period		tHD		960		CLKIN
HSD Back Porch		tHBP	84	100	115	CLKIN
HSD Front Porch		tHFP	14	686	718	CLKIN
HSD Pulse Width		tHSW	1	1	tHBP-1	CLKIN
VSD Period Time		tV	242.5	262.5	450.5	H
Vertical Display Area		tVD		240		H
VSD Back Porch	Odd	tVBP	1	21	31	H
	Even		1.5	21.5	31.5	
VSD Front Porch	Odd	tVFP	1.5	1.5	179.5	H
	Even		1	1	179	
VSD Pulse Width		tVSW	1	1	6	H
1 Frame			485	525	901	H

6.4. UPS052 Interface Timing Characteristic

A. UPS052 (320mode/NTSC/24.535Mhz) Time Specifications

(VDD=+3.0 to +3.6V, VSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
CLKIN Frequency		fCLKIN	20.45	24.535	30	MH_Z
HSD Period		tH	1306	1560	1907	CLKIN
HSD Display Period		tHD		1280		CLKIN
HSD Back Porch		tHBP	3	241	255	CLKIN
HSD Front Porch		tHFP	25	39	372	CLKIN
HSD Pulse Width		tHSW	1	1	200	CLKIN
VSD Period Time		tV	242.5	262.5	450.5	H
Vertical Display Area		tVD		240		H
VSD Back Porch	Odd	tVBP	1	21	31	H
	Even		1.5	21.5	31.5	
VSD Front Porch	Odd	tVFP	1.5	1.5	179.5	H
	Even		1	1	179	
VSD Pulse Width		tVSW	1	1	6	H
1 Frame			485	525	901	H

B. UPS052 (320mode/PAL/24.375Mhz) Time Specifications

(VDD=+3.0 to +3.6V, VSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
CLKIN Frequency		fCLKIN	20.45	24.375	30	MH_Z
HSD Period		tH	1306	1560	1907	CLKIN
HSD Display Period		tHD		1280		CLKIN
HSD Back Porch		tHBP	3	241	255	CLKIN
HSD Front Porch		tHFP	25	39	385	CLKIN
HSD Pulse Width		tHSW	1	1	200	CLKIN
VSD Period Time		tV	292.5	312.5	450.5	H
Vertical Display Area		tVD		288		H
VSD Back Porch	Odd	tVBP	3	23	34	H
	Even		3.5	23.5	34.5	
VSD Front Porch	Odd	tVFP	1.5	1.5	128.5	H
	Even		1	1	128	
VSD Pulse Width		tVSW	1	1	6	H
1 Frame			585	625	901	H

C.UPS052 (360mode/NTSC/ 27Mhz) Time Specifications

(VDD=+3.0 to +3.6V, VSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
CLKIN Frequency		fCLKIN	23	27	30	MHz
HSD Period		tH	1466	1716	1907	CLKIN
HSD Display Period		tHD		1440		CLKIN
HSD Back Porch		tHBP	3	241	255	CLKIN
HSD Front Porch		tHFP	25	35	312	CLKIN
HSD Pulse Width		tHSW	1	1	200	CLKIN
VSD Period Time		tV	242.5	262.5	450.5	H
Vertical Display Area		tVD		240		H
VSD Back Porch	Odd	tVBP	1	21	31	H
	Even		1.5	21.5	31.5	
VSD Front Porch	Odd	tVFP	1.5	1.5	179.5	H
	Even		1	1	179	
VSD Pulse Width		tVSW	1	1	6	H
1 Frame			485	525	901	H

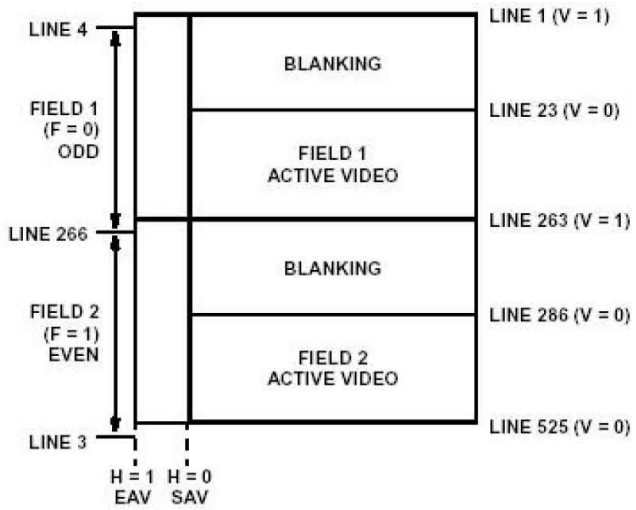
D.UPS052 (360mode/PAL/ 27Mhz) Time Specifications

(VDD=+3.0 to +3.6V, VSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
CLKIN Frequency		fCLKIN	23	27	30	MHz
HSD Period		tH	1466	1728	1920	CLKIN
HSD Display Period		tHD		1440		CLKIN
HSD Back Porch		tHBP	3	241	255	CLKIN
HSD Front Porch		tHFP	25	47	255	CLKIN
HSD Pulse Width		tHSW	1	1	200	CLKIN
VSD Period Time		tV	292.5	312.5	450.5	H
Vertical Display Area		tVD		288		H
VSD Back Porch	Odd	tVBP	3	23	34	H
	Even		3.5	23.5	34.5	
VSD Front Porch	Odd	tVFP	1.5	1.5	128.5	H
	Even		1	1	128	
VSD Pulse Width		tVSW	1	1	6	H
1 Frame			585	625	901	H

6.5. CCIR 656 Vertical Timing Characteristic

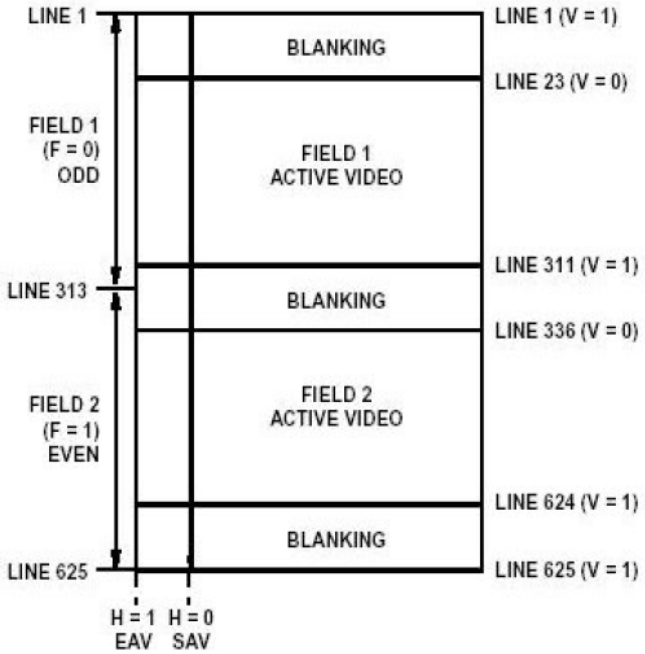
A.NTSC mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACIVE VIDEO

B.PAL mode



LINE NUMBER	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	ACIVE VIDEO

6.6. YUV720 and YVU640 Input Timing

A.YUV720 mode(NTSC Input Timing)

Parameter		Symbol	Min.	Typ.	Max.	Unit
CLKIN Frequency		fCLKIN	--	27	--	MH_Z
HSD Period		tH	--	1716	--	CLKIN
HSD Display Period		tHD		1440		CLKIN
HSD Back Porch		tHBP	--	240	--	CLKIN
HSD Front Porch		tHFP	--	36	--	CLKIN
HSD Pulse Width		tHSW	--	1	--	CLKIN
VSD Period Time		tV	--	262.5	--	H
Vertical Display Area		tVD		240		H
VSD Back Porch	Odd	tVBP	--	21	--	H
	Even		--	21.5	--	
VSD Front Porch	Odd	tVFP	--	1.5	--	H
	Even		--	1	--	
VSD Pulse Width		tVSW	--	1	--	H
1 Frame			--	525	--	H

B.YUV720 mode(PAL Input Timing)

Parameter		Symbol	Min.	Typ.	Max.	Unit
CLKIN Frequency		fCLKIN	--	27	--	MH_Z
HSD Period		tH	--	1728	--	CLKIN
HSD Display Period		tHD		1440		CLKIN
HSD Back Porch		tHBP	--	240	--	CLKIN
HSD Front Porch		tHFP	--	48	--	CLKIN
HSD Pulse Width		tHSW	--	1	--	CLKIN
VSD Period Time		tV	--	312.5	--	H
Vertical Display Area		tVD		288		H
VSD Back Porch	Odd	tVBP	--	24	--	H
	Even		--	24.5	--	
VSD Front Porch	Odd	tVFP	--	0.5	--	H
	Even		--	0	--	
VSD Pulse Width		tVSW	--	1	--	H
1 Frame			--	625	--	H

C.YUV640 mode(NTSC Input Timing)

Parameter		Symbol	Min.	Typ.	Max.	Unit
CLKIN Frequency		fCLKIN	--	24.535	--	MH_Z
HSD Period		tH	--	1560	--	CLKIN
HSD Display Period		tHD		1280		CLKIN
HSD Back Porch		tHBP	--	240	--	CLKIN
HSD Front Porch		tHFP	--	40	--	CLKIN
HSD Pulse Width		tHSW	--	1	--	CLKIN
VSD Period Time		tV	--	262.5	--	H
Vertical Display Area		tVD		240		H
VSD Back Porch	Odd	tVBP	--	21	--	H
	Even		--	21.5	--	
VSD Front Porch	Odd	tVFP	--	1.5	--	H
	Even		--	1	--	
VSD Pulse Width		tVSW	--	1	--	H
1 Frame			--	525	--	H

D.YUV640 mode(PAL Input Timing)

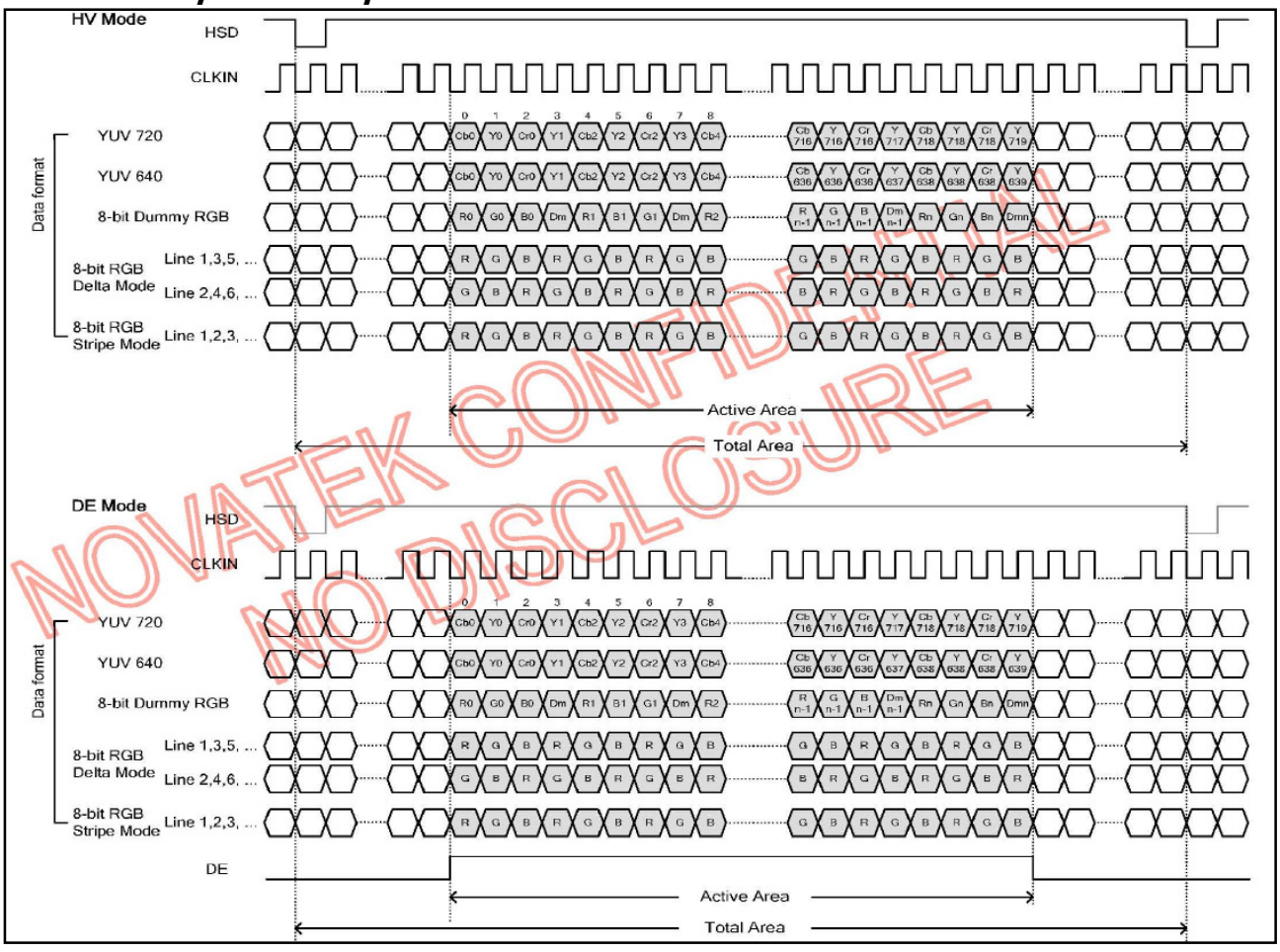
Parameter		Symbol	Min.	Typ.	Max.	Unit
CLKIN Frequency		fCLKIN	--	24.375	--	MH_Z
HSD Period		tH	--	1560	--	CLKIN
HSD Display Period		tHD		1280		CLKIN
HSD Back Porch		tHBP	--	240	--	CLKIN
HSD Front Porch		tHFP	--	40	--	CLKIN
HSD Pulse Width		tHSW	--	1	--	CLKIN
VSD Period Time		tV	--	312.5	--	H
Vertical Display Area		tVD		288		H
VSD Back Porch	Odd	tVBP	--	24	--	H
	Even		--	24.5	--	
VSD Front Porch	Odd	tVFP	--	0.5	--	H
	Even		--	0	--	
VSD Pulse Width		tVSW	--	1	--	H
1 Frame			--	625	--	H

6.7. Parallel RGB Input Timing

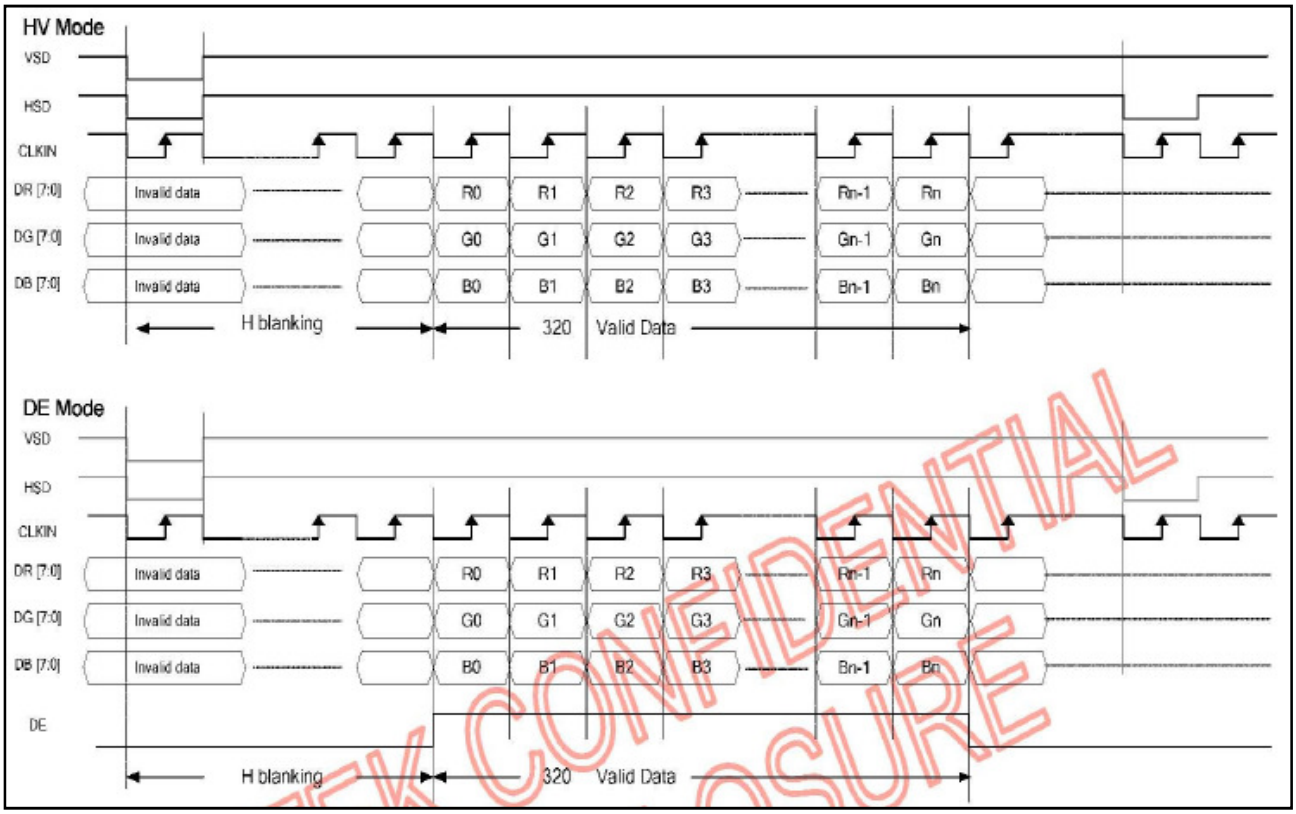
Parameter		Symbol	Min.	Typ.	Max.	Unit
CLKIN Frequency		fCLKIN	--	6,2	7,5	MH_Z
HSD Period		tH	--	390	--	CLKIN
HSD Display Period		tHD		320		CLKIN
HSD Back Porch		tHBP	40	61	--	CLKIN
HSD Front Porch		tHFP	--	9	--	CLKIN
HSD Pulse Width		tHSW	--	1	--	CLKIN
VSD Period Time		tV	--	262.5	--	H
Vertical Display Area		tVD		240		H
VSD Back Porch	Odd	tVBP	--	21	--	H
	Even		--	21.5	--	
VSD Front Porch	Odd	tVFP	--	1.5	--	H
	Even		--	1	--	
VSD Pulse Width		tVSW	--	1	--	H
1 Frame			--	525	--	H

6.8. Data Input Format

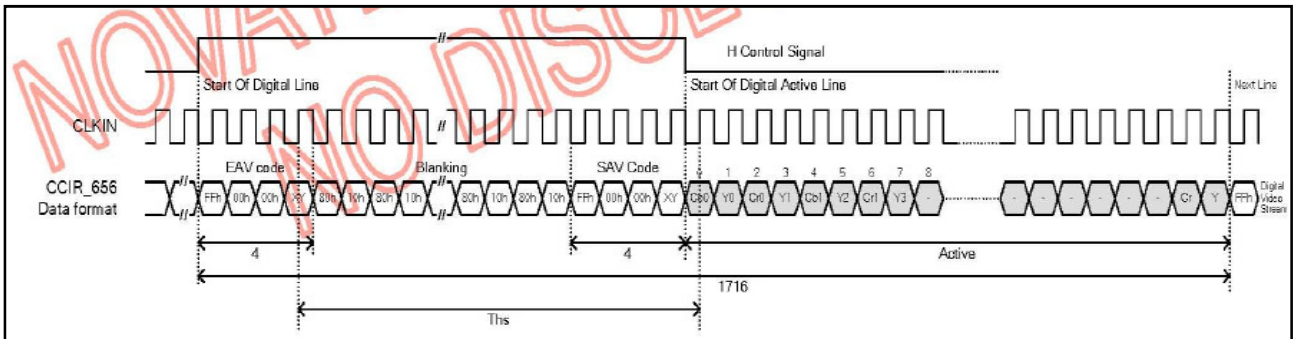
A .UPS051/UPS052/YUV Mode



B. Parallel RGB Mode



C.CCIR MODE



- FF 00 00 XY signals are involved with HSD,VSD and Field
- XY encode following bits:

  F=field select
  V=indicate vertical blanking
  H=1 if EAV else 0 for SAV
  P3-P0=protection bits :
  P3=V⊕H P2=F⊕H P1=F⊕V P0=F⊕V⊕H ⊕: Represents the exclusive-OR function

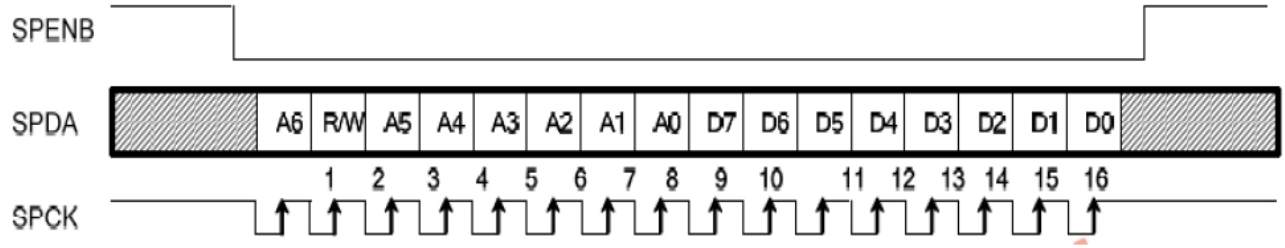
XY							
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0
1	F	V	H	P3	P2	P1	P0

- Control is provided through "End of Video" (EAV) and "Start of Video" (SAV) timing references.
- Horizontal blanking section consists of repeating pattern 80 10 80 10

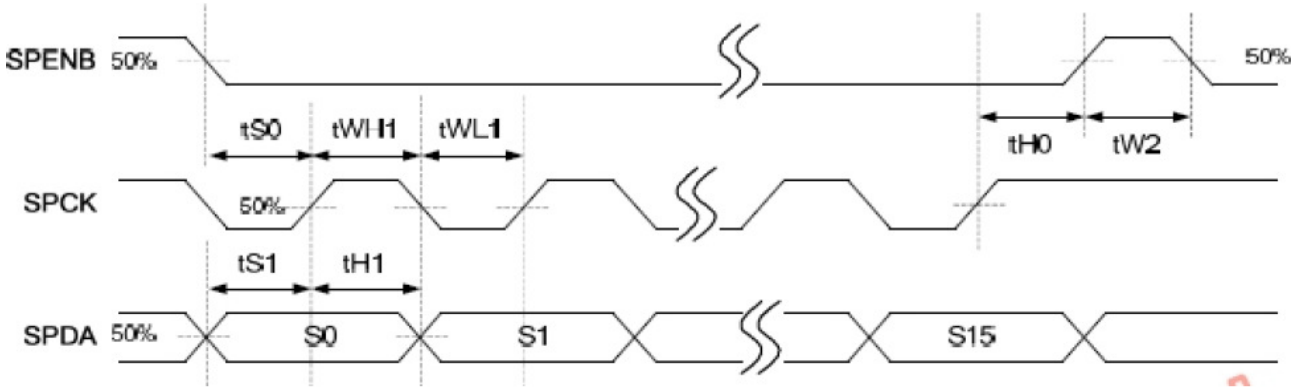
6.9. Internal Register Description

The 3-wire CPU serial interface is used and set to the data writing in these internal registers. Each serial command consists of 16 bits of data that is loaded one bit a time at the rising edge of serial clock SPCK. Command loading operation starts from the falling edge of SPENB and is completed at the next rising edge of SPENB

★ 3 Wire Serial Command Format



★ Serial Control Timing



Item	Symbol	Min.	Typ.	Max.	Unit
SPENB Input Setup Time	tS0	50	--	--	ns
Serial Data Input Setup Time	tS1	50	--	--	ns
SPENB Input Hold Time	tH0	50	--	--	ns
Serial Data Input Hold Time	tH1	50	--	--	ns
SPCK Pulse High Width	tWH1	50	--	--	ns
SPCK Pulse Low Width	tWL1	50	--	--	ns
SPENB Pulse High Width	tW2	400	--	--	ns

Register Summary
3-Wire Register Table

Register	Register Address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	Y_CbCr (0)	CCIR601 (0)	x	x	VCOM_AC (0110)			
R1	0	0	0	0	0	0	0	1	VCDCE (1)	0	VCOM_DC (21h)					
R3	0	0	0	0	0	0	1	1	Brightness (40h)							
R4	0	0	0	0	0	1	0	0	Narrow (0)	YUV (0)	SEL (00)		NTSC/PAL (10)		VDIR (1)	HDIR (1)
R5	0	0	0	0	0	1	0	1	DRV_FREQ (0)	GRB (1)	PWM_DUTY (011)			SHDB2 (1)	SHDB1 (1)	STB (0)
R6	0	0	0	0	0	1	1	0	HBLK_EN (0)	LED_Current (00)		VBLK (15h)				
R7	0	0	0	0	0	1	1	1	HBLK (46h)							
R8	0	0	0	0	1	0	0	0	BL_DRV (00)		x	x	x	0	0	0
R11	0	0	0	0	1	0	1	1	REGSEL (0)		x	x	x	x	SOPC (01)	
R12	0	0	0	0	1	1	0	0	PAIR (00)		DESEL (0)	CbCr (0)	DEpol (0)	VDpol (1)	HDpol (1)	CLKINpol (0)
R13	0	0	0	0	1	1	0	1	CONTRAST_B (40h)							
R14	0	0	0	0	1	1	1	0	x	SUB-CONTRAST_R (40h)						
R15	0	0	0	0	1	1	1	1	x	SUB-BRIGHTNESS_R (40h)						
R16	0	0	0	1	0	0	0	0	x	SUB-CONTRAST_B (40h)						
R17	0	0	0	1	0	0	0	1	x	SUB- BRIGHTNESS _B (40h)						
R18	0	0	0	1	0	0	1	0	TRMEN (00)							
R19	0	0	0	1	0	0	1	1	x	x	x	0	CF_SEL (0)	0	0	0
R22	0	0	0	1	0	1	1	0	x	x	x	x	x	GAMMA2.2 (1)	x	x
R23	0	0	0	1	0	1	1	1	x	GMA_V16 (101)			x	GMA_V8 (100)		
R24	0	0	0	1	1	0	0	0	x	GMA_V50 (101)			x	GMA_V32 (100)		
R25	0	0	0	1	1	0	0	1	x	GMA_V96 (100)			x	GMA_V72 (011)		
R26	0	0	0	1	1	0	1	0	x	GMA_V120 (101)			x	GMA_V110 (100)		
R85	1	0	0	1	0	1	0	1	0	INV_SEL (0)	0	0	x	x	x	0
R86	1	0	0	1	0	1	1	0	x	x	x	x	x	x	VGH_SEL (11)	
R87	1	0	0	1	0	1	1	1	VGHL_ENB (0)	x	x	x	x	x	VGL_SEL (10)	

Notes:
1. When RSTB is low, all registers reset to default values.
2. Serial Commands are executed at next VSD signal.

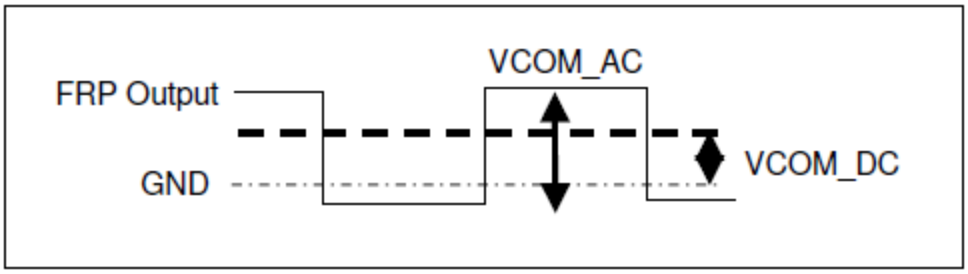
Register Description (3 wire)

★R0-Vcom_AC(R0[3:0]:Common Voltage AC Level Selection

Register	Register Address								Register Data (Default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	Y-CbCr (0)	CCIR601 (0)	X	X	VCOM_AC (0110)			

D3	D2	D1	D0	Voltage(V)
0	0	0	0	3.6
0	0	0	1	3.7
0	0	1	0	3.8
0	0	1	1	3.9
0	1	0	0	4.0
0	1	0	1	4.1
0	1	1	0	4.2(Default)
0	1	1	1	4.3
1	0	0	0	4.4
1	0	0	1	4.5
1	0	1	0	4.6
1	0	1	1	4.7
1	0	X	X	4.8

Note : The default value will change by VCOMDC trim function



★R0-CCIR601(R0[6]) : CCIR601 input timing selection

CCIR601	Function
0	Disable CCIR601 (Default)
1	Enable CCIR601 (Please refer to the table of R4(SEL) for detail description

★R0-Y_CbCr(R0[7])

Y&CbCr exchange position (only valid for 8-bit input YUV640/YUV720)

Y_CbCr='0' (Default)

Under R12[4] CbCr='0'

Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3

Under R12[4] CbCr= '1'

Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3

Y_CbCr='1'

Under R12[4] CbCr='0'

Y0	Cb0	Y1	Cr0	Y2	Cb2	Y3	Cr2

Under R12[4] CbCr= '1'

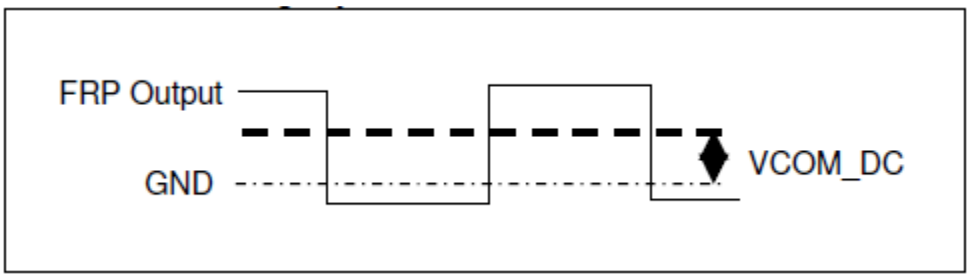
Y0	Cr0	Y1	Cb0	Y2	Cr2	Y3	Cb2

★R1-VCOM_DC(R1[5:0]) : Common voltage DC level selection (20Mv/step)

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R1	0	0	0	0	0	0	0	1	VCDCE (1)	0	VCOM_DC (21h)					

D5~D0	VCOM DC Level
00h	0.24
:	:
21h	0.90 (Default)
:	:
3Fh	1.5

Note : The default value will change by VCOMDC trim function



★R1-VCDCE(R1[7]) : VCOM_DC enable control

D7	VCDCE Function
0	VCOM_DC Function Disabled. The VCOMDC pin is disabled.
1	VCOM_DC Function Enabled. The VCOMDC voltage follows VCOM_DC setting

★R3-Brightness(R3[7:0])

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R3	0	0	0	0	0	0	1	1	Brightness(40h)							

Setting Accuracy 1Bit/Step

D7~D0	Brightness Gain
00h	Dark. (-64)
40h	Center(0). (Default)
FFh	Bright. (+191)

★R4-HDIR(R4[0]) : Shift registers of source driver direction selection

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R4	0	0	0	0	0	1	0	0	Narrow (0)	YUV (0)	SEL (00)		NTCS/PAL (10)		VDIR (1)	HDIR (1)

D0	HDIR Function
0	Shift from right to left. Y0<-Y1<-……<-Y959<-Y960
1	Shift from right to left. Y0->Y1->……->Y959->y960 (Default)

★R4-VDIR (R4[1]) : Gate driver output direction selection

D1	VCDCE Function
0	Shift from down to up. L0<-L1<-……<-L239<-L240
1	Shift from up to down. L0->L1->……->L2440->L240 (Default)

★R4-NTSC/PAL (R4[3:2]) : NTSC or PAL input mode selection

D3	D2	NTSC/PAL Mode
0	0	PAL.
0	1	NTSC.
1	X	Auto Detection. (Default)

★R4-SEL (R4[5:4]) : Input data timing format selection

CCIR601	YUV	SEL		Input Timing Format
		D5	D4	
0	0	0	0	8-bit RGB. (Default)
0	0	0	1	8-bit Dummy RGB 320X240.
0	0	1	X	8-bit Dummy RGB 360X240.
0	1	X	X	CCIR656
1	1	0	X	YUV640
1	1	1	0	YUV720

★R4-YUV (R4[6]) : YUV(CCIR656) or RGB input selection

D6	Data Format
0	RGB input. (Default)
1	CCIR656 / YUV640 / YUV720 input.

★R4-Narrow (R4[7]) : Normal Display and Narrow Display selection

D7	Function
0	Normal display. (Default)
1	Narrow display.

R4[7] = 0

R4[7] = 1

★R5-STB (R5[0]) : Standby (Power Saving) Mode

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R5	0	0	0	0	0	1	0	1	DRV_FREQ (0)	GRB (1)	PWM_DUTY (011)			SHDB2 (1)	SHDB1 (1)	STB (0)

D0	STB Function
0	Standby Mode. (Default)
1	Normal Operation

Note : In standby mode, source driver output. VGH, VGL, and FRP are all 0V.

★R5-SHDB1 (R5[1]) : Shut down for bank light power converter

D1	SHDB1 Function
0	The back light power converter is off
1	The back light power converter is controlled by STB's power sequence (Default)

★R5-SHDB2 (R5[2]) : Shut down for VGH/VGL charge pump

D1	SHDB2 Function
0	VGH/VGL charge pump is always off
1	VGH/VGL charge pump is controlled by STB's power On/Off sequence. (Default)

★R5-PWM_DUTY (R5[5:3]) : PWM duty cycle selection for back light power convert

SHDB1 Function			Function
D5	D4	D3	PWM duty cycle
0	0	0	55%
0	0	1	60%
0	1	0	65%
0	1	1	70%(Default)
1	0	0	75%
1	0	1	80%
1	1	0	85%
1	1	1	90%

★R5-PWM_DUTY (R5[6]) : Global Reset

D6	GRB Function
0	Reset all registers to default value
1	Normal operation. (Default)

★R5-DRV_FREQ (R5[7]) : DRV signal frequency setting

D7	DRV Frequency
0	CLKIN/64. (Default)
1	CLKIN/128

★R6-VBLK (R6[4:0])

Vertical blanking setting for 8-bit RGB, 8-bit Dummy RGB&CCIR656

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R6	0	0	0	0	0	1	1	0	HBLK_EN (0)	LED_Current (00)		VBLK (15h)				
R7	0	0	0	0	0	1	1	1	HBLK (46h)							

For 8-bit RGB, 8-bit Dummy RGB, CCIR656, YUV640 and YUV720 NTSC mode, Parallel RGB input mode (PSEL="LOW").

D4~D0	VBLK Function	Unit
00h~03h	3.	H
04h	4.	
15h	31. (Default)	
1Fh	31	

For 8-bit Dummy RGB,CCIR656,YUV640 and YUV720 PAL mode.(Vertical blanking+3)

D4~D0	VBLK Function	Unit
00h	3.	H
15h	24. (Default)	
1Fh	34	

★R6—LED_CURRENT (R6[6:5]): LED current adjustable for DC-DC feedback threshold voltage

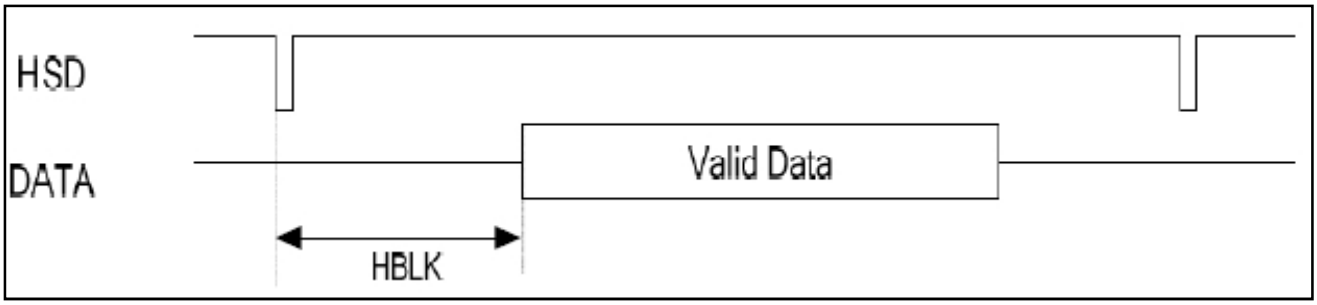
D6~D5	VBLK Function
00	0.6V. (Default)
01	0.75V
10	0.45V
11	0.3V

★R6/R7—HBLK_EN(r6[7]): HBLK function enable

HBLK (R6[7:0]): Horizontal blanking setting

HBLK_EN	D7~D0	HBLK	UNIT	NTSC/PAL Mode
X	32h	50	CLKIN(*)	8-bit RGB
X	46h	70		
X	FFh	255	CLKIN(*)	8-bit Dummy RGB
X	XXh	240	CLKIN(*)	YUV840, YUV720
1	00h~03h	3	CLKIN(*)	
	04h~255	4~255		
0	X	61	CLKIN(*)	Parallel RGB
	28h~	4~63		

*The frequency of CLKIN is different under different input timing



★ R8—BL_DRV(R8[7:6]): Backlight driving capability setting

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R8	0	0	0	0	1	0	0	0	BL_DRV (00)		X	X	X	0	0	0

D7	D6	BL_DRV capability
0	0	Normal capability (Default)
0	1	2 times the Normal capability
1	0	4 times the Normal capability
1	1	8 times the Normal capability

★ R11-SOPC(R11[1:0]): Source output driving capability selection

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R11	0	0	0	0	1	0	1	1	REGSEL (0)	X	X	X	X	X	SOPC (01)	

D1	D0	Source driver capability
0	0	-25%
0	1	Normal. (Default)
1	0	+25%
1	1	+50%

★ R11-REGSEL(R11[7]) : Source output driving capability selection

D7	REGSEL Function
0	VCOM DC[5:0] is read from MTP memory. (Default)
1	VCOM DC[5:0] is switch to the 3-wire register memory when use want to adjust the VCOMDC level for test propose. Refer to the "TRMEN" control register for the proper MPT write operation.

★ R12-CLKINpol(R12[0]):CLKIN polarity selection

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R12	0	0	0	0	1	1	0	0	PAIR (00)		DESEL (0)	CbCr (0)	Depol (0)	Vdpol (1)	Hdpol (1)	CLKINpol (0)

D0	CLKINpol Function
0	Positive polarity. (Default)
1	Negative polarity

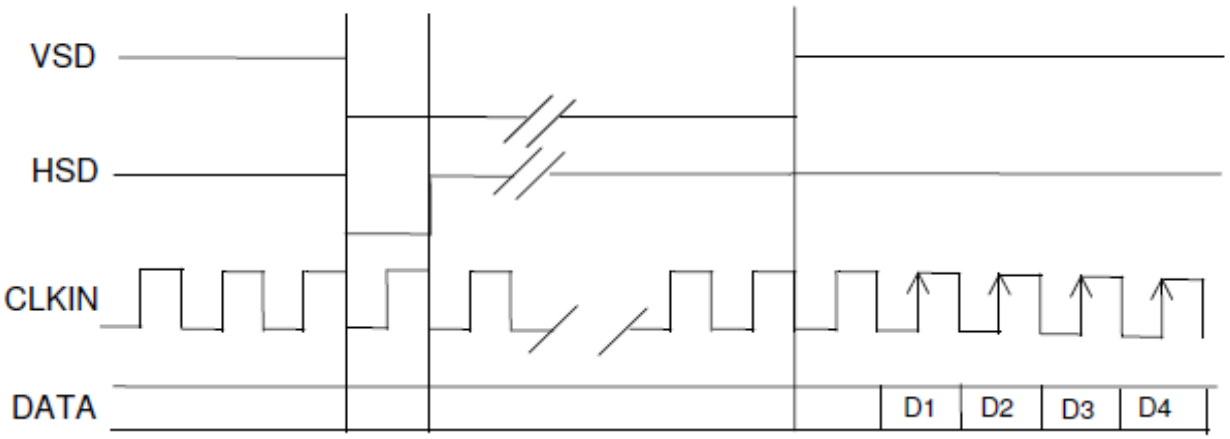
★ R12-HDpol (R12[1]) : HSD polarity selection

D1	HDpol Function
0	Positive polarity.
1	Negative polarity. (Default)

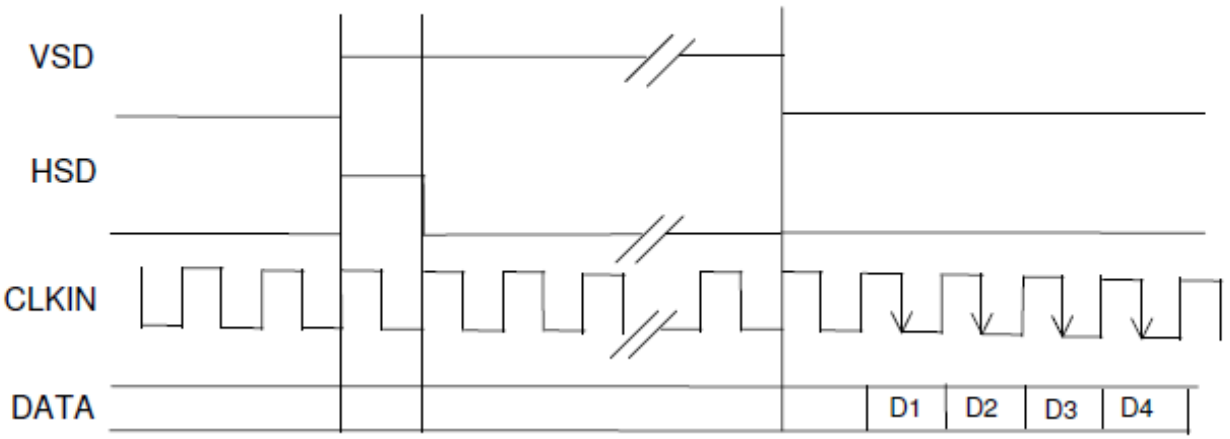
★ R12-HDpol (R12[2]) : VSD polarity selection

D2	VDpol Function
0	Positive polarity.
1	Negative polarity. (Default)

HDpol=1,VDpol=1,CLKINpol=0



HDpol=0,VDpol=0,CLKINpol=1



★ R12-EDpol (R12[3]) : DEN polarity selection

D3	EDpol Function
0	Positive polarity. (Default)
1	Negative polarity.

★ R12-CbCr (R12[4]) : Cb&Cr exchange position (Valid for CCIR656 and YUV640/YUV720)

D4	CbCr Function
0	Cb->Y->Cr. (Default)
1	Cr->Y->Cb.

★ R12-DESEL (R12[5]) : DE Mode selection

D5	DESEL Function
0	HV mode selected. (Default)
1	DE mode selected.

*DESEL only controls the HV and DE mode at 8-bit Dummy RGB and parallel Mode

★ R12-PAIR (R2[7:6]) : Vertical start time of Odd/Even Frame

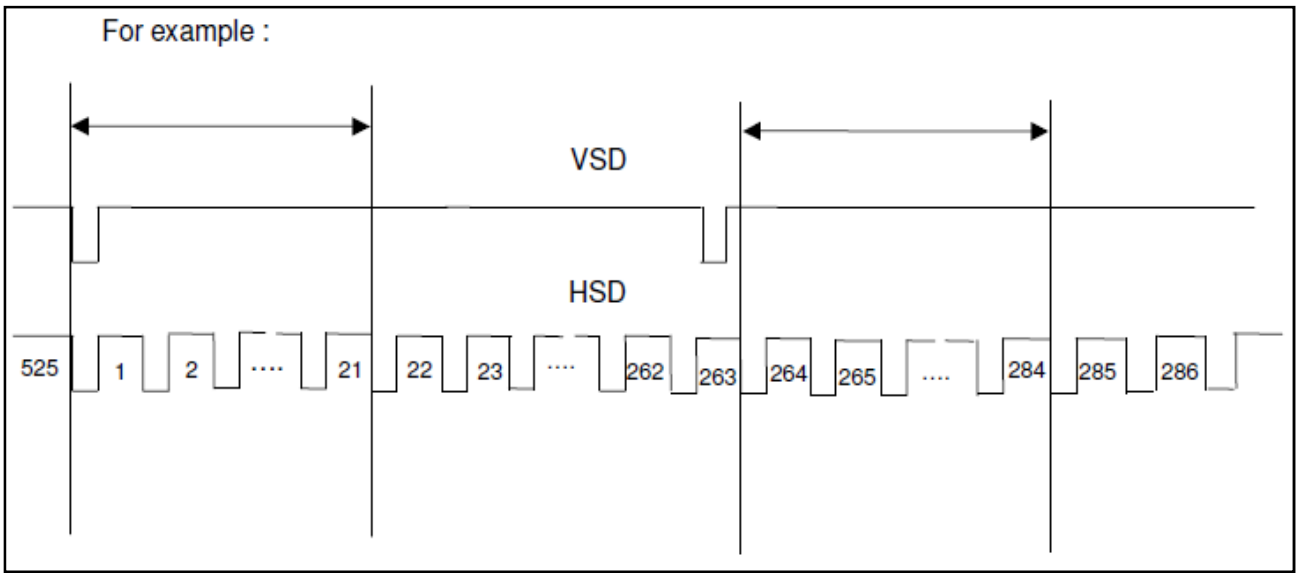
8-bit RGB / 8-bit Dummy RGB NTSC / 8—bit Dummy RGB PAL (*)
Parallel RGB input mode (PSEL="Low")

PAIR		VBLK	Unit
D7	D6		
X	0	21/21 (Default)	H(Line)
X	1	21/20	

CCIR656 / YUV640 / YUV720 NTSC / PAL(**)

PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
0	0	22/22 (Default)	H(Line)
0	1	22/23	
1	0	23/22	
1	1	23/23	

(*)The typical value of VBLK of 8-bit Dummy RGB PAL(24H) is different than 8-bit RBB/ 8-bit Dummy RGB NTSC(21H)
(**)The typical vaule of VBLK of CCIR656 PAL (24H) is different than CCIR656 NTSC(21H)
Note: V-Blanking must be adjusted base on the input data



★ R13-CONTRAST_B(R13[7:0]) : RGB contrast level setting, the gain changes (1/64)/bit

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R13	0	0	0	0	1	1	0	1	CONTRAST_B (40h)							

D7~D0	Contrast Gain
00h	0
40h	1 (Default)
FFh	3.984

★ R14-SUB CONTRAST_R(R14[6:0]) : RGB sub-pixel contrast level setting, the gain changes (1/256)/bit

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R14	0	0	0	0	1	1	1	0	X	SUB-CONTRST-R (40h)						

D6~D0	Contrast Gain
00h	0.75
40h	1 (Default)
7Fh	1.246

★ R15-SUB BRIGHTNESS_R(R15[6:0]) : Red sub-pixel brightness level setting, setting accuracy : 1 step/bit

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R15	0	0	0	0	1	1	1	1	X	SUB-BRIGHTNESS-R (40h)						

D6~D0	R Brightness Gain
00h	DARK (-64)
40h	Center (0) (Default)
7Fh	Bright (+63)

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R16	0	0	0	1	0	0	0	0	X	SUB-CONTRAST-B (40h)						

★ R16-SUB CONRAST_B(R16[6:0]) : Blue sub-pixel contrast level setting, the gain changes(1/256)/bit

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R16	0	0	0	1	0	0	0	0	X	SUB-CONTRAST-B (40h)						

D6~D0	B Contrast Gain
00h	0.75
40h	1 (Default)
7Fh	1.246

★ R17-SUB BRIGHTNESS_B(R17[6:0]) : Blue sub-pixel brightness level setting, setting accuracty : 1step/bit

Register	Register address								Register Data (default)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R17	0	0	0	1	0	0	0	1	X	SUB-BRIGHTNESS-B (40h)						

D6~D0	B Brightness Gain
00h	Dark (-64)
40h	Center (0) (Default)
7Fh	Brightness (+63)

★ R19-CF_SEL(R0[3]) : Color filter selection register

CF_SEL	Function
0	Delta color filter. (Default)
1	Stripe color filter.

★ R22-GAMMA 2.2(R22[2]) : Select auto or manual gamma setting

D2	Gamma 2.2 Function
0	Manual set gamma by R23~R26
1	Auto set to gamma 2.2 (Default)

★ **R23~R26**

GMA_V8 (R23[2:0]):Gamma reference voltage V8
GMA_V16 (R23[6:4]):Gamma reference voltage V16;
GMA_V32 (R24[2:0]):Gamma reference voltage V32;
GMA_V50 (R24[6:4]):Gamma reference voltage V50;
GMA_V72 (R25[2:0]):Gamma reference voltage V72;
GMA_V96 (R25[6:4]):Gamma reference voltage V96;
GMA_V110 (R26[2:0]):Gamma reference voltage V110;
GMA_V120 (R26[6:4]):Gamma reference voltage V120;

★ **R85-INV_SEL(R85[6]) : Inversion selection**

D6	INV_SEL Function
0	One line inversion. (Default)
1	Column inversion.

★ **R86-VGH_SEL(R86[0:1]) : VGH voltage level selection**

D1	D0	VGH SEL Function
0	0	[VGL]+9V.
0	1	[VGL]+10V.
1	0	[VGL]+11V.
1	1	[VGL]+12V. (Default)

★ **R87-VGH_SEL(R87[0:1]) : VGH voltage level selection**

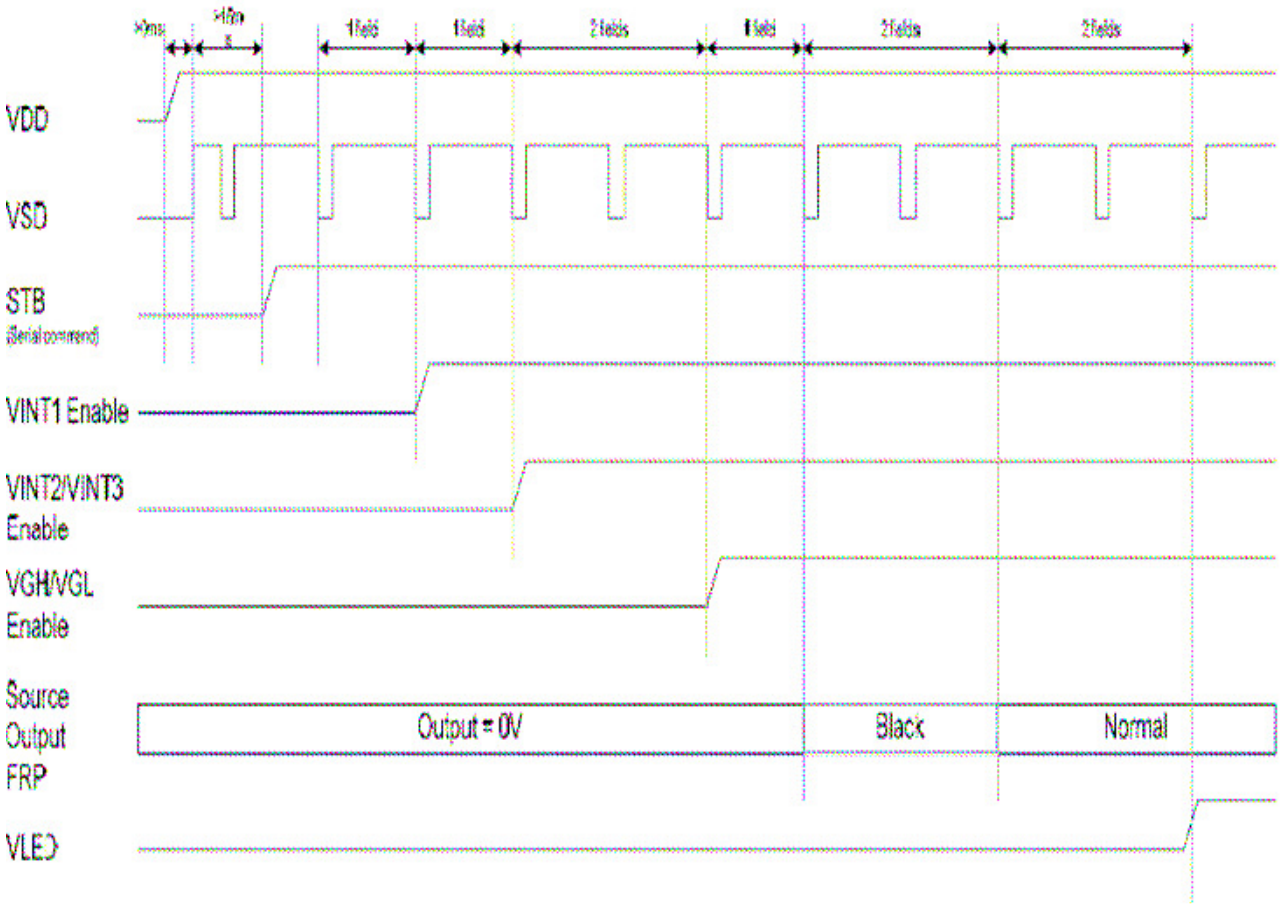
D7	VGHL ENB Function
0	VGH/VGL Charge pump enable (Default)
1	VGH/VGL Charge pump disable, for external VGH/VGL application

*Don’t apply external power to VGH and VGL pad when SHDB2=0 and VGHL_ENB=0

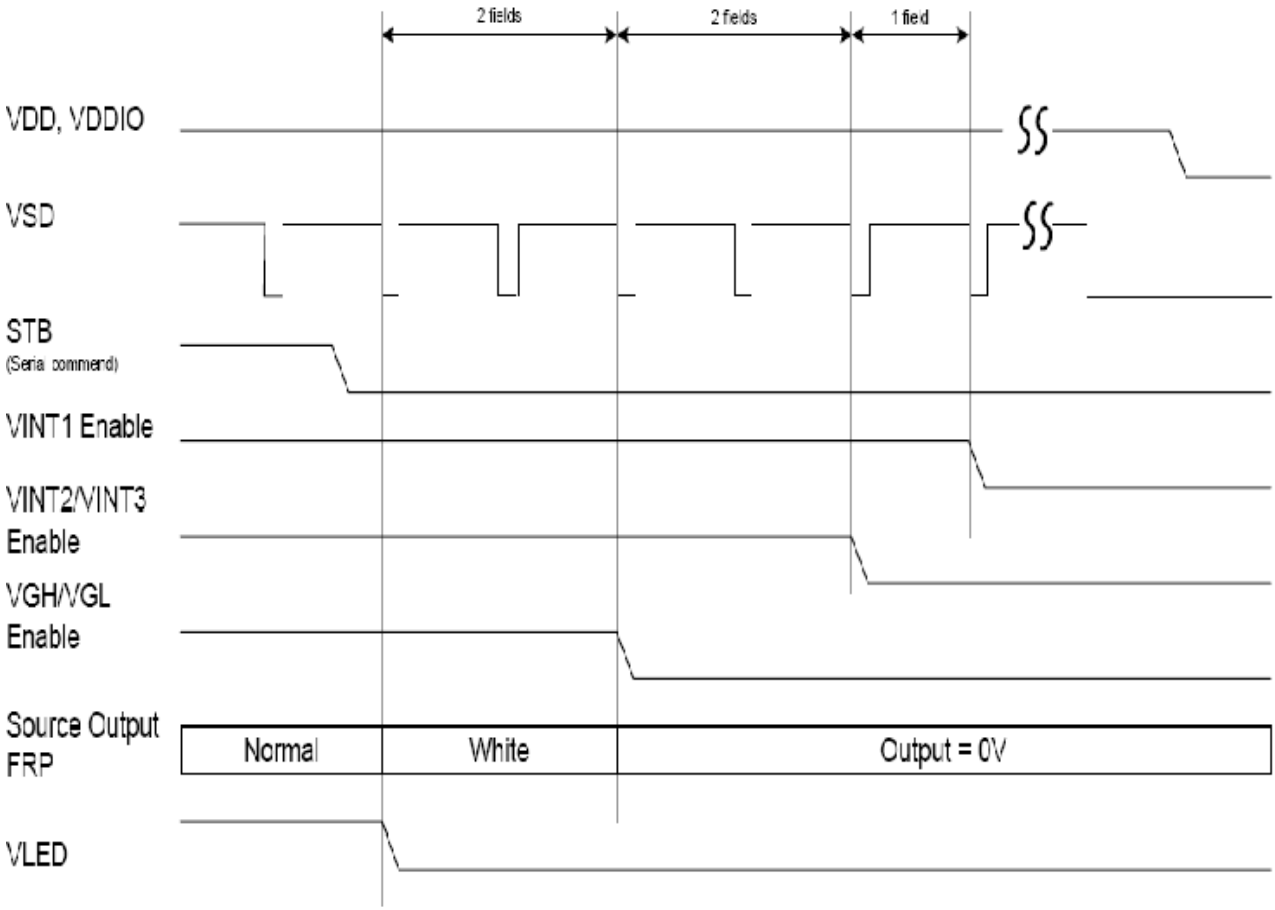
7. Power On/Off Sequence

Special care should be taken that the large current may cause a permanent damage to the LSI when voltage is applied to the LCD drive power supply terminals in the condition that the logic power supply terminals are floating.

The following sequences are recommended from the power supply ON to the image display.



The following sequences are recommended from the image display to the power supply OFF.

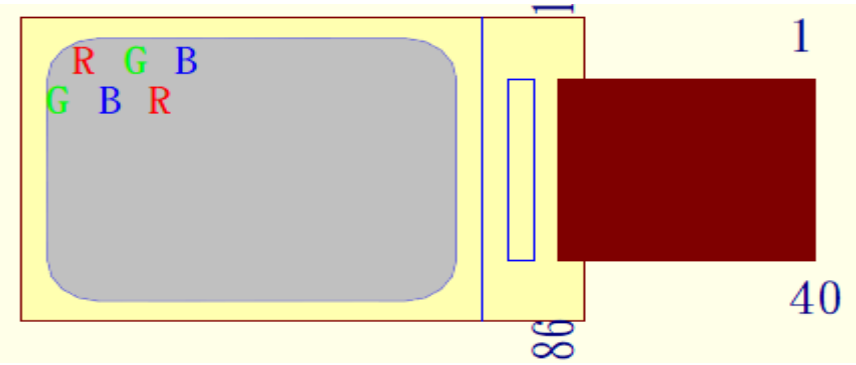


8. Block Diagram

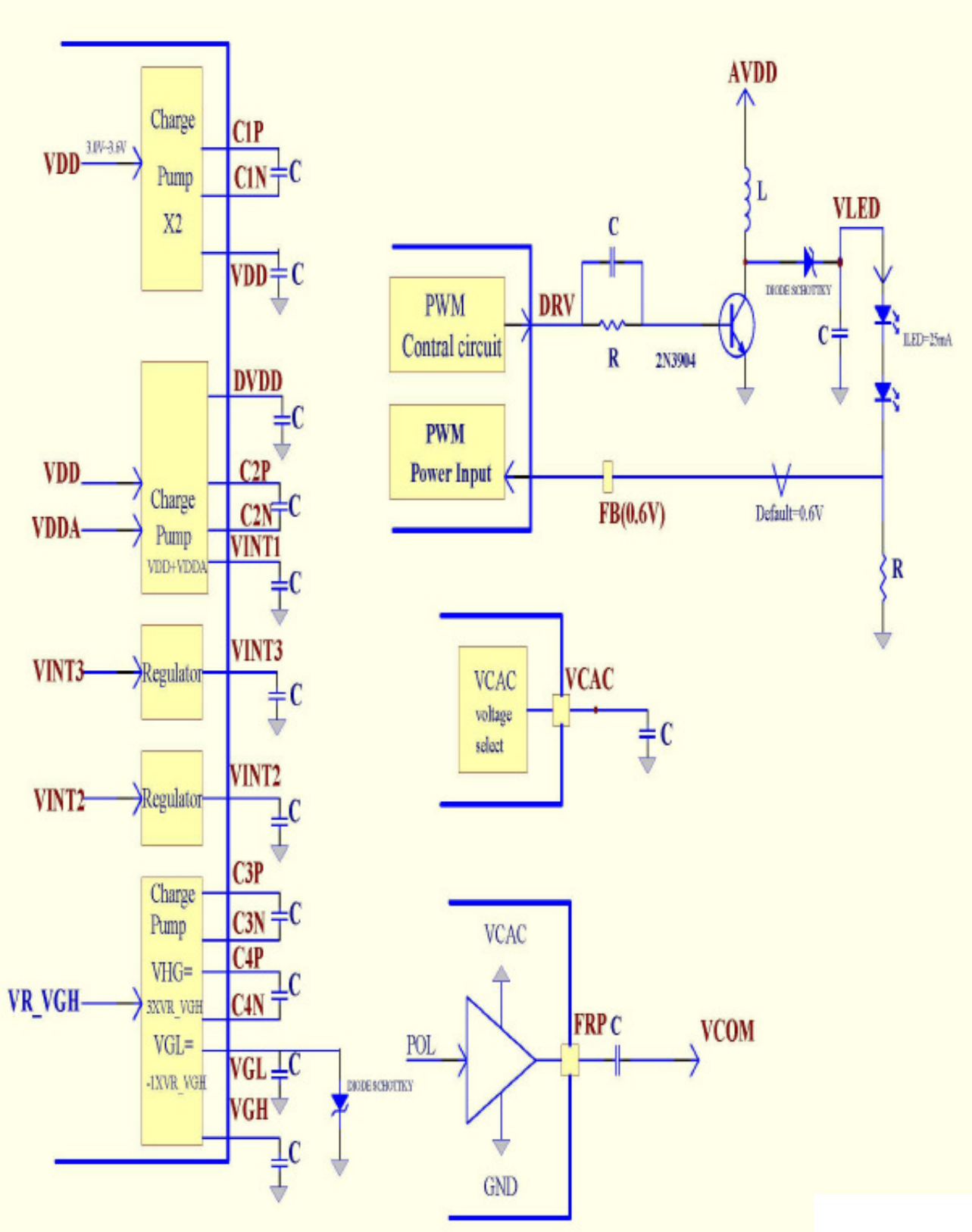
8.1 Display Color and Gray Scale Reference

Color		Input Color Data																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

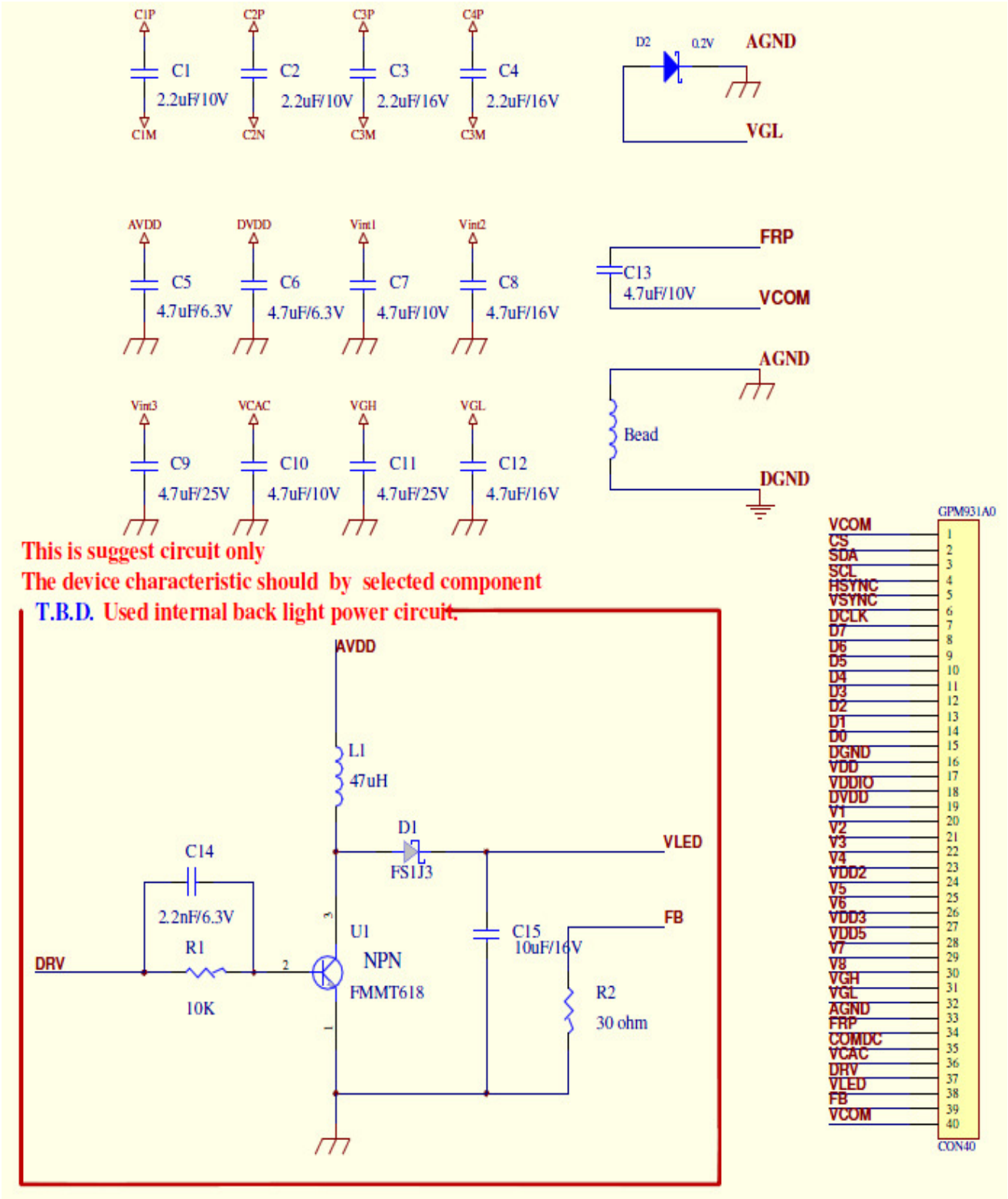
8.2 Pixel Arrangement and Input Pin Connector No.



8.3 Reference Circuit for LCD Module



8.4 Reference Application Note



9. Backlight

9.1 Standard Lamp Styles (Edge Lighting Type):

The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:

9.2 The Main Advantages of the LED Backlight are as Following:

The brightness of the backlight can simply be adjusted.
By a resistor or a potentiometer.

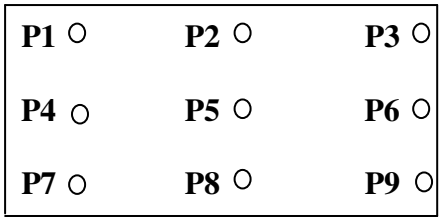
9.3 Data About LED Backlight:

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
LED Voltage	VLED	6.4	-	7.0	V	
LED Current	I_F	-	25	-	mA	2pcs LED
Feedback Voltage	V_{FB}		0.6		V	

NOTE:

1. Test Instrument : BM-7 (Distance=500mm ; Field =1°)
2. Light Source : LED * 2White)
3. Conditions : I_F=25mA, VLED=6.4V~7.0V
4. Uniformity : (Min. Brightness / Max. Brightness) *100%
5. Uniformity ≧ 70%

9.4 Measured Method:



(Effective spatial Distribution)
Hole Diameter±1ø ; 1 to 9per Position Measured Luminous

10. Reliability

10.1 MTTF

The LCD module shall be designed to meet a minimum MTTF value of 50,000 hours with normal condition. (25°C in the room without sunlight; not include lifetime of backlight).

10.2 Tests

No.	Item	Condition	Criterion
1	High Temperature Operating	+60°C 240hrs	◦ No defect of operational function in room temperature are allowable (23±5°C). ◦ Leakage current should be below double of initial value.
2	Low Temperature Operating	-10°C 240hrs	
3	High Temperature Non-Operating	+80°C 240hrs	
4	Low Temperature Non-Operating	-25°C 240hrs	
5	High Temperature / Humidity Non-Operating	60°C ; 90%RH ; 240hrs	
6	Temperature Shock Non-Operating	-20°C ←→ 70°C (30min) (5min) (30min) 100 Cycles	
7	Electro-Static Discharge Test Non-Operating	HBM: ±2kV	

8	Vibration Test	5~500HZ 0.015G2/Hz, 2~5Hz,500~600Hz±6dB/Oct, 1hr/axis(Unit:Case)	
9	Mechanical Shock	100G,6ms, ±X, ±Y, ±Z 3times for each direction	
10	Vibration (with carton)	Random Vibration $0.015G^2/H_Z$ form 5~200H_Z -6dB/Octave from 200~500H_Z	
11	Drop (with carton)	Height : 60 cm 1 corner,3edges,6surfaces	

Note 1: Test after 24 hours in room temperature (23±5°C).
Note 2: The sampling above is individually for each reliability testing condition.
Note 3: The color fading of polarizing filter should not care.
Note 4: All of the reliability testing chamber above, is using D.I. water.
(Min value:1.0 MΩ-cm)
Note 5: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.