i510x

CompactFlash Memory Card Controller Datasheet

Version 1.3

iCreate Technologies Corporation

Data sheet marking

iCreate uses various markings in the data sheet to designate each document phase as it relates to the product development stage.

Marking	**Description**
Objective Specification	The objective specification contains data for new product development.
Advance Information	The information is on products in the design phase. Your designs should not be finalized with this information.
Preliminary	This is preliminary information on new products but not yet fully characterized. The specifications in these data sheets are subject to change in any manner without notice.
No Marking	Information contained in the data sheet is on products in full production.

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1. Introduction

General description

i510X is a high performance flash memory controller for CompactFlash/ATA interface memory devices. This chip is based on iCreate 2nd-generation flash engine to achieve high data transfer rate. The enhanced designs include high-speed RISC CPU, multi-bank flash access, 8/16-bit flash interface, and ECC capability. Power-on-reset, RC oscillator and LDO regulator are integrated to reduce BOM cost and PCB area. Typical applications of i510X are CompactFlash memory card, IDE flash disk module/chip and PCMCIA flash card.

Features

- Compliant to CompactFlash, PCMCIA, and ATA standards
- 8-bit/16-bit host data transfer
- Support PIO mode 4
- 5V and 3.3V host interface
- Integrated power-on-reset, RC oscillator and LDO regulator
- On-the-fly ECC
- Wear-leveling mechanism
- Support Samsung 2KB/page BLC NAND flash
- Number of flash chips:
  - i5100: 8 chips
  - i5101: 16 chips
- Package:
  - i5100: TQFP 100 pin
  - i5101: TQFP 128 pin

Block diagram

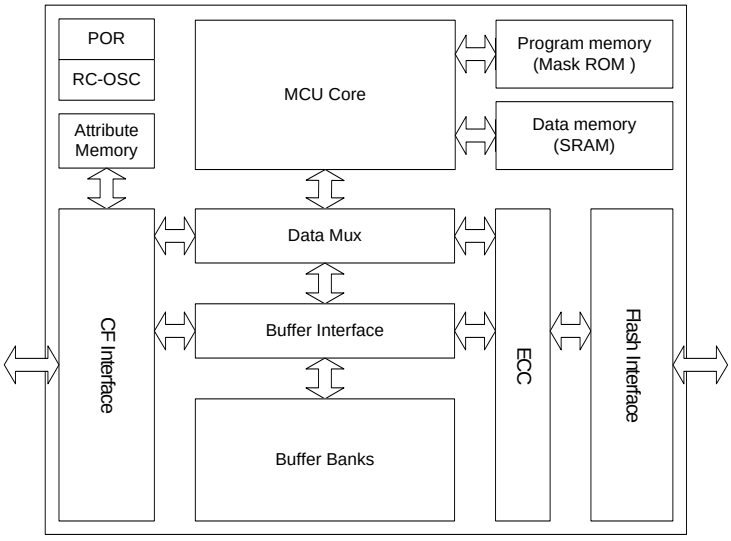


Figure 1. Block diagram

2. Pin configuration and definition

2.1. Pin diagrams

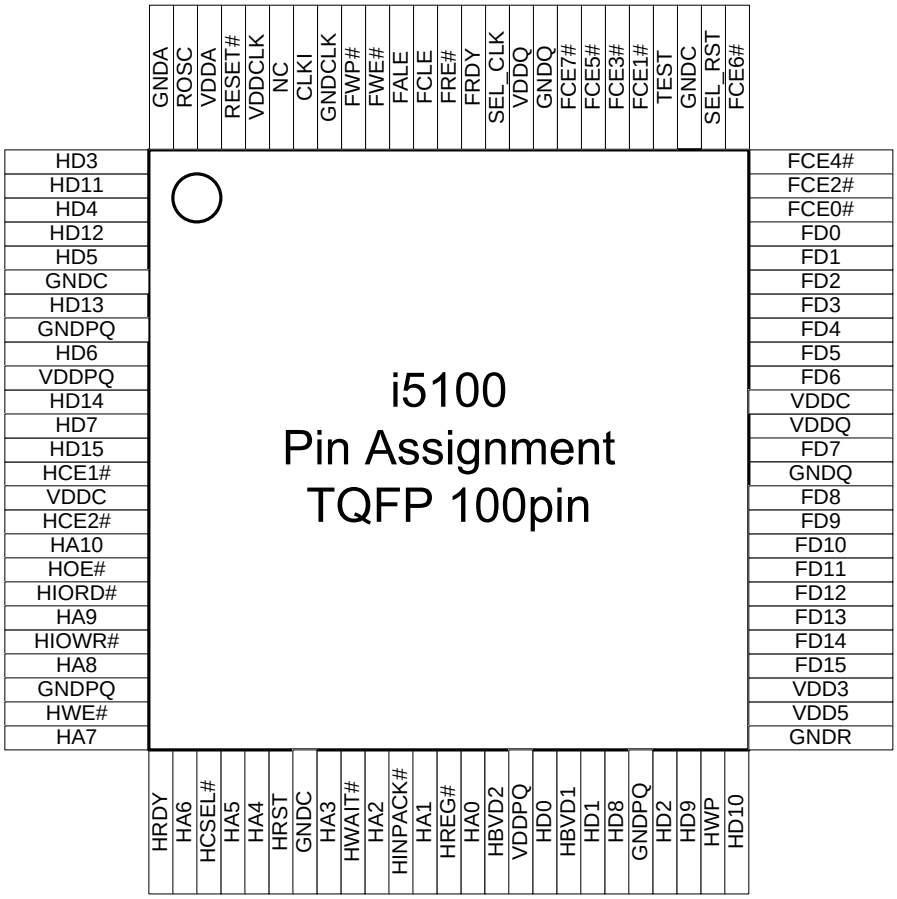


Figure 2. 100-pin configuration

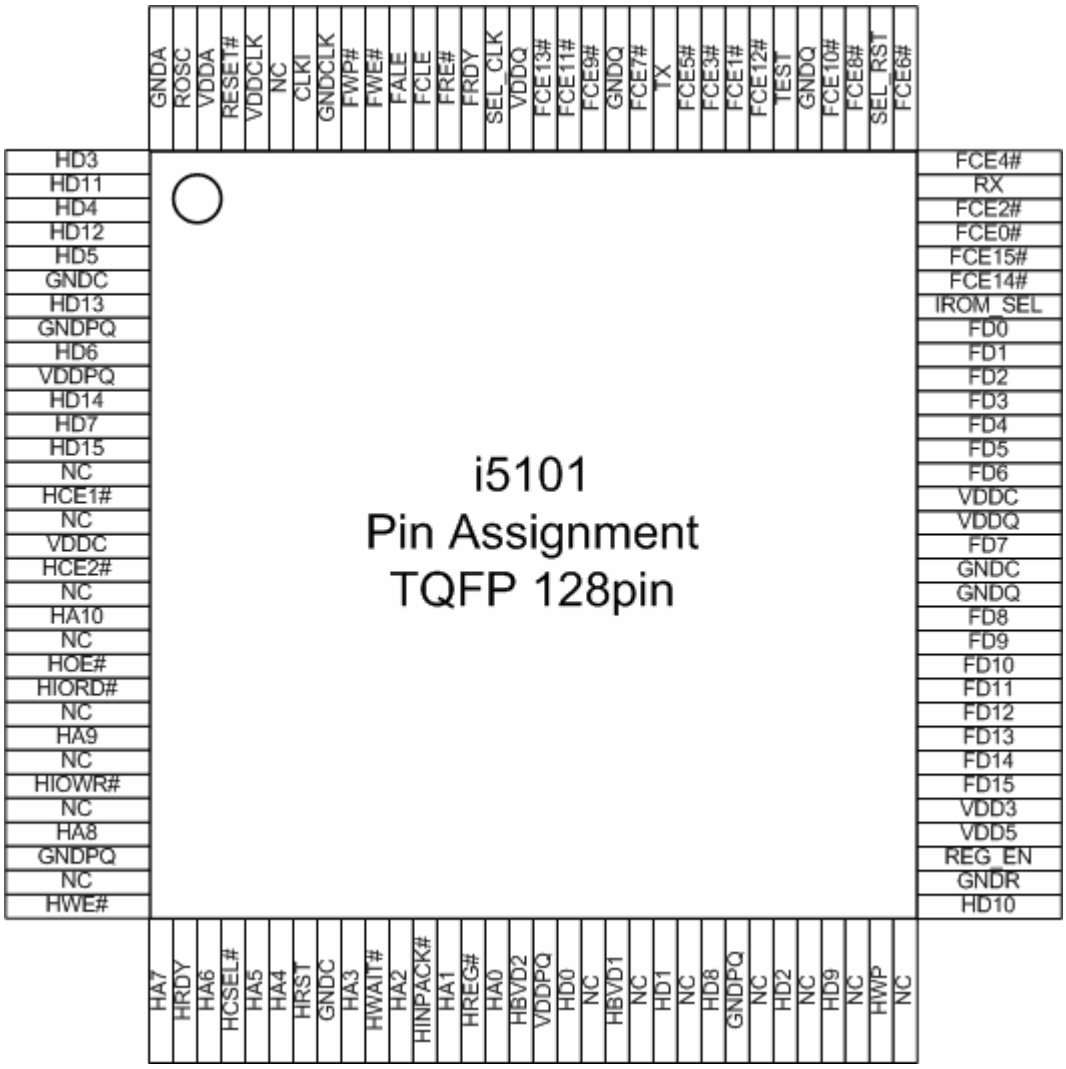


Figure 3. 128-pin configuration

2.2. Pin function

Host interface

Pin Name	Pin No. (100pin)	Pin No. (128pin)	Type	Function (Refer to CF Specification)
HA0 ~ HA10	17, 20, 22, 25, 27, 29, 30, 33, 35, 37, 39	20, 25, 29, 33, 35, 37, 38, 41, 43, 45, 47	5V/3.3V In, Schmitt Trigger	HA0 ~ HA10 (PC Card Memory Mode) HA0 ~ HA10 (PC Card I/O Mode) HA0 ~ HA2 (True IDE Mode)
HBVD1	43	52	5V/3.3V In/Out, Schmitt Trigger, 4mA	BVD1 (PC Card Memory Mode) STSCHG# (PC Card I/O Mode) PDIAG# (True IDE Mode)
HBVD2	40	48	5V/3.3V In/Out, Schmitt Trigger, 4mA	BVD2 (PC Card Memory Mode) SPKR# (PC Card I/O Mode) DASP# (True IDE Mode)

HCE1#, HCE2#	14, 16	15, 18	5V/3.3V In, Schmitt Trigger, Pull up	CE1#, CE2# (PC Card Memory Mode) CE1#, CE2# (PC Card I/O Mode) Card Enable CS0#, CS1# (True IDE Mode)
HCSEL#	28	36,	5V/3.3V In, Schmitt Trigger, Pull up	CSEL# (PC Card Memory Mode) CSEL# (PC Card I/O Mode) CSEL# (True IDE Mode)
HD0 ~ HD15	1, 2, 3, 4, 5, 7, 9, 11, 12, 13, 42, 44, 45, 47, 48, 50	1, 2, 3, 4, 5, 7, 9, 11, 12, 13, 50, 54, 56, 59, 61, 65	5V/3.3V In/Out, Schmitt Trigger, 8mA	HD0 ~ HD15 (PC Card Memory Mode) HD0 ~ HD15 (PC Card I/O Mode) HD0 ~ HD15 (True IDE Mode)
HINPACK#	36	44	5V/3.3V Output, 4mA	INPACK# (PC Card Memory Mode) INPACK# (PC Card I/O Mode) INPACK# (True IDE Mode)
HIORD#	19	23	5V/3.3V In, Schmitt Trigger, Pull up	IORD# (PC Card Memory Mode) IORD# (PC Card I/O Mode) IORD# (True IDE Mode)
HIOWR#	21	27	5V/3.3V In, Schmitt Trigger, Pull up	IOWR# (PC Card Memory Mode) IOWR# (PC Card I/O Mode) IOWR# (True IDE Mode)
HOE#	18	22	5V/3.3V In, Schmitt Trigger, Pull up	OE# (PC Card Memory Mode) OE# (PC Card I/O Mode) ATASEL# (True IDE Mode)
HRDY	26	34	5V/3.3V Output, 4mA	RDY/BSY# (PC Card Memory Mode) IREQ# (PC Card I/O Mode) INTRQ (True IDE Mode)
HREG#	38	46	5V/3.3V In, Schmitt Trigger, Pull up	REG# (PC Card Memory Mode) REG# (PC Card I/O Mode) REG# (True IDE Mode)
HRST	31	39	5V/3.3V In, Schmitt Trigger, Pull up	RESET (PC Card Memory Mode) RESET (PC Card I/O Mode) RESET# (True IDE Mode)
HWAIT#	34	42	5V/3.3V Output, 4mA	WAIT# (PC Card Memory Mode) WAIT# (PC Card I/O Mode) IORDY (True IDE Mode)
HWE#	24	32	5V/3.3V In, Schmitt Trigger, Pull up	WE# (PC Card Memory Mode) WE# (PC Card I/O Mode) WE# (True IDE Mode)
HWP	49	63	5V/3.3V In, Schmitt Trigger	WP (PC Card Memory Mode) IOIS16# (PC Card I/O Mode) IOIS16# (True IDE Mode)

Flash interface

Pin Name	Pin No. (100)	Pin No. (128)	Type	Function

FD0 ~ FD15	54, 55, 56, 57, 58, 59, 60, 61, 63, 66, 67, 68, 69, 70, 71, 72	70, 71, 72, 73, 74, 75, 76, 77, 80, 83, 84, 85, 86, 87, 88, 89	In/Out, 3mA	Flash Data Bus 0 ~ 7. Connect to flash memory pins FD0 ~ FD7.
FALE	90	118	Out, 3mA	Flash Address Latch Enable. Connect to flash memory pin ALE
FCLE	89	117	Out, 3mA	Flash Command Latch Enable. Connect to flash memory pin CLE
FRE#, FWE#	88 , 91	116, 119	Out, 3mA	Flash Read/Write Enable. Connect to flash memory pin RE/WE.
FCE0# ~ FCE7#	73, 74, 75, 76, 80, 81, 82, 83	93, 94, 96, 97, 104, 105, 106, 108	Out, 2mA	Flash Chip Enable. Connect to flash memory pin CE.
FCE8# ~ FCE15#	-	91, 92, 99, 100, 103, 110, 111, 112,	Out, 2mA	Flash Chip Enable. Connect to flash memory pin CE.
FWP#	92	120	Out, 3mA	Flash Write-Protect. Connect to flash memory pin WP.
FRDY	87	115	In	Flash Ready/BSY signal. Connect to flash memory pin Ready/Busy#.

System interface & power pins

Pin Name	Pin No. (100)	Pin No. (128)	Type	Function
SEL_CLK	86	114	In	Connected to 3.3V to select internal oscillator, or GND for external clock.
SEL_RST	77	98	In	Connected to 3.3V to select internal power-on-reset or GND for external reset
TEST	79	102	In	Test mode enable pin. Connected to GND.
RX	-	95	In	Test pin. Connected to 3.3V or GND.
TX	-	107	Out, 3mA	Test pin. Not connected.
CLKI	94	122	In	Clock input
RESET#	97	125	In	Reset input if reset is provided externally. If SEL_RST is high, this pin is connected to GND through a capacitor.
ROSC	99	127	Analog In	Connected to the same power source as VDDA through a resistor to configure oscillator frequency
REG_EN	-	67	In	Regulator enable
IROM_SEL	-	90	In	Test pin. Connected to 3.3V or NC.

VDDPQ	10, 41	10, 49,		Power for CF interface (3.3V or 5V)
GNDPQ	8, 23, 46	8, 30, 57		Ground for CF interface
VDDQ	64, 85	81, 113		3.3V power for flash interface
GNDQ	62, 84	78, 101, 109		Ground for flash interface
VDDC	15, 65,	17, 82		3.3V power for core
GNDC	6, 32, 78	6, 40, 79		Ground for core
VDD5	52	68		Power input for LDO regulator (3.3V or 5V)
VDD3	53	69	O	3.3V LDO regulator output
GNDR	51	66		Ground for LDO regulator
VDDA	98	126		3.3V power for reset circuit
GNDA	100	128		Ground for analog circuit
VDDCLK	96	124		3.3V power for oscillator
GNDCLK	93	121		Ground for oscillator

3. Reset voltage detector and RC oscillator

Power-on-reset and brown-out-reset

The internal reset control unit has power-on-reset (POR) and brown-out-reset (BOR) functions. To use internal POR, set SEL_RST to 1 and RESET# must be connected to an external capacitor as shown in Fig. 3. To use external reset signal, set SEL_RST to 0 and RESET# becomes the reset signal input.

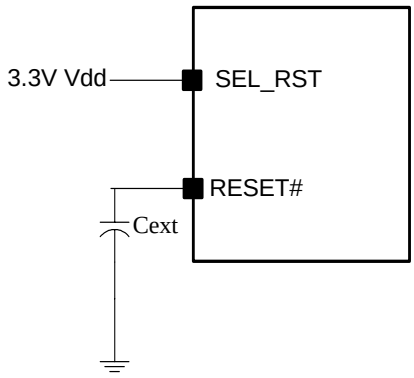


Figure 3. Pin connection to use internal power-on-reset/brown-out-reset

Internal RC oscillator

An integrated RC oscillator can be used to reduce BOM cost. When the internal oscillator is enabled, ROSC must be connected to 3.3V through a resistor, as shown in Figure 4, while CLKI is not connected. The value of Rext determines the oscillator frequency. The relationship of Rext and typical oscillator frequency is as follows.

Rext	15KΩ	22KΩ	30KΩ	58KΩ
Fosc	50MHz	40MHz	33MHz	20MHz

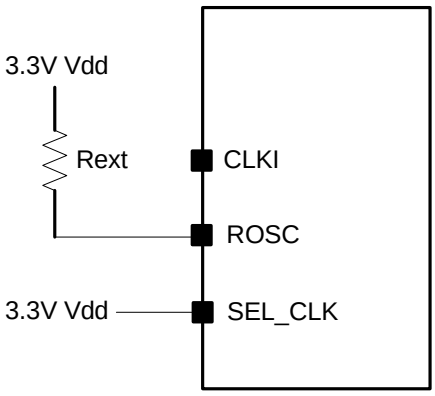


Figure 4. Pin connection to use internal Oscillator

4. Electrical specifications

Absolute maximum ratings

Symbol	Description	Value	Unit	Notes
V_{CC}	V_{CC} Voltage	- 0.3 to +6.5	V	VDDPQ
V_{DD}	V_{DD} Voltage	- 0.3 to +4.6	V	VDDC, VDDQ
V_{IN}, V_{OUT}	All input/output voltages	- 0.3 to VCC + 0.3	V	CF interface
V_{IN}, V_{OUT}		- 0.3 to VDD + 0.3	V	Other I/O except CF interface
Tstg	Storage temperature range	- 25 to +125	°C	

Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	V_{CC} voltage	4.5	5	5.5	V
		3.15	3.3	3.45	V
V_{DD}	V_{DD} voltage	3.15	3.3	3.45	V
T_{OPR}	Operating temperature	0		70	^{o}C

DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH3}	High level input voltage for 3.3V domain	2.4			V
V_{IL3}	Low level input voltage for 3.3V domain			0.6	V
V_{OH3}	High level output voltage for 3.3V domain	2.4			V
V_{OL3}	Low level output voltage for 3.3V domain			0.4	V
V_{IH53}	High level input voltage for 5V domain under 3.3V	2.4			V
V_{IL53}	Low level input voltage for 5V domain under 3.3V			0.6	V
V_{OH53}	High level output voltage for 5V domain under 3.3V	Vcc-0.8			V
V_{OL53}	Low level output voltage for 5V domain under 3.3V			0.4	V

V_{IH55}	High level input voltage for 5V domain under 5V	4.0			V
V_{IL55}	Low level input voltage for 5V domain under 5V			0.8	V
V_{OH55}	High level output voltage for 5V domain under 5V	Vcc-0.8			V
V_{OL55}	Low level output voltage for 5V domain under 5V			0.4	V

Power-on-reset characteristics

Symbol	Parameter	Typ.	Unit
V_T(POR)	Threshold voltage of power-on-reset	2.8	V
V_T(BOR)	Threshold voltage for brown-out-reset	2.6	V

CF attribute memory read and write AC characteristics

For the definitions of parameters, please refer to CompactFlash Specification Rev. 2.1.

Symbol	Parameter	Min.	Max.	Unit
tcR	Read cycle time	300		Ns
ta(A)	Address access time		300	Ns
ta(CE)	Card Enable access time		300	ns
ta(OE)	Output Enable access time		150	ns
tdis(CE)	Output disable time from CE		100	ns
tdis(OE)	Output disable time from OE		100	ns
tsu(A)	Address setup time	30		ns
ten(CE)	Output enable time from CE	5		ns
ten(OE)	Output enable time from OE	5		ns
tv(A)	Data valid time from address change	0		ns
tcW	Write cycle time	250		ns
tw(WE)	Write pulse width	150		ns
trec(WE)	Write recovery time	30		ns
tsu(D-WEH)	Data setup time for WE	80		ns
th(D)	Data hold time	30		ns

Common memory read and write AC characteristics

For the definitions of parameters, please refer to CompactFlash Specification Rev. 2.1.

Symbol	Parameter	Min.	Max.	Unit
ta(OE)	Output Enable access time		125	ns
tdis(OE)	Output disable time from OE		100	ns
tsu(A)	Address setup time	30		ns
th(A)	Address hold time	20		ns
tsu(CE)	Card Enable setup time	0		ns
th(CE)	Card Enable hold time	20		ns
tw(WT)	Wait width time		3000	ns
tw(WE)	Write pulse time	150		ns
tsu(D-WEH)	Data setup time for WE	80		ns
th(D)	Data hold time	30		ns
trec(WE)	Write recover time	30		ns
tv(WT-OE)	Wait delay falling from OE		35	ns
tv(D-WT)	Data setup for wait release		0	Ns
tv(WT-WE1)	Wait delay falling from WE		35	ns
tv(WT-WE2)	WE high from wait release	0		ns

I/O access read and write AC characteristics

For the definitions of parameters, please refer to CompactFlash Specification Rev. 2.1.

Symbol	Parameter	Min.	Max.	Unit
td(IORD)	Data delay after IORD		100	ns
th(IORD)	Data hold time following IORD	0		ns
tw(IORD)	IORD pulse width	165		ns
tsuA(IORD)	Address setup time for IORD	70		ns
thA(IORD)	Address hold time from IORD	20		ns
tsuCE(IORD)	Card Enable setup time for IORD	5		ns
thCE(IORD)	Card Enable hold time from IORD	20		ns
tsuREG(IORD)	REG setup time for IORD	5		ns
thREG(IORD)	REG hold time from IORD	0		ns
tdfINP(IORD)	INPACK delay falling from IORD	0	45	ns
tdrINP(IORD)	INPACK delay rising from IORD		45	ns
tdfIO16(IORD)	IOIS16 delay falling from address		35	ns
tdrIO16(IORD)	IOIS16 delay rising from address		35	ns
tdWT(IORD)	Wait delay falling from IORD		35	ns

td(WT)	Data delay from wait rising		0	ns
tsu(IOWR)	Data setup time for IOWR	60		ns
th(IOWR)	Data hold time from IOWR	30		ns
tw(IOWR)	IOWR pulse width	165		ns
tsuA(IOWR)	Address setup time for IOWR	70		ns
thA(IOWR)	Address hold time from IOWR	20		ns
tsuCE(IOWR)	Card Enable setup time for IOWR	5		ns
thCE(IOWR)	Card Enable hold time from IOWR	20		ns
tsuREG(IOWR)	REG setup time for IOWR	5		ns
thREG(IOWR)	REG hold time from IOWR	0		ns
tdWT(IOWR)	Wait delay falling from IOWR		35	ns
tdrIOWR(WT)	IOWR high from wait high	0		ns
tw(WT)	Wait width time		3000	ns

True-IDE mode I/O access read and write AC characteristics

For the definitions of parameters, please refer to CompactFlash Specification Rev. 2.1.

Symbol	Parameter	Min.	Max.	Unit
t0	Cycle time	120		ns
t1	Address valid to IORD/IOWR setup	25		ns
t2	IORD/IOWR	70		ns
t2	IORD/IOWR register (8bit)	70		ns
t3	IOWR data setup	20		ns
t4	IOWR data hold	10		ns
t5	IORD data setup	20		ns
t6	IORD data hold	5		ns
t6Z	IORD data tri-state		30	ns
t9	IORD/IOWR to address valid hold	10		ns
tRD	Read data valid to IORDY active, if IORDY initially low after tA	0		ns
tA	IORDY setup time	35		ns
tB	IORDY pulse width		1250	ns
tC	IORDY assertion to release		5	ns

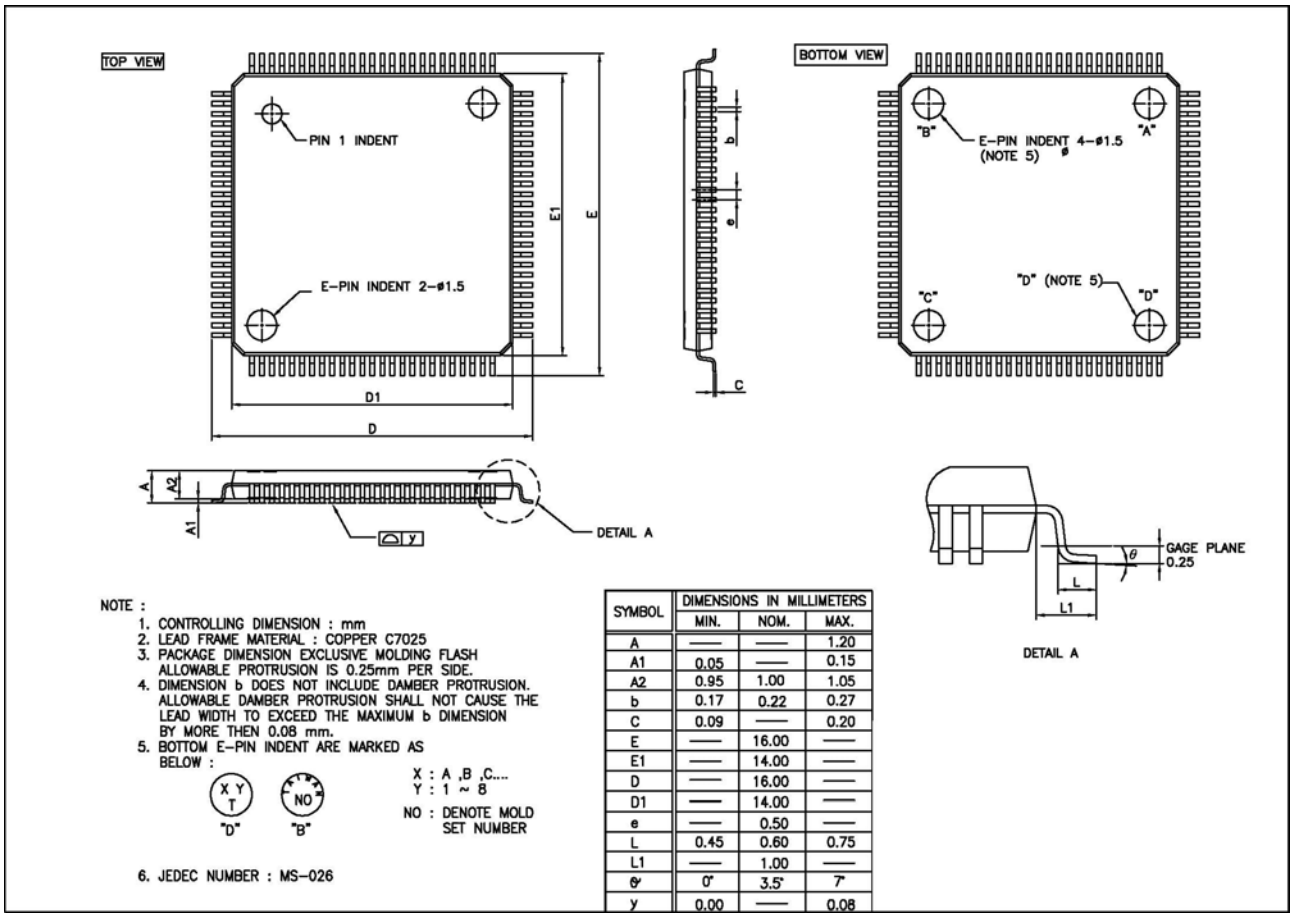
Read/write timing for NAND type flash

For the definition of parameters, please refer to Toshiba flash datasheet.

Symbol	Parameter	Min.	Max.	Unit
tCLS	FCLE setup time	0		ns
tCLH	FCLE hold time	10		ns
tCS	FCE# setup time	0		ns
tCH	FCE# hold time	10		ns
tCEH	FCE# high hold time	100		ns
tWP	FWE# pulse width	25		ns
tALS	FALE setup time	0		ns
tALH	FALE hold time	10		ns
tDS	Data Setup time	20		ns
tDH	Data hold time	10		ns
tWH	FWE# high hold time	15		ns
tWW	FWP high to FWE# low	100		ns
tRR	Ready-to-FRE# Falling edge	20		ns
tRP	FRE# pulse width	25		ns
tREH	FRE# high hold time	15		ns
tRHW	FRE# high to FWE# low	0		ns
tWHC	FWE# high to FCE# low	30		ns
tWHR	FWE# high to FRE# low	60		ns
tAR	FALE low to FRE# low	10		ns
tCLR	FCLE low to FRE# low	10		ns

5. Package dimensions

100 Pin package



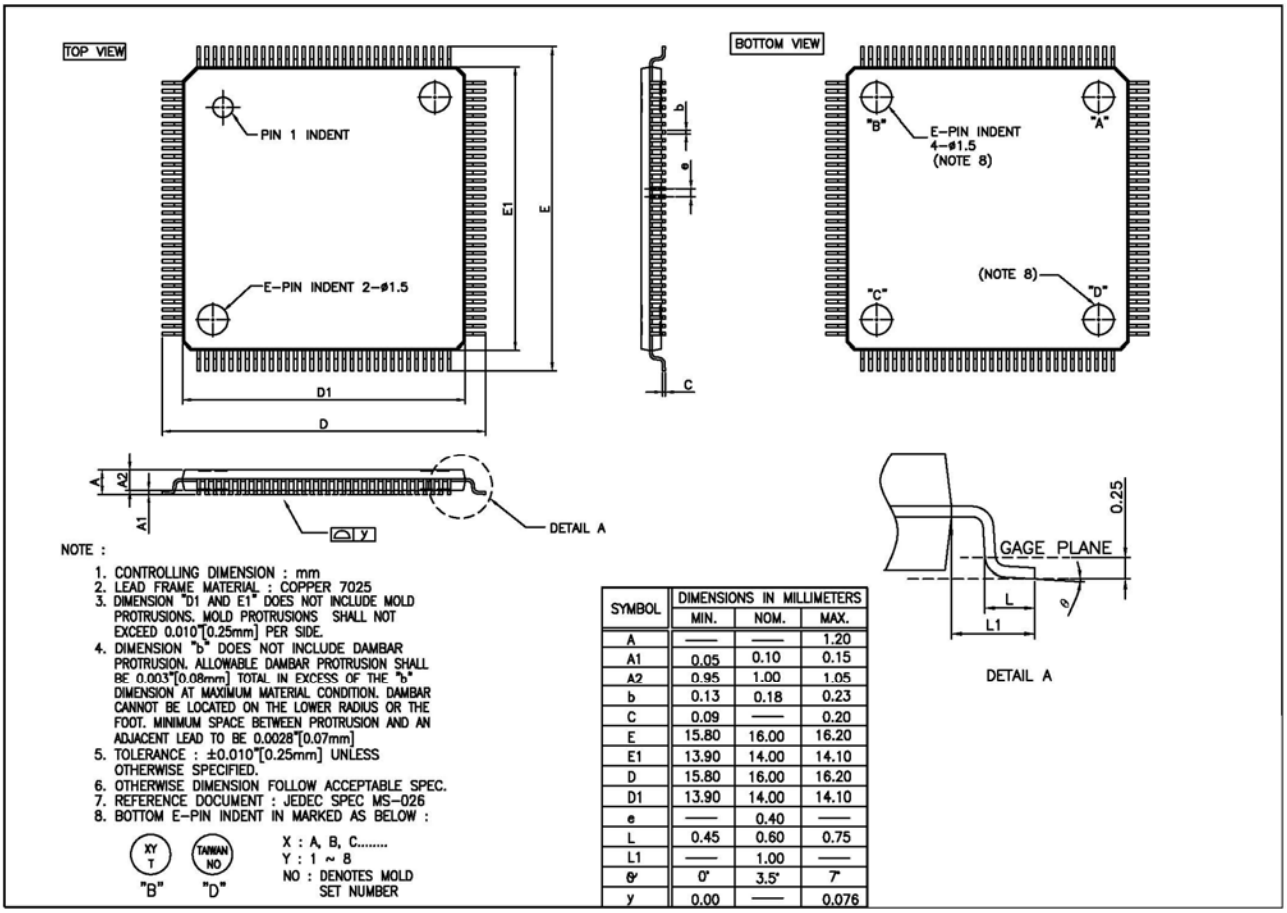
NOTE :
1. CONTROLLING DIMENSION : mm
2. LEAD FRAME MATERIAL : COPPER C7025
3. PACKAGE DIMENSION EXCLUSIVE MOLDING FLASH ALLOWABLE PROTRUSION IS 0.25mm PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. ALLOWABLE DAMBER PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08 mm.
5. BOTTOM E-PIN INDENT ARE MARKED AS BELOW :

X : A ,B ,C....
Y : 1 ~ 8
NO : DENOTE MOLD SET NUMBER

6. JEDEC NUMBER : MS-026

SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
C	0.09	—	0.20
E	—	16.00	—
E1	—	14.00	—
D	—	16.00	—
D1	—	14.00	—
e	—	0.50	—
L	0.45	0.60	0.75
L1	—	1.00	—
θ	0°	3.5°	7°
y	0.00	—	0.08

128 Pin package



NOTE :

1. CONTROLLING DIMENSION : mm
2. LEAD FRAME MATERIAL : COPPER 7025
3. DIMENSION "D1 AND E1" DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-026
8. BOTTOM E-PIN INDENT IN MARKED AS BELOW :

X : A, B, C.....
Y : 1 ~ 8
NO : DENOTES MOLD SET NUMBER

SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	——	——	1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.13	0.18	0.23
C	0.09	——	0.20
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
e	——	0.40	——
L	0.45	0.60	0.75
L1	——	1.00	——
θ	0°	3.5°	7°
y	0.00	——	0.076