# i5141-TG

## SD/MMC Memory Card Controller Datasheet

**Version 1.1**

**iCreate Technologies Corporation**

**2006/9/28**

**Data sheet marking**

iCreate uses various markings in the data sheet to designate each document phase as it relates to the product development stage.

| **Marking** | **Description** |
|---|---|
| Objective Specification | The objective specification contains data for new product development. |
| Advance Information | The information is on products in the design phase. Your designs should not be finalized with this information. |
| Preliminary | This is preliminary information on new products but not yet fully characterized. The specifications in these data sheets are subject to change in any manner without notice. |
| No Marking | Information contained in the data sheet is on products in full production. |

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## Revision History

| Date | Revision | Description |
|---|---|---|
| 2006/9/25 | 1.0 | Initial release version |
| 2006/9/28 | 1.1 | Update new package outline |
| | | |

# 1. Introduction

## 1.1. General description

i5141-TG is a high performance flash memory controller for SD/MMC interface flash memory cards. This chip is based on iCreate 3rd-generation flash engine to achieve high data transfer rate. The enhanced designs include high performance CPU, multi-bank flash access, 8/16-bit flash interface, and Reed-Solomon based ECC capability. Voltage-Regulator, Power-on-reset and RC oscillator are integrated to reduce BOM cost and PCB area. Typical applications of i5141-TG are SD, miniSD, MMC and RS-MMC memory card.

## 1.2. Features

- Compliant to SD1.1, MMC4.1 standards
- 1/4/8-bit host data transfer
- SD/MMC Clock frequency 0 ~ 52 MHz
- Integrated power-on-reset and RC oscillator
- On-the-fly ECC (4 Byte per 528 Byte)
- Wear-leveling mechanism
- Support large block NAND type flash
- Support small block NAND type flash
- Support AG-AND type flash
- 4 flash chips enable
- Auto-suspend to conserve energy

## 1.3. Block diagram

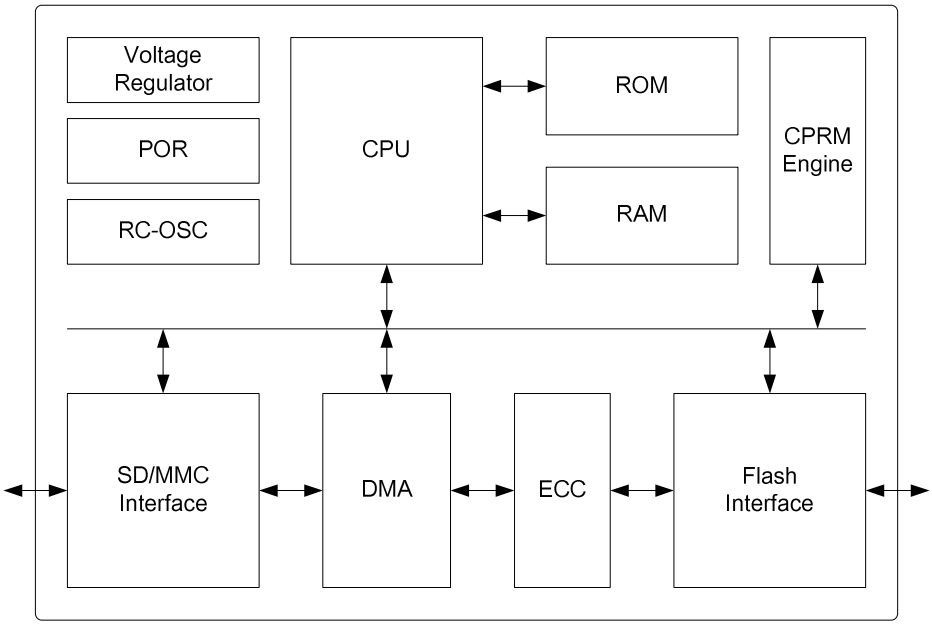



Figure 1. Block diagram

# 2. Pin Diagram and Description

## 2.1. Pin Diagram

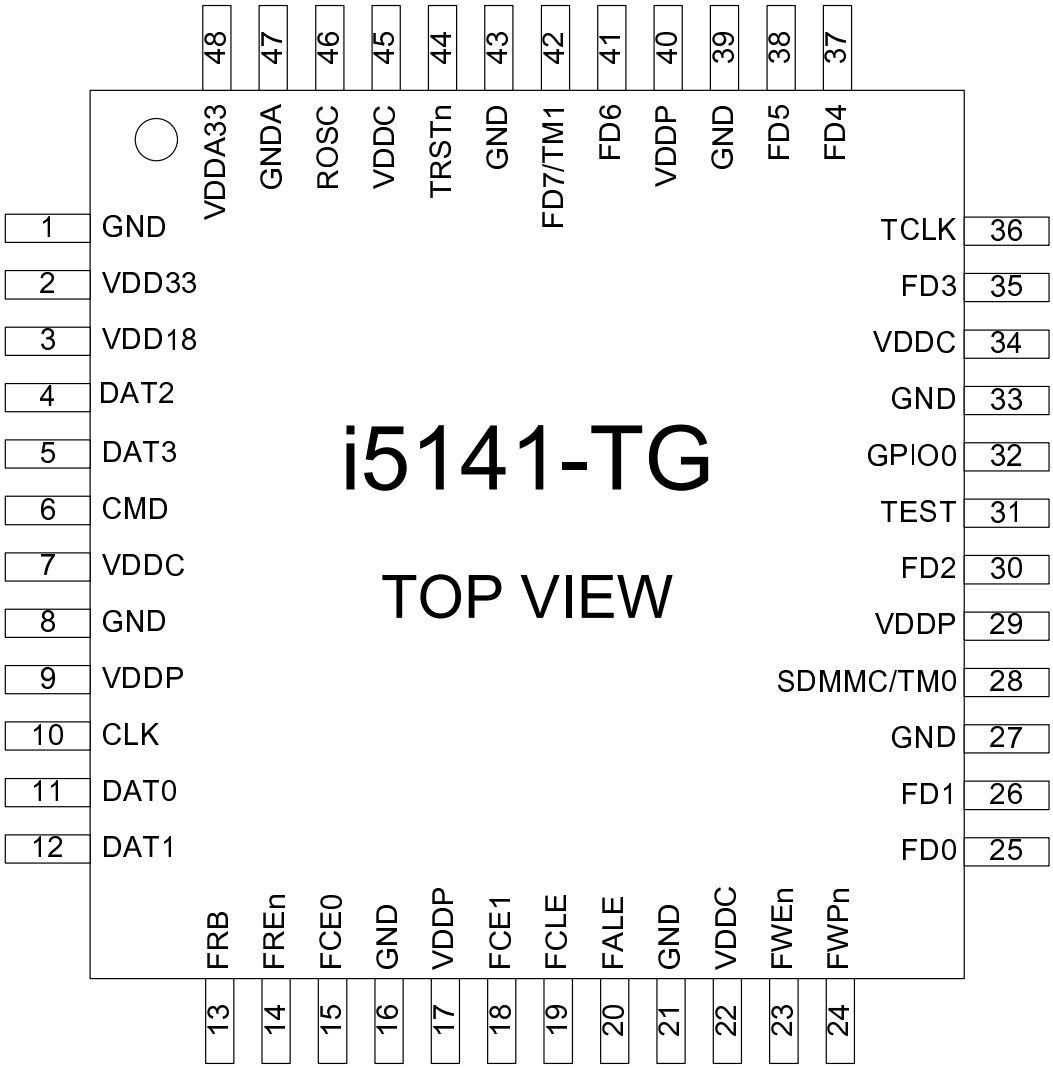



Figure 2. Pin Diagram

## 2.2. Pin Description

| Pin Name | Type*1 | Description |
|---|---|---|
| VDD33 | Power | Internal regulator 3.3V input pin. |
| VDD18 | Power | Internal regulator 1.8V output pin. |
| VDDC | Power | 1.8V power supply for core. |
| VDDP | Power | 3.3V power supply for I/O. |
| GND | Power | Power supply ground. |
| VDDA33 | Power | 3.3V power supply for analog block. |
| GNDA | Power | Power supply ground for analog block. |
| ROSC | Analog | Connect 3.9K Ohm resister to VDD18 for internal 50MHz clock generator. |
| DAT0~3 | IO/ST/PUC | SD/MMC Data Bus |
| CMD | IO/ST/PUC | SD/MMC Command/Response signal |
| CLK | I/ST | SD/MMC Clock input. |
| FCE0~1 | IO/ST/PUC | Flash chip enable signal. |
| FRBn | IO/ST/PUC | Flash Ready/Busy signal |
| FCLE | IO/ST/PUC | Flash command latch enable |
| FALE | IO/ST/PUC | Flash address latch enable. |
| FREn | IO/ST/PUC | Flash read enable. |
| FWEn | IO/ST/PUC | Flash write enable. |
| FWPn | IO/ST/PUC | Flash write protect. |
| FD0~FD7 | IO/ST/PUC | Flash data bus. |
| SDMMC | I | SD/MMC Selection. MMC Mode when Tie-High and SD Mode when Tie-Low. |
| TEST | I/PD | Test mode enable. This pin must floating or tie-low when normal operation. |
| TCLK | I/ST | Clock for test mode. |
| TRSTn | I/PD | Reset for test mode. |
| GPIO0 | IO/ST/PUC | General purpose I/O pin. |

*1: I/O Type I: Input pin. IO: Bidirectional pin.ST: pin with S Trigger. Analog: Analog pin

PD: pin with pull-down resister. PUC: pin with controllable pull-up resister. Power: Power Pin

Table 1. Pin Description

# 3. Internal Regulator, Power-ON Reset and RC oscillator

## 3.1. Regulator

The internal voltage regulator input 3.3V and output 1.8V used for core power supply as shown in Figure 3.

## 3.2. Power-on-reset and brown-out-reset

The internal reset control unit has power-on-reset (POR). To use internal POR, only provide 3.3V to VDDA33 and GNDA connected to ground as shown in Figure 3.

## 3.3. RC oscillator

An integrated RC oscillator can be used to reduce BOM cost. ROSC must be connected to 1.8V through a resistor, as shown in Figure 3.

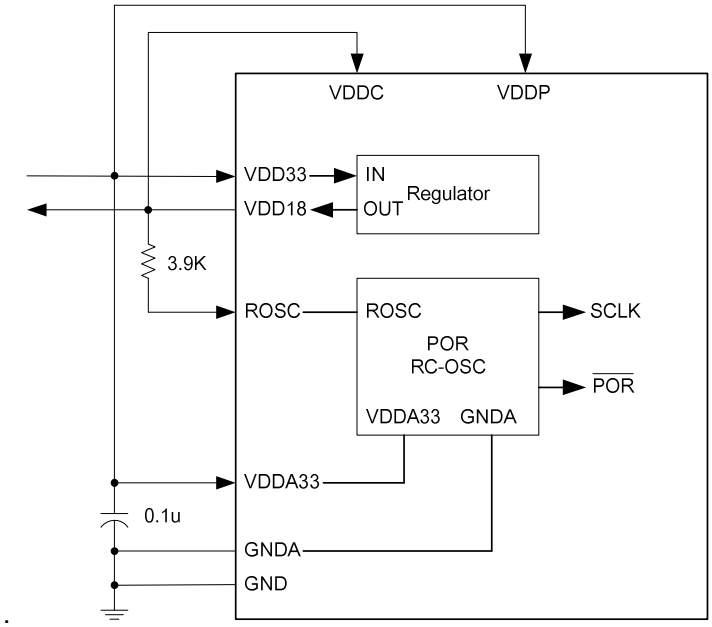



Figure 3. Pin connection to use internal Regulator, Power-ON Reset and Oscillator

# 4. Electrical specifications

## 4.1. Absolute maximum ratings

| Symbol | Description | Value | Unit | Notes |
|---|---|---|---|---|
| $V_{DD}$ | I/O Power Supply Voltage | - 0.3 to +3.6 | V | VDDP, VDD33, VDD33A |
| $V_{DDC}$ | Core Power Supply Voltage | - 0.3 to +1.98 | V | VDDC |
| $V_{IN}$, $V_{OUT}$ | All input/output voltages | - 0.3 to VDD + 0.3 | V | |
| Tstg | Storage temperature range | - 45 to +85 | ℃ | |

Table 2. Absolute maximum ratings

## 4.2. Recommended operating conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | I/O Power Supply Voltage | 2.7 | 3.3 | 3.6 | V |
| $V_{DDC}$ | Core Power Supply Voltage | 1.62 | 1.8 | 1.98 | V |
| $T_{OPR}$ | Operating temperature | 0 | | 70 | $^{o}$C |

Table 3. Recommended operation conditions

## 4.3. Power-on-reset characteristics

| Symbol | Parameter | Typ. | Unit |
|---|---|---|---|
| $V_T$(POR) | Threshold voltage of power-on-reset | 2.6 | V |

Table 4. Power-on-reset characteristics

## 4.4. Bus Operating Conditions

### 4.4.1. General

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Peak voltage on all lines | | -0.5 | 3.6 | V | |
| **All inputs** | | | | | |
| Input Leakages Current | | -10 | 10 | μA | |
| **All outputs** | | | | | |
| Output Leakages Current | | -10 | 10 | μA | |

Table 5. Bus Operating Conditions – General

### 4.4.2. Bus Signal Level

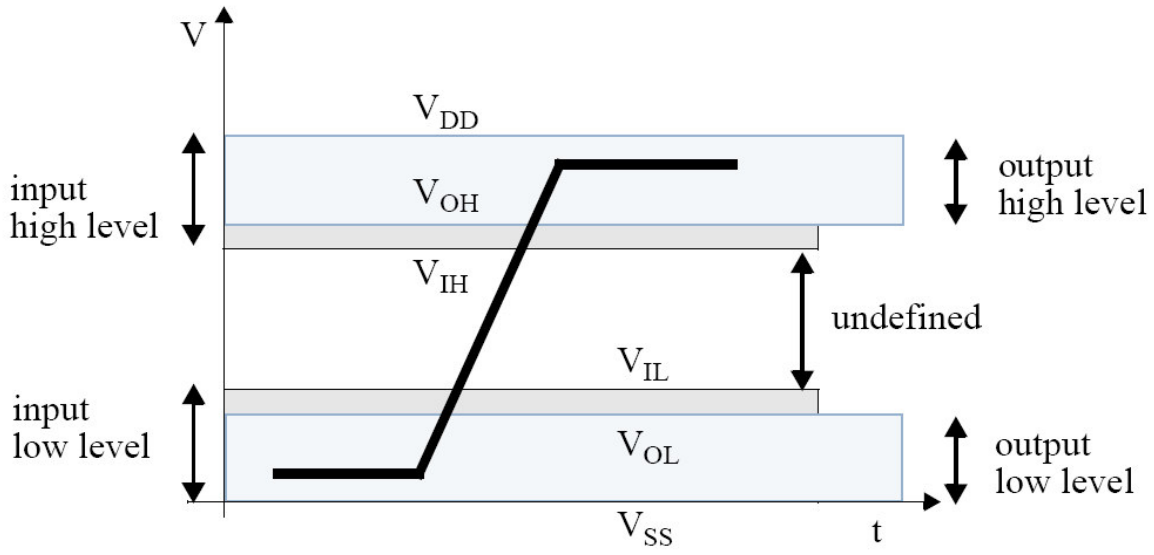



Figure 4. Bus Signal Level

## 4.5. SD Mode Bus Operating Conditions

### 4.5.1. Deault

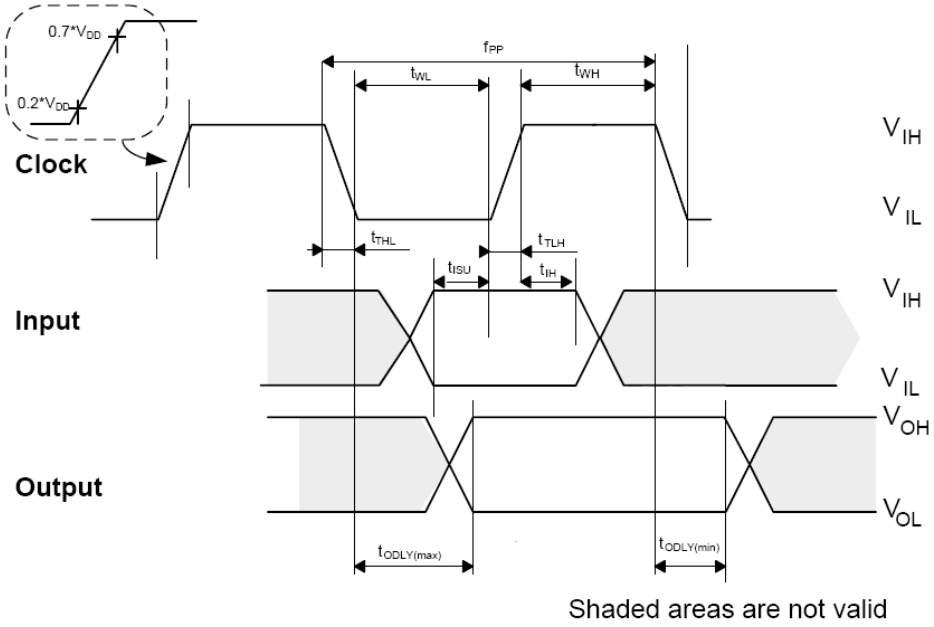



Figure 5. SD Mode: Timing Diagram Data Input/Output Referenced to Clock (Default)

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| **Clock CLK** (All values are referred to min($V_{IH}$) and max ($V_{IL}$), | | | | | |
| Clock frequency Data Transfer Mode | $f_{PP}$ | 0 | 25 | MHz | $C_{CARD} \leq 10pF$ (1 card) |
| Clock frequency Identification Mode | $f_{OD}$ | $0_{(1)}$/100 | 400 | KHz | $C_{CARD} \leq 10pF$ (1 card) |
| Clock low time | $t_{WL}$ | 10 | | ns | $C_{CARD} \leq 10pF$ (1 card) |
| Clock high time | $t_{WH}$ | 10 | | ns | $C_{CARD} \leq 10pF$ (1 card) |
| Clock rise time | $t_{TLH}$ | | 10 | ns | $C_{CARD} \leq 10pF$ (1 card) |
| Clock fall time | $t_{THL}$ | | 10 | ns | $C_{CARD} \leq 10pF$ (1 card) |

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| **Input CMD, DAT** (referenced to CLK) | | | | | |
| Input set-up time | $t_{ISU}$ | 5 | | ns | $C_{CARD} \leq 10pF$ (1 card) |
| Input hold time | $t_{IH}$ | 5 | | ns | $C_{CARD} \leq 10pF$ (1 card) |
| **Outputs CMD, DAT** (referenced to CLK) | | | | | |
| Output Delay time during Data Transfer Mode | $t_{ODLY}$ | 0 | 14 | ns | $C_L \leq 40pF$ (1 card) |
| Output Delay time during Identification Mode | $t_{ODLY}$ | 0 | 50 | ns | $C_L \leq 40pF$ (1 card) |

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

Table 6. SD Mode: Bus Timing – Parameters Value (Default)

### 4.5.2. High Speed

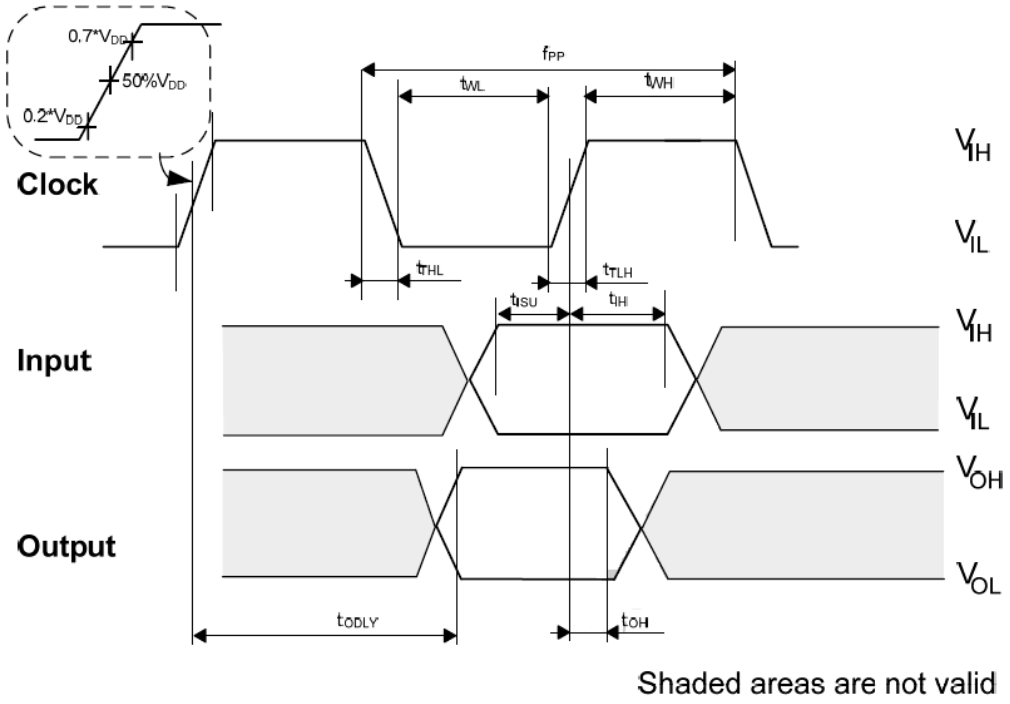



Figure 6. SD Mode: Timing Diagram Data Input/Output Referenced to Clock (High-Speed)

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| **Clock CLK** (All values are referred to min($V_{IH}$) and max ($V_{IL}$), | | | | | |
| Clock frequency Data Transfer Mode | $f_{PP}$ | 0 | 50 | MHz | $C_{CARD} \leq 10pF$ (1 card) |
| Clock low time | $t_{WL}$ | 7 | | ns | $C_{CARD} \leq 10pF$ (1 card) |
| Clock high time | $t_{WH}$ | 7 | | ns | $C_{CARD} \leq 10pF$ (1 card) |
| Clock rise time | $t_{TLH}$ | | 3 | ns | $C_{CARD} \leq 10pF$ (1 card) |
| Clock fall time | $t_{THL}$ | | 3 | ns | $C_{CARD} \leq 10pF$ (1 card) |

| Parameter | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| **Input CMD, DAT** (referenced to CLK) | | | | | |
| Input set-up time | $t_{ISU}$ | 6 | | ns | $C_{CARD} \leq 10pF$ (1 card) |
| Input hold time | $t_{IH}$ | 2 | | ns | $C_{CARD} \leq 10pF$ (1 card) |
| **Outputs CMD, DAT** (referenced to CLK) | | | | | |
| Output Delay time during Data Transfer Mode | $t_{ODLY}$ | | 14 | ns | $C_L \leq 40pF$ (1 card) |
| Output Hold time | $t_{OH}$ | 2.5 | | ns | $C_L \geq 15pF$ (1 card) |
| Total System capacitance for each line | $C_L$ | | 40 | pF | 1 card |

(1) In order to satisfy severe timing, host shall drive only one card.

Table 7. SD Mode: Bus Timing – Parameters Values (High-Speed)

## 4.6. MMC Mode Bus Operating Conditions

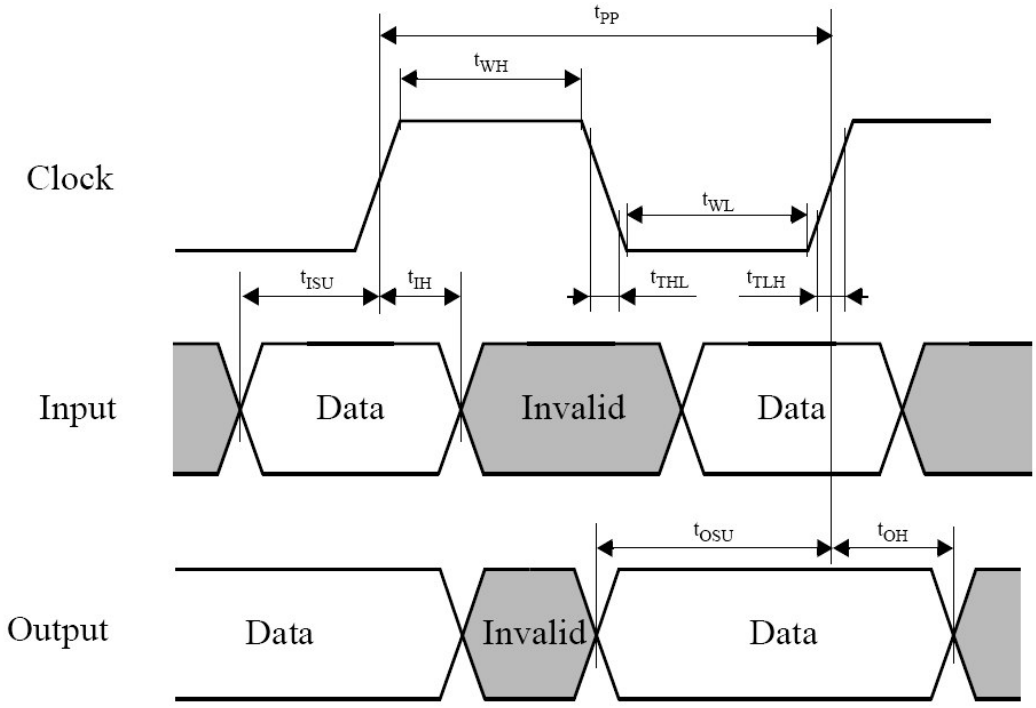



Figure 7. MMC Mode: Timing Diagram - Data Input/Output

### 4.6.1. Card Interface Timing

| Parameter | Symbol | Min | Max. | Unit | Remark |
|---|---|---|---|---|---|
| **Clock CLK**[1] | | | | | |
| Clock frequency Data Transfer Mode (PP)[2] | $f_{PP}$ | 0 | 26/52 | MHz | $C_L$ <= 30 pF<br>Tolerance: +100KHz |
| Clock frequency Identification Mode (OD) | $f_{OD}$ | 0 | 400 | kHz | Tolerance: +20KHz |
| Clock low time | $t_{WL}$ | 6.5 | | ns | $C_L$ <= 30 pF |
| Clock rise time[3] | $t_{TLH}$ | | 3 | ns | $C_L$ <= 30 pF |
| Clock fall time | $t_{THL}$ | | 3 | ns | $C_L$ <= 30 pF |
| **Inputs CMD, DAT** (referenced to CLK) | | | | | |
| Input set-up time | $t_{ISU}$ | 3 | | ns | $C_L$ <= 30 pF |
| Input hold time | $t_{IH}$ | 3 | | ns | $C_L$ <= 30 pF |
| **Outputs CMD, DAT** (referenced to CLK) | | | | | |
| Output set-up time | $t_{OSU}$ | 5 | | ns | $C_L$ <= 30 pF |
| Output hold time | $t_{OH}$ | 5 | | ns | $C_L$ <= 30 pF |

| Parameter | Symbol | Min | Max. | Unit | Remark |
|---|---|---|---|---|---|
| Signal rise time[4] | $t_{rise}$ | | 3 | ns | $C_L$ <= 30 pF |
| Signal fall time | $t_{fall}$ | | 3 | ns | $C_L$ <= 30 pF |

Table 8. MMC Mode: High-Speed Card Interface Timing

1) All timing values are measured relative to 50% of voltage level
2) A MultiMediaCard shall support the full frequency range from 0-26Mhz, or 0-52MHz
3) Rise and fall times are measured from 10%-90% of voltage level
4) Rise and fall times are measured from 10%-90% of voltage level

| Parameter | Symbol | Min | Max. | Unit | Remark |
|---|---|---|---|---|---|
| **Clock CLK**[1] | | | | | |
| Clock frequency Data Transfer Mode (PP) | $f_{PP}$ | 0 | 20 | MHz | $C_L$ <= 30 pF |
| Clock frequency Identification Mode (OD) | $f_{OD}$ | 0 | 400 | kHz | |
| Clock low time | $t_{WL}$ | 10 | | ns | $C_L$ <= 30 pF |
| Clock rise time[2] | $t_{TLH}$ | | 10 | ns | $C_L$ <= 30 pF |
| Clock fall time | $t_{THL}$ | | 10 | ns | $C_L$ <= 30 pF |
| **Inputs CMD, DAT** (referenced to CLK) | | | | | |
| Input set-up time | $t_{ISU}$ | 3 | | ns | $C_L$ <= 30 pF |
| Input hold time | $t_{IH}$ | 3 | | ns | $C_L$ <= 30 pF |
| **Outputs CMD, DAT** (referenced to CLK) | | | | | |
| Output set-up time | $t_{OSU}$ | 13.1 | | ns | $C_L$ <= 30 pF |
| Output hold time | $t_{OH}$ | 9.7 | | ns | $C_L$ <= 30 pF |

1) All timing values are measured relative to 50% of voltage level
2) Clock rise and fall times are measured from VIL to VIH of voltage level

Table 9. MMC Mode: Backwards Compatible Card Interface Timing

## 4.7. Flash Interface Command Write AC characteristics

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tCLS | FCLE setup time | 0 | | ns |
| tCLH | FCLE hold time | 10 | | ns |
| tCS | FCE# setup time | 0 | | ns |
| tCH | FCE# hold time | 10 | | ns |
| tWP | FWE# pulse width | 25 | | ns |
| tALS | FALE setup time | 0 | | ns |
| tALH | FALE hold time | 10 | | ns |
| tDS | Data Setup time | 20 | | ns |
| tDH | Data hold time | 10 | | ns |

Table 10. Timing Parameters: Flash Interface Command Write

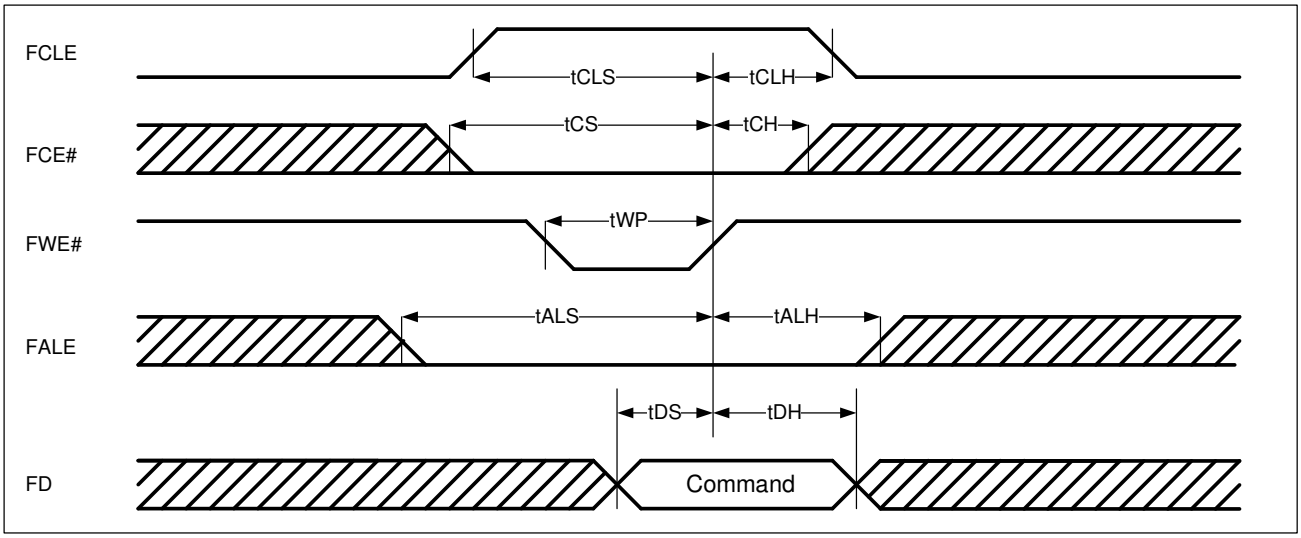



Figure 8. Timing Diagram: Flash Interface Command Write

## 4.8. Flash Interface Address Write AC characteristics

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tCLS | FCLE setup time | 0 | | ns |
| tCS | FCE# setup time | 0 | | ns |
| tCH | FCE# hold time | 10 | | ns |
| tWP | FWE# pulse width | 25 | | ns |
| tWH | FWE# high hold time | 15 | | ns |
| tALS | FALE setup time | 0 | | ns |
| tALH | FALE hold time | 10 | | ns |
| tDS | Data Setup time | 20 | | ns |
| tDH | Data hold time | 10 | | ns |
| tWC | Flash write cycle time | 50 | | |

Table 11. Timing Parameters: Flash Interface Address Write

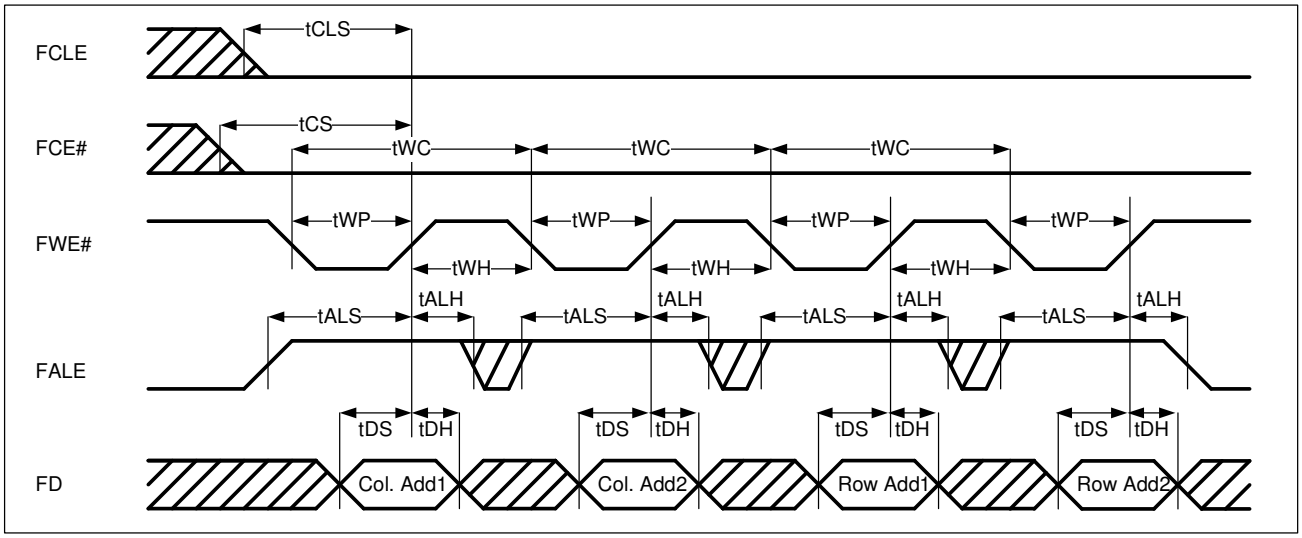



Figure 9. Timing Diagram: Flash Interface Address Write

## 4.9. Flash Interface Data Write AC characteristics

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tCLH | FCLE hold time | 10 | | ns |
| tCH | FCE# hold time | 10 | | ns |
| tWP | FWE# pulse width | 25 | | ns |
| tWH | FWE# high hold time | 15 | | ns |
| tALS | FALE setup time | 0 | | ns |
| tDS | Data setup time | 20 | | ns |
| tDH | Data hold time | 10 | | ns |
| tWC | Flash write cycle time | 50 | | ns |

Table 12. Timing Parameters: Flash Interface Data Write

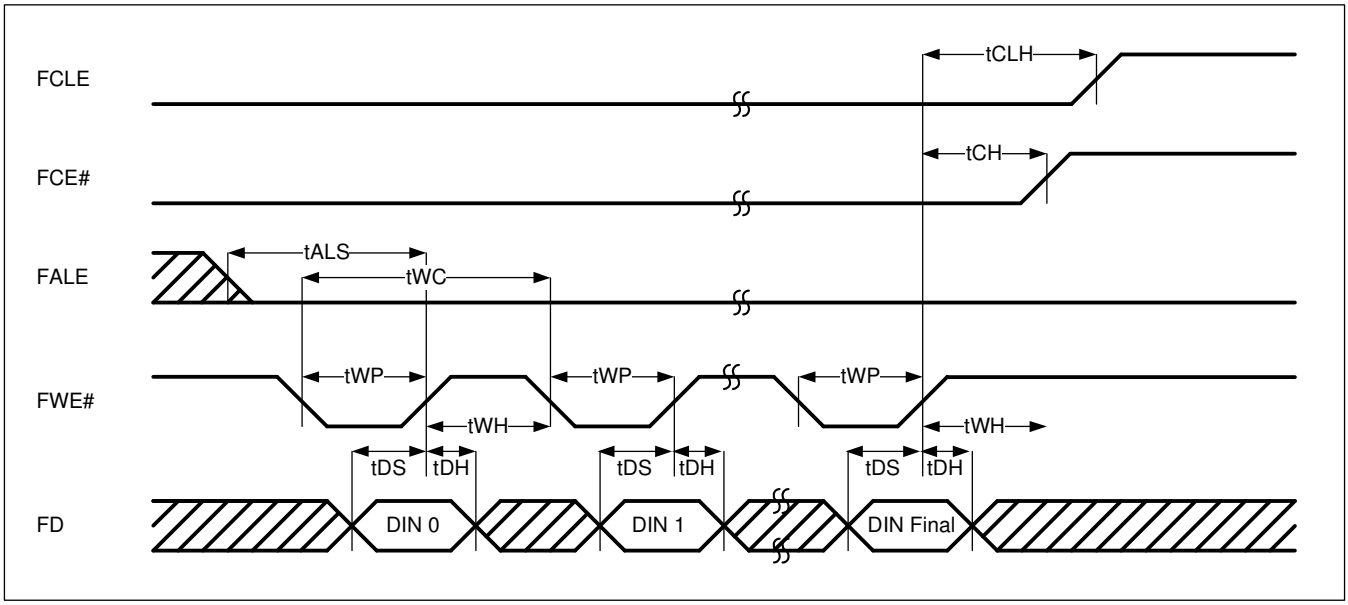



Figure 10. Timing Diagram: Flash Interface Data Write

## 4.10. Flash Interface Data Read AC characteristics

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tCLR | FCLE to FRE# delay | 10 | | ns |
| tAR | ALE to FRE# delay | 10 | | ns |
| tRR | Ready to FRE# low | 20 | | ns |
| tRC | Read cycle time | 30 | | ns |

Table 13. Timing Parameters: Flash Interface Data Read

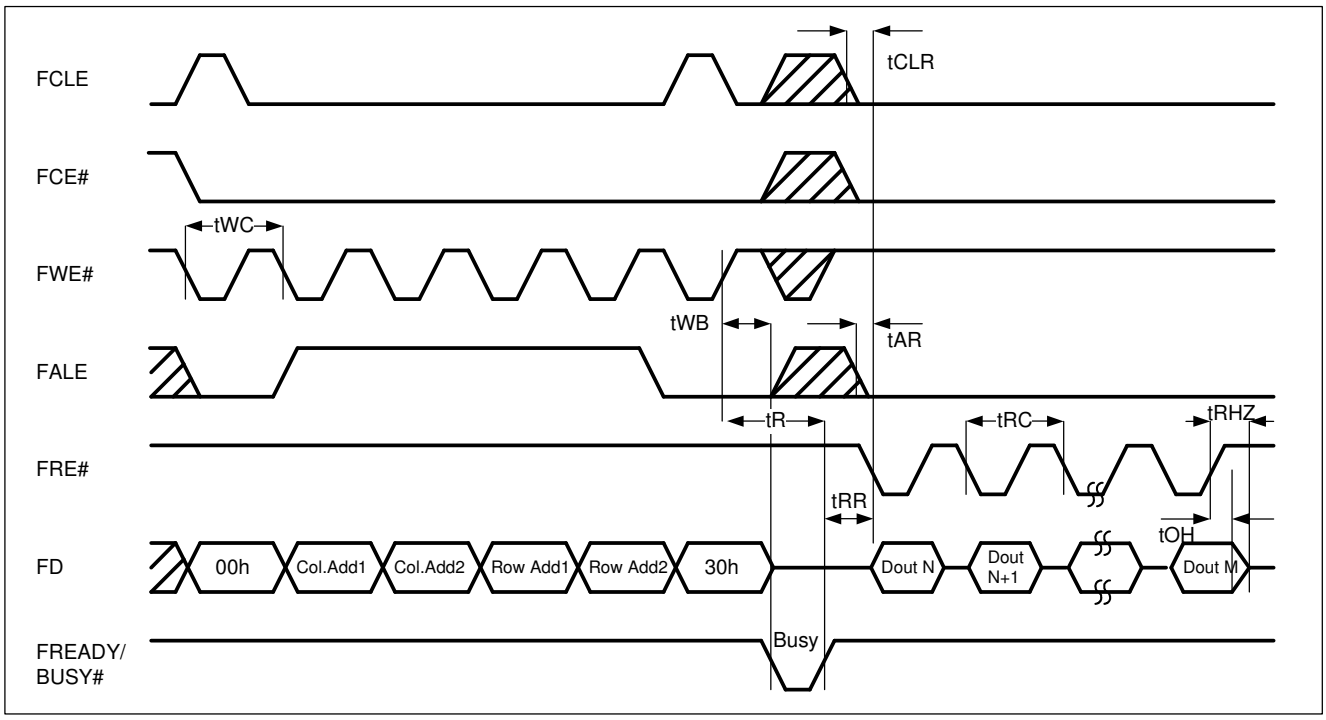
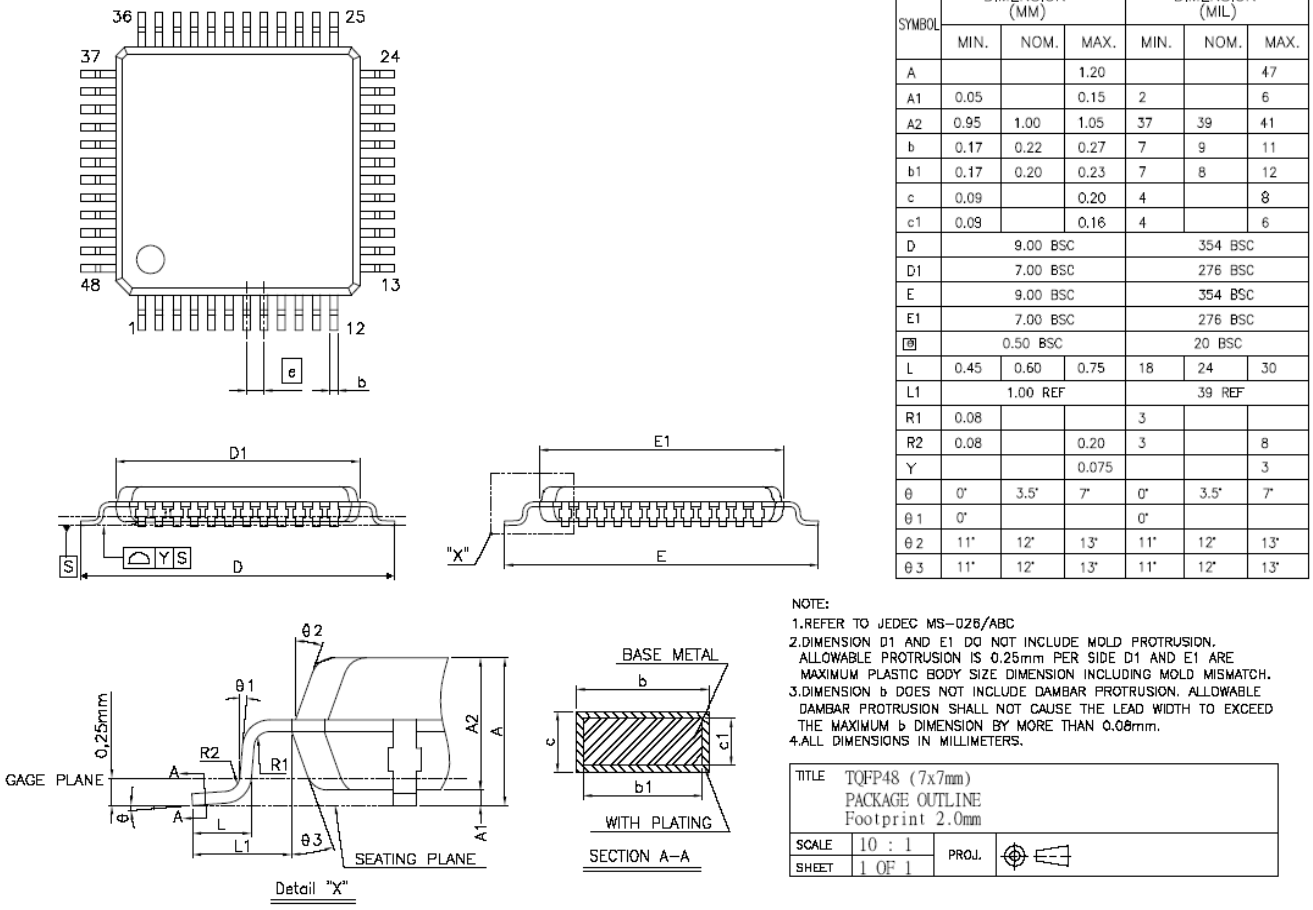



Figure 11. Timing Diagram: Flash Interface Data Read

# 5. Package Dimensions




| SYMBOL | DIMENSION (MM) | | | DIMENSION (MIL) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.20 | | | 47 |
| A1 | 0.05 | | 0.15 | 2 | | 6 |
| A2 | 0.95 | 1.00 | 1.05 | 37 | 39 | 41 |
| b | 0.17 | 0.22 | 0.27 | 7 | 9 | 11 |
| b1 | 0.17 | 0.20 | 0.23 | 7 | 8 | 12 |
| c | 0.09 | | 0.20 | 4 | | 8 |
| c1 | 0.09 | | 0.16 | 4 | | 6 |
| D | 9.00 BSC | | | 354 BSC | | |
| D1 | 7.00 BSC | | | 276 BSC | | |
| E | 9.00 BSC | | | 354 BSC | | |
| E1 | 7.00 BSC | | | 276 BSC | | |
| e | 0.50 BSC | | | 20 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 18 | 24 | 30 |
| L1 | 1.00 REF | | | 39 REF | | |
| R1 | 0.08 | | | 3 | | |
| R2 | 0.08 | | 0.20 | 3 | | 8 |
| Y | | | 0.075 | | | 3 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | | | 0° | | |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |

NOTE:
1.REFER TO JEDEC MS-026/ABC
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

| | | | |
|---|---|---|---|
| TITLE | TQFP48 (7x7mm) PACKAGE OUTLINE Footprint 2.0mm | | |
| SCALE | 10 : 1 | PROJ. | |
| SHEET | 1 OF 1 | | |

Figure 12. i5141-TG Package Diagram