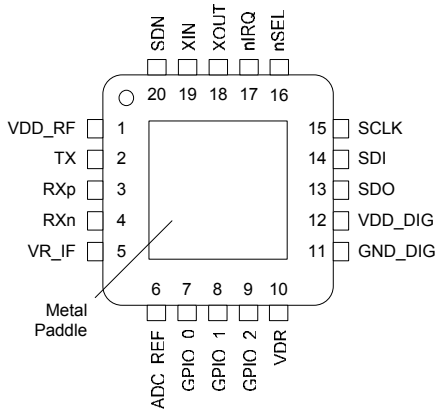
IA4432 ISM Transceiver

IA4432

QFN-20 PIN ASSIGNMENT



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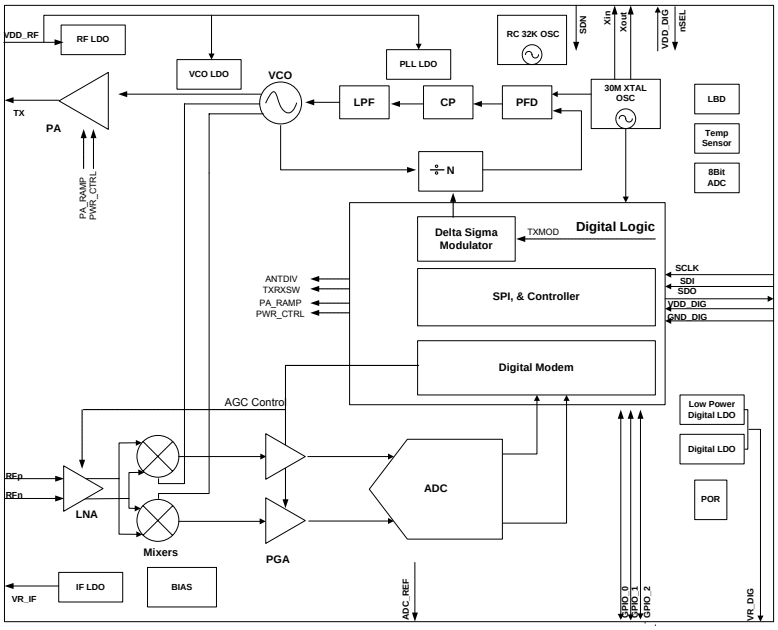
DESCRIPTION

Integration's IA4432 transceiver is a member of the new EZRadioPRO™ family. While retaining all the attractive features of earlier products such as high integration, low cost, flexibility, low Bill of Materials (BOM) cost, and easy design-in, these parts are targeted to more sophisticated applications and offer several enhanced parameters and features, including continuous frequency coverage from 240-930MHz and output power up to +20dBm. Also included are built-in features like antenna diversity algorithm, wake-up timer, low battery detector, temperature sensor, general purpose Analog to Digital Converter (ADC), TX/RX First-In First-Out Buffers (FIFO's), power-on-reset (POR), and general purpose I/Os (GPIOs). The chip incorporates a high performance ADC in the RX path and digital modem which performs demodulation, filtering, and packet handling in the digital domain making it ideal for configuration to multiple applications. These features simplify the task of the system designer and allow for the use of lower-end Microcontrollers. A highly efficient +20dBm power amplifier (PA) is completely integrated which eliminates the need for an external PA and makes the part ideal for Frequency Hopping Systems where maximum range is desired. The devices comply with FCC and ETSI requirements when used in any of the standard ISM bands. Only a 30MHz crystal and a limited number of passive matching/filtering components are necessary as external components making the device ideal for high volume production in applications where size and cost are critical.

The IA4432 is a CMOS Radio Frequency Integrated circuit which incorporates all of the transmit and receive functions required for ISM band applications. The chip is designed to operate over a wide range of frequencies, voltages, and temperature with extremely low current consumption which makes it ideal for low-data rate battery powered applications.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

- Frequency Range = 240-930MHz
- Sensitivity =-117dBm
- +20dBm Max Output Power
  - o Configurable +11 to +20dBm
- Low Power Consumption
  - o 17mA Receive
  - o 60mA Transmit @+20dBm
  - o 27mA@+13dBm
- Data Rate = 1 to 128kbps
- Power Supply = 1.8 to 3.6V
- Ultra Low Power Shutdown Mode
- Digital RSSI
- Wake-On-Radio
- Auto-Frequency Calibration (AFC)
- Antenna Diversity & TR Switch Control
- Configurable Packet Structure
- Preamble Detector
- TX & RX 64 byte FIFOs
- Low Battery Detector
- Temperature Sensor and 8bit ADC
- -40°C - +85°C Temperature Range
- Integrated Voltage Regulators
- Frequency Hopping Capability
- On-chip Crystal Tuning
- 20-Pin QFN Package
- FSK, GFSK, and OOK Modulation
- Low BOM
- Power-on-Reset(POR)

TYPICAL APPLICATIONS

- Remote Control
- Home Security & Alarm
- Telemetry
- Personal Data Logging
- Toy Control
- Tire Pressure Monitoring
- Wireless PC Peripherals
- Remote Meter Reading
- Remote Keyless Entry
- Home Automation
- Industrial Control
- Sensor Networks
- Health Monitors
- Tag Readers

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1 DETAILED DESCRIPTION

Integration's IA4432 transceiver is a member of the new EZRadioPRO™ family. While retaining all the attractive features of earlier products such as high integration, low cost, flexibility, low Bill of Materials (BOM) cost, and easy design-in, these parts are targeted to more sophisticated applications and offer several enhanced parameters and features, including continuous frequency coverage from 240-930MHz and output power up to +20dBm. Also included are built-in features like wake-up timer, low battery detector, temperature sensor, general purpose Analog to Digital Converter (ADC), TX/RX First-In First-Out Buffers (FIFO's), power-on-reset (POR), and general purpose I/Os (GPIOs). The chip incorporates a high performance ADC in the RX path and digital modem which performs demodulation, filtering, and packet handling in the digital domain making it ideal for configuration to multiple applications. These features simplify the task of the system designer and allow for the use of lower-end Microcontrollers. A highly efficient +20dBm power amplifier (PA) is completely integrated which eliminates the need for an external PA and makes the part ideal for Frequency Hopping Systems where maximum range is desired. The devices comply with FCC and ETSI requirements when used in any of the standard ISM bands. Only a 30MHz crystal and a limited number of passive matching/filtering components are necessary as external components making the device ideal for high volume production in applications where size and cost are critical.

The IA4432 is a CMOS Radio Frequency Integrated circuit which incorporates all of the transmit and receive functions required for ISM band applications. The chip is designed to operate over a wide range of frequencies, voltages, and temperature with extremely low current consumption which makes it ideal for low-data rate battery powered applications.

The protocol used by the system utilizes Time Division Duplexing (TDD), in which the transceiver alternately transmits and receives in a burst-like nature. The receive path uses a single-conversion architecture which image-reject mixes the 2-level FSK/GFSK/OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance ΣΔ ADC so filtering, demodulation, slicing, error correction, and packet handling are performed in the digital domain where they can be done more efficiently. The resulting demodulated signal is then output to the Microcontroller through a programmable GPIO or over the standard SPI bus by reading the FIFO.

A single local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver are never on at the same time. The LO is generated by an integrated VCO and ΣΔ Fractional-N PLL synthesizer. The synthesizer is designed to allow for configurable data rate, output frequency, frequency deviation, and Gaussian Filtering at any frequency between 240-930MHz. The transmit FSK data is modulated directly into the Δ-Σ data stream. The data may shaped by a Gaussian low-pass filter to achieve a more desirable spectrum.

The PA exhibits a maximum output power of +20dBm. The output power is configurable between +11 and +20dBm in 3dB steps. The PA is single-ended to allow for easy matching and low BOM cost. The PA incorporates its own ramp-up and ramp-down of the burst signal to prevent unwanted spectral splatter.

With the integrated +20dBm PA, easy frequency hopping control, TXRX switch control, and antenna diversity switch control, significant advantages can be achieved. Antenna Diversity is completely integrated into the IA4432 and can improve the system link budget by 8-10dB in a typical environment. Antenna diversity can improve the range by 50-100% depending on the environment. The +20dBm power amplifier can also be used to compensate for a lower cost, lower performance antenna reducing the overall system cost and geometrical size but still achieving maximum range.

2 FUNCTIONAL DESCRIPTION

The IA4432 is designed to work with a Microcontroller, crystal, and a few passives to create a very low cost system as shown Figure 1. Voltage regulators are integrated on-chip which allow for a wide range of operating supply voltage conditions from +1.8 to +3.6V. A standard four pin SPI bus is used to communicate with the Microcontroller. Three configurable general purpose I/Os are available for use to tailor towards the needs of the system. A more complete list of the available GPIO functions is shown in section 9 Auxiliary Functions but just to name a few, Microcontroller clock output, Antenna Diversity, TRSW control, POR, and specific interrupts. A limited number of passive components are needed to match the LNA and PA; refer to Section 11, Reference Design for the required component values at different frequency ranges.

The application below is designed for a system with Antenna Diversity. Using Antenna Diversity can increase the link budget of the system by as much as 10dB. The Antenna Diversity Control Algorithm is completely integrated into the chip and is discussed further in Section 9.8 Antenna-Diversity.

For a simpler application example not using Antenna Diversity see the Reference Design section.

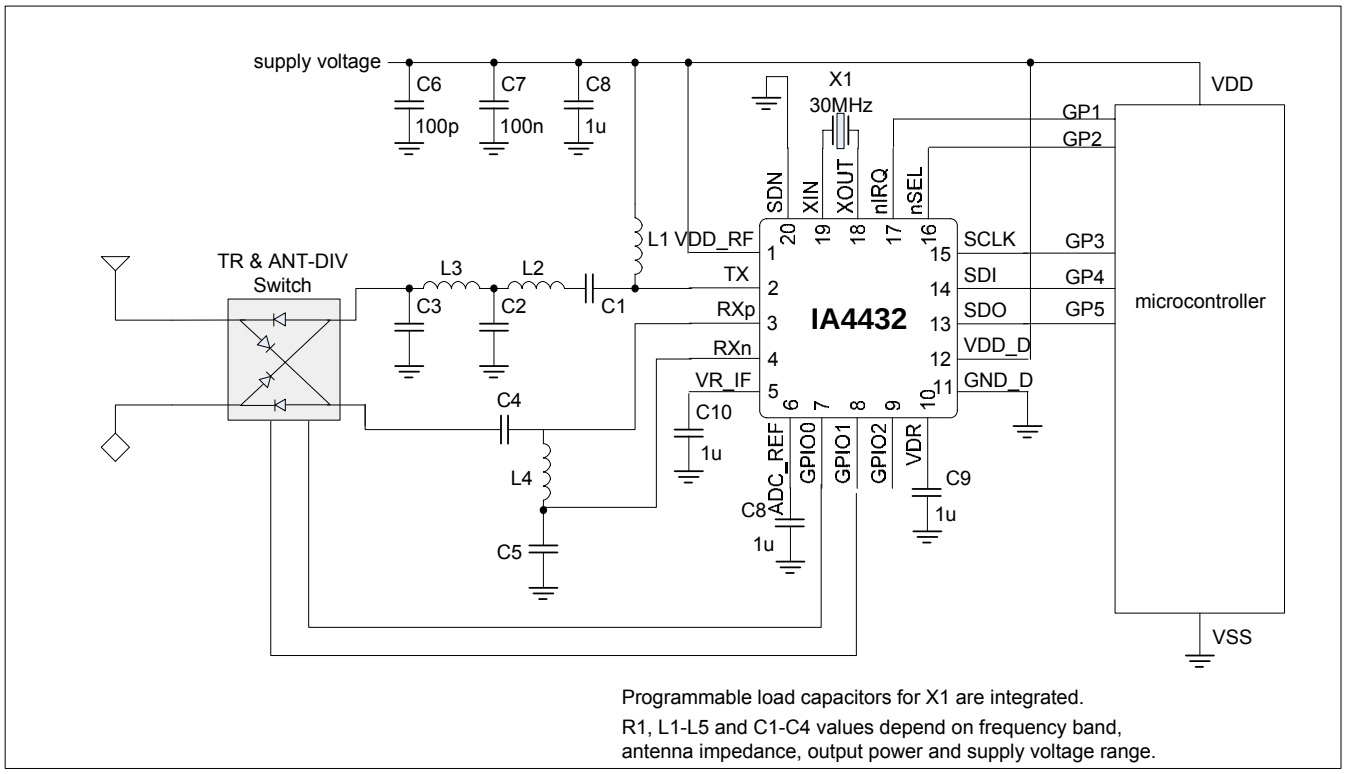


Figure 1: +20dBm Application with Antenna Diversity and FHSS

2.1 Pin Connection Diagram

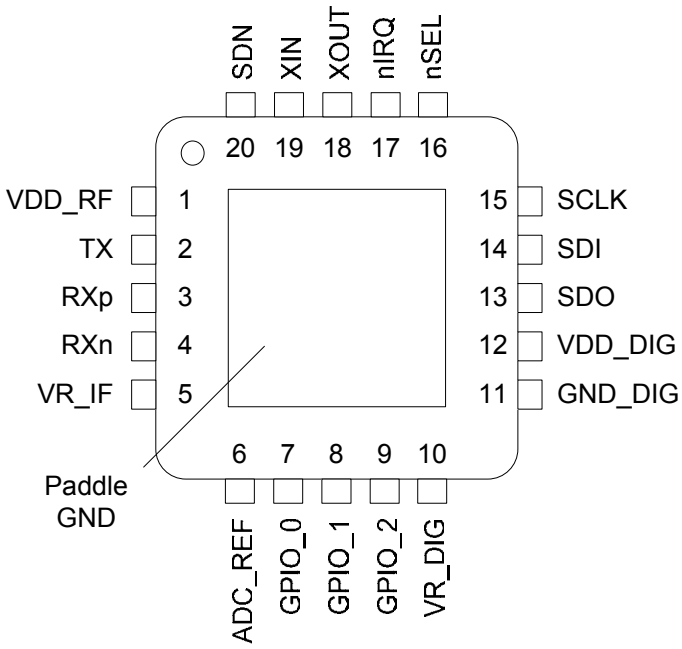


Figure 2: IA4432 Pinout

2.2 Package Pin Definitions

Table 1: Pin Descriptions

Pin	Pin Name	I/O	Description
1	VDD_RF	VDD	+1.8V to +3.6V supply voltage input to all analog +1.7V regulators. The recommended VDD supply voltage is +3.3V.
2	TX	O	Transmit output pin. The maximum level in TX mode is +20dBm. The PA output is an open-drain connection so the L-C match must supply VDD (+3.3 VDC nominal) to this pin.
3	RXp	I	Differential RF input pins of the LNA. See application schematic for example matching network.
4	RXn	I	
5	VR_IF	O	Regulated Output Voltage of the IF 1.7V Regulator. A 1µF decoupling capacitor is required.
6	ADC_REF	O	ADC Reference Voltage Decoupling. A 1uF decoupling capacitor is required.
7	GPIO_0	I/O	General Purpose Digital I/O that may be configured through the SPI registers to perform various functions including: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc. See the SPI GPIO Configuration Registers, Address 0Bh, 0Ch, and 0Dh for more information.
8	GPIO_1	I/O	
9	GPIO_2	I/O	
10	VR_DIG	O	Regulated Output Voltage of the Digital 1.7V Regulator. A 1µF decoupling capacitor is required.
11	GND_DIG	O	Digital ground supply pin. All analog grounds are connected to the paddle inside the package. The Digital ground is brought out separately to help isolate the digital and analog domains.
12	VDD_DIG	VDD	+1.8V to +3.6V supply voltage input to the Digital +1.7V Regulator. The recommended VDD supply voltage is +3.3V.
13	SDO	O	0-VDD V digital output that provides a serial readback function of the internal control registers.
14	SDI	I	Serial Data input pin. 0–VDD V digital input. This pin provides the serial data stream for the 4-line serial data bus.
15	SCLK	I	Serial Clock input pin. 0–VDD V digital input. This pin provides the serial data clock function for the 4-line serial data bus. Data is clocked into the RFIC on positive edge transitions.
16	nSEL	I	Serial Interface Select input pin. 0– VDD V digital input. This pin provides the Select/Enable function for the 4-line serial data bus. The signal is also used to signify burst read/write mode.
17	nIRQ	O	General Microcontroller Interrupt Status output pin. When the RFIC exhibits anyone of the Interrupt Events the nIRQ pin will be set low='0'. Please see the Control Logic Registers section for more information on the Interrupt Events. The Microcontroller can then determine the state of the interupt by reading a corresponding SPI Interrupt Status Registers, Address 03h and 04h.
18	XOUT	O	Crystal Oscillator Output. Connect to an external 30MHz crystal or leave floating if driving the Xin pin with an external signal source.
19	XIN	I	Crystal Oscillator Input. Connect to an external 30MHz crystal or to an external source. If using an external clock source with no crystal, DC coupling with a nominal 0.8VDC level is recommended with a minimum AC amplitude of 700mVpp.
20	SDN	I	Shutdown input pin. 0-VDD V digital input. SDN should be = '0' in all modes except Shutdown mode. When SDN ='1' the chip will be completely shutdown and the contents of the registers will be lost.
PKG	PADDLE_GND	GND	The exposed metal paddle on the bottom of the RFIC supplies the RF and circuit ground(s) for the entire chip. It is very important that a good solder connection is made between this exposed metal paddle and the ground plane of the PCB underlying the RFIC.

2.3 Operating Modes

The following table summarizes the modes of operation of the RFIC. In general, any given mode of operation may be classified as an Active mode or a Power Saving mode. The table indicates which block(s) are enabled (active) in each corresponding mode. With the exception the Shutdown mode, all can be dynamically selected by sending the appropriate commands over the SPI in order to optimize the average current consumption. An "X" in any cell means that in the given mode of operation that block can be independently programmed to be either ON or OFF, without noticeably affecting the current consumption. The SPI circuit block includes the SPI interface and the Register Space. The 32kHz OSC circuit block includes the 32.768KHz RC oscillator or 32.768KHz Crystal Oscillator, and Wake-Up-Timer. AUX (Auxiliary Blocks) includes the Temperature Sensor, General Purpose ADC, and Low-Battery Detector.

Table 2: Operating Modes

Mode Name	Circuit Blocks								
	Digital LDO	**SPI**	**32kHz OSC**	**AUX**	**30MHz XTAL**	**PLL**	**PA**	**RX**	**I_{VDD}**
Shutdown	OFF (Register contents lost)	OFF OF	F	OFF	OFF	OFF	OFF	OFF	10nA
Standby ON	ON (Register contents retained)		OFF	OFF	OFF	OFF	OFF	OFF	300nA
Sleep		ON	ON X		OFF	OFF	OFF	OFF	600nA
Sensor		ON	X ON		OFF	OFF	OFF	OFF	5uA
Ready ON			X	X	ON	OFF	OFF	OFF	600uA
Tuning		ON	X X		ON	ON	OFF	OFF	8mA
Transmit		ON	X X		ON	ON	ON	OFF	27mA**
Receive		ON X		X	ON	ON	OFF	ON	17mA

** 27mA at +11dBm

3 ELECTRICAL SPECIFICATIONS

Notes:

Note 1: Guaranteed by design and/or simulation but not tested.

Note 2: Guaranteed by Engineering Qualification testing at Extreme Test Conditions. Test data available upon request.

Note 3: Guaranteed by 100% Production Test Screening at Production Test Conditions.

Table 3: DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range [2]	V_{dd}		1.8 3.0	3.6		V
Power Saving Modes [2] [3]	$I_{Shutdown}$	RC Oscillator,Main Digital Regulator, and Low Power Digital Regulator OFF. (depends only on process leakage) [2]	10		TBD	nA
	$I_{Standby}$	Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator, and RC Oscillator OFF[2]	300		TBD	nA
	I_{Sleep}	RC Oscillator and Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator OFF[2]	600		TBD	nA
	$I_{Sensor-LBD}$	Main Digital Regulator and Low Battery Detector ON, Crystal Oscillator and all other blocks OFF[2]	5		TBD	µA
	$I_{Sensor-TS}$	Main Digital Regulator and Temperature Sensor ON, Crystal Oscillator and all other blocks OFF[2]	5		TBD	µA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF. Crystal Oscillator buffer should be disabled[3]	600		TBD	µA
TUNE Mode Current [3]	I_{Tune}			8	TBD	mA
RX Mode Current [3]	I_{RX}			17	TBD	mA
TX Mode Currents [3]	I_{TX_+20}	txpow[1:0] = '11' (+20dBm), VDD=3.3V		60	TBD	mA
	I_{TX_+11}	txpow[1:0] = '00' (+11dBm), VDD=3.3V		27	TBD	mA

Table 4: Synthesizer AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range (2) (3)	$F_{SYNTH-LB}$	Low Band	240		480	MHz
	$F_{SYNTH-HB}$	High Band	480	930		MHz
Synthesizer Frequency Resolution	F_{RES-LB}	Low Band		156.25		Hz
	F_{RES-HB}	High Band		312.5		Hz
Reference Frequency	f_{REF}	Divided from 30MHz Crystal OSC		10		MHz
Reference Frequency Input Level (2) (3)	f_{REF_LV}	When using reference frequency instead of crystal. Measured peak-to-peak (Vpp)	0.7		1.6	V
Synthesizer Settling Time (2)	t_{LOCK}	Measured from leaving Ready mode with XOSC running to any frequency including VCO Calibration		200 TBD		µsec
Residual FM (2)	ΔF_{RMS}	RMS, integrated over ±250 kHz bandwidth (500 Hz lower bound of integration)	2		4	kHz
Phase Noise (2)	$L\phi(f_M)$	ΔF = 10 kHz	-80		TBD	dBc/Hz
		ΔF = 100 kHz	-90		TBD	dBc/Hz
		ΔF = 1 MHz	-115		TBD	dBc/Hz
		ΔF = 10 MHz	-130		TBD	dBc/Hz
Spurious Emissions (2)	P_{OB-TX1}	< 1 GHz			-50	dBm
	P_{OB-TX2}	1 GHz – 12.75 GHz, non-intential radiator			-70	dBm

Table 5: Receiver AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RX Frequency Range (2) (3)	$F_{SYNTH-LB}$	Low Band	240		480	MHz
	$F_{SYNTH-HB}$	High Band	480	930		MHz
RX Sensitivity	P_{RX_2}	(BER < 0.1%) (2 kbps, GFSK, BT=0.5, Δf = ±5kHz) (2)		-117	TBD	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT=0.5, Δf = ±20kHz) (2)	-106		TBD	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT=0.5, Δf = ±50kHz) (3)	-102		TBD	dBm
	P_{RX_OOK}	(BER < 0.1%) (4.8kbps, OOK) (2)	-110		TBD	dBm
RX Bandwidth	BW		2.4		620	kHz
Residual BER Performance (2)	P_{RX_RES}	Up to +5dBm Input Level		0	0.1	ppm
Input Intercept Point, 3rd Order (2)	$IIP3_{RX}$	Measured with inputs at 915 and 916MHz at -40dBm input power	-20		TBD	dBm
LNA Input Impedance	R_{IN-RX}	Unmatched, measured differentially across RX input pins	250			Ω
RSSI Resolution	RES_{RSSI}			±0.5		dB
±1-Ch Offset Selectivity (2) (BER < 0.1%)	C/I_{1-CH}	Desired Ref Signal 3dB above sensitivity. Interferer and desired modulated with 40 kbps ΔF = 20kHz GFSK with BT = 0.5, channel spacing = 150kHz		-31	TBD	dB
±2-Ch Offset Selectivity (2) (BER < 0.1%)	C/I_{2-CH}		-35		TBD	dB

Parameter	Symbol	Conditions	Min	Typ	Max	Units
≥ ±3Ch Offset Selectivity(2) (BER < 0.1%)	$C/I_{3\text{-}CH}$			-40	TBD	dB
Blocking at 1MHz(2) 1M	BLOCK	Desired Ref Signal 3dB above sensitivity. Interferer and desired modulated with 40 kbps ΔF = 20kHz GFSK with BT = 0.5		-52	TBD	dB
Blocking at 4MHz(2) 4M	BLOCK			-56	TBD	dB
Blocking at 8MHz(2) 8M	BLOCK		-63		TBD	dB
Image Rejection	Im_{REJ}	IF=937kHz	-30			dB
Spurious Emissions (2)	P_{OB_RX1}	Measured at RX pins (LO feedthrough)			-54	dBm

Table 6: Transmitter AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TX Frequency Range (2) (3)	$F_{SYNTH\text{-}LB}$	Low Band	240 480			MHz
	$F_{SYNTH\text{-}HB}$	High Band	480 930			
FSK Modulation Data Rate(2) (3) DR	FSK		1		128	kb/s
OOK Modulation Data Rate (2) (3) DR	OOK		2.4		40	kb/s
Modulation Deviation(2) (3)	Δf	At maximum PLL BW	±0.625		±320	kHz
Modulation Deviation Resolution	Δf_{RES}			0.625		kHz
Output Power Range(2) (3)	P_{TX}	For both High and Low Bands(240-930MHz), Output Power Controlled by txpow[1:0] Register Production Test: txpow[1:0] = '11', Measured at 915MHz	+11 +20			dBm
TX RF Output Steps (2)	ΔP_{RF_OUT}	TXPWR[1:0] = '00' thru '11'	TBD	3	TBD	dB
TX RF Output Level Variation vs. Voltage(2)	ΔP_{RF_V}	Measured from VDD=3.6V to VDD=1.8V		2	TBD	dB
TX RF Output Level (2) Variation vs. Temperature	ΔP_{RF_TEMP}	-40°C to +85°C	2		TBD	dB
TX RF Output Level Variation vs. Frequency (2)	ΔP_{RF_FREQ}	Measured across any one frequency band.		1	TBD	dB
Transmit Modulation Data Rate (2) (3)	DR		1		128	kbps
Transmit Modulation Filtering	B*T	Gaussian Filtering Bandwith Time Product		0.5		
Spurious Emissions (2)	$P_{OB\text{-}TX1}$	< 1 GHz			-50	dBm
	$P_{OB\text{-}TX2}$	1 GHz – 12.75 GHz, excluding harmonics			-70	dBm
Harmonics (2)	P_{2HARM}	Using Reference Design TX Matching Network and Filter with Max Output Power (20dBm). Harmonics reduce linearly with output power			-42	dBm
	P_{3HARM}				-42	dBm

Table 7: Auxiliary Block Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Temperature Sensor Accuracy[2] TS	$_A$	When calibrated using temp sensor offset register	0.5			°C
Temperature Sensor Sensitivity[2] TS	$_S$			5		mV/°C
Low Battery Detector Resolution[2]	LBD_{RES}			50		mV
Low Battery Detector Conversion Time[2]	LBD_{CT}			250 µsec		
Microcontroller Clock Output Frequency[2]	MC	Configurable to 30MHz, 15MHz, 10MHz, 4MHz, 3MHz, 2MHz, 1MHz, or 32.768kHz	32.768K		30M	Hz
General Purpose ADC Accuracy	ADC_{ENB}			8		bit
General Purpose ADC resolution	ADC_{RES}			4		mV
Temp Sensor & General Purpose ADC Conversion Time	ADC_{CT}			305 µsec		
30MHz XTAL Start-Up time	t_{30M}			1		msec
30MHz XTAL Cap Resolution	$30M_{RES}$			97		fF
32kHz XTAL Start-Up Time	t_{32k}			6		sec
32kHz XTAL Accuracy	$32K_{RES}$			100		ppm
32kHz RC OSC Accuracy	$32KRC_{RES}$			2500		ppm
POR Reset Time	t_{POR}			16		msec
Software Reset Time	t_{soft}			100 µsec		

Table 8: Digital IO Specifications (SDO, SDI, SCLK, nSEL, and nIRQ)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise time	T_{RISE} 0.1*V	$_{DD}$ to 0.9*V_{DD}, C_L= 5pF			8	ns
Fall time	T_{FALL} 0.9*V	$_{DD}$ to 0.1*$V_{DD,}$ C_L= 5pF			8	ns
Input capacitance	C_{IN}				1	pF
Logic high level input voltage	V_{IH}		V_{DD}-0.6			V
Logic low level input voltage	V_{IL}				0.6	V
Input current	I_{IN} 0<V	$_{IN}$< V_{DD} -100			100	nA
Logic high level output voltage	V_{OH}	I_{OH}<1mA source, V_{DD}=1.8V	V_{DD}-0.6			V
Logic low level output voltage	V_{OL}	I_{OL}<1mA sink, V_{DD}=1.8V			0.6	V

Table 9: GPIO Specifications (GPIO_0, GPIO_1, and GPIO_2)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise time	T_{RISE} 0.1*V	$_{DD}$ to 0.9*V_{DD}, C_L= 10pF, DRV<1:0>='HH'			8	ns
Fall time	T_{FALL} 0.9*V	$_{DD}$ to 0.1*$V_{DD,}$ C_L= 10pF, DRV<1:0>='HH'			8	ns
Input capacitance	C_{IN}				1	pF
Logic high level input voltage	V_{IH}		V_{DD}-0.6			V
Logic low level input voltage	V_{IL}				0.6	V
Input current	I_{IN} 0<V	$_{IN}$< V_{DD} -100			100	nA
Input current if pull-up is activated	I_{INP}	V_{IL}=0V 5			25	uA
Maximum output current	I_{OmaxLL} DRV<1:0>='LL'		0.1	0.5	0.8	mA
Maximum output current	I_{OmaxLH} DRV<1:0>='LH'		0.9	2.3	3.5	mA
Maximum output current	I_{OmaxHL} DRV<1:0>='HL'		1.5	3.1	4.8	mA
Maximum output current	I_{OmaxHH} DRV<1:0>='HH'		1.8	3.6	5.4	mA
Logic high level output voltage	V_{OH}	I_{OH}< I_{Omax} source, V_{DD}=1.8V	V_{DD}-0.6			V
Logic low level output voltage	V_{OL}	I_{OL}< I_{Omax} sink, V_{DD}=1.8V			0.6	V

3.1 Definition of Test Conditions

Production Test Conditions:

T_A = +25°C
V_{DD} = +3.3VDC
External reference signal (XIN) = 1.0 Vpp at 30MHz, centered around 0.8VDC
Production test schematic of Figure 3 (unless noted otherwise)
All RF input and output levels referred to the pins of the RFIC (not the RF module)

Extreme Test Conditions:

T_A = -40°C to +85°C
V_{DD} = +1.8 to +3.6 VDC
External reference signal (XIN) = 0.7 to 1.6 Vpp at 30MHz centered around 0.8VDC
Production test schematic of Figure 3 (unless noted otherwise)
All RF input and output levels referred to the pins of the RFIC (not the RF module)

Test Notes:

All electrical parameters with Min/Max values are guaranteed by one (or more) of the following test methods. Electrical parameters shown with only Typical values are not guaranteed.

1. Guaranteed by design and/or simulation but not tested.
2. Guaranteed by Engineering Qualification testing at Extreme Test Conditions. Test data available upon request.
3. Guaranteed by 100% Production Test Screening at Production Test Conditions.

Production Test Schematic

Insert Schematic here

Figure 3: Production Test Schematic

3.2 Absolute Maximum Ratings

V_{DD} to GND: .....–0.3 V, +3.6V

V_{DD} to GND on TX Output Pin: .....–0.3 V, +8.0V

Voltage on Digital Control Inputs:.....–0.3 V, V_{DD} + 0.3 V

Voltage on Analog Inputs:.....–0.3 V, V_{DD} + 0.3 V

RX Input Power .....+10 dBm

Operating Ambient Temperature Range T_A:..... -40°C to +85°C

Thermal Impedance Θ_{JA}:..... 30°C /W

Junction Temperature T_J:..... +125°C

Storage Temperature Range T_{STG}:..... –40°C to +125°C

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Caution: ESD sensitive device.

Power Amplifier may be damaged if switched on without proper load connected.

4 CONTROLLER INTERFACE

4.1 Serial Peripheral Interface (SPI)

The control logic is designed to accept data over a 3 wire SPI interface, SCLK, SDI, and nSEL. The control logic will also read out data from internal registers on a fourth SDO output pin. AN SPI transaction is a 16 bit sequence which consists of a Read-Write (RW) select bit, followed by a 7 bit address field(ADDR), and an 8 bit data field(DATA), as demonstrated in Figure 4. The 7 bit address field supports reading from or writing to one of the 128, 8-bit control registers. The RW select bit determines whether the SPI transaction is a write or read transaction. If RW=1 it signifies a WRITE transaction and if RW=0 then it signifies a READ transaction. The contents (ADDR or DATA) are latched into the digital block every eight clock cycles. The timing parameters for the SPI interface are shown in the Serial Interface Timing Parameters Table below. The clock rate for SCLK is flexible with a maximum rate of 10MHz.

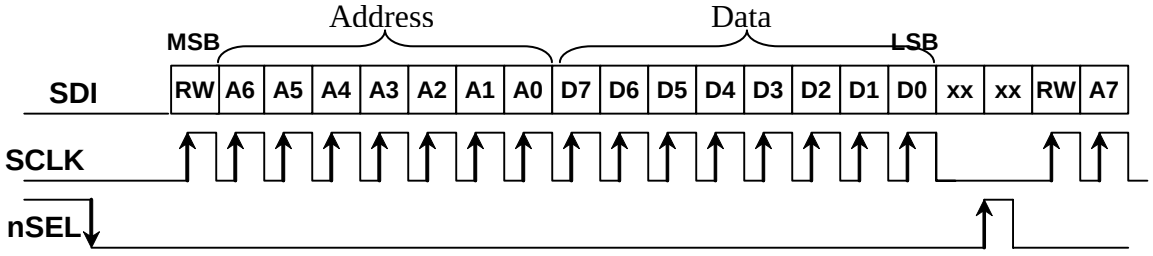
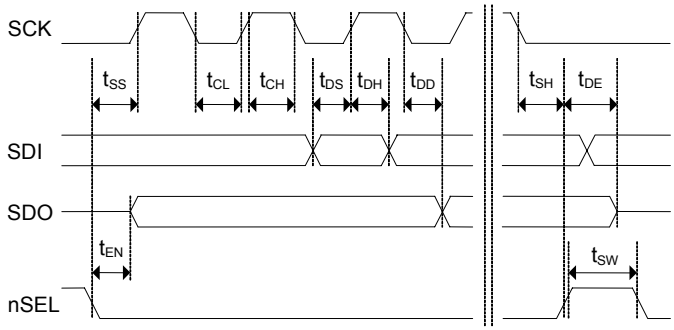


Figure 4: SPI Timing

Table 10: Serial Interface Timing Parameters

Symbol	Parameter	Min	Diagram
t_{CH}	Clock high time	40	
t_{CL}	Clock low time	40	
t_{DS}	Data setup time	20	
t_{DH}	Data hold time	20	
t_{DD}	Output data delay time	20	
t_{EN}	Output enable time	20	
t_{DE}	Output disable time	50	
t_{SS}	Select setup time	20	
t_{SH}	Select hold time	50	
t_{SW}	Select high period	80	

The SPI may also be used to read data back from the RFIC. In order to read back data from the RFIC the RW bit must be set to '0' followed by the 7-bit address of the register from which to read. The 8 bit DATA field following the 7 bit ADDR field is ignored when RW='0'. The next eight positive edge transitions of the SCLK signal will clock out the contents of the selected register. The data read from the selected register will be available on the SDO output pin. The READ function is shown in Figure 5 below. After the READ function is completed the SDO pin will remain at either a logic '1' or logic '0' state depending on the last data bit clocked out (D0). When nSEL goes high the SDO output pin will be pulled high by internal pull-up.

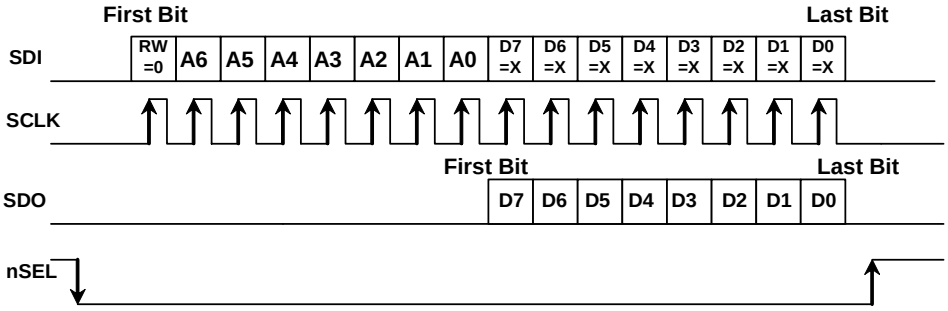


Figure 5: SPI Timing –READ Mode

The SPI interface contains a burst read/write mode which will allows for reading/writing sequential registers without having to re-send the SPI address. When the nSEL bit is held low while continuing to send SCLK pulses, the SPI interface will automatically increment the ADDR and read from/write to the next address. An SPI Burst Write transaction is demonstrated in Figure 6, and burst read in Figure 5. As long as nSEL is held low, input data will be latched into the digital block every eight SCLK cycles. A Burst Read Transaction is also demonstrated in Figure 7:

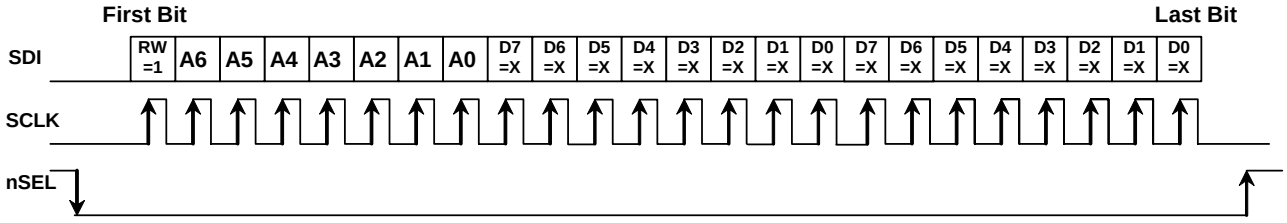


Figure 6: SPI Timing –Burst Write Mode

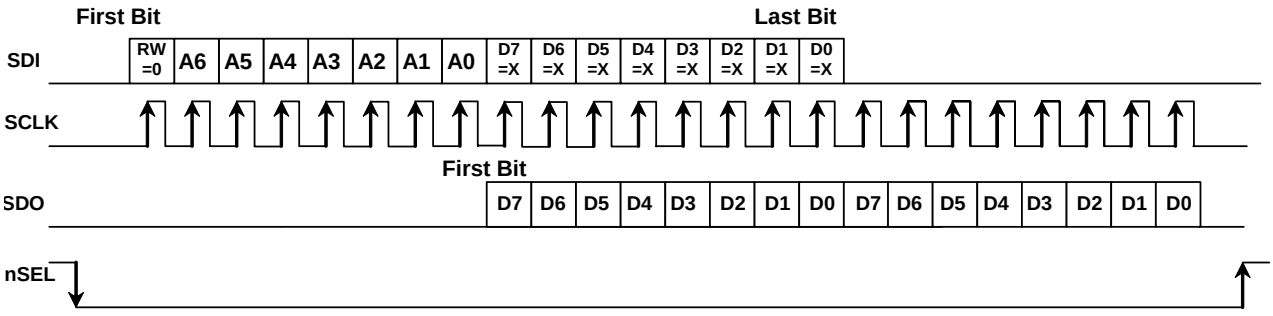


Figure 7: SPI Timing –Burst Read Mode

4.2 Operating Mode Control

There are four main states in the Main State Machine, SHUTDOWN, IDLE, TX, and RX (see Figure 8:). The SHUTDOWN state completely shuts down the radio to minimize current consumption. There are five different configurations/options for the IDLE state which can be selected to optimize the chip to the applications needs. SPI Registers 07h controls which operating mode/state is selected. The TX and RX state may be reached automatically from any of the IDLE states by selecting either the txon or rxon bits. Table 11: shows each of the operating modes with the time required to reach either RX or TX mode as well as the current consumption of each mode.

The output of the LPLDO is internally connected in parallel to the output of the Main Digital Regulator (and is available externally at the VR_DIG pin); this common digital supply voltage is connected to all digital circuit blocks, including the Digital Modem, Crystal Oscillator, and the SPI and Register Space. The LPLDO has extremely low quiescent current consumption but limited current supply capability; it is used only in the IDLE-STANDBY and IDLE-SLEEP modes.

Add	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
07	R/W	Operating & Function Control 1	swres	enlbd	enwt	x32ksel	txon	rxon	pllon	xton	01h

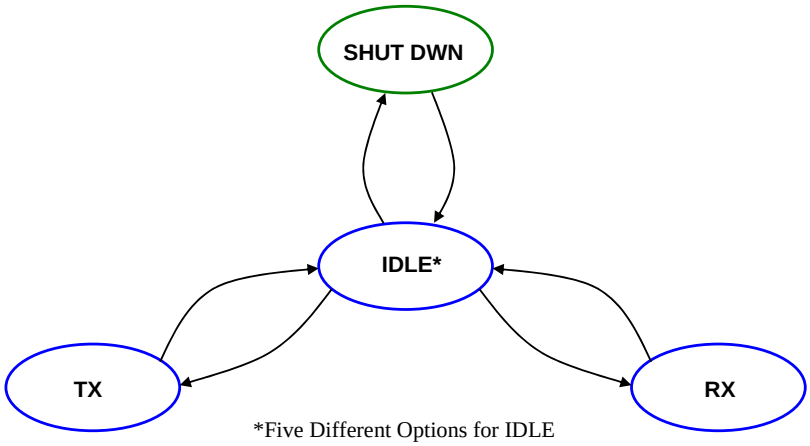


Figure 8: State Machine Diagram

Table 11: Operating Modes

State / Mode	xtal	pll	wt	LBD or TS	Response time to:		Current in State / Mode [uA]
					TX	RX	
Shut Down State	X X		X	X	16.21msec	16.21msec	10nA
Idle States							
Standby Mode	0	0	0	0	1.21msec	1.21msec	300nA
Sleep Mode	0	0	1	0			600nA
Sensor Mode	0	0	X	1			5uA
Ready Mode	1	0	X	X	210usec	210usec	600uA
Tune Mode	1	1	X	X	200usec	200usec	8mA
TX State	1 1		X	X	NA	200usec	60mA → +20dBm
RX State	1 1		X	X	200usec	NA	17mA

4.2.1 Shutdown State

The shutdown state is the lowest current consumption state of the chip with nominally only 5nA of current consumption. The shutdown state may be entered by setting the SDN pin (Pin 20) ='1'. The SDN pin should be = '0' in all states except SHUTDOWN state. In SHUTDOWN state the contents of the registers are lost and there is no SPI access.

When the chip is connected to the power supply, a POR will be initiated after the falling edge of SDN.

4.2.2 Idle State

There are five different modes in the IDLE state which may be selected by the SPI Register, 07h. All of the modes have a different tradeoff between current consumption and response time to TX mode. This is shown above in Table 11:. After the POR event, SWRESET, or exiting from the SHUTDOWN state the chip will default to the IDLE-READY mode.

4.2.2.1 STANDBY Mode

STANDBY mode has the lowest current consumption possible with only the LPLDO enabled to maintain the SPI register values. In this mode the registers can be accessed in both read and write mode. The standby mode can be entered by writing 0h to register 07h. If an interrupt has occurred (i.e. the nIRQ pin = '0') the interrupt registers must be read to achieve the minimum current consumption. Also, the ADC should not be selected as an input to the GPIO in this mode and will cause excess current consumption.

4.2.2.2 SLEEP Mode

In SLEEP mode the LPLDO is enabled along with the Wake-Up-Timer, which can be used to accurately wake-up the radio at specified intervals. See section 9.6 for more information on the Wake-Up-Timer. Sleep mode is entered by setting enwt='1' (40h) in register 07h. If an interrupt has occurred (i.e. the nIRQ pin = '0') the interrupt registers must be read to achieve the minimum current consumption. Also, the ADC should not be selected as an input to the GPIO in this mode and will cause excess current consumption.

4.2.2.3 SENSOR Mode

In SENSOR Mode either the Low Battery Detector, Temperature Sensor, or both may be enabled in addition to the LPLDO and Wake-Up-Timer. The Low Battery Detector may be enabled to setting enlbd='1' and the temperature sensor can be enabled by setting ents='1' in register 07h. See sections 9.4 and 9.5 for more information on these features. If an interrupt has occurred (i.e. the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption.

4.2.2.4 READY Mode

READY Mode is designed to give fast response time to TX mode with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to either TX mode by eliminating the crystal start-up time. Ready mode is entered by setting xton ='1' in register 07h. To achieve the lowest current consumption state the crystal oscillator buffer should be disabled. This is done by setting the value of register 62h to a value of 02h. To exit ready mode bit 2 of this register must be set back to 0.

4.2.2.5 TUNE Mode

In TUNE Mode the PLL remains enabled in addition to the other blocks which are enabled in the other IDLE Modes. This will give the fastest response to TX mode because the PLL will remain locked but it comes at the price of the highest current consumption. This mode of operation is designed for Frequency Hopping Systems. Tune mode is entered by setting pllon = '1' in register 07h, i.e. the value of register 07h should be 02h. It is not necessary to set xton to '1' for this mode, the internal state machine knows that the crystal oscillator needs to be running in this mode and will enable it automatically.

4.2.3 TX State

The TX state may be entered from any of the Idle Modes when the txon bit is set to '1' in SPI Register 07h. A built-in sequencer takes care of all the actions required to transition between states from enabling the Crystal Oscillator to ramping up the PA to prevent unwanted spectral splatter. The following sequence of events will occur automatically when going from STANDBY mode to TX mode by setting the txon bit.

1. Enable the Main Digital LDO and the Analog LDOs
2. Start up crystal oscillator and wait until ready (controlled by timer)
3. Enable PLL
4. Calibrate VCO (this action is skipped when the vcocal bit is "0", default value is "1")
5. Wait until PLL settles to required transmit frequency (controlled by timer)
6. Activate Power Amplifier and wait until power ramping is completed (controlled by timer)
7. Transmit Packet

The first few steps may be eliminated depending on which IDLE mode the chip is configured to prior to setting the txon bit. By default, the VCO and PLL are calibrated every time the PLL is enabled. If the ambient temperature is constant and the same frequency band is being used these functions may be skipped by setting the appropriate bits in SPI Register 55h.

4.2.4 RX State

The RX state may be entered from any of the Idle modes when the rxon bit is set to '1' in the SPI Register 07h. A built-in sequencer takes care of all the actions required to transition from one of the IDLE modes to the RX state. The following sequence of events will occur automatically to get the chip into RX mode when going from STANDBY mode to RX mode by setting the rxon bit:

1. Enable the Main Digital LDO and the Analog LDOs
2. Start up crystal oscillator and wait until ready (controlled by timer)
3. Enable PLL
4. Calibrate VCO (this action is skipped when the vcocal bit is "0", default value is "1")
5. Wait until PLL settles to required transmit frequency (controlled by timer)
6. Enable receive circuits: LNA, mixers, and ADC
7. Calibrate ADC (RC calibration)
8. Enable receive mode in the Digital Modem

Depending on the configuration of the radio all or some of the following functions will be performed automatically by the Digital Modem: AGC, AFC (optional), update status registers, bit synchronization, packet handling (optional) including sync word, header check, and CRC.

4.2.5 Device Status

Add	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
02 R		Device Status	*ffovfl f*	*funfl*	*rxffem*	*headerr*	*freqerr*	*lockdet*	*cps[1]*	*cps[0]*	-

The operational status of the chip can be read from register 02h. A description of each Status bit is shown in the table below.

Address: 02h – Device Status

Bit	R/W	Default	Function
7	R	0	**ffovfl** = RX/TX FIFO Overflow status.
6	R	0	**ffunfl** = RX/TX FIFO Underflow status.
5	R	0	**rxffem** = RX FIFO Empty status. When rxffem ='1' the RX FIFO is empty.
4	R	0	**headerr** = Header Error status. The actual received packet has a header check error.
3	R	0	**freqerr** = Frequency Error status. The programmed frequency is outside of the operating range. The actual frequency is saturated to the max/min value.
2	R	0	**lockdet** = Synthesizer Lock Detect status.
[1:0]	R	0	**cps[1:0]** = Chip Power State: 00 – Idle State 01 – RX State 10 – TX State

4.2.6 Interrupts

The RFIC is capable of generating an interrupt signal when certain events occur. The chip notifies the Microcontroller that an interrupt event has been detected by setting the nIRQ output pin LOW ='0'. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) shown below occur. The nIRQ pin will remain low until the Microcontroller reads the Interrupt Status register(s) (SPI Registers 03h-04h) containing the active Interrupt Status bit; the nIRQ output signal will then be reset until the next change in status is detected. All of the interrupts must be enabled by the corresponding enable bit in the Interrupt Enable Registers (SPI Registers 05h-06h). All enabled interrupt bits will be cleared when the microcontroller reads the interrupt status register. If the interrupt is not enabled when the event occurs inside of the chip it will not trigger the nIRQ pin but the status may still be read correctly at anytime in the Interrupt Status registers. The Interrupt Status and Interrupt Enable registers are found in addresses 03h-06h.

Add	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
03	R	Interrupt Status 1	*ifferr*	*itxffafull*	*itxffaem*	*irxffafull*	*iext*	*ipksent*	*ipkvalid*	*icrcerror*	-
04	R	Interrupt Status 2	*iswdet*	*ipreaval*	*ipreainval*	*irssi*	*iwut*	*ilbd*	*ichiprdy*	*ipor*	-
05	R/W	Interrupt Enable 1	enfferr	entxffafull	entxffaem	enrxffafull	enext	enpksent	enpkvalid	encrcerror	00h
06	R/W	Interrupt Enable 2	enswdet	enpreaval	enpreainval	enrssi	enwut	enlbd	enchiprdy	enpor	01h

A description of each of the different interrupts is given in the tables below.

Address: 03h – Interrupt or Status 1

Bit R/W		Default	Function
[7]	R	-	**ifferr** = FIFO Underflow/Overflow Error. When set to '1' the TX or RX FIFO has overflowed or underflowed.
[6]	R	-	**itxffafull** = TX FIFO Almost Full. When set to '1' the TX FIFO has met its almost full threshold and needs to be transmitted.
[5]	R	-	**itxffaem**= TX FIFO Almost Empty. When set to '1' the TX FIFO is almost empty and needs to be filled.
[4]	R	-	**irxffafull** = RX FIFO Almost Full. When set to '1' the RX FIFO has met its almost full threshold and needs to be read by the microcontroller
[3] R		-	**iext** = External Interrupt. When set to '1' an interrupt occurred on one of the GPIO's if it is programmed so. The status can be checked in register 0Eh. See GPIOx Configuration section for the details.
[2]	R	-	**ipksent** = Packet Sent Interrupt. When set to'1' a valid packet has been transmitted.
[1]	R	-	**ipkvalid** = Valid Packet Received. When set to '1' a valid packet has been received.
[0]	R	-	**icrcerror** = CRC Error. When set to '1' the cyclic redundancy check is failed.

When does the individual Status bits get Set/Cleared, if not enabled as an Interrupt?

Bit	Status Name	Set/Clear conditions:
[7]	**ifferr**	Set if there is a Tx or RX FIFO Overflow or Underflow. It is cleared only by applying FIFO reset to the specific FIFO that caused the condition.
[6]	**itxffafull**	Will be set when the number of bytes written to TX FIFO is greater than the Almost Full threshold set by SPI. It is automatically cleared when we start transmitting and the FIFO data is read out and the number of bytes left in the FIFO is smaller or equal to the threshold).
[5]	**itxffaem**	Will be set when the number of bytes (not yet transmitted) in TX FIFO is smaller or equal than the Almost Empty threshold set by SPI. It is automatically cleared when we write enough data to TX FIFO so that the number of data bytes not yet transmitted is above the Almost Empty threshold.
[4]	**irxffafull**	Will be set when the number of bytes received (and not yet read-out) in RX FIFO is greater than the Almost Full threshold set by SPI. It is automatically cleared when we read enough data from RX FIFO so that the number of data bytes not yet read is below the Almost Full threshold.
[3]	**iext**	External interrupt source
[2]	**ipksent**	Will go high once a packet is sent all the way through (no TX abort). This status will be cleaned if 1) We leave FIFO mode or 2) In FIFO mode we start a new transmission.
[1]	**ipkvalid**	Goes high once a packet is fully received (no RX abort). It is automatically cleaned once we receive and acknowledge the Sync Word for the next packet.
[0]	**icrcerror**	Goes High once the CRC computed during RX differs from the CRC sent in the packet by the TX. It is cleaned once we start receiving new data in the next packet.

Address: 04h – Interrupt or Status 2

Bit R/W		Default	Function
[7]	R	-	**iswdet** = Sync Word Detected. When a sync word is detected this bit will be set to 1.
[6]	R	-	**ipreaval** = Valid Preamble Detected. When a preamble is detected this bit will be set to 1.
[5]	R	-	**ipreainval** = Invalid Preamble Detected. When the preamble is not found within a period of time after the RX is enabled, this bit will be set to 1.
[4]	R	-	**irssi** = RSSI. When RSSI level exceeds the programmed thershold this bit will be set to 1.
[3]	R	-	**iwut** = Wake-Up-Timer. On the expiration of programmed wake-up timer this bit will be set to 1.
[2] R		-	**ilbd** = Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled.
[1]	R	-	**ichiprdy** = Chip Ready (XTAL). When a chip ready event has been detected this bit will be set to 1.
[0]	R	-	**ipor** = Power-on-Reset (POR). When the chip detectes a Power on Reset above the desired setting this bit will be set to 1.

When does the individual Status bits get Set/Cleared, if not enabled as an Interrupt?

Bit	Status Name	Set/Clear conditions:
[7]	**iswdet**	Goes high once the Sync Word is detected. Goes low once we are done receiving the current packet.
[6]	**ipreaval**	Goes high once the preamble is detected. Goes low once the sync is detected or the RX wait for the sync times-out.
[5]	**ipreainval**	Self cleaning, user should use this as an interrupt source rather than a status.
[4]	**irssi**	Should remain high as long as the RSSI value is above programmed threshold level
[3]	**iwut**	Wake time timer interrupt. Use as an interrupt, not as a status.
[2]	**ilbd**	Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. Probably the status is cleared once the battery is replaced.
[1]	**ichiprdy**	Chip ready goes high once we enable the xtal, Tx or RX and a settling time for the Xtal clock elapses. The status stay high unless we go back to Idle mode.
[0]	**ipor**	Power on status.

4.2.7 Device Code

The device version code will be internally hardwired and readable from Register 01h. This is a read only register.

Add	R / W	Function / Description	Data								POR Default	Notes
			D7	D6	D5	D4	D3	D2	D1	D0		
01	R	Device Version	0	0	0	vc[4]	vc[3]	vc[2]	vc[1]	vc[0]	00h	DV

4.2.8 System Timing

The system timing for TX and RX modes is shown in Figures 9 and 10. The timing is shown transitioning from STANDBY mode to TX mode and going automatically through the built-in sequencer of required steps. If a small range of frequencies is being used and the temperature range is fairly constant a calibration may only be needed at the initial power up of the device and may be skipped after this to save time. The relevant system timing registers are shown below.

Add	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
53	R/W	PLL Tune Time	pllts[4]	pllts[3]	pllts[2]	pllts[1]	pllts[0]	pllt0[2]	pllt0[1]	pllt0[0]	45h
54	R/W	Reserved 1	X	X	X X		X X		X	X	00h
55 R/	W	Calibration Control			*adccaldone*	enrcfcal	rccal	vcocaldp	vcocal	skipvco	04h

The VCO will automatically calibrate at every frequency change or power up. The VCO CAL may also be forced by setting the vcocal bit. The 32.768kHz RC oscillator is also automatically calibrated but the calibration may also be forced. The enrcfcal will enable the RC Fine Calibration which will occur every 30 seconds. The rccal bit will force a complete calibration of the RC oscillator which will take approximately 2msec. The PLL T0 time is to allow for bias settling of the VCO, the default for this should be adequate. The PLL TS time is for the settling time of the PLL, which has a default setting of 200us. This should be safe for all applications but this time may be reduced if small frequency jumps are used.

Address: 53h – PLL Tune Time

Bit R/W		Default	Function
[7:3] R/W		01000	**pllts[4:0]** = PLL Soft Settling Time (T_S). This register will set the settling time for the PLL from a previous locked frequency in Tune mode. The value is configurable between 0 µs and 310 µs, in 10 µs intervals. The default plltime corresponds to 80 µs. See formula above.
[2:0] R/W		101	**pllt0** = PLL Settling Time (T_O). This register will set the time allowed for PLL settling after the calibrations are completed. The value is configurable between 0 µs and 70 µs, in 10 µs steps. The default pllt0 corresponds to 50 µs. See fomula above.

Address: 55h – Calibration Control

Bit R/W		Default	Function
[7:5] R		-	RESERVED
4 R		-	**adccaldone** = Delta-sigma ADC Calibration Done. Reading this bit gives '1' if the calibration process has been finished.
3 R/W		0	**enrcfcal** = RC Oscillator Fine Calibration enable. If this bit is set to '1' then the RC oscillator performs fine calibration in every app. 30 s.
2 R/W		0	**rccal** = RC Calibration Force. If setting rccal='1' will automatically perform a forced calibration of the 32kHz RC Oscillator. The RC OSC will automatically be calibrated if the Wake-Up-Timer is enabled or if in the Wake-on-Receiver state. The calibration takes 2ms. The 32kHz RC oscillator must be enabled to perform a calibration. Setting this signal from a '0' to '1' will initiate the calibration. This bit is cleared automatically.
1 R/W		0	**vcocal** = VCO Calibration Force. If in Idle Mode and pllon='1', setting vcocal='1' will force a one time calibration of the synthesizer VCO. This bit is cleared automatically.
0 R/W		0	**skipvco** = Skip VCO Calibration. Setting skipvco='1' will skip the VCO calibration when going from the Idle state to the TX or RX state.

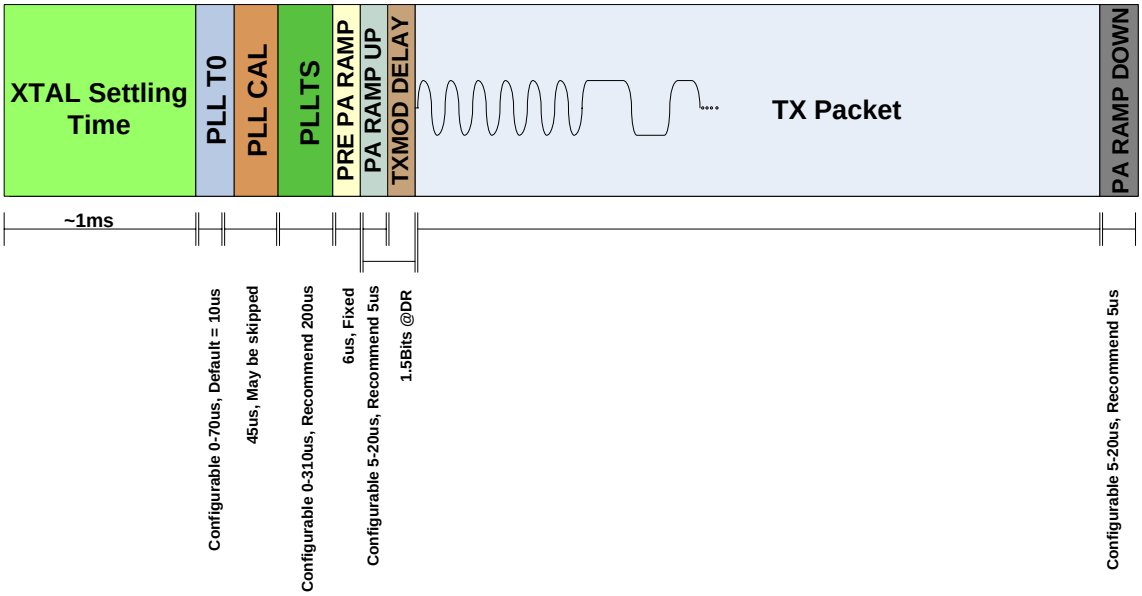


Figure 9: TX Timing

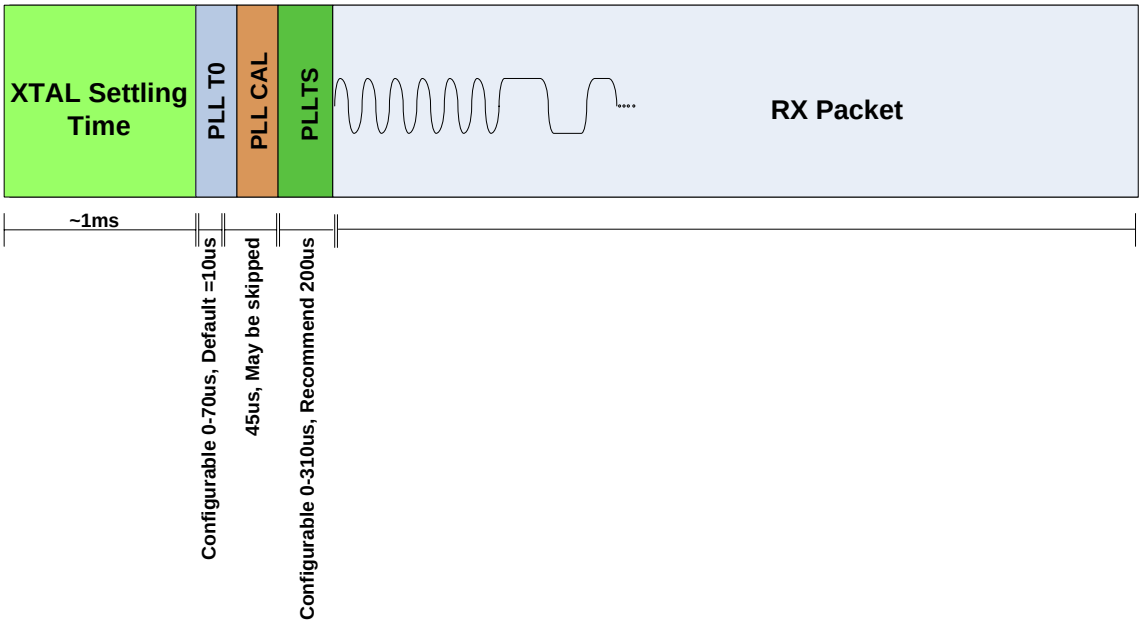


Figure 10: RX Timing

4.2.9 Frequency Control

For all frequency register settings it is easiest to use the easy control window in Integration's Wireless Design Suite (WDS) or the Excel Calculator available on the product website. A detailed description is offered below on how to calculate manually.

4.2.9.1 Carrier Generation

The carrier frequency is generated by a Fractional-N Synthesizer, using 10MHz both as the reference frequency and the clock of the (3rd order) ΔΣ modulator. This modulator uses modulo 64000 accumulators. This design choice was made to obtain the desired frequency resolution of the synthesizer. The overall division ratio of the feedback loop consist of an integer part (N) and a fractional part (F). In a generic sense the output frequency of the synthesizer:

F_{out} = 10MHz *(N+F).

The fractional part (F) is determined by three different values, Carrier Frequency (fc[15:0]), Frequency Offset (fo[8:0]), and Frequency Modulation (fd[7:0]). Due to the fine resolution and high loop bandwidth of the synthesizer, FSK modulation is applied inside the loop and is done by varying F according to the incoming data; this is discussed further in Section 4.2.9.4 below. Also, a fixed offset can be added to fine-tune the carrier frequency and counteract crystal tolerance errors. For simplicity assume that only the fc[15:0] register will only determine the fractional component. The equation for selection of the output frequency is shown below:

$$f_{TX} = 10MHz * (hbsel + 1) * (N + F)$$

$$f_{TX} = 10MHz * (hbsel + 1) * (fb[4:0] + 24 + \frac{(fc[15:0])}{64000}$$

Add	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
73	R/W	Frequency Offset 1	fo[7]	fo[6]	fo[5]	fo[4]	fo[3]	fo[2]	fo[1]	fo[0]	00h
74	R/W	Frequency Offset 2							fo[9]	fo[8]	00h
75	R/W	Frequency Band Select		-	hbsel	fb[4]	fb[3]	fb[2]	fb[1]	fb[0]	35h
76	R/W	Nominal Carrier Frequency 1	fc[15]	fc[14]	fc[13]	fc[12]	fc[11]	fc[10]	fc[9]	fc[8]	BBh
77	R/W	Nominal Carrier Frequency 0	fc[7]	fc[6]	fc[5]	fc[4]	fc[3]	fc[2]	fc[1]	fc[0]	80h

The integer part (N) is determined by fb[4:0]. Additionally, the output frequency can be halved by connecting a ÷2 divider to the output. This divider is not inside the loop and is controlled by the hbsel bit in Frequency Band Select Register 75h. This effectively partitions the entire 240-930 MHz frequency range into two separate bands: High Band (HB) for hbsel=1, and Low Band (LB) for hbsel=0. The valid range of fb[4-0] is from 0 to 23. If a higher value is written into the register, it will default to a value of 23. The integer part has a fixed offset of 24 added to it as shown in the formula above. *Table 12:* demonstrates the selection of fb[4:0] for the corresponding frequency band.

After selection of the fb (N) the fractional component may be solved with the following equation:

$$fc[15:0] = \frac{f_{TX} * 64000}{10MHz * (hbsel + 1) * fb[4:0] + 24}$$

fb, and fc are the actual numbers stored in the corresponding registers.

Table 12: Frequency Band Selection

fb[4:0] Value	N	Frequency Band	
		hbsel=0	hbsel=1
0 24		240-249.9MHz	480-499.9MHz
1 25		250-259.9MHz	500-519.9MHz
2 26		260-269.9MHz	520-539.9MHz
3 27		270-279.9MHz	540-559.9MHz
4 28		280-289.9MHz	560-579.9MHz
5 29		290-299.9MHz	580-599.9MHz
6 30		300-309.9MHz	600-619.9MHz
7 31		310-319.9MHz	620-639.9MHz
8 32		320-329.9MHz	640-659.9MHz
9 33		330-339.9MHz	660-679.9MHz
10 34		340-349.9MHz	680-699.9MHz
11 35		350-359.9MHz	700-719.9MHz
12 36		360-369.9MHz	720-739.9MHz
13 37		370-379.9MHz	740-759.9MHz
14 38		380-389.9MHz	760-779.9MHz
15 39		390-399.9MHz	780-799.9MHz
16 40		400-409.9MHz	800-819.9MHz
17 41		410-419.9MHz	820-839.9MHz
18 42		420-429.9MHz	840-859.9MHz
19 43		430-439.9MHz	860-879.9MHz
20 44		440-449.9MHz	880-899.9MHz
21 45		450-459.9MHz	900-919.9MHz
22 46		460-469.9MHz	920-930MHz
23 47		470-479.9MHz	X

The chip will automatically shift the frequency of the Synthesizer downwards by 937.5 kHz (30MHz ÷ 32) to achieve the proper Intermediate Frequency (IF) when RX mode is entered. Low-side injection is used in the RX Mixing architecture. Therefore no frequency reprogramming is required when using the same TX frequency and switching between RX/TX modes.

4.2.9.2 Easy Frequency Programming for FHSS

While Registers 73h-77h may be used to program the carrier frequency of the RFIC, it is often easier to think in terms of "channels" or "channel numbers" rather than an absolute frequency value in Hz. Also, there may be some timing-critical applications (such as for Frequency Hopping Systems) in which it desirable to change frequency by programming a single register. An Easy Frequency Programming Register is provided to accommodate these needs. A nominal frequency is first set using Registers 73h-77h, as described above. Registers 79h and 7Ah are then used to set a channel step size and channel number, relative to the nominal setting. The Frequency Hopping Step Size (fhs[7:0]) is set in increments of 10kHz with a maximum channel step size of 2.56MHz. The Frequency Hopping Channel Select Register then selects channels based on multiples of the step size.

$$F_{TX} = Fnom + fhs[7:0] * (fhch[7:0] * 10kHz)$$

For example: the nominal frequency is set to 900MHz using Registers 73h-77h and the channel step size is set to 1 MHz using Register 79h. If the Frequency Hopping Channel Select Register 78h is set to 5d, the resulting carrier frequency would be 905MHz. Once the nominal frequency and channel step size are programmed in the registers, it is only necessary to program the fhch[7:0] register in order to change the frequency.

Add	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
79	R/W	Frequency Hopping Channel Select	fhch[7]	fhch[6]	fhch[5]	fhch[4]	fhch[3]	fhch[2]	fhch[1]	fhch[0]	00h
7A	R/W	Frequency Hopping Step Size	fhs[7]	fhs[6]	fhs[5]	fhs[4]	fhs[3]	fhs[2]	fhs[1]	fhs[0]	00h

4.2.9.3 Automatic Frequency Change

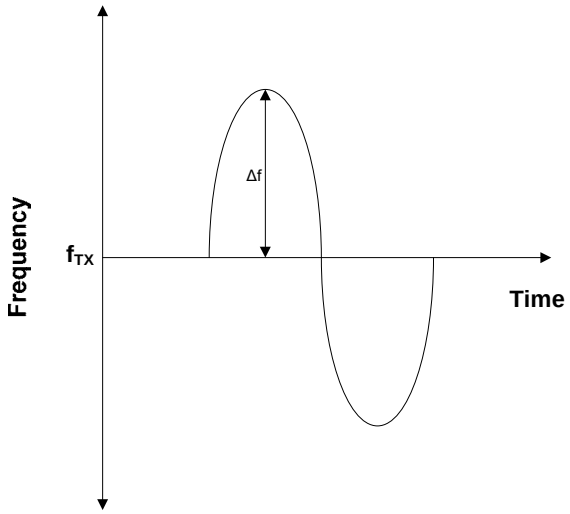
If registers 79h or 7Ah are changed in either TX or RX mode then the state machine will automatically transition the chip back to Tune change the frequency and automatically go back to either TX or RX. This feature is useful to reduce the number of SPI commands required in a Frequency Hopping System.

4.2.9.4 Frequency Deviation

The peak frequency deviation is configurable from ±1 to ±160kHz. The Frequency Deviation (Δf) is controlled by the Frequency Deviation Register (fd), address 72h and is independent of the carrier frequency setting that is, regardless of the setting of the hbsel bit (high band or low band) the resolution of the frequency deviation will remain in increments of 625 Hz. When using frequency modulation the carrier frequency will deviate from the nominal center channel carrier frequency by +/- Δf:

$$\Delta f = fd[7:0] * 625Hz$$

$$fd[7:0] = \frac{\Delta f}{625Hz} \qquad \Delta f = \text{peak deviation}$$



The above equation should be used to calculate the desired frequency deviation. If desired, frequency modulation may also be disabled in order to obtain an unmodulated carrier signal at the channel center frequency; see Section 5.1 for further details.

Add	R / W	Function / Description	Data								POR Default	Notes
			D7	D6	D5	D4	D3	D2	D1	D0		
72	R/W	Frequency Deviation	fd[7]	fd[6] f	d[5]	fd[4] f	d[3]	fd[2]	fd[1]	fd[0]	43h	FDEV

4.2.9.5 Frequency Offset Adjustment

When the AFC is disabled the Frequency offset can be adjusted manually by fo[9:0] in registers 73h and 74h. The Frequency offset adjustment and the AFC both are implemented by shifting the Synthesizer Local Oscillator frequency. This register is a signed register so in order to get a negative offset you will need to take the 2's compliment of the positive offset number. The offset can be calculated by:

$$DesiredOffset = 156.25Hz * (hbsel + 1) * fo[9:0]$$

$$fo[9:0] = \frac{DesiredOffset}{156.25Hz * (hbsel + 1)}$$

The adjustment range in high band is: +/- 160 kHz, and adjustment range in low band is: +/- 80 kHz. For example to compute an offset of +50kHz in high band mode fo[9:0] should be set to 0A0h. For an offset of -50kHz in high band mode the fo[9:0] register should be set to 360h.

When AFC is enabled the same registers can be used to read the offset value as automatically obtained by the AFC.

Add	R / W	Function / Description	Data								POR Default	Notes
			D7	D6	D5	D4	D3	D2	D1	D0		
73	R/W	Frequency Offset	fo[7]	fo[6] f	o[5]	fo[4] f	o[3]	fo[2]	fo[1]	fo[0]	00h	73
74	R/W	Frequency Offset							fo[9]	fo[8]	00h	

4.2.9.6 Auto Frequency Control (AFC)

Automatic Frequency Control (AFC) is added in the receive modem to compensate for frequency differences between transmit and receive frequency caused by tolerances and temperature dependencies from the reference crystal from both receiver and transmitter. The AFC may be disabled if the frequency errors are tolerable. E.g about 3dB of sensitivity is lost when the frequency error is ±5% of the signal bandwidth (= required channel filter bandwidth). Higher frequency error will result in more desensitization.

The maximum frequency error that the AFC can handle is about 50% of the channel filter bandwidth. The required channel filter bandwidth can be calculated as: BW = 2 x C x (Fdev + 0.5Rb) where C = 1 for FSK and 0.9 for GFSK, Fdev is the frequency deviation and Rb is the data rate.

The AFC function shares registers 73h and 74h with the Frequency Offset setting. If AFC is enabled then reading this value will show the results of the AFC algorithm for the current receive slot. When the AFC is enabled the Frequency Offset will initially be reset to zero when the receiver is enabled and then settle to the final value.

The AFC is enabled by register 1Dh.

Add	R / W	Function / Description	Data								POR Default	Notes
			D7	D6	D5	D4	D3	D2	D1	D0		
1D	R/W	AFC Loop Gearshift Override	-	enafc	-	-	-	-	-	-	41h	1D

When the AFC is enabled the preamble length needs to be long enough to settle the AFC. In general four bytes of preamble is sufficient. If the AFC is disabled the preamble can be shorter, 2 bytes preamble length can be sufficient assuming no AFC tuning is required.

The AFC measures the frequency error and consequently it corrects the frequency by changing the frequency of the Fractional-N PLL that determines the exact receive frequency.

During RX the AFC correction will be stored internally such that TX mode can be corrected by the same frequency, see table below:

	Frequency correction	
	RX	TX
AFC disabled	Freq offset register	Freq offset register
AFC enabled	AFC	Stored AFC

When the AFC is disabled the frequenc y offset will be contro lled by the value in the Fre q offset register. This value might be the result of a previous AFC action or by just overriding the Frequency Offset Register over the SPI bus, whichever was the latest.

4.2.10 TX Data Rate Generator

The data rate is configurable between 1-128kbps. The TX date rate is determined by the following formula:

$$DR\_TX = \frac{txdr[15:0] \cdot 1MHz}{2^{16}}$$

$$txdr[15:0] = \frac{DR\_TX * 2^{16}}{1MHz}$$

The resolution of the data rate is determined by 1MHz/2^16 or approximately 15.26 Hz. The txdr register may be found in the below registers.

Add	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
6E	R/W	TX Data Rate 1	txdr[15]	txdr[14]	txdr[13] t	xdr[12]	txdr[11] t	xdr[10]	txdr[9]	txdr[8]	0Ah
6F	R/W	TX Data Rate 0	txdr[7]	txdr[6]	txdr[5]	txdr[4]	txdr[3]	txdr[2]	txdr[1]	txdr[0]	AAh

5 MODULATION OPTIONS

5.1 Modulation Type

There are three different options for the type of modulation: GFSK (Gaussian Frequency Shift Keying), FSK (Frequency Shift Keying), OOK (On-Off Keying). GFSK is the recommended modulation type as it provides the best performance and cleanest modulation spectrum compared to FSK. Figure 11 demonstrates the difference between FSK and GFSK for a Data Rate of 64kbps. In the time domain plots on the left you can see the effects of the Gaussian filtering. On right hand side plot of Figure 11 demonstrate the obvious spectral benefit to GFSK over FSK. The type of modulation is selected with the modtyp[1:0] bits in Register 71h. Note that it is also possible to obtain an unmodulated carrier signal by setting modtyp[1:0]=00.

modtyp[1:0]	Modulation Source
00	Unmodulated Carrier
01 OOK	
10	FSK
11	GFSK (enable TX Data CLK when direct mode is used)

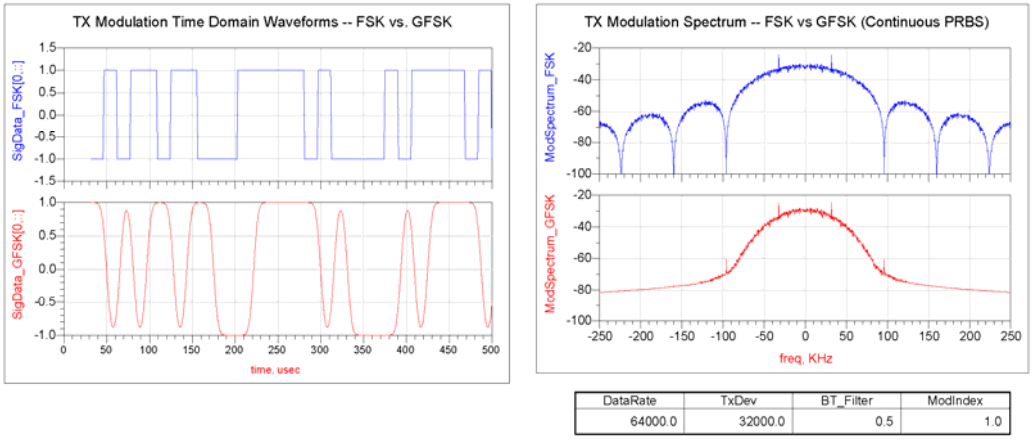


Figure 11: FSK vs. GFSK Spectrum

5.2 Modulation Data Source

The chip may be configured to obtain its modulation data from one of three different sources: FIFO mode, Direct Mode, and PN9 mode. Furthermore, in Direct Mode the TX modulation data may be obtained from several different input pins. These options are set through the dtmod[1:0] field in Register 71h.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
71	R/W	Modulation Mode Control 2	trclk[1] t	rclk[0]	dtmod[1]	dtmod[0]	eninv	-	modtyp[1]	modt yp[0]	23h

dtmod[1:0]	Modulation Source
00	Direct Mode using TX_Data via GPIO pin (GPIO needs programming accordingly as well)
01	Direct Mode using TX_Data via SDI pin (only when nSEL is high)
10	FIFO Mode
11	PN9 (internally generated)

5.3 FIFO Mode

In FIFO mode the integrated FIFOs are used to transmit and receive the data. The FIFOs are accessed over the SPI through Register 7Fh with burst read/write capability. The FIFOs may be configured specific to the application packet size, etc. (see Section 7.0 for further information).

When in FIFO mode the chip will automatically exit TX or RX State when either the ipksent or ipkvalid interrupt occurs. The chip will return to any of other states based on the settings in Register 07h. For instance if the chip is put into TX mode and both the txon and pllon bits are set, the chip will transmit all of the contents of the FIFO and the ipksent interrupt will occur. When this event occurs the chip will clear the txon bit and return to pllon or Tune Mode. If no other bits are set in register 07h besides txon initially then the chip will return to the Idle state.

In RX mode the rxon bit will only be cleared if ipkvalid occurs. A CRC, Header, or Sync error will only generate an interrupt and the microcontroller will need to decide on the next action.

5.4 Direct Mode

For larger packets bigger than the FIFO size of 64bytes it may not be desirable to use the FIFO so a direct mode is available. In this scenario a Direct Mode is provided which bypasses the FIFOs entirely. In Direct Mode the TX modulation data is applied to an input pin of the chip and processed in "real time" (i.e., not stored in a register for transmission at a later time). There are various configurations for choosing which pin is used for the TX Data. Furthermore, an additional input pin is required for the TX Data Clock if GFSK modulation is desired (only the TX Data input pin is required for FSK). Two options for the source of the TX Data are available in the dtmod[1:0] field, and various configurations for the source of the TX Data Clock may be selected through the trclk[1:0] field.

trclk[1:0]	TX Data Clock Configuration
00	No TX Clock (only for FSK)
01	TX Data Clock is available via GPIO (GPIO needs programming accordingly as well)
10	TX Data Clock is available via SDO pin (only when nSEL is high)
11	TX Data Clock is available via the nIRQ pin

The eninv bit in Address 71h will invert the TX Data for testing purposes.

5.5 PN9 Mode

In this mode the TX Data is generated internally using a pseudorandom (PN9 sequence) bit generator. The primary purpose of this mode is to use as a test mode to observe continuously the modulated spectrum without having to load/provide data.

5.6 Synchronous vs. Asynchronous

In Asynchronous mode no clock is used to synchronize the data to the internal modulator. This mode can only be used with FSK. The advantage of this mode that it saves a microcontroller pin because no data clock is required. The disadvantage is that you don't get the clean spectrum and limited BW of GFSK. If Asynchronous FSK is used the TX_DR register should be set to its maximum value.

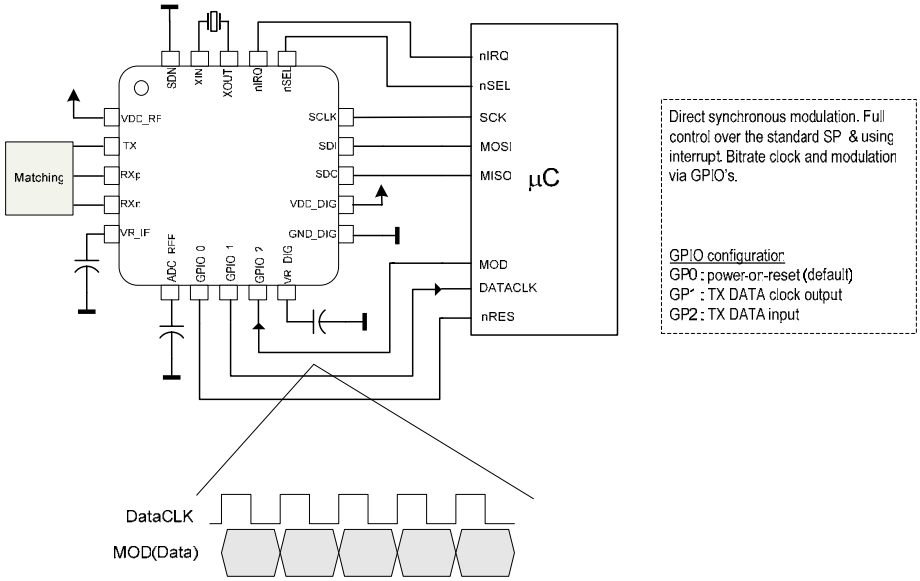


Figure 12: Direct Synchronous Mode Example

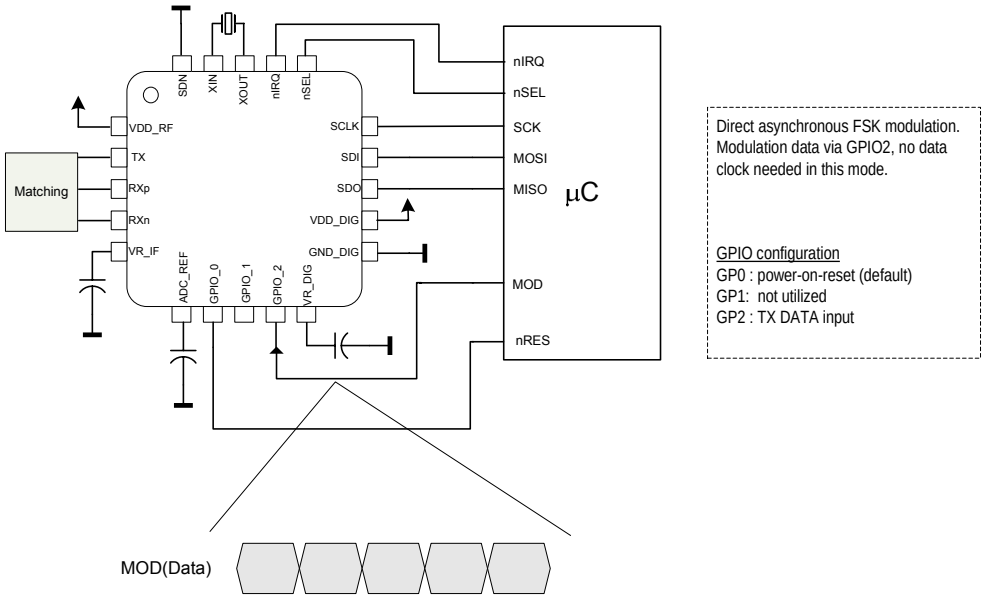


Figure 13: Direct Asynchronous Mode Example

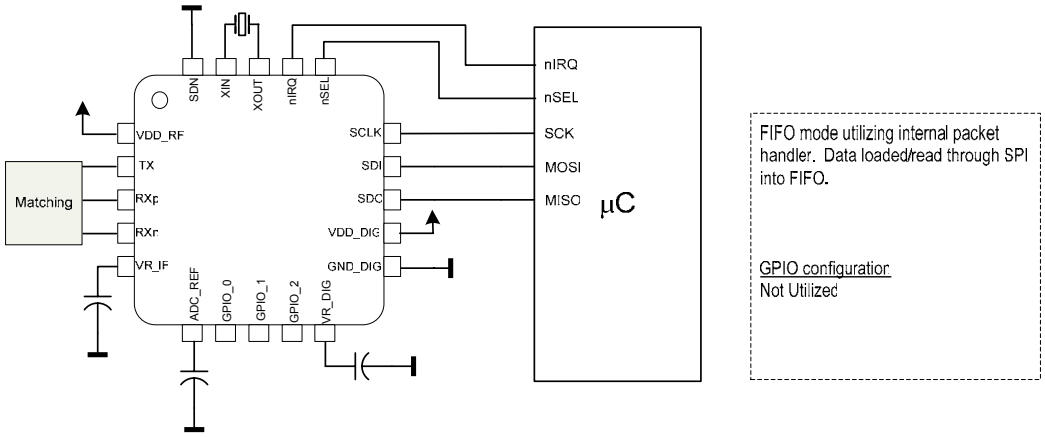


Figure 14: FIFO Mode Example

6 INTERNAL FUNCTIONAL BLOCKS

6.1 RX LNA

The input frequency range for the LNA is 240-930MHz. The LNA provides gain with a noise figure low enough to suppress the noise of the following stages. The LNA has one step of gain control which is controlled by the analog gain control (AGC) algorithm. The AGC algorithm adjusts the gain of the LNA and PGA so the receiver can handle signal levels from sensitivity to +5dBm with optimal performance.

6.2 RX I-Q Mixer

The output of the LNA is fed internally to the input of the receive mixer. The receive mixer is implemented as an I-Q mixer that provides both I and Q channel outputs to the complex IF filter. The mixer consists of two double-balanced mixers whose RF inputs are driven in parallel, local oscillator (LO) inputs are driven in quadrature, and separate I and Q Intermediate Frequency (IF) outputs drive the complex filter. The receive LO signal is supplied by an integrated VCO and PLL synthesizer operating between 240-930 MHz. The necessary quadrature LO signals are derived from the divider at the VCO output.

6.3 Programmable Gain Amplifier

The Programmable Gain Amplifier (PGA) provides the necessary gain to boost the signal level into the Dynamic Range of the ADC. The PGA must also have enough gain switching to allow for large input signals to ensure a linear RSSI range up to -30dBm. The PGA is designed to have steps of 3dB which will be controlled by the AGC algorithm in the digital modem.

6.4 ADC

The amplified I &Q IF signals are digitized using an Analog-to-Digital Converter (ADC). This architecture allows for low current consumption and high dynamic range. The bandpass response of the ADC provides exceptional rejection of out of band blockers.

6.5 Digital Modem

Using high performance ADC's allows channel filtering, image rejection, and demodulation to be performed in the digital domain where it can be done with less area, be more reconfigurable, and flexible. The digital modem performs the following functions:

- Channel Selection Filter
- TX Modulation
- RX Demodulation
- AGC
- Preamble Detector
- Invalid Preamble Detector
- Radio Signal Strength Indicator (RSSI)
- Automatic Frequency Compensation (AFC)
- Packet Handling including EZMac™ features
- Cyclic Redundancy Check (CRC)

The digital Channel Filter and Demodulator are optimized for ultra low power consumption and are highly configurable. Supported modulation types are GFSK, FSK, and OOK. The Channel Filter can be configured to support a large choice of bandwidths ranging from 600kHz down to as low as 2.4kHz. Also a large variety of data rates are supported ranging from 1 Kbps up to 128 kbps. The AGC algorithm is implemented digitally using an advanced control loop optimized for fast response time.

The main purpose of the configurable Preamble Detector is to improve the reliability of the Sync-word detection. The Sync-word detector is enabled only when a valid preamble is detected reducing the probability of false Sync-word detection considerably.

The Invalid Preamble Detector issues an interrupt when no valid preamble signal is found. After the receiver is enabled (Antenna Diversity disabled) the Invalid Preamble Detector output is ignored for 16Tb (Tb is the time of the bit duration) to allow the receiver to settle. The Invalid Preamble Detect interrupt can be handy to save power and speed-up search in receive mode. It is advised to mask the invalid preamble interrupt when Antenna Diversity is enabled. The Received Signal Strength Indicator (RSSI) provides a measure of the signal strength received on the tuned channel. The resolution of the RSSI read-out is in increments of 0.5dB, such a high resolution enables accurate channel assessment needed for CCA (Clear Channel Assessment), CS (Carrier Sense) and LBT(Listen Before Talk) functionality..

Frequency detuning caused by crystal inaccuracies can be compensated by enabling the digital Automatic Frequency Compensation (AFC) in receive mode.

A comprehensive programmable Packet Handler including key features of Integration's EZMac™ is integrated to create a variety of communication topologies ranging from peer-to-peer networks to mesh networks. The extensive programmability of the packet header allows for advanced packet filtering which in turn enables a mix of broadcast, group and point-to-point communication.

A wireless communication channel can be distorted by noise and interference, and it is therefore important to know if the received data is free of errors. A Cyclic Redundancy Check (CRC) is use to detect the presence of erroneous bits in each packet. A CRC is computed and appended at the tail of each transmitted packet and verified by the receiver to confirm that no errors have occurred. The Packet Handler and CRC are extremely valuable features which can significantly reduce the load on the Microcontroller allowing for a simpler and cheaper Microcontroller. However, these functions can be disabled if it desired to perform them in the Microcontroller.

The Digital Modem includes the TX Modulator which converts the TX Data bits into the corresponding stream of digital modulation values to be summed with the fractional input to the sigma-delta modulator. This modulation approach results in highly accurate resolution of the frequency deviation. A Gaussian filter is implemented to support GFSK, considerably reducing the energy in the adjacent channels.

6.6 Synthesizer

An integrated Sigma Delta (ΣΔ) Fractional-N PLL synthesizer capable of operating from 240-930MHz is provided on-chip. Using a ΣΔ synthesizer has many advantages; it provides large amounts of flexibility in choosing data rate, deviation, channel frequency, and channel spacing. The transmit modulation is applied directly to the loop in the digital domain through the fractional divider which results in very precise accuracy and control over the transmit deviation.

The PLL and Δ-Σ modulator scheme is designed to support any desired frequency and channel spacing in the range from 240-930MHz with a frequency resolution of 156.25Hz (Low Band) or 312.5Hz (High Band). The transmit data rate may be programmed to be between 1-128kb/s and the frequency deviation may be programmed to be between ±1-160kHz. These parameters may be adjusted by setting the appropriate SPI Register(s), as shown in Section 4.2.9.

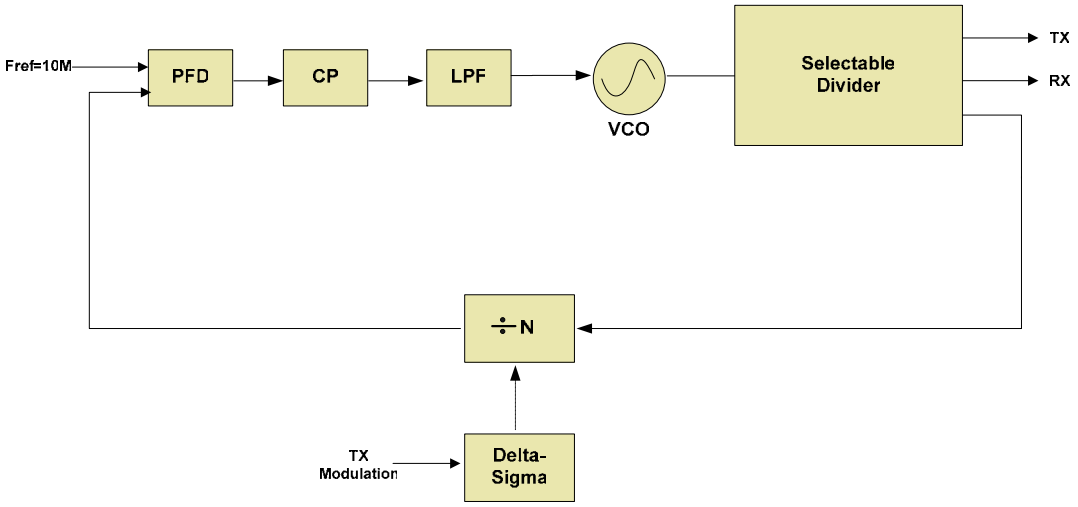


Figure 15: PLL Synthesizer Block Diagram

The reference frequency to the PLL is 10MHz. The PLL utilizes a differential L-C VCO, with integrated on-chip spiral inductors. The output of the VCO is followed by a configurable divider which will divide down the signal to the desired output frequency band. The modulus of this divider stage is controlled dynamically by the output from the Δ-Σ modulator. The tuning resolution of the Δ-Σ modulator is determined largely by the over-sampling rate and the number of bits carried internally. The tuning resolution is sufficient to tune to the commanded frequency with a maximum accuracy of 312.5 Hz anywhere in the range between 240-930MHz.

6.6.1 VCO

The output of the VCO is automatically divided down to the correct output frequency depending on the hbsel and fb[4:0] fields in the Frequency Band Select Register 75h. A 2X VCO is utilized to help avoid problems due to frequency pulling, especially when turning on the integrated Power Amplifier. In receive mode, the LO frequency is automatically shifted downwards (without reprogramming) by the IF frequency of 937.5 kHz, allowing transmit and receive operation on the same frequency. The VCO integrates the resonator inductor, tuning varactor, so no external VCO components are required.

The VCO uses capacitance bank to cover the wide frequency range specified. The capacitance bank will automatically be calibrated every time the synthesizer is enabled. In certain fast hopping applications this might not be desirable so the VCO calibration may be skipped by setting the appropriate SPI register.

6.7 Power Amplifier

The RFIC contains an internal integrated power amplifier (PA) capable of transmitting at output levels between +11 to +20dBm. The output power is programmable in 3dB steps through the txpow[1:0] field in SPI Register 6Dh.

The PA design is single-ended and is implemented as a two stage class CE amplifier with efficiency in the range of 45-50% while transmitting at +20dBm. The efficiency drops to approximately 20% when operating at +11dBm. Due to the high efficiency a simple filter is required on the board to filter the harmonics. The PA output is ramped up and down to prevent unwanted spectral splatter.

6.7.1 Output Power Selection

The output power is configurable in 3dB steps from +11dBm to +20dBm with the txpow[1:0] field in SPI Register 6Dh. Note that Frequency Hopping (FHSS) is required by the FCC when using an output power level of +20dBm. Please see Section 9.12 for further information on FHSS. The PA output is ramped up and down to prevent unwanted spectral splatter.

The extra output power can allow use of a cheaper smaller antenna, greatly reducing the overall BOM cost. The higher power setting of the chip achieves maximum possible range, but of course comes at the cost of higher TX current consumption. However, depending on the duty cycle of the system the effect on battery life may be insignificant. Contact Integration Support for help in evaluating this tradeoff.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
6D	R/W	TX Power							txpow[1]	txpow[0]	07h

txpow[1:0]	Output Power
00	+11dBm
01	+14dBm
10	+17dBm
11	+20dBm

6.8 Crystal Oscillator

The RFIC includes an integrated 30MHz crystal oscillator with a fast start-up time of less than 1ms. The design is differential with the required crystal load capacitance integrated on-chip to minimize external components. All that is required off-chip is the 30MHz crystal blank.

The crystal load capacitance may be tuned to slightly adjust the frequency of the crystal oscillator. The tuning of the crystal load capacitance is programmed through the xlc[6:0] field of SPI Register 09h. The total internal capacitance is 12.5pF and is adjustable in approximately 127 steps (97fF/step). If AFC is disabled then the synthesizer frequency may be further adjusted by programming the Frequency Offset field fo[9:0]in SPI Registers 73h and 74h, as discussed in Section 4.2.9.

The crystal oscillator frequency is divided down internally and may be output to the Microcontroller through one of the GPIO pins for use as the System Clock. In this fashion, only one crystal oscillator is required for the entire system and the BOM cost is reduced. The available clock frequencies (i.e., internal division ratios) and the GPIO configuration are discussed further in Section 9.2.

The RFIC may also be driven with an external 30MHz clock signal through the XIN pin.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
09	R/W	Crystal Oscillator Load Capacitance	X	xlc[6]	xlc[5]	xlc[4]	xlc[3]	xlc[2]	xlc[1]	xlc[0]	40h

6.9 Regulators

There are a total of six regulators integrated onto the RFIC. With the exception of the IF and Digital all regulators are designed to operate with only internal decoupling. The IF and Digital regulators both require an external 1µF decoupling capacitor. All of the regulators are designed to operate with an input supply voltage from +1.8 to +3.6V, and produce a nominal regulated output voltage of +1.7V ±5%. The internal circuitry nominally operates from this regulated +1.7V supply. The output stage of the of Power Amplifier (PA) is not connected internally to a Regulator and is connected directly to the Battery Voltage.

From the application level only a voltage should be connected to the VDD pins. No voltage should be forced on the IF or DIG regulator outputs.

7 DATA HANDLING AND PACKET HANDLER

7.1 RX and TX FIFOs

Two 64 byte FIFOs are integrated into the chip, one for RX and one for TX, as shown in Figure 12. SPI Register 7Fh is used to access both FIFOs. A burst write, as described in Section 4.1, to address 7Fh will write data to the TX FIFO. A burst read from address 7Fh will read data from the RX FIFO.

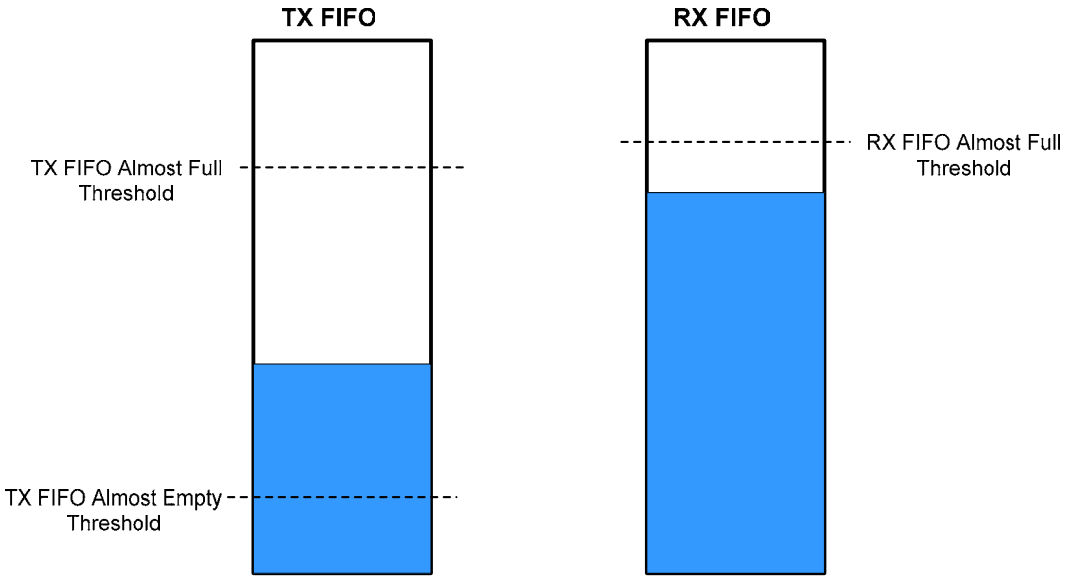


Figure 16: FIFO Thresholds

The TX FIFO has two programmable thresholds. An interrupt event occurs when the data in the TX FIFO reaches these thresholds. The first threshold is the FIFO Almost Full threshold, txafthr[5:0]. The value in this register corresponds to the desired threshold value in number of bytes. When the data being filled into the TX FIFO reaches this threshold limit, an interrupt to the Microcontroller is generated so the chip can enter TX mode to transmit the contents of the TX FIFO. The second threshold for TX is the FIFO Almost Empty Threshold, txaethr[5:0]. When the data being shifted out of the TX FIFO reaches the Almost Empty threshold an interrupt will be generated. The Microcontroller will need to switch out of TX mode or fill more data into the TX FIFO. The Transceiver may be configured so that when the TX FIFO is empty the chip will automatically move to the Ready state. In this mode the TX FIFO Almost Empty Threshold may not be useful. This functionality is set by the ffidle bit in Register 08h.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
08	R/W	Operating & Function Control 2	antdiv[2]	antdiv[1] ant	div[0]	rxmpk	autotx	enldm	ffclrrx	ffclrtx	00h
7C	R/W	TX FIFO Control 1			txafthr[5]	txafthr[4]	txafthr[3]	txafthr[2]	txafthr[1]	txafthr[0]	37h
7D	R/W	TX FIFO Control 2			txaethr[5]	txaethr[4] t	xaethr[3]	txaethr[2]	txaethr[1] t	xaethr[0]	04h

The RX FIFO has one programmable threshold called the FIFO Almost Full Threshold, rxafthr[5:0]. When the incoming RX data reaches the Almost Full Threshold an interrupt will be generated to the Microcontroller via the nIRQ pin. The Microcontroller will then need to read the data from the RX FIFO.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
7E	R/W	RX FIFO Control	X	X	rxafthr[5]	rxafthr[4]	rxafthr[3]	rxafthr[2]	rxafthr[1]	rxafthr[0]	37h

Both the TX and RX FIFO's may be cleared or rest with the ffclrtx and ffclrrx bits in SPI Register 08h. All interrupts may be enabled by setting the Interrupt Enabled bits in Registers 05h and 06h. If the interrupts are not enabled the function will not generate an interrupt on the nIRQ pin but the bits will still be read correctly in the Interrupt Status Registers.

7.2 Packet Configuration

When using the FIFOs, automatic packet handling may be enabled for TX mode, RX mode, or both. Register 71h and Registers 30h-49h control the configuration for Packet Handling. The usual fields for network communication (such as preamble, synchronization word, headers, packet length, and CRC) may easily be configured to be automatically added to the data payload. The fields needed for packet generation usually change infrequently and can therefore be stored in SPI registers. Registers 30h-49h are used to set the different fields in the packet structure. Automatically adding these fields to the data payload greatly reduces the amount of communication between the Microcontroller and the RFIC and therefore also reduces the required computational power of the Microcontroller.

The general packet structure is shown below in Figure 17: The length of each field is shown below the field. The preamble pattern is always a series of alternating ones and zeroes, starting with a one. All the fields have programmable lengths to accommodate multiple types of applications. The most common CRC polynominals are available for selection.

Figure 17: Packet Structure

7.3 Packet Handler TX Mode

In the TX packet handler if the packet length is set then the packet handler will only send the number of bytes selected in the packet length field and then it will return to ready mode and assert the packet sent interrupt. In order to send the next byte in the FIFO the Microcontroller will have to command the chip to enter TX mode again. For example in Figure 18 demonstrates the case where the packet length is set to three bytes.

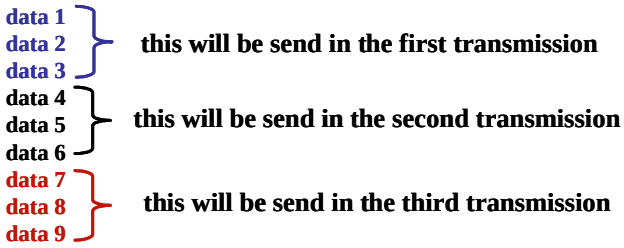


Figure 18: Multiple Packets in TX Packet Handler

7.4 Packet Handler RX Mode

7.4.1 Packet Handler Disabled

When the packet handler is disabled certain portions of the packet handler are still required. For the modem to work properly it will need preamble and sync, as shown in Figure 19. Everything after sync will be treated as data with no checks. The advantage of this mode is that it allows for very flexible packet handler but it does not allow for the use of data whitening, CRC, or header checks. Manchester encoding is still supported in this mode.

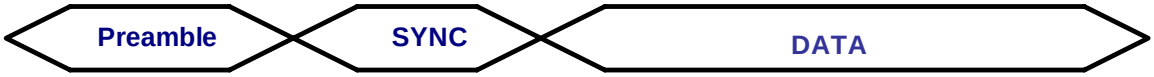


Figure 19: Required RX Packet Structure with Packet Handler Disabled

7.4.2 Packet Handler Enabled

When the packet handler is enabled all the fields of the packet structure will need to be configured. If multiple packets are desired to be stored in the FIFO then there are options available for the different fields that will be stored into the FIFO. Figure 20 demonstrates the options and settings available when multiple packets are enabled. Figure 21 demonstrates the operation of fixed packet length and correct/incorrect packets.

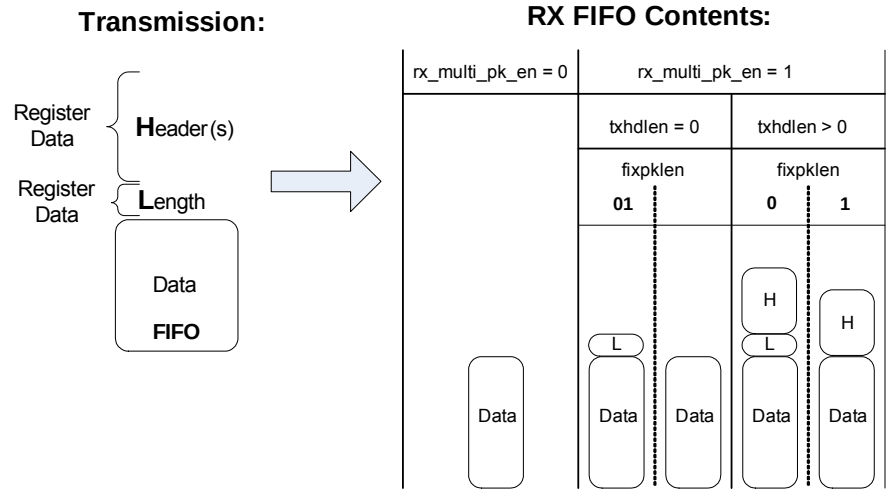


Figure 20: Multiple Packets in RX Packet Handler

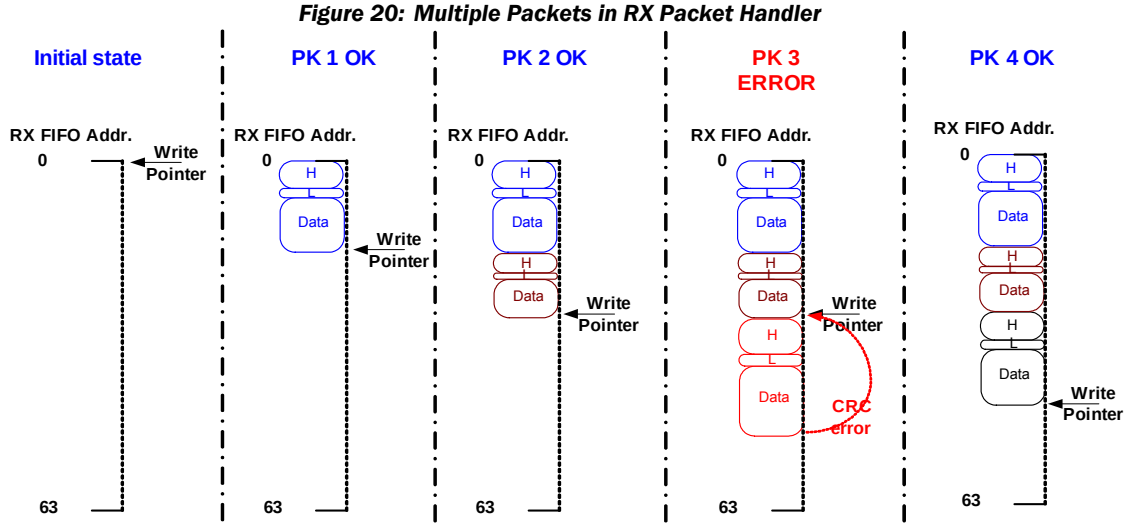


Figure 21: Multiple Packets in RX with CRC or Header Error

Data modes	dtmod[1:0]	enpacrx	Direct Data and CLK IO	Preamble & Sync word detection	Header Handling	Data Storage in FIFO	CRC Handling	Manchester and Whitening
FIFO_PH	10	1	option	set	option	set	option	option
FIFO	10	0	option	set	-	set	-	option
Direct	0X	X	set	set	-	-	-	Manchester optional for sync-detection

Table 13: RX Packet Handler Configuration

7.5 Packet Handler Registers and Descriptions

	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
30	R/W	Data Access Control	enpacrx	lsbfrst	crcdonly	autophdet	enpactx	encrc	crc[1]	crc[0]	1Dh
31	R	EzMAC status	0	0	pksrch	pkrx	pkvalid	crcerror	pktx	pksent	-
32	R/W	Header Control 1	enbcast[1]	enbcast[1]	enbcast[1]	enbcast[0]	hdch[3]	hdch[2]	hdch[1]	hdch[0]	0Ch
33	R/W	Header Control 2		txhdlen[2]	txhdlen[1]	txhdlen[0] f	ixpklen	synclen[1]	synclen[0]	prealen[8]	22h
34 R/	W	Preamble Length	prealen[7]	prealen[6]	prealen[5]	prealen[4]	prealen[3]	prealen[2]	prealen[1]	prealen[0]	07h
35 R/	W	Preamble Detection Control	preath[4]	preat h[3]	preath[2]	preath[1]	preath[0]	preach[2]	preach[1]	preach[0]	40h
36	R/W	Sync Word 3	sync[31]	sync[30]	sync[29]	sync[28]	sync[27]	sync[26]	sync[25]	sync[24]	2Dh
37	R/W	Sync Word 2	sync[23]	sync[22]	sync[21]	sync[20]	sync[19]	sync[18]	sync[17]	sync[16]	D4h
38	R/W	Sync Word 1	sync[15]	sync[14]	sync[13]	sync[12]	sync[11]	sync[10]	sync[9]	sync[8]	00h
39	R/W	Sync Word 0	sync[7]	sync[6]	sync[5]	sync[4]	sync[3]	sync[2]	sync[1]	sync[0]	00h
3A	R/W	Transmit Header 3	txhd[31]	txhd[30]	txhd[29]	txhd[28]	txhd[27]	txhd[26]	txhd[25]	txhd[24]	00h
3B	R/W	Transmit Header 2	txhd[23]	txhd[22]	txhd[21]	txhd[20]	txhd[19]	txhd[18]	txhd[17]	txhd[16]	00h
3C	R/W	Transmit Header 1	txhd[15]	txhd[14]	txhd[13]	txhd[12]	txhd[11]	txhd[10]	txhd[9]	txhd[8]	00h
3D	R/W	Transmit Header 0	txhd[7]	txhd[6]	txhd[5]	txhd[4]	txhd[3]	txhd[2]	txhd[1]	txhd[0]	00h
3E	R/W	Transmit Packet Length	pklen[7]	pklen[6]	pklen[5]	pklen[4]	pklen[3]	pklen[2]	pklen[1]	pklen[0]	00h
3F	R/W	Check Header 3	chhd[31]	chhd[30]	chhd[29]	chhd[28]	chhd[27]	chhd[26]	chhd[25]	chhd[24]	00h

40	R/W	Check Header 2	chhd[23]	chhd[22]	chhd[21]	chhd[20]	chhd[19]	chhd[18]	chhd[17]	chhd[16]	00h
41	R/W	Check Header 1	chhd[15]	chhd[14]	chhd[13]	chhd[12]	chhd[11]	chhd[10]	chhd[9]	chhd[8]	00h
42	R/W	Check Header 0	chhd[7]	chhd[6]	chhd[5]	chhd[4]	chhd[3]	chhd[2]	chhd[1]	chhd[0]	00h
43	R/W	Header Enable 3	hden[31]	hden[30]	hden[29]	hden[28]	hden[27]	hden[26]	hden[25]	hden[24]	FFh
44	R/W	Header Enable 2	hden[23]	hden[22]	hden[21]	hden[20]	hden[19]	hden[18]	hden[17]	hden[16]	FFh
45	R/W	Header Enable 1	hden[15]	hden[14]	hden[13]	hden[12]	hden[11]	hden[10]	hden[9]	hden[8]	FFh
46	R/W	Header Enable 0	hden[7]	hden[6]	hden[5]	hden[4]	hden[3]	hden[2]	hden[1]	hden[0]	FFh
47	R	Received Header 3	rxhd[31]	rxhd[30]	rxhd[29]	rxhd[28]	rxhd[27]	rxhd[26]	rxhd[25]	rxhd[24]	-
48 R		Received Header 2	rxhd[23]	rxhd[22]	rxhd[21]	rxhd[20]	rxhd[19]	rxhd[18]	rxhd[17]	rxhd[16]	-
49 R		Received Header 1	rxhd[15]	rxhd[14]	rxhd[13]	rxhd[12]	rxhd[11]	rxhd[10]	rxhd[9]	rxhd[8]	-
4A R		Received Header 0	rxhd[7]	rxhd[6]	rxhd[5]	rxhd[4]	rxhd[3]	rxhd[2]	rxhd[1]	rxhd[0]	-
4B	R	Received Packet Length	rxplen[7]	rxplen[6]	rxplen[5]	rxplen[4]	rxplen[3]	rxplen[2]	rxplen[1]	rxplen[0]	-

Address: 30h – Data Access Control

Bit R/W	Default	Function
7 R/W	1	**enpacrx** = Enable Packet RX Handling. If FIFO Mode (dtmod='10') is being used automatic packet handling may be enabled. Setting enpacrx='1' will enable automatic packet handling in the RX path. Register 30-4D allow for various configurations of the packet structure. Setting enpacrx='0' will not do any packet handling in the RX path. It will only receive everything after the sync word and fill up the RX FIFO.
6 R/W	0	**lsbfrst** = LSB First enable. The LSB of the data will be transmitted/received first if this bit is set.
5 R/W	0	**crcdonly** = CRC Data Only enable When this bit is set to '1' the CRC is calculated on and check against the packet data fields only.
4 R/W	0	**autophdet** = Auto Phase Detection enable. Automatic Manchester phase detection during RX if this bit is set.
3 R/W	1	**enpactx** = Enable Packet TX Handling. If FIFO Mode (dtmod='10') is being used automatic packet handling may be enabled. Setting enpactx='1' will enable automatic packet handling in the TX path. Register 30-4D allow for various configurations of the packet structure. Setting enpactx='0' will not do any packet handling in the TX path. It will only transmit what is loaded to the FIFO.
2 R/W	1	**encrc** = CRC enable. Cyclic Redundancy Check generation is enabled if this bit is set.
[1:0] R/W	01	**crc[1:0]** = CRC polynomial selection. 00 – CCITT 01 – CRC-16 10 – IEC-16 11 – Biacheva

Address: 31h – EzMAC Status

Bit R/W	Default	Function
[7:6] R	0	RESERVED
5 R	0	**pksrch** = Packet Searching. When pksrch = '1' the radio is searching for a valid packet.
4 R	0	**pkrx** = Packet Receiving. When pkrx = '1' the radio is currently receiving a valid packet.
3 R	0	**pkvalid** = Valid Packet Received. When a pkvalid = '1' a valid packet has been received by the receiver. (Same bit as in register 03, but reading it does not reset the IRQ)
2 R	0	**crcerror** = CRC Error. When crcerror = '1' a Cyclic Redundancy Check error has been detected. (Same bit as in register 03, but reading it does not reset the IRQ)
1 R	0	**pktx** = Packet Transmitting. When pktx = '1' the radio is currently transmitting a packet.
0 R	0	**pksent** = Packet Sent. A pksent = '1' a packet has been sent by the radio. (Same bit as in register 03, but reading it does not reset the IRQ)

Address: 32h – Header Control 1

Bit R/W	Default	Function
[7:4] R/W	0	**bcen[3:0]** = Broadcast Address (FFh) Check enable. If it is enabled together with Header Byte Check then the header check is OK if the incoming header byte equals with the appropriate check byte *or* FFh). One hot encoding. 0000 – No broadcast address enable. 0001 – Broadcast address enable for header byte 0. 0010 – Broadcast address enable for header byte 1. 0011 – Broadcast address enable for header bytes 0 & 1. 0100 – …
[3:0] R/W	1100	**hdch[3:0]** = Received Header bytes to be checked against the Check Header bytes. One hot encoding. The receiver will use hdch[2:0] to know the position of the Header Bytes. 0000 – No Received Header check 0001 – Received Header check for byte 0. 0010 – Received Header check for bytes 1. 0011 – Received header check for bytes 0 & 1. 0100 – …

Address: 33h – Header Control 2

Bit	R/W	Default	Function
7	R	0	RESERVED
[6:4]	R/W	010	**hdlen[2:0] =** Transmit/Receive Header Length. Length of header used if packet handler is enabled for TX (enpactx) or for RX (enpacrx). Headers are sent or received in descending order. 000 – No TX header 001 – Header 3 010 – Header 3 and 2 011 – Header 3 and 2 and 1 100 – Header 3 and 2 and 1 and 0
3	R/W	0	**fixpklen =** Fix Transmit/Receive Packet Length. When fixpklen = '1' the packet length (pklen[7:0]) is not included in the packet structure. When fixpklen = '0' the packet length is included in the packet.
[2:1]	R/W	01	**synclen[1:0]** = Synchronization Word Length. The value in this register corresponds to the number of bytes used in the Synchronization Word. The synchronization word bytes are transmitted in descending order. 00 – Synchronization Word 3 01 – Synchronization Word 3 and 2 10 – Synchronization Word 3 and 2 and 1 11 – Synchronization Word 3 and 2 and 1 and 0
0	R/W	0	**prealen[8]** = MSB of Preamble Length. See register Preamble Length.

Address: 34h – Preamble Length

Bit	R/W	Default	Function
[7:0]	R/W	07h	**prealen[7:0]** = Preamble Length. The value in the prealen[8:0] register + 1 corresponds to the number of nibbles (4 bits) in the packet. For example prealen[8:0] = '00 0001000' corresponds to a preamble length of 32 bits (8*4bits) or 4 Bytes. The maximum preamble length is prealen[8:0] = '111111111' which corresponds to a 255 Bytes Preamble. Writing a value of 0 to this register will have the same effect as 1 and one nibble will be sent.

Address: 35h – Preamble Detection Control 1

Bit	R/W	Default	Function
[7:3]	R/W	0100	preath[4:0] = Number of nibbles processed during detection.
[2:0]	R/W	000	preach[2:0] = Number of non-consecutive bit errors allowed during detection.

Address: 36h – Synchronization Word 3

Bit	R/W	Default	Function
[7:0]	R/W	2Dh	**sync[31:24]** = Synchronization Word 3. 4th byte of the synchronization word.

Address: 37h – Synchronization Word 2

Bit	R/W	Default	Function
[7:0]	R/W	D4h	**sync[23:16]** = Synchronization Word 2. 3rd byte of the synchronization word.

Address: 38h – Synchronization Word 1

Bit	R/W	Default	Function
[7:0]	R/W	0	**sync[15:8]** = Synchronization Word 1. 2nd byte of the synchronization word.

Address: 39h – Synchronization Word 0

Bit	R/W	Default	Function
[7:0]	R/W	0	**sync[7:0]** = Synchronization Word 0. 1st byte of the synchronization word.

Address: 3Ah – Transmit Header 3

Bit	R/W	Default	Function
[7:0]	R/W	0	**txhd[31:24]** = Transmit Header 3. 4th byte of the header to be transmitted.

Address: 3Bh – Transmit Header 2

Bit	R/W	Default	Function
[7:0]	R/W	0	**txhd[23:16]** = Transmit Header 2. 3rd byte of the header to be transmitted.

Address: 3Ch – Transmit Header 1

Bit	R/W	Default	Function
[7:0]	R/W	0	**txhd[15:8]** = Transmit Header 1. 2nd byte of the header to be transmitted.

Address: 3Dh – Transmit Header 0

Bit	R/W	Default	Function
[7:0]	R/W	0	**txhd[7:0]** = Transmit Header 0. 1st byte of the header to be transmitted.

Address: 3Eh –Transmit Packet Length

Bit	R/W	Default	Function
[7:0]	R/W	0	**pklen[7:0]** – Packet Length. The value in the pklen[7:0] register corresponds directly to the number of bytes in the Transmit Packet. For example pklen[7:0] = '00001000' corresponds to a packet length of 8 Bytes. The maximum packet length is pklen[7:0] = '11111111', a 255 byte packet. If a '0' is written no data bytes will be sent in the packet structure.

Address: 3Fh – Check Header 3

Check Header bytes 3 to 0 are checked against the corresponding bytes in the Received Header if the check is enabled in the Header Control Register (31h).

Bit	R/W	Default	Function
[7:0]	R/W	0	**chhd[31:24]** = Check Header 3. 4th byte of the check header.

Address: 40h – Check Header 2

Bit	R/W	Default	Function
[7:0]	R/W	0	**chhd[23:16]** = Check Header 2. 3rd byte of the check header.

Address: 41h – Check Header 1

Bit	R/W	Default	Function
[7:0]	R/W	0	**chhd[15:8]** = Check Header 1. 2nd byte of the check header.

Address: 42h – Check Header 0

Bit	R/W	Default	Function
[7:0]	R/W	0	**chhd[7:0]** = Check Header 0. 1st byte of the check header.

Address: 43h –Header Enable 3

Header Enable bytes 3 to 0 control which bits of the Check Header bytes are checked against the corresponding bits in the Received Header. Only those bits are compared where the enable bits are set to 1.

Bit	R/W	Default	Function
[7:0]	R/W	0	hden[31:24] = Header Enable 3. 4th byte of the check header.

Address: 44h – Header Enable 2

Bit	R/W	Default	Function
[7:0]	R/W	0	**hden[23:16]** = Header Enable 2. 3rd byte of the check header.

Address: 45h – Header Enable 1

Bit	R/W	Default	Function
[7:0]	R/W	0	**hden[15:8]** = Header Enable 1. 2nd byte of the check header.

Address: 46h – Header Enable 0

Bit	R/W	Default	Function
[7:0]	R/W	0	**hden[7:0]** = Header Enable 0. 1st byte of the check header.

Address: 47h – Received Header 3

Bit	R/W	Default	Function
[7:0]	R	0	**rxhd[31:24]** = Received Header 3. 4th byte of the received header.

Address: 48h – Received Header 2

Bit	R/W	Default	Function
[7:0]	R	0	**rxhd[23:16]** = Received Header 2. 3rd byte of the received header.

Address: 49h – Received Header 1

Bit	R/W	Default	Function
[7:0]	R	0	**rxhd[15:8]** = Received Header 1. 2nd byte of the received header.

Address: 4Ah – Received Header 0

Bit	R/W	Default	Function
[7:0]	R	0	**rxhd[7:0]** = Received Header 0. 1st byte of the received header.

Address: 4Bh – Received Packet Length

Bit	R/W	Default	Function
[7:0]	R	0	**rxplen[7:0]** = Length byte of the received header.

7.6 Data Whitening, Manchester Encoding, and CRC

Data whitening can be used to avoid long sequences of 0s or 1s in the transmitted data stream to help achieve a more uniform spectrum by removing the discrete tones. When enabled, the payload data bits are EXOR-ed with a pseudorandom sequence, which is the output of the built-in PN9 generator. The generator is initialized at the beginning of the payload. The receiving end can reconstruct the original data by repeating the same operation. Manchester encoding may also be used to ensure a DC-free transmission and good synchronization properties. When Manchester encoding is used the effective datarate will remain the same but the actual datarate, preamble length, etc will appear doubled due to the inherent nature of this encoding. The effective datarate when using Manchester encoding is limited to 64kbps due to the doubling nature. Data Whitening, and Manchester encoding may be selected with SPI Register 70h. CRC enable and to enable only the data only is available in SPI Register 30h.

Since Manchester Encoding essentially doubles the data-rate, the maximum data-rate when Manchester is enabled is 64kbps.

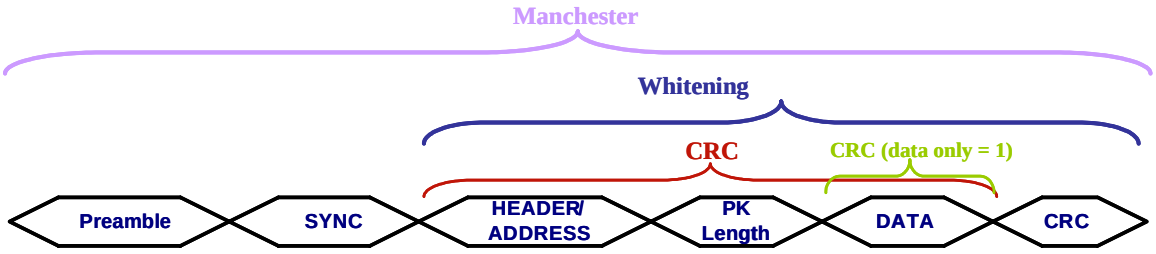


Figure 22: Operation of Data Whitening, Manchester Encoding, and CRC

7.7 Preamble Detector

A Preamble Detection circuit is integrated into the chip. The preamble length is configurable from 1-256 bytes by the prealen[7:0] field in Registers 33h and 34h, as described in Section 7.2. The minimum length of preamble required for the Preamble Detector to operate correctly is 1 byte, with the programmable length in increments of half bytes or nibbles. The Preamble Detector output may be programmed onto one of the GPIOs or read in the Interrupt Status Registers.

7.8 Preamble Length

The preamble length is adjustable up to 256 bytes to be tailored to different applications and requirements. Depending on the mode being utilized inside the chip the preamble length will need to be adjusted. As described above the preamble length is adjusted via SPI Register 34h.

Table 14: Minimum Preamble Length

Mode	Min Preamble Length	Comments
AFC Disabled	23 Bytes	1 Byte may be sufficient depending on application and tolerance to false detects
AFC Enabled	4 Bytes	Extra time needed to settle the AFC
AFC+Antenna Diversity Enabled	8 Bytes	Longer due to need to evaluate both antennas

7.9 Invalid Preamble Detector

In addition to the Preamble Detect there is also an Invalid Preamble Detect signal. When scanning channels in a Frequency Hopping System, it is desirable to scan a channel in the minimum amount of time possible. As soon as a few errors are detected in the preamble, the nPQD signal is asserted indicating that channel may be skipped with no need to check the full length of the pream ble. Both the Preamble Detect and Invalid Preamble Detect signals are available in the Interrupt Status Registers 03h-04h.

The Invalid Pre amble Detector issues an interrupt when no valid preamble signal is found. After the receiver is enabled the Invalid Preamble Detector will be held low for 16Tb (Tb is the time of the bit duration) to a llow the receiver to settle. After the 1 6Tb if a pattern occurs which is not preamble (10101 0) then the Invalid P reamble bit will be set. T he 16Tb is a f ixed time wh ich will work with a 4Byte Preamble (or long er) when AFC is enabled or a 3Byte preamble (or longer) when AFC is disabled. The invalid preamb le detect inter rupt can be useful to save power and speed-up search in rece ive mode. It is a dvised to dis able the inv alid preamb le interrupt when Antenna Diversity is enabled. The Invalid Pre amble Detect interrupt ma y be triggered during the Anten na Diversity algorithm if one of the antenna s is weak b ut the other is capab le of s till rec eiving the s ignal if the Antenn a Div ersity algori thm is allowed to complete.

7.10 TX Retransmission and Auto TX

The chip is capable of automatica lly retransmitting the last packet that was stored into the FIFO, so if no new packet is loaded into the TX FIFO. Automatic Retransmission is achieved simply by entering the TX state again with the txon bit set. This feature is useful for Beacon t ransmission or w hen retransmission i s req uired due to absence of a valid acknowledgement. O nly p ackets that f it completely in the TX FIFO are valid fo r the retransmit feature. When it is necessary to transmit lo nger packets the TX FIFO us es its circular read/write capability.

An Automatic Transmission is also available. When autotx = ‘ 1’ the transceiver will ente r automatically TX State when the TX FIFO is almost full. When the TX FIFO is empty the transceiver will automatically return to the IDLE State.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
08	R/W	Operating & Function Control 2	antdiv[2]	antdiv[1] ant	div[0]	rxmpk	autotx	enldm	ffclrrx	ffclrtx	00h

8 RX MODEM CONFIGURATION

8.1 Channel Filter BW

The digital modem performs channel selection, and demodulation in the digital domain. The channel filter BW is configurable from 600kHz down to 2.4kHz. Depending on the desired data-rate, modulation index, and bandwidth seven registers (1C-25) need to be set in the SPI registers table. Modulation Index is equal to 2 times the peak deviation divided by the DR (data-rate). The following table gives the modem settings for various common data-rates. First select the desired data-rate, and modulation index and then program the SPI registers with the values given in the table. For data-rates or modulation indexes not listed in the table, the calculator within WDS may be used.

$$ModIndex = \frac{2 * \Delta f}{DR}$$

Table 15: RX Modem Configuration

RX Modem Settings									
DR	**F_{DEV}**	**Mod Index**	**BW_{3dB}**	**Dec-by-3**	**ndec[2:0]**	**filset[3:0]**	**rxosr[10:0]**	**ncoff[19:0]**	**crgain[10:0]**
2.0 kbps	+/- 5.0 kHz	H= 5.0	11.5 kHz	Not Byp	3'h3	4'h3	11'hFA	20'h08312	11'h054
2.4 kbps	+/- 4.8 kHz	H= 4.0	11.5 kHz	Not Byp	3'h3	4'h3	11'hD0	20'h09D49	11'h100
2.4 kbps	+/- 36.0 kHz	H= 30.0	69.2 kHz	Not Byp	3'h1	4'h7	11'h341	20'h02752	11'h010
4.8 kbps	+/- 4.8 kHz	H= 2.0	14.2 kHz	Not Byp	3'h3	4'h5	11'h68	20'h13A93	11'h400
4.8 kbps	+/- 45.0 kHz	H= 18.8	90.0 kHz	Not Byp	3'h0	4'h3	11'h341	20'h02752	11'h010
9.6 kbps	+/- 4.8 kHz	H= 1.0	17.5 kHz	Not Byp	3'h3	4'h7	11'h34	20'h27525	11'h7FF
9.6 kbps	+/- 45.0 kHz	H= 9.4	90.0 kHz	Not Byp	3'h0	4'h3	11'h1A1	20'h04EA5	11'h038
10.0 kbps	+/- 5.0 kHz	H= 1.0	18.9 kHz	Not Byp	3'h2	4'h1	11'h64	20'h147AE	11'h7FF
10.0 kbps	+/- 40.0 kHz	H= 8.0	83.2 kHz	Not Byp	3'h0	4'h2	11'h190	20'h051EC	11'h044
19.2 kbps	+/- 9.6 kHz	H= 1.0	34.7 kHz	Not Byp	3'h2	4'h7	11'h34	20'h27525	11'h7FF
20.0 kbps	+/- 10.0 kHz	H= 1.0	37.7 kHz	Not Byp	3'h1	4'h1	11'h64	20'h147AE	11'h7FF
20.0 kbps	+/- 40.0 kHz	H= 4.0	95.3 kHz	Not Byp	3'h0	4'h4	11'hC8	20'h0A3D7	11'h108
38.4 kbps	+/- 19.6 kHz	H= 1.0	69.2 kHz	Not Byp	3'h1	4'h7	11'h34	20'h27525	11'h7FF
40.0 kbps	+/- 20.0 kHz	H= 1.0	75.2 kHz	Not Byp	3'h0	4'h1	11'h64	20'h147AE	11'h7FF
40.0 kbps	+/- 40.0 kHz	H= 2.0	75.2 kHz	Not Byp	3'h0	4'h5	11'h64	20'h147AE	11'h428
50.0 kbps	+/- 25.0 kHz	H= 1.0	95.3 kHz	Not Byp	3'h0	4'h4	11'h50	20'h1999A	11'h7FF
57.6 kbps	+/- 28.8 kHz	H= 1.0	112.1 kHz	Not Byp	3'h0	4'h5	11'h45	20'h1D7DC	11'h7FF
100.0 kbps	+/- 50.0 kHz	H= 1.0	225.6 kHz	Bypassed	3'h0	4'h1	11'h78	20'h11111	11'h7FF
125.0 kbps	+/- 62.5 kHz	H= 1.0	249.6 kHz	Bypassed	3'h0	4'h2	11'h60	20'h15555	11'h7FF

The required channel filter bandwidth is calculated as: BW = 2 x C x (Fdev + 0.5Rb) where C = 1 for FSK and 0.9 for GFSK, Fdev is the frequency deviation and Rb is the data rate.

9 AUXILIARY FUNCTIONS

9.1 POR

The IA4432 contains an enhanced integrated POR circuit. The POR circuit contains both a classic level threshold reset as well as a slope detector POR. This reset circuit was designed to produce reliable reset signal in any circumstances. Reset will be initiated if any of the following conditions occur:

- Initial power on, when VDD starts from 0V: reset is active from V_{SR} till VDD reaches V_{RR} (see table);
- When VDD decreases below V_{LD} for any reason: reset is active till VDD reaches V_{RR} again;
- If software reset was commanded through SPI bus in register 08h: reset is active for time T_{SWRST}
- On the rising edge of a VDD glitch when the supply voltage exceeds the following time functioned limit:

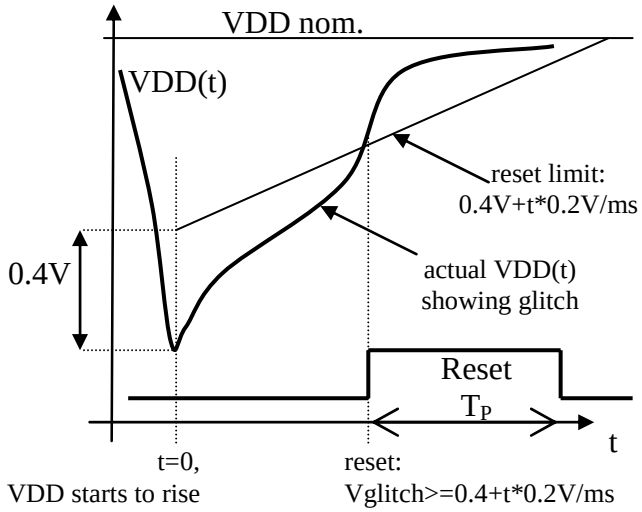


Figure 23: POR Glitch Parameters

Table 16: POR Parameters

Parameter	Symbol	Comment	Min	Typ	Max	Unit
Release reset voltage	V_{RR}		0.85	1.3	1.75	V
Turn on reset voltage	V_{SR}	for min. 40ms			150	mV
Power-on VDD slope	S_{VDD}	tested VDD slope region	0.03		300	V/ms
Low VDD limit	V_{LD}	$V_{LD}<V_{RR}$ is guaranteed	0.7	1	1.3	V
Software reset pulse	T_{SWRST}		50		470	us
Threshold voltage	V_{TSD}			0.4		V
Reference slope	k			0.2		V/ms
VDD glitch reset pulse	T_P		5	15	40	ms

The reset will reset all registers to their default values. The reset signal is also available for output and use by the Microcontroller by using the default setting for GPIO_0. The inverted reset signal is available by default on GPIO_1.

9.2 Microcontroller Clock

The crystal oscillator frequency is divided down internally and may be output to the Microcontroller through GPIO2. This feature is useful to lower BOM cost by using only one crystal in the system application. The system clock frequency is selectable from one of 8 different options, as shown below. Except for the 32.768 kHz option, all other frequencies are derived by dividing the Crystal Oscillator frequency. The 32.768 kHz clock signal is derived from an internal RC Oscillator or an external 32kHz Crystal, depending on which is selected. The GPIO2 default is the microcontroller clock with a 1MHz microcontroller clock output.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
0A	R/W	Microcontroller Output Clock			clkt[1]	clkt[0]	enlfc	mclk[2]	mclk[1]	mclk[0]	0Bh

mclk[2:0]	Modulation Source
000	30MHz
001	15MHz
010	10MHz
011	4MHz
100	3MHz
101	2MHz
110	1MHz
111	32.768KHz

If the Microcontroller clock option is being used there may be the need of a System Clock for the Microcontroller while the RFIC is in SLEEP mode. Since the Crystal Oscillator is disabled in SLEEP mode in order to save current, the low-power 32.768kHz clock may be switched to automatically become the Microcontroller clock. This feature is called Enable Low Frequency Clock and is enabled by the enlfc bit. When enlfc = '1' and the chip is in SLEEP mode then the 32.768kHz clock will be provided to the Microcontroller as the System Clock, regardless of the setting of mclk[2:0]. For example, if mclk[2:0] = '000', 30 MHz will be provided through the GPIO output pin to the Microcontroller as the System Clock in all IDLE, TX, or RX states. When the chip is commanded to SLEEP mode, the System Clock will become 32.768kHz.

Another available feature for the Microcontroller clock is the Clock Tail, clkt[1:0]. If the Enable Low Frequency Clock feature is not enabled (enlfc = '0'), then the System Clock to the Microcontroller is disabled in SLEEP mode. However, it may be useful to provide a few extra cycles for the Microcontroller to complete its operation prior to the shutdown of the System Clock signal. Setting the clkt[1:0] field will provide additional cycles of the System Clock before it shuts off.

clkt[1:0]	Modulation Source
00 0	cycles
01 128	cycles
10 256	cycles
11 512	cycles

If an interrupt is triggered the microcontroller clock will remain enabled regardless of the selected mode. As soon as the interrupt is read the state machine will then move to the selected mode. For instance if the chip is commanded to Sleep mode but an interrupt has occurred the 30MHz XTAL will not disable until the interrupt has been cleared.

9.3 General Purpose ADC

An 8 bit SAR ADC is integrated onto the chip for general purpose use, as well as for digitizing the temperature sensor reading. SPI Register 0Fh must be configured depending on the use of the GPADC before use. The architecture of the ADC is demonstrated in Figure 24. First the input of the ADC must selected by setting the ADCSEL[2:0] depending on the use of the ADC. For instance if the ADC is going to be used to read out the internal temperature sensor then, ADCSEL[2:0] should be set to '000'. Next the input reference voltage to the ADC must be chosen. By default, the ADC uses the bandgap voltage as a reference so the input range of the ADC is from 0-1.25V with an LSB resolution of 4.90mV (1.25/256). Changing the ADC reference will change the LSB resolution accordingly.

Every time the ADC convesion is desired the ADCStart bit in SPI Register 0Fh must be set to '1'. This is a self clearing bit that will be cleared at the end of the conversion cycle of the ADC. The conversion time for the ADC is 350us. After the 350us or when the ADCstart/done bit is cleared then the ADC value may be read out of Register 11h. Setting the SPI Register 10h, ADC Sensor Amplifier Offset is only necessary when the ADC is configured to used as a Bridge Sensor as described in the following section.

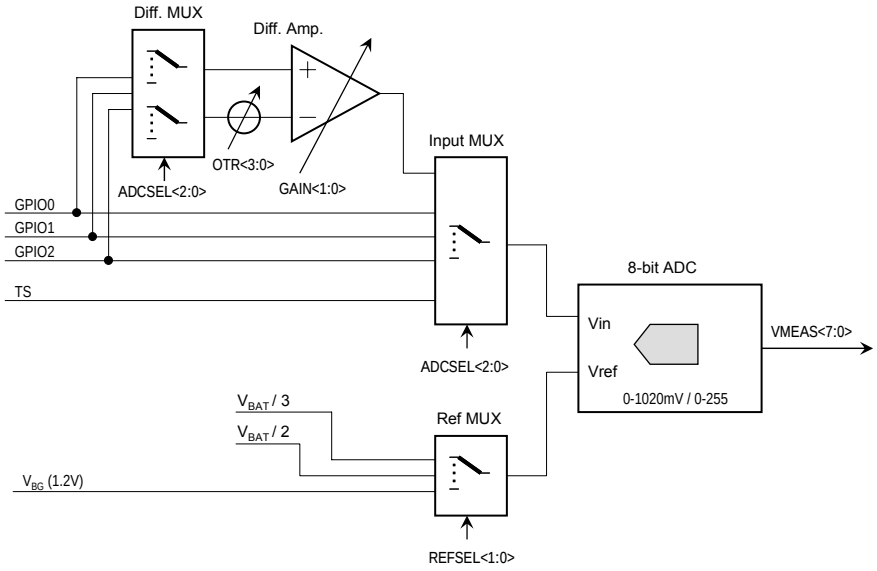


Figure 24: General Purpose ADC Architecture

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
0F	R/W	ADC Configuration	adcstart / *adcdone*	adcsel[2]	adcsel[1]	adcsel[0]	adcref[1]	adcref[0]	adcgain[1]	adcgain[0]	00h
10	R/W	ADC Sensor Amplifier Offset					adcoffs[3]	adcoffs[2]	adcoffs[1]	adcoffs[0]	00h
11	R	ADC Value	*adc[7] a*	*dc[6]*	*adc[5]*	*adc[4]*	*adc[3]*	*adc[2]*	*adc[1]*	*adc[0]*	-

Address: 0Fh – ADC Configuration

Bit R/W		Default	Function
7 R/W		0	**adcstart / adcdone** = ADC Measurement Start bit. Reading this bit gives '1' if the ADC measurement cycle has been finished.
[6:4]	R/W	00	**adcsel[2:0]** = ADC Input Source selection. The internal 8 bit ADC input source can be selected as follows: 000 – Internal Temperature Sensor 001 – GPIO0, single-ended 010 – GPIO1, single-ended 011 – GPIO2, single-ended 100 – GPIO0(+) - GPIO1(-), differential 101 – GPIO1(+) - GPIO2(-), differential 110 – GPIO0(+) - GPIO2(-), differential 111 – GND
[3:2] R/W		00	**adcref[1:0]** = ADC Reference Voltage selection. The reference voltage of the internal 8 bit ADC can be selected as follows: 0X – bandgap voltage (1.2V) 10 – VDD / 3 11 – VDD / 2
[1:0] R/W		000	**adcgain[1:0]** = ADC Sensor Amplifier Gain selection. The full scale range of the internal 8 bit ADC in differential mode (see adcsel) can be set as follows: adcref[0] = 0: FS = 0.014 * (adcgain[1:0] + 1) * VDD adcref[0] = 1: FS = 0.021 * (adcgain[1:0] + 1) * VDD

9.3.1 ADC Differential Input Mode – Bridge Sensor Example

The differential input mode of ADC8 is designed to directly interface any bridge-type sensor, which is demonstrated in the figure below. As seen in the figure the use of the ADC in this configuration will utilize two GPIO pins. The supply source of the bridge and chip should be the same to eliminate the measuring error caused by battery discharging. For proper operation one of the VDD dependent references (VDD/2 or VDD/3) should be selected for the reference voltage of ADC8. The differential input mode supports programmable gain to match the input range of ADC8 to the characteristic of the sensor and VDD proportional programmable offset adjustment to compensate the offset of the sensor.

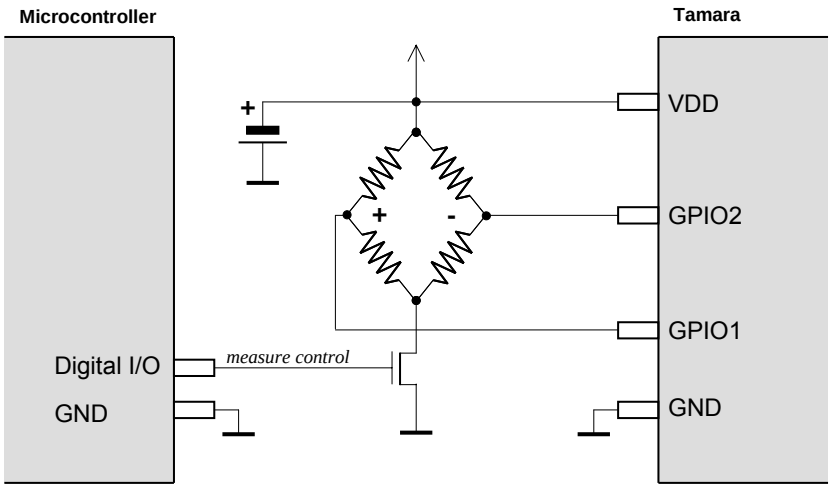


Figure 25: ADC Differential Input Example – Bridge Sensor

The adcgain<1:0> bits in Register 0Eh determines the gain of the differential/single ended amlifier. This is used to fit the input range of the ADC8 to bridge sensors having different sensitivity:

GAIN<1>	GAIN<0>	Differential gain	Input range (% of VDD) [2]
0	0	22/13	16.8
0 1		44/13	12.6
1 0		66/13	8.4
1 1		88/13	4.2

Note 2: The input range is the differential voltage measured between the selected GPIO pins corresponding to the full ADC range (255).

The differential offset can be coarse compensated by the adcoffs[3:0] bits found in Register 11h. Fine compensation should be done by the microcontroller software. The main reason of the offset compensation is to shift the negative offset voltage of the bridge sensor to the positive differential voltage range. This is essential as the differential input mode is unipolar. The offset compensation is VDD proportional, so the VDD change has no infuence on the measured value.

adcoffs<3>	Input offset (% of VDD) [3]
0	adcoffs<2:0> * 0.21
1	- adcoffs<2:0> * 0.21

9.4 Temperature Sensor

An an alog tem perature sensor is integ rated into the chip. The temperature sensor will be automatically enabled w hen the temperature se nsor is selected as the input of the ADC or wh en the an alog temp voltage is selected on the analog test bu s. The temperature se nsor value may be digitized using the general- purpose ADC and read out ov er the SPI thro ugh Register 10h. The range of the t emperature se nsor is select able to conf igure to the desired application and performance. The table below demonstrates the settings for the different temperature ranges and performance.

A simple step-by-step procedure to use the Temp Sensor:

#1 – Set input for ADC to be Temperature Sensor – adcsel[2:0]='000'

#2 – Set Reference for ADC – adcref[1:0]='00'

#3 – Set Temperature Range for ADC – tsrange[1:0]

#4 – Trigger ADC Reading – adcstart='1'

#5 – Read-out Value – Read Address 11h

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
12	R/W	Temperature Sensor Control	tsrange[1] t	srange[0]	entsoffs	entstrim	vbgtrim[3]	vbgt rim[2]	vbgtrim[1]	vbgtrim[0]	20h
13	R/W	Temperature Value Offset	tvoffs[7]	tvoffs[6]	tvoffs[5]	tvoffs[4]	tvoffs[3]	tvoffs[2]	tvoffs[1]	tvoffs[0]	00h

Address: 12h – Temperature Sensor Calibration Configuration

Bit R/W	Default	Function
[7:6] R/W	00	**tsrange[1:0]** = Temperature Sensor Range selection (FS range is 0..1024mV) 00 – -64°C .. 64°C (full operating range), with 0.5°C resolution (1 LSB in the 8 bit ADC) 01 – -64°C .. 192°C, with 1°C resolution (1 LSB in the 8 bit ADC) 11 – 0°C .. 128°C, with 0.5°C resolution (1 LSB in the 8 bit ADC) 10 – -40°F .. 216°F, with 1°F resolution (1 LSB in the 8 bit ADC)
5 R/W	1	**entoff** = Temperature Sensor Offset enable
4 R/W	0	**envbgcal** = Temperature Sensor Calibration enable
[3:0] R/W	0	**vbgcal[3:0]** = Temperature Sensor Calibration value

entoff	tsrange<1>	tsrange<0>	Temp. range	Unit	Slope	ADC8 LSB
1	0	0	-64 … 64	°C	8 mV/°C	0.5 °C
1	0	1	-64 … 192	°C	4 mV/°C	1 °C
1	1	0	0 … 128	°C	8 mV/°C	0.5 °C
1	1	1	-40 … 216	°F	4 mV/°F	1 °F
0*	1	0	0 … 341	°K	3 mV/°K	1.333 °K

* Absolute temperature mode, no temperature shift. This mode is only for test purposes. POR value of EN_TOFF is 1

Control to adjust the temperature sensor accuracy is available by adjusting the bandgap voltage. By enabling the envbgcal and using the vbgcal[3:0] bits to trim the bandgap the temperature sensor accuracy may be fine tuned in the final application. The slope of the temperature sensor is v ery linear and monot onic but the exact accu racy or offset in temp erature is difficult to control better than **±10°C. With the vbgtrim or bandgap trim though the initial temperature offset can be easily adjusted and be better than ±3°C.**

The different ranges for the temperature sensor and ADC8 are demonstrated in the figure below. The val ue of the A DC8 may be translated to a temperature reading by ADC8Value*ADC8 LSB + Lowest Temp erature in Temp Rang e. For instanc e for a tsrange=00, Temp = ADC8Value*0.5 – 64.

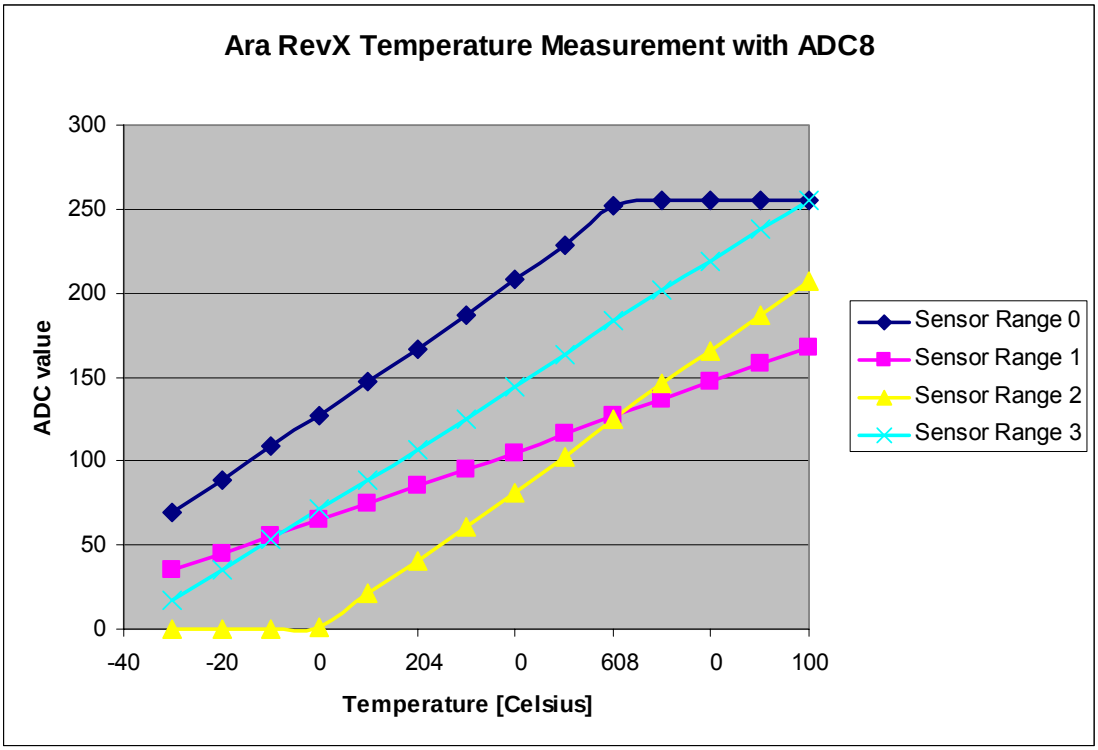


Figure 26: Temperature Ranges using ADC8

9.5 Low Battery Detector

A Low Battery Detector (LBD) with digital read-out is integrated into the chip. A digital threshold may be programmed into the lbdt[4:0] field in Register 1Ah. When the digitized battery voltage reaches this threshold an interrupt will be generated on the nIRQ pin to the Microcontroller. The Microcontroller will then need to verify the interrupt by reading the Interrupt Status Registers, Addresses 03h and 04h.

If the Low-Battery Detector is enabled while the chip is in SLEEP mode, it will automatically enable the RCO scillator which will periodically turn on the Low-Battery Detector circuit to measure the battery voltage. The battery voltage may also be read out through SPI Register 1Bh at any time when the Low Battery Detector is enabled. The Low Battery Detect function is enabled by setting enlbd='1' in Register 07h.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
1A	R/W	Low Battery Detector Threshold				lbdt[4]	lbdt[3]	lbdt[2]	lbdt[1]	lbdt[0]	14h
1B	R	Battery Voltage Level	0	0	0	vbat[4]	vbat[3]	vbat[2]	vbat[1]	vbat[0]	-

The Low Battery Detector output is digitized by a 5 bit ADC. When the Low Battery Detector function is enabled, enlbd='1' in Register 07H, the battery voltage may be read at anytime by reading the Battery Voltage Level Register, Address 1Bh. A Battery Voltage Threshold may be programmed to register 1Ah. When the battery voltage level drops below the battery voltage threshold an interrupt will be generated on nIRQ pin to the Microcontroller. The Microcontroller will then need to verify the interrupt by reading the interrupt status register, Addresses 03 and 04H. The LSB step size for the LBD ADC is 50mV, with the ADC range demonstrated in the table below. When the ADC is enabled a conversion or update will occur approximately every 250us.

$$BatteryVoltage = 1.7 + 50mV * ADCValue$$

ADC value	VDD voltage [V]
0 <	1.7
1	1.7-1.75
2	1.75 - 1.8
…	…
29	3.1 - 3.15
30	3.15 - 3.2
31 >	3.2

9.6 Wake-Up Timer

The chip contains an integrated Wake-Up Timer which periodically wakes the chip from SLEEP mode. The Wake-Up-Timer runs from the internal 32.768 kHz RC Oscillator. The Wake-Up-Timer function occurs when in SLEEP mode. If enwt='1' in Register 07h when entering SLEEP mode, the Wake-Up-Timer will count for a time specified by the Wake-Up Timer Period in Registers 10h-12h. At the expiration of this period an interrupt will be generated on the nIRQ pin. The Microcontroller will then need to verify the interrupt by reading the Interrupt Status Registers 03h-04h. The Wake-Up Timer Value may be read at any time by the wtv[15:0] read only Registers 13h-14h.

The formula for calculating the Wake-Up Period is the following:

$$WUT = \frac{32 * M * 2^{R-D}}{32.768} ms$$

WUT Register	Description
wtr[3:0]	R Value in Formula
wtd[1:0]	D Value in Formula
wtm[15:0]	M Value in Formula

Use of the D variable in the formula is only necessary if finer resolution is required than the R value gives.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
14	R/W	Wake-Up Timer Period 1			wtr[3]	wtr[2]	wtr[1]	wtr[0]	wtd[1]	wtd[0]	00h
15	R/W	Wake-Up Timer Period 2	wtm[15]	wtm[14]	wtm[13]	wtm[12]	wtm[11]	wtm[10]	wtm[9]	wtm[8]	00h
16	R/W	Wake-Up Timer Period 3	wtm[7]	wtm[6]	wtm[5]	wtm[4]	wtm[3]	wtm[2]	wtm[1]	wtm[0]	00h
17	R	Wake-Up Timer Value 1	*wtv[15]*	*wtv[14]*	*wtv[13] wtv[12]*		*wtv[11] wtv[10]*		*wtv[9]*	*wtv[8]*	-
18	R	Wake-Up Timer Value 2	*wtv[7] wtv[6]*		*wtv[5] wtv[4]*		*wtv[3] wtv[2]*		*wtv[1] wtv[0]*		-

9.7 Low Duty Cycle Mode

The Low Duty Cycle Mode is available to automatically wake-up the receiver to check if a valid signal is available. The basic operation of the Low Duty Cycle Mode is demonstrated in the figure below. If a valid preamble or sync word is not detected the chip will return to sleep mode until the beginning of a new WUT period. If a valid preamble and sync are detected the receiver on period will be extended for the Low Duty Cycle Mode Duration (TLDC) to receive all of the packet. The time of the TLDC is determined by the formula below:

$$TLDC = ldc[7:0] * \frac{2*(R-D)*32}{32.768} ms$$

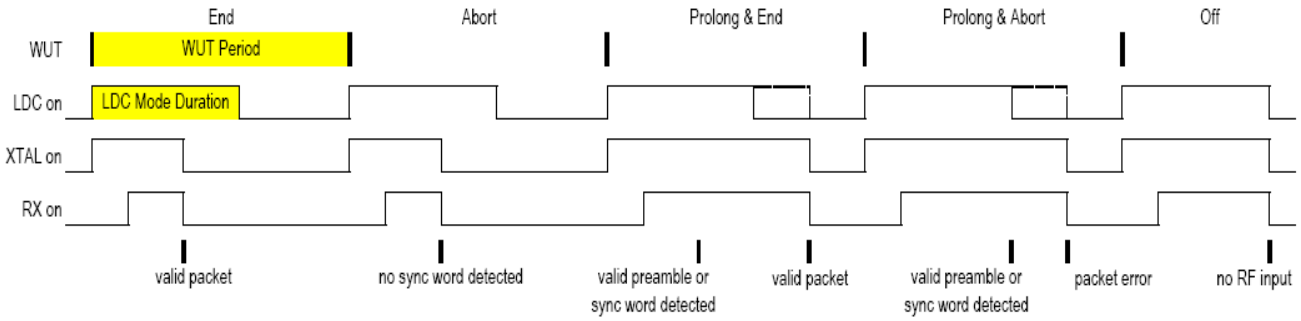


Figure 27: Low Duty Cycle Mode

9.8 GPIO Configuration

Three general purpose I/O's (GPIOs) are available for configuration to satisfy the requirements of the desired application. Many functions such as specific interrupts, TRSW control, Antenna Diversity Switch control, Micro controller Output, etc. are available as shown in the tables below. When in Shutdown mode all the GPIO pads are pulled low ='0'.

Note – the ADC should not be selected as an input to the GPIO in Standby or Sleep Modes and will cause excess current consumption.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
0B	R/W	GPIO0 Configuration	gpio0drv[1]	gpio0drv[0]	pup0	gpio0[4]	gpio0[3]	gpio0[2]	gpio0[1]	gpio0[0]	00h
0C	R/W	GPIO1 Configuration	gpio1drv[1]	gpio1drv[0]	pup1	gpio1[4]	gpio1[3]	gpio1[2]	gpio1[1]	gpio1[0]	00h
0D	R/W	GPIO2 Configuration	gpio2drv[1]	gpio2drv[0]	pup2	gpio2[4]	gpio2[3]	gpio2[2]	gpio2[1]	gpio2[0]	00h
0E	R/W	I/O Port Configuration		*extitst[2]*	*xtitst[1]*	*extitst[0]*	itsdo	dio2	dio1	dio0	00h

Address: 0Bh, 0Ch, 0Dh – GPIO Port Configuration

Bit	R/W	Default	Function
[7:6]	R	-	RESERVED
5	R/W	0	**pupx =** Pull-up Resistor enable on GPIOx. When set to '1' the a 200 kohm resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.
[4:0]	R/W	0000	**gpiox[4:0] =** GPIOx pin function select: 00000 – Power-On-Reset Inverted (output) 00001 – Wake-Up Timer: '1' when WUT has expired (output) 00010 – Low Battery Detect: '1' when battery is below threshold setting (output) 00011 – Direct Digital Input 00100 – External Interrupt, falling edge (input) 00101 – External Interrupt, rising edge (input) 00110 – External Interrupt, state change (input) 00111 – ADC Analog Input 01000 – Reserved (Analog Test N Intput) 01001 – Reserved (Analog Test P Intput) 01010 – Direct Digital Output 01011 – Reserved (Digital Test Output) 01100 – Reserved (Analog Test N Output) 01101 – Reserved (Analog Test P Output) 01110 – Reference Voltage (output) 01111 – TX Data CLK output to be used in conjunction with TX Data pin (output) 10000 – TX Data input for direct modulation (input) 10001 – External Retransmission Request (input) 10010 – TX State (output) 10011 – TX FIFO Almost Full (output) 10100 – RX Data (output) 10101 – RX State (output) 10110 – RX FIFO Almost Full (output) 10111 – Antenna 1 Switch used for antenna diversity (output) 11000 – Antenna 2 Switch used for antenna diversity (output) 11001 – Valid Preamble Detected (output) 11010 – Invalid Preamble Detected (output) 11011 – Sync Word Detected (output) 11100 – Clear Channel Assessement (output) 11101 – VDD else – GND

The GPIO settings for GPIO1 and GPIO2 are t he same as for GPIO 0 with the exception of t he 00000 default setting. The default settings for each GPIO are listed below:

GPIO	00000 – Default Setting
GPIO0	POR
GPIO1 POR	Inverted
GPIO2 Microcontroller	Clock

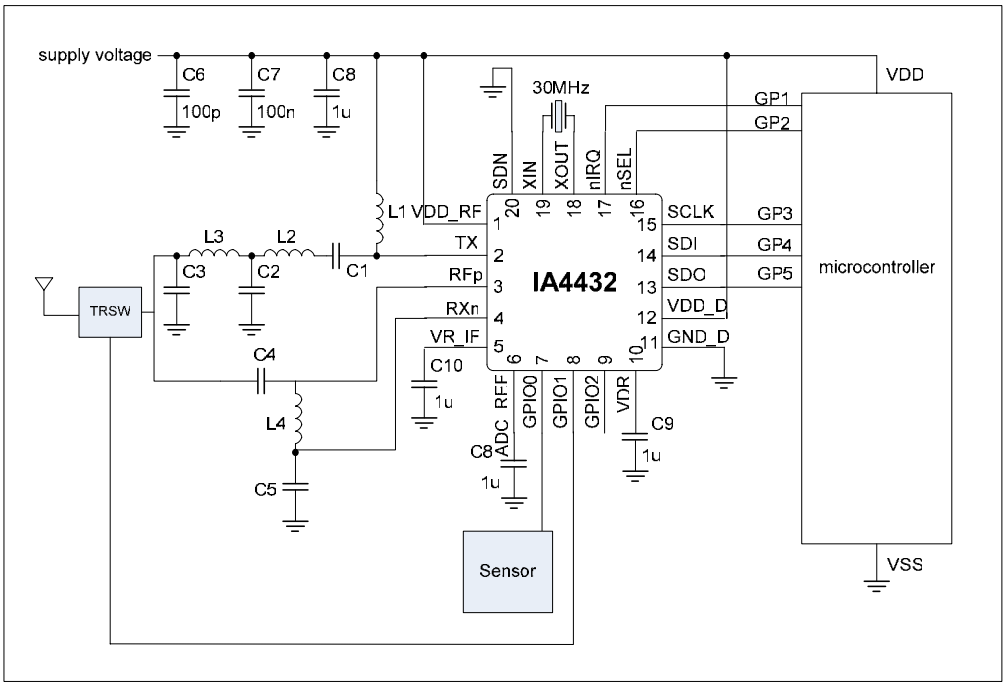
Address: 0Eh – I/O Port Configuration

Bit R/W		Default	Function
7 R		0	RESERVED
6 R		0	**extitst[2]** = External Interrupt Status. If the GPIO2 is programmed to be external interrupt sources then the status can be read here.
5 R		0	**extitst[1]** = External Interrupt Status. If the GPIO1 is programmed to be external interrupt sources then the status can be read here.
4 R		0	**extitst[0]** = External Interrupt Status. If the GPIO0 is programmed to be external interrupt sources then the status can be read here.
3 R/W		0	**itsdo** = Interrupt Request Output on the SDO Pin. nIRQ output is present on the SDO pin if this bit is set and the nSEL input is inactive (high).
2 R/W		0	**dio2** = Direct I/O for GPIO2. If the GPIO2 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO2 is configured to be a direct input then the value of the pin can be read here.
1	R/W	0	**dio1** = Direct I/O for GPIO1. If the GPIO1 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO1 is configured to be a direct input then the value of the pin can be read here.
0	R/W	0	**dio0** = Direct I/O for GPIO0. If the GPIO0 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO0 is configured to be a direct input then the value of the pin can be read here.

The diagrams below show two different configurations/usage of the GPIO. In Configuration A an external sensor is used and the GPIO is configured as an input with the 00101 External Interrupt, Rising Edge setting. When the sensor is triggered the nIRQ pin will go high and the M icrocontroller w ill b e ab le to read the interru pt r egister and know that an ev ent occurred on the sen sor. The advantage of th is configuration is that it saves a M icrocontroller pin. This application utilizes the high outp ut power so a TRSW is required.

In Configuration B, the chip is configured to provide the System Clock output to the Microcontroller so that only one crystal is needed in the system, therefore reducing the BOM cost. For the TX Data Source, Direct Mode is used because long packets are desired with a unique packet handling format already implemented in the Microcontroller. In this configuration the TX Data Clock is configured onto GPIO0, the TX Data is configured onto GPIO1, and the Microcontroller System Clock coc k output is configured onto GPIO2. In this application only the lowest output power setting is required so no TRSW is needed.

GPIO Configuration A



GPIO Configuration B

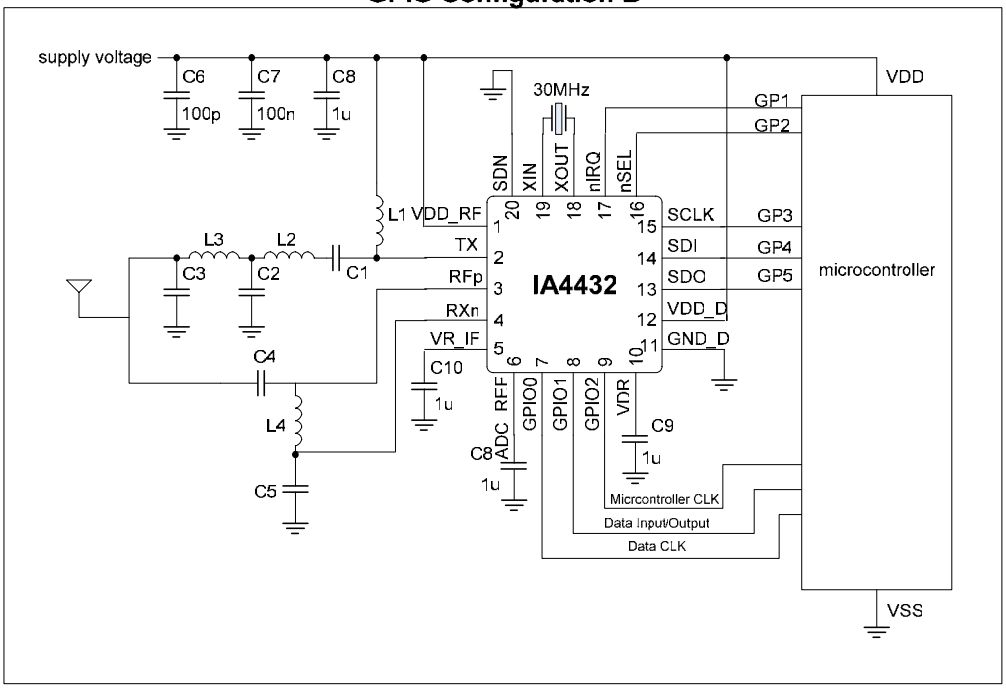


Figure 28: GPIO Usage Examples

9.9 Antenna-Diversity

To avoid the problem of frequency-selective fading due to multi-path propagation, many transceiver systems use a scheme known as Antenna Diversity. In this scheme, two antennas are used. Each time the transceiver enters RX mode the receive signal strength from each antenna is evaluated. This evaluation process takes place during the preamble portion of the packet. The antenna with the strongest received signal is then used for the remainder of that RX packet. The same antenna will also be used for the next corresponding TX packet.

This chip fully supports Antenna Diversity with an integrated Antenna Diversity Control Algorithm. By setting GPIOx[4:0]='10111' and '11000', the required signal needed to control an external SPDT RF switch (such as PIN diode or GaAs switch) is made available on the GPIOx pins. The operation of these switches is programmable to allow for different Antenna Diversity architectures and configurations. The antdiv[2:0] register is found in register 08h. The GPIO pin is capable of sourcing up to 5mA of current, so it may be used directly to forward-bias a PIN diode if desired.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
08	R/W	Operating & Function Control 2	antdiv[2]	antdiv[1]	ant div[0]	rxmpk	autotx	enldm	ffclrrx	ffclrtx	00h

Table 17: Antenna Diversity Control

antdiv[2:0]	RX/TX state		non RX/TX state	
	GPIO Ant1	GPIO Ant2	GPIO Ant1	GPIO Ant2
000	1	0	0	0
001	0	1	0	0
010	1	0	1	1
011	0	1	1	1
100	antenna diversity algorythm		0	0
101	antenna diversity algorythm		1	1
110	antenna diversity algorythm in beacon mode		0	0
111	antenna diversity algorythm in beacon mode		1	1

9.10 TX/RX Switch Control

When using the maximum output power of +20dBm a TX/RX Switch (TRSW) may be required. The control for the switch with the proper timing will be available on the GPIO pins. See application schematics for various options using a TX/RX Switch.

9.11 RSSI and Clear Channel Assessment

The RSSI (Received Signal Strength Indicator) signal is an estimate of the signal strength in the channel to which the receiver is tuned. When sync word detection is enabled the RSSI value will be frozen after the sync word has been detected. When sync word detection is disabled or a sync word is not detected, the RSSI value will be updated continuously. The RSSI value can be read from an 8-bit register with 0.5dB resolution per bit, for a total RSSI range of 127.5dB. Figure 29: demonstrates the relationship between input power level and RSSI value.

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
26	R	Received Signal Strength Indicator	rssi[7]	rssi[6]	rssi[5]	rssi[4]	rssi[3]	rssi[2]	rssi[1]	rssi[0]	-
27	R/W	RSSI Threshold for Clear Channel Indicator	rssith[7]	rssith[6]	rssith[5]	rssith[4]	rssith[3]	rssith[2]	rssith[1]	rssith[0]	00h

For Clear Channel Assessment a threshold is programmed into rssith[7:0] in Register 27h. After the RSSI is evaluated in the preamble, a decision is made if the signal strength on this channel is above or below the threshold. If the signal strength is above the programmed threshold then a '1' will be shown in the RSSI status bit in the Device Status Register 02h, Interrupt Status Register 04h, or configurable GPIO (GPIOx[3:0]='1110').

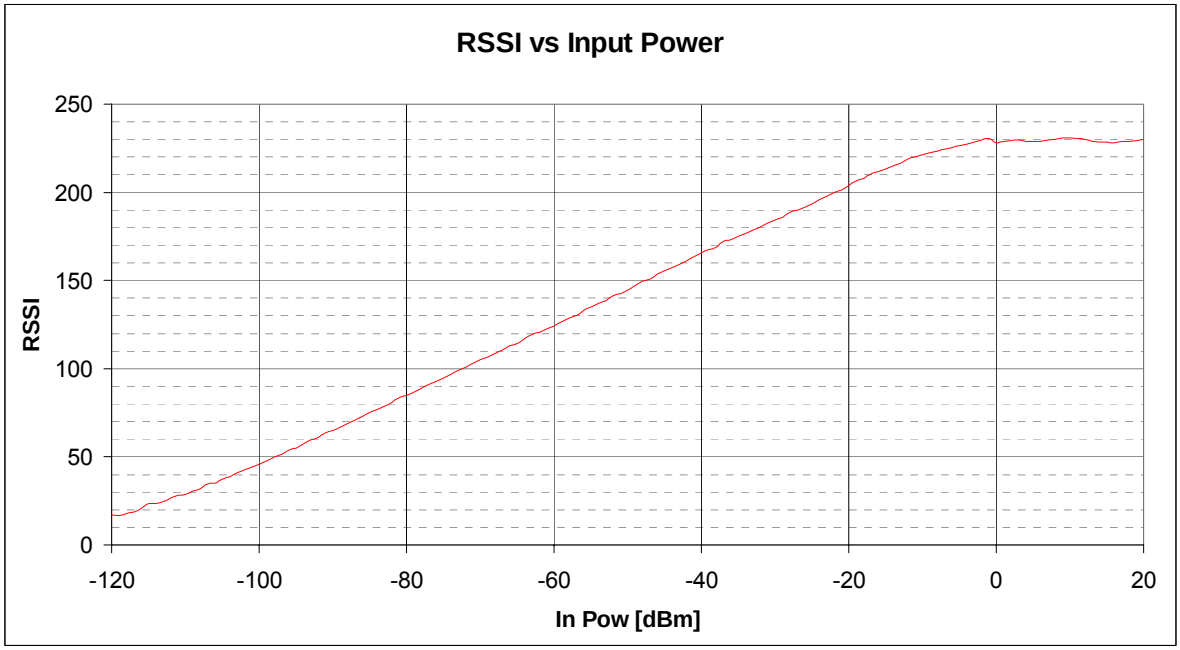


Figure 29: RSSI Value vs. Input Frequency

9.12 Analog and Digital Test Bus

A differential analog test bus (ATB) is integrated into the RFIC to provide access to internal analog signals for debugging and test purposes. The available signals are shown below in Table 18: and are controlled by the atb[4:0] field in SPI Register 50h. The ATB signals are available on GPIO pins.

Address	R / W	Function / Description	Data								POR Default	Notes
			D7	D6	D5	D4	D3	D2	D1	D0		
50	R/W	Analog Test Bus				atb[4]	atb[3]	atb[2]	atb[1]	atb[0]	00h	ATB
51	R/W	Digital Test Bus			ensctest	dtb[4]	dtb[3]	dtb[2]	dtb[1]	dtb[0]	00h	DTB

Table 18: Analog Test Bus

atb[4:0]	GPIOx	GPIOx
1	MixIp	MixIn
2	MixQp	MixQn
3	PG A_Ip	PGA_In
4	PG A_QP	PGA_Qn
5	ADC_vcm	ADC_vbn
6	ADC_refmid	ADC_vbiasp
7	ADC_vcm	ADC_vcmb
8	ADC_ipol y10u	ADC_ref
9	ADC_refd ac_p	ADC_refdac_m
10	ADC_Res1i_p	ADCRes1i_m
11	ADC_Res1q_p	ADC_Res1q_m
12	ADC_Res2i_p	ADCRes2i_m
13	ADC_Res2q_p	ADC_Res2q_m
14	ADC_Res3i_p	ADCRes3i_m
15	ADC_Res3q_p	ADC_Res3q_m
16	spare	spare
17	ADC_RES_CAL _cap	ADC_RES_CAL_res
18	ICP_Test	PLL_IBG_05
19	PLL_VBG	VSS_VCO
20	Vctrl_Test	PLL_IPTAT_05
21	PA_vbias	spare
22	DIGB G	DIGVFB
23	IFBG	IFVFB
24	PLLBG	PLLVReg
25	IBias10u	IBias5u
26	32KRC_Ucap	32KRC_Ures
27	ADC8_VIN	ADC8_VDAC
28	LBDcomp	LBDcompref
29	TSBG	TSVtemp
30	RFBG	RFVREG
31	V COBG	VCOVREG

A digital test bus (DTB) is also integrated into the digital portion of the design. The DTB may be configured for output on the GPIOs. For configuring of the GPIO see registers 0Bh-0Dh. The available digital test points are controlled by the dtb[4:0] field in Register 51h.

Table 19: Digital Test Bus

dtb[4:0]	GPIO0	Signal	GPIO1	Signal	GPIO2	Signal
0	wkup_clk_32k	wake-up 32kHz clock	rbase_en	first divided clock	clk_base	timebase clock
1	wkup_clk_32k	wake-up 32kHz clock	wake_up	wake-up event	tm1sec	1 sec timebase
2	ts_adc_en	aux. ADC enable	adc_rdy_n	aux. ADC conversion ready	adc_done	aux. ADC measurement done
3	cont_lbd	low battery continouos mode	lbd_on	low battery ON signal	lbd	unfiltered output of LBD
4	div_clk_g	gated divided clock	uc_clk	microcontroller clock	ckout_rcsel	slow clock selected
5	en_div_sync	clock divider enable (sync'ed)	en_ckout	clock out enable	en_ckout_s	clock out enable (sync'ed)
6	osc30_en	oscillator enable	osc30_bias2x	oscillator bias control	xok	chip ready
7	xok	chip ready	zero_cap	cap. load zero	osc30_buff_en	buffer enable
8	tsadc_needed	aux. ADC enable	ext_retran	ext. retransmission request	tx_mod_gpio	TX modulation inpit
9	gpio_0_oen_n	GPIO0 output enable	gpio_0_aen	GPIO0 analog selection	gpio_0_aden	GPIO0 ADC input line enable
10	int_ack1	interrupt acknowledge 1	int_ack2	interrupt acknowledge 2	int_store	interrupt latch closed
11	ext_int2	ext. interrupt from GPIO2	irq_bit8	combined external status	msk_bit8	combined masked ext. int.
12	sdo_aux_sel	SDO aux. function select	sdo_aux	SDO aux. signal	nirq_aux_sel	nIRQ aux. function select
13	trdata_on_sdi	TX/RX data on SDI	tx_mod	TX modulation input	tx_clk_out	TX clock output
14	start_full_sync	RC osc. full calibration start	start_fine_sync	RC osc. fine calibration start	xtal_req	crystal req. for RC osc. cal.
15	coarse_rdy	RC osc. coarse cal. ready	fine_rdy	RC osc. fine cal. ready	xtal_req_sync	sync'ed crystal request
16	vco_cal_rst_s_n	VCO calibration reset	vco_cal	VCO calibration is running	vco_cal_done	VCO calibration done
17	vco_cal_en	VCO calibration enable	en_ref_cnt	reference counter enable	en_freq_cnt_s	frequency counter enable
18	vco_cal_en	VCO calibration enable	pos_diff	positive difference to goal	en_freq_cnt_s	frequency counter enable
19	dsm_clk_mux	DSM multiplexed clock	pll_fb_clk_tst	PLL feedback clock	pll_ref_clk_tst	PLL reference clock
20	dsm[0]	delta-sigma output	dsm[1]	delta-sigma output	dsm[2]	delta-sigma output
21	dsm[3]	delta-sigma output	pll_fbdiv15		dsm_rst_s_n	delta-sigma reset
22	pll_en	PLL enable: TUNE state	pllt0_ok	PLL initial settling OK	pllts_ok	PLL soft settling OK
23	ch_freq_req	frequency change request	pllts_ok	PLL soft settling OK	vco_cal_done	VCO calibration done
24	vco_cal_en	VCO calibration enable	pll_vbias_shunt_en	VCO bias shunt enable	prog_req	frequency recalculation req.
25	bandgap_en	bandgap enable	frac_div_en	fractional divider enable	buff3_en	buffer3 enable
26	pll_pfd_up	PFD up signal	pll_pfd_down	PFD down signal	pfd_up_down	PFD output change (XOR'ed)
27	pll_lock_detect	PLL lock detect	pll_en	PLL enable: TUNE state	pllt0_ok	PLL initial settling OK
28	pll_en	PLL enable: TUNE state	pll_lock_detect	PLL lock detect	pllts_ok	PLL soft settling OK
29	pwst[0]	internal power state	pwst[1]	internal power state	pwst[2]	internal power state

Internal digital signals available on the Digital Test Bus (continued from the previous page):

dtb[4:0]	GPIO0	Signal	GPIO1	Signal	GPIO2	Signal
30	xok	chip ready: READY state	pll_en	PLL enable: TUNE state	tx_en	TX enable: TX state
31	ts_en	temperature sensor enable	auto_tx_on	automatic TX ON	tx_off	TX OFF
32	ch_freq_req	frequency change request	return_tx	return from TX	pk_sent	packet sent
33	retran_req	retransmission request	tx_ffpt_store	TX FIFO pointer store	tx_ffpt_restore	TX FIFO pointer restore
34	pa_on_trig	PA ON trigger	dly_5us_ok	5 us delay expired	mod_dly_ok	modulator delay expired
35	tx_shdwn	TX shutdown	ramp_start	modulator ramp down start	ramp_done	modulator ramp down ended
36	pk_sent_dly	delayed packet sent	tx_shdwn_done	TX shutdown done	pa_ramp_en	PA ramp enable
37	tx_en	TX enable: TX state	ldo_rf_precharge	RF LDO precharge	pa_ramp_en	PA ramp enable
38	pa_on_trig	TX enable: TX state	dp_tx_en	packet handler (TX) enable	mod_en	modulator enable
39	reg_wr_en	register write enable	reg_rd_en	register rdead enable	addr_inc	register address increment
40	dp_tx_en	packet handler (TX) enable	data_start	start of TX data	pk_sent	packet has been sent
41	data_start	start of TX data	tx_out	packet handler TX data out	pk_sent	packet has been sent
42	ramp_done	ramp is done	data_start	start of TX data	pk_tx	packet is being transmitted
43	tx_ffaf	TX FIFO almost full	tx_fifo_wr_en	TX FIFO write enable	tx_ffem_tst	internal TX FIFO empty
44	clk_mod	modulator gated 10MHz clock	tx_clk	TX clock from NCO	rd_clk_x8	read clock = tx_clk / 10
45	mod_en	modulator enable	ramp_start	start modulator ramping down	ramp_done	modulator ramp done
46	data_start	data input start from PH	ook_en	OOK modulation enble	ook	OOK modulation
47	prog_req	freq. channel update request	freq_err	wrong freq. indication	dsm_rst_s_n	dsm sync. reset
48	mod_en	modulator enable	tx_rdy	TX ready	tx_clk	TX clock from NCO
49	dp_rx_en	packet handler (RX) enable	prea_valid	valid preamble	pk_srch	packet is being searched
50	pk_srch	packet is being searched	sync_ok	sync. word has been detected	rx_data	packet handler RX data input
51	pk_rx	packet is being received	sync_ok	sync. word has been detected	pk_valid	valid packet received
52	sync_ok	sync. word has been detected	crc_error	CRC error has been detected	hdch_error	header error detected
53	direct_mode	direct mode	rx_ffaf	RX FIFO almost full	rx_fifo_rd_en	RX FIFO read enable
54	bit_clk	bit clock	prea_valid	valid preamble	rx_data	demodulator RX data output
55	prea_valid	valid preamble	prea_inval	invalid preamble	ant_div_sw	antenna switch (algorythm)
56	sync_ok	sync. word has been detected	bit_clk bit	clock	rx_data	demodulator RX data output
57	clk_demod	demodulator gated 30MHz clk	adc_lsb_i	ADC I channel data LSB demod_t	st[0]	demodulator test
58	prea_valid	valid preamble	demod_tst[2]	demodulator test	demod_tst[1]	demodulator test
59	agc_smp_clk	AGC sample clock	win_h_tp	window comparator high	win_l_tp	window comparator low dly'd
60	agc_smp_clk	AGC sample clock	win_h_dly_tp	window comparator high	win_l_dly_tp	window comparator low dly'd
61	ldc_on	active low duty cycle	pll_en	PLL enable: TUNE state	rx_en	RX enable: RX state
62	ldc_on	active low duty cycle	no_sync_det	no sync word detected	prea_valid	valid preamble
63	adc_en	ADC enable	adc_refdac_en	ADC reference DAC enable	adc_rst_n	combined ADC reset

10 PACKAGE INFORMATION

10.1 Dimensions

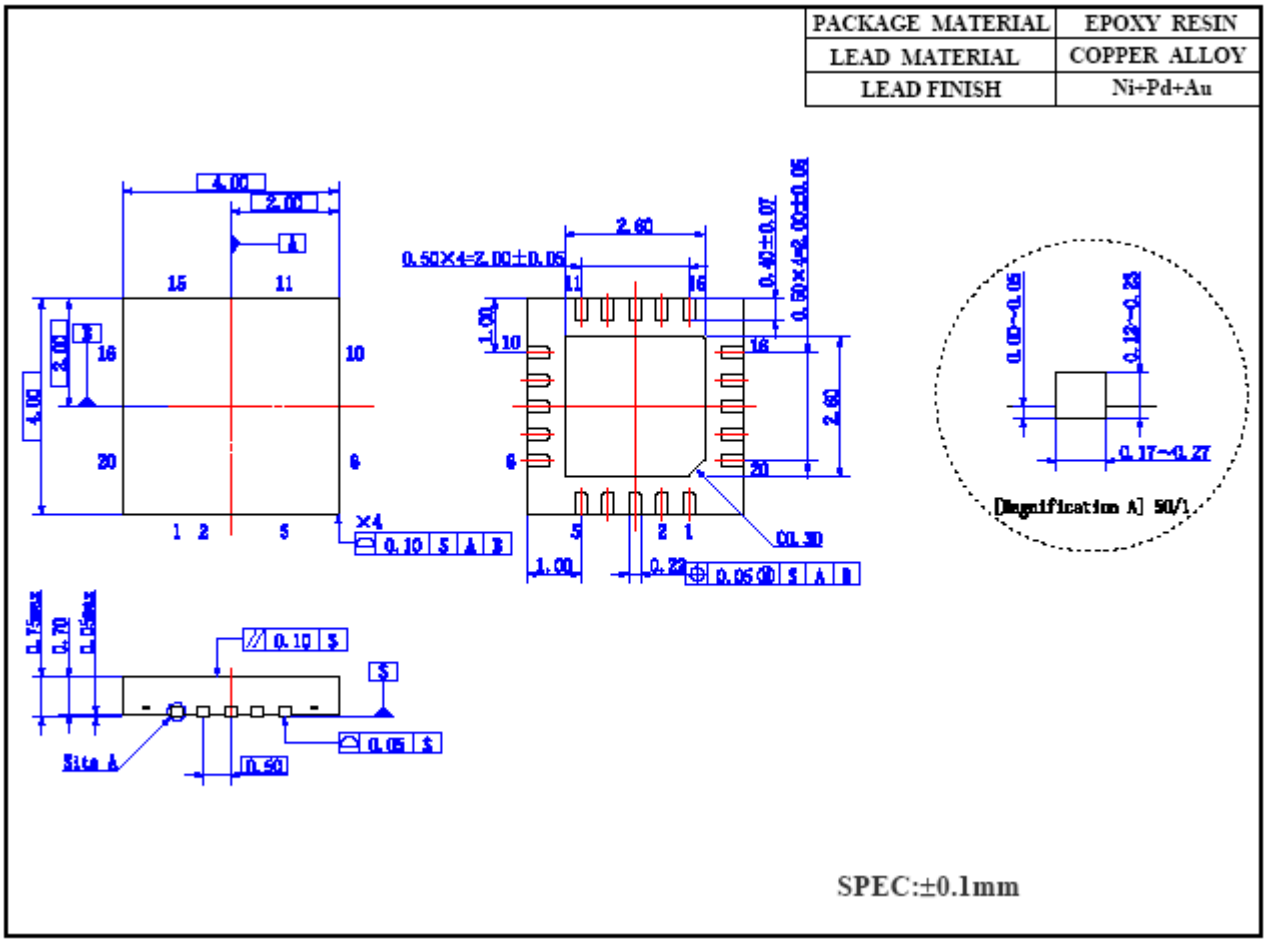


Figure 30: Package Dimensions

11 REFERENCE DESIGN

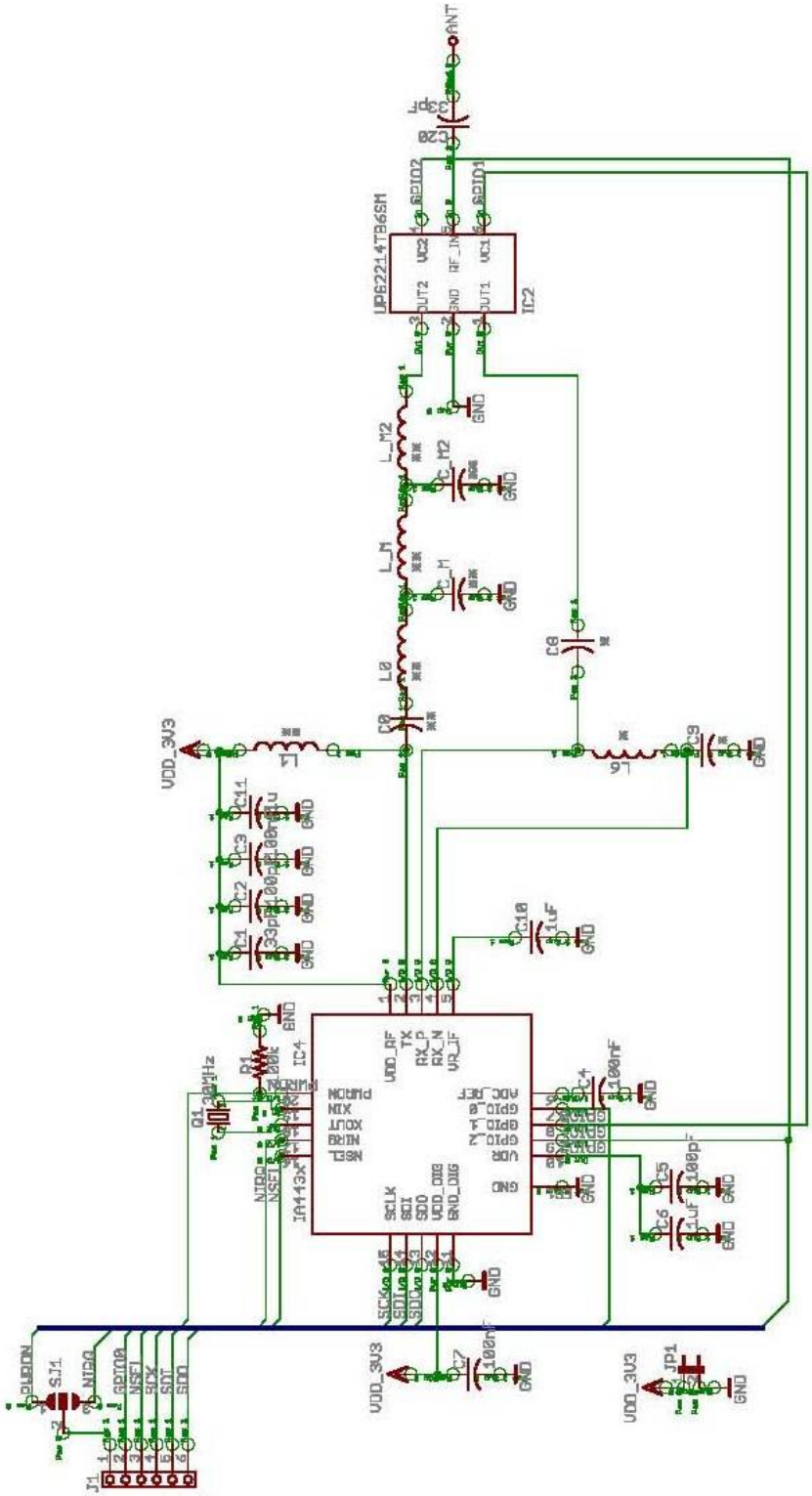


Figure 31: Reference Design Schematic

Part	Value	Device	Package	Description
ANT	915 MHz	ANTENNA	-	Helical antenna
C1	33pF	C-USC0603K	C0603K	Murata, GRM39C0G330J50D500
C2	100pF	C-USC0603K	C0603K	Murata, GRM39C0G101J50D500
C3	100nF	C-USC0603K	C0603K	Murata, GRM39X7R104K50D52K
C4	100nF	C-USC0603	C0603	Murata, GRM39X7R104K50D52K
C5	100pF	C-USC0603K	C0603K	Murata, GRM39C0G101J50D500
C6	1uF	C-USC0603K	C0603K	Murata, GRM39X5R105K16D52K
C7	100nF	C-USC0603K	C0603K	Murata, GRM39X7R104K50D52K
C10	1uF	C-USC0603	C0603	Murata, GRM39X5R105K16D52K
C11	1uF	C-USC0603K	C0603K	Murata, GRM39X5R105K16D52K
C20	33pF	C-USC0402	C0402	Murata, GRM36C0G330J50Z500
IC2	UPG2214TB6SM	UPG2214TB6SM	6-PIN_SUPER_MINIMOLD	NEC GaAs RF switch
IC4	IA443x	IA443x	QFN-20	RF transceiver
J1	PIN6S	PIN6S	PIN6S	Pinhead
JP1	N/A	JP1E	JP1	JUMPER
Q1	30MHz	CRYSTAL-4PINSX-2520-NEW1	QUARTZ_SIWARD_2520_NEW1	SIWARD Quartz
R1	100k	R-US_R0603	R0603	RESISTOR

Elements of the matching network [for 868/915/950 MHz]

Part	Value	Device	Package	Description
C0	22 pF	C-USC0402	C0402	Murata GRM36C0G220J50Z500
C_M	3.9 pF	C-USC0402	C0402	Murata GRM36C0G3R9C50Z500
C_M2	3.9 pF	C-USC0402	C0402	Murata GRM36C0G3R9C50Z500
L0	12 nH	INDUCTCOILCRAFT-0402	L1005	Coilcraft 0402CS-12NX_L_
L1	100 nH	INDUCTCOILCRAFT-0603	L1608	Coilcraft 0603CS-R10X_L_
L_M	18 nH	INDUCTCOILCRAFT-0402	L1005	Coilcraft 0402CS-18NX_L_
L_M2	8.2 nH	INDUCTCOILCRAFT-0402	L1005	Coilcraft 0402CS-8N2X_L_
C8	6.8 pF	C-USC0402	C0402	Murata GRM36C0G6R8D50Z500
C9	3 pF	C-USC0402	C0402	Murata GRM615C0G030B50
L6	10 nH	INDUCTCOILCRAFT-0402	L1005	Coilcraft 0402CS-14NX_L_

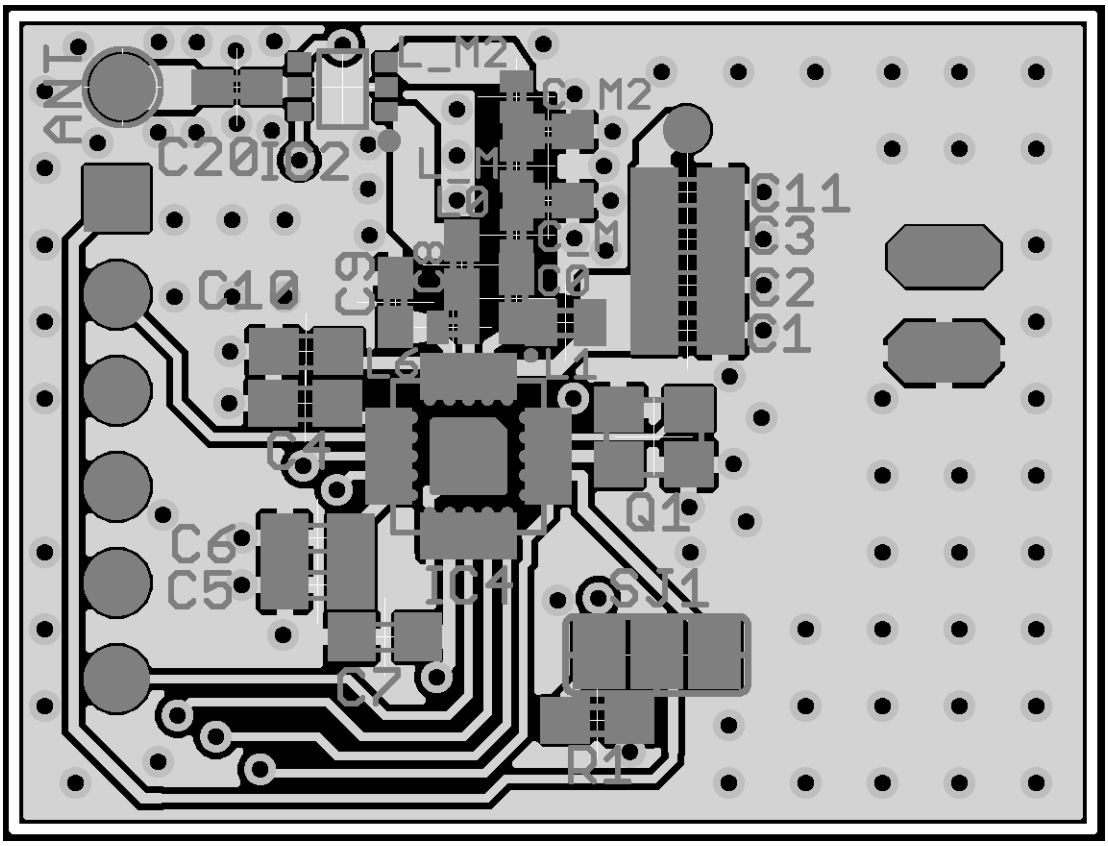


Figure 32: Reference Design Layout

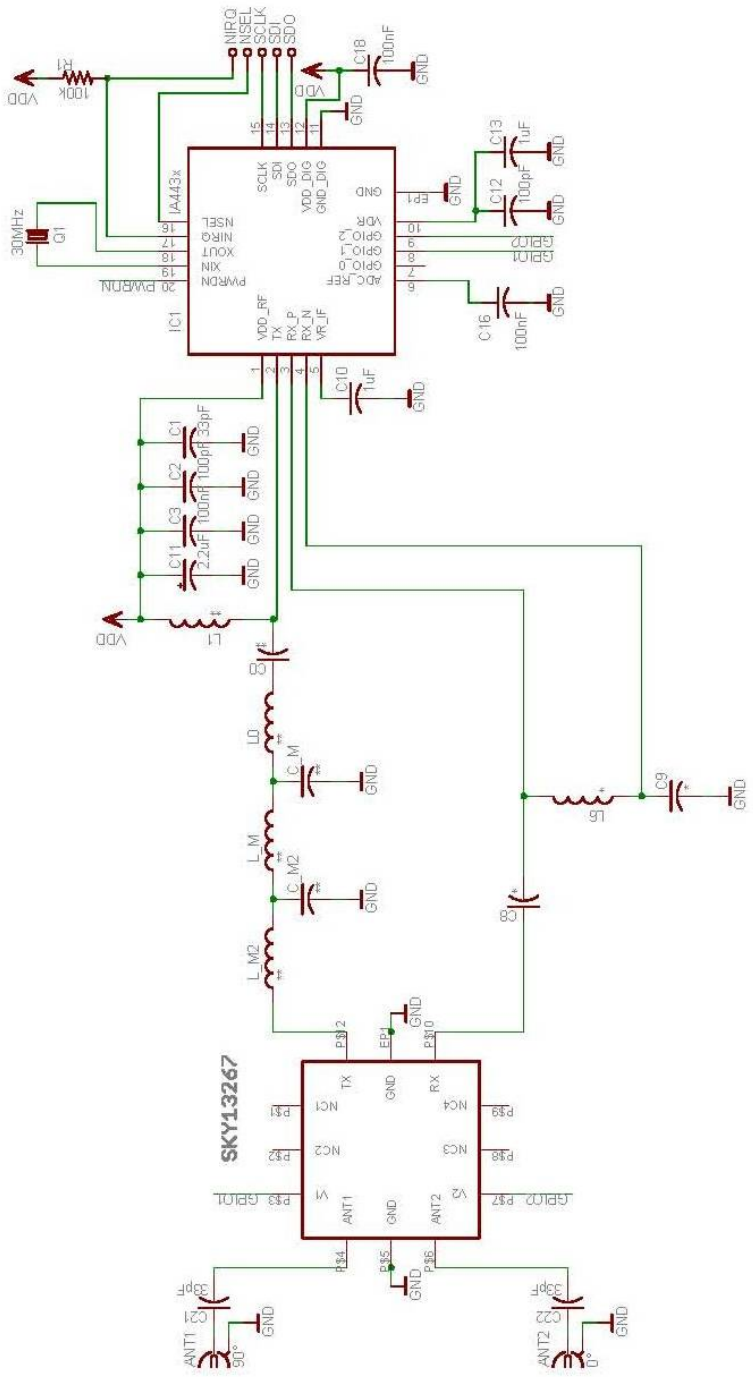


Figure 33: Antenna Diversity Reference Design Schematic

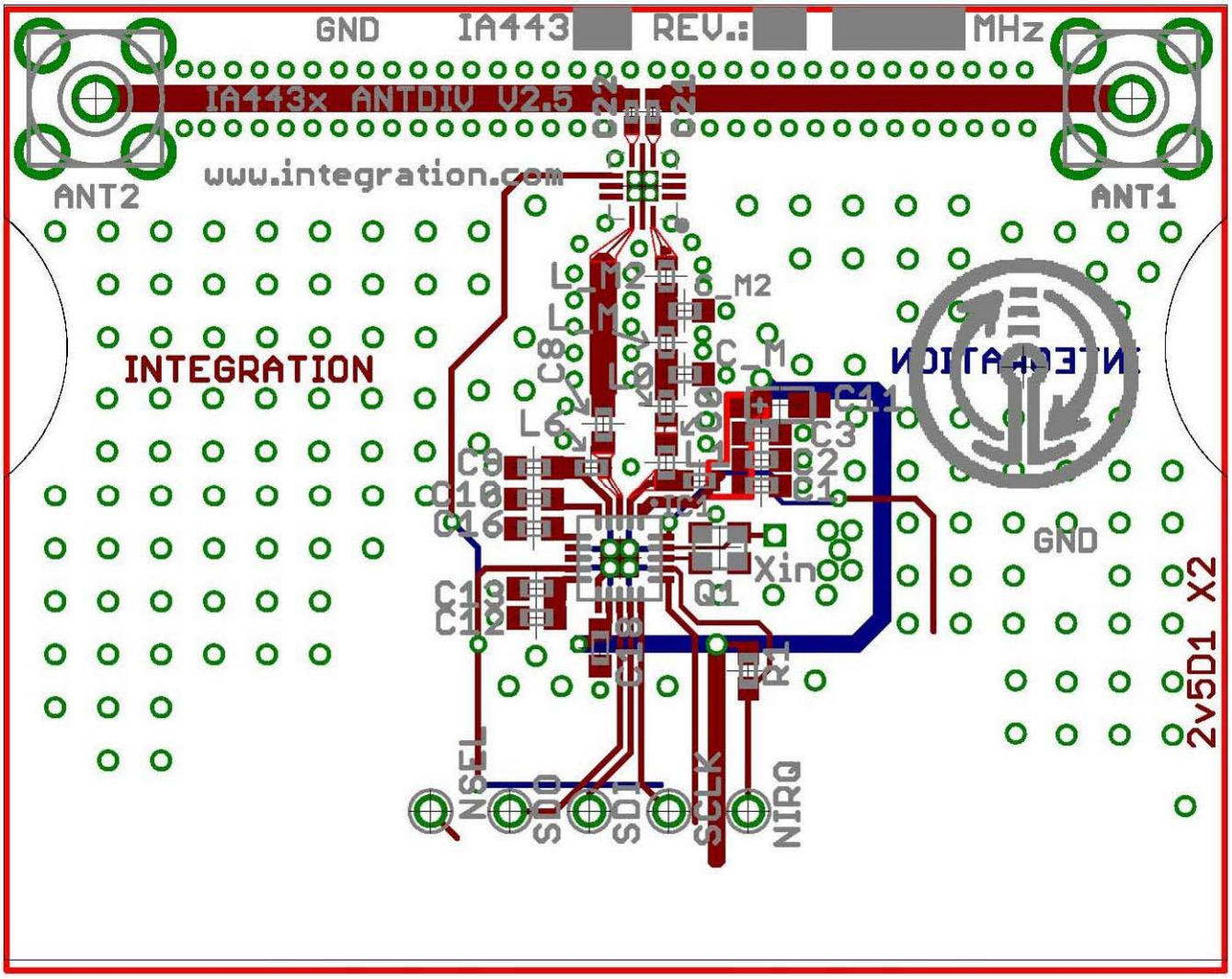


Figure 34: Antenna Diversity Reference Design Layout

12 MEASUREMENT RESULTS

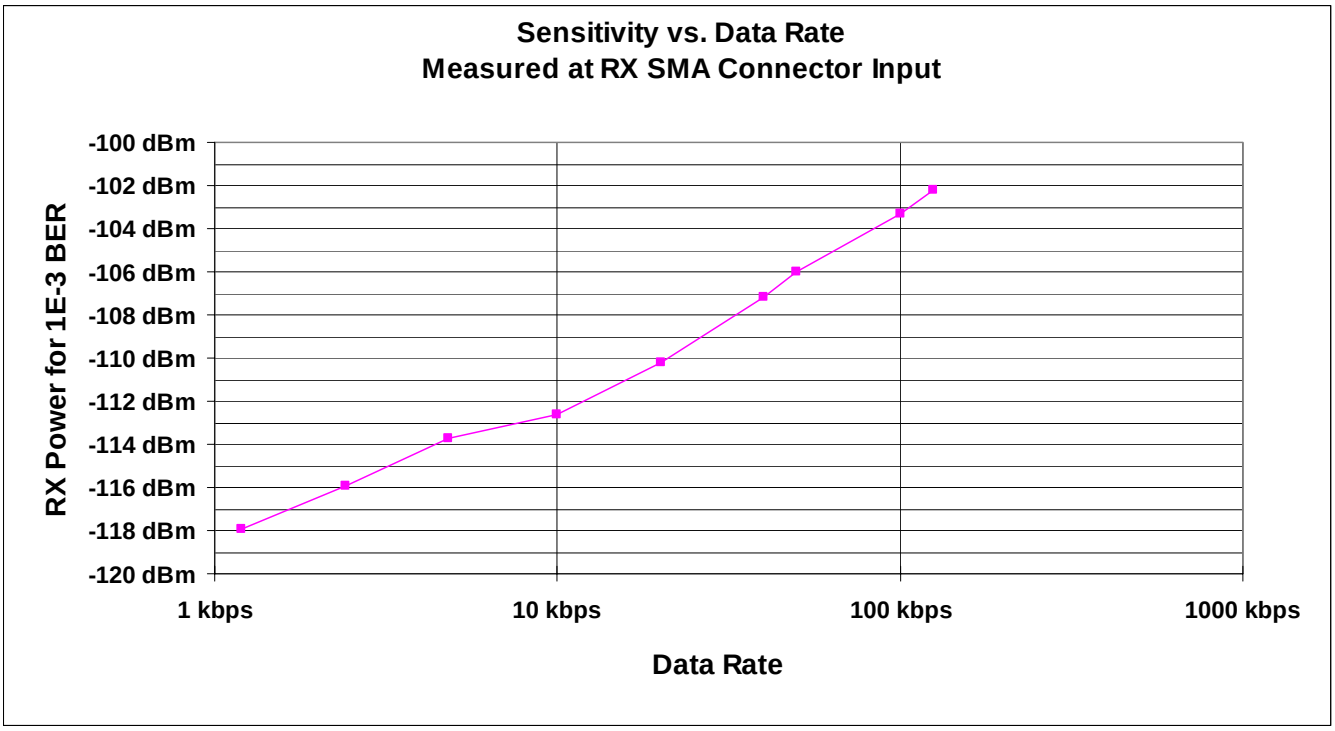
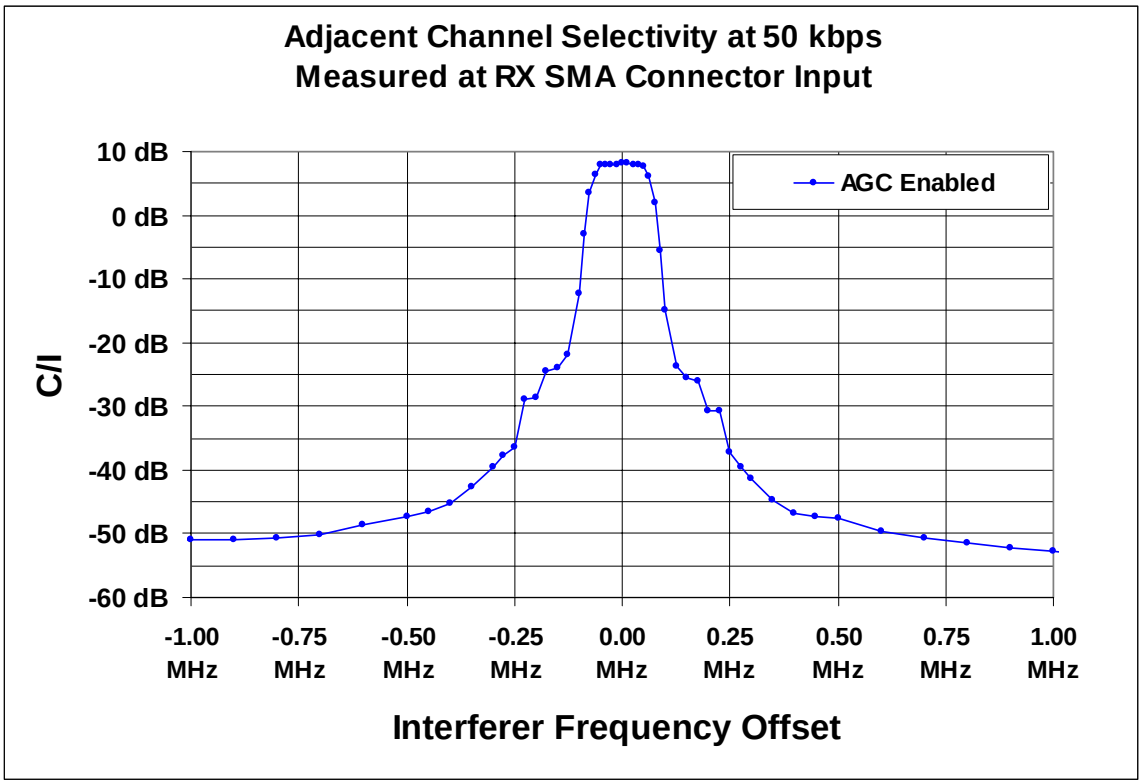


Figure 35: Sensitivity vs. Data Rate



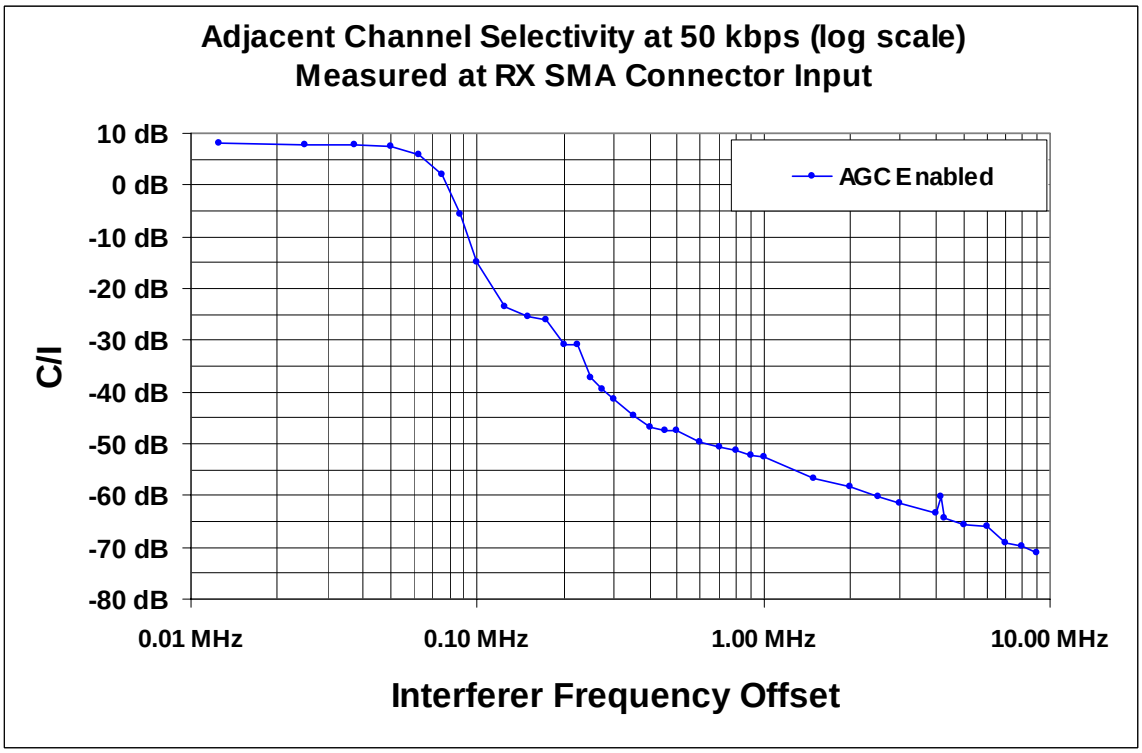


Figure 36: Receiver Selectivity

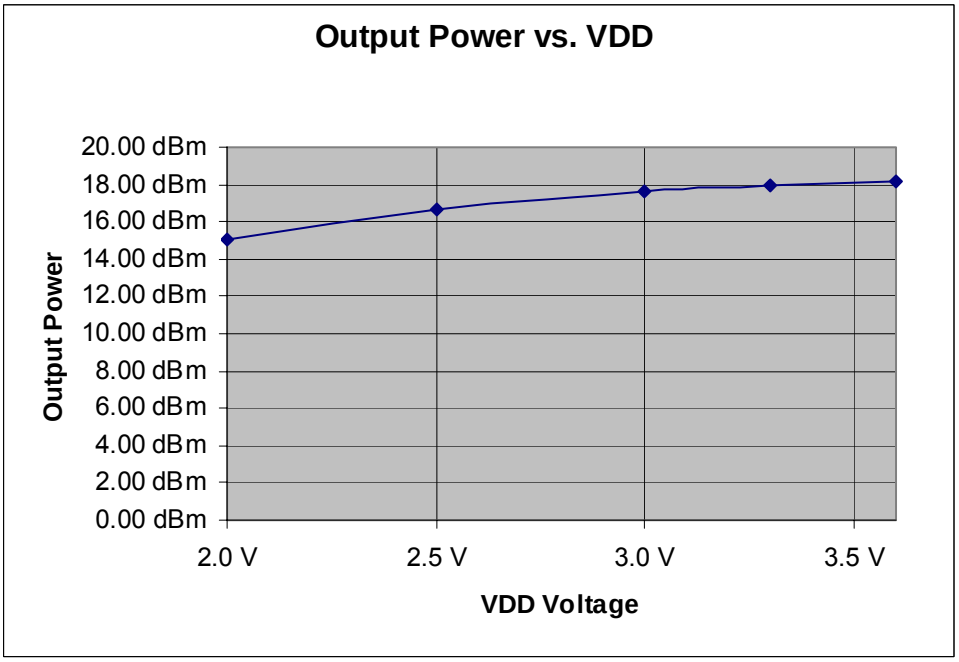


Figure 37: TX Output Power vs. VDD voltage

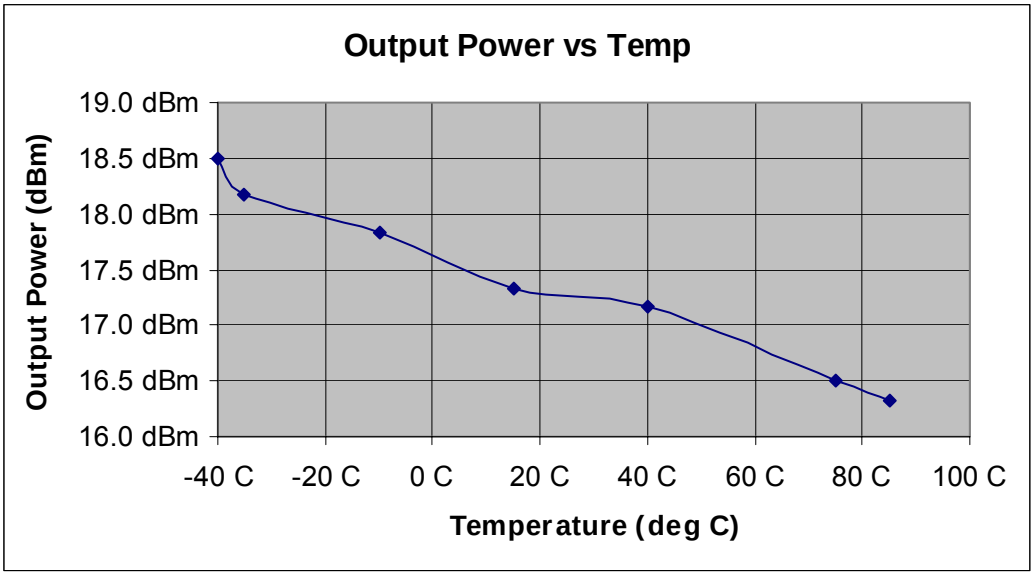


Figure 38: TX Output Power vs Temperature

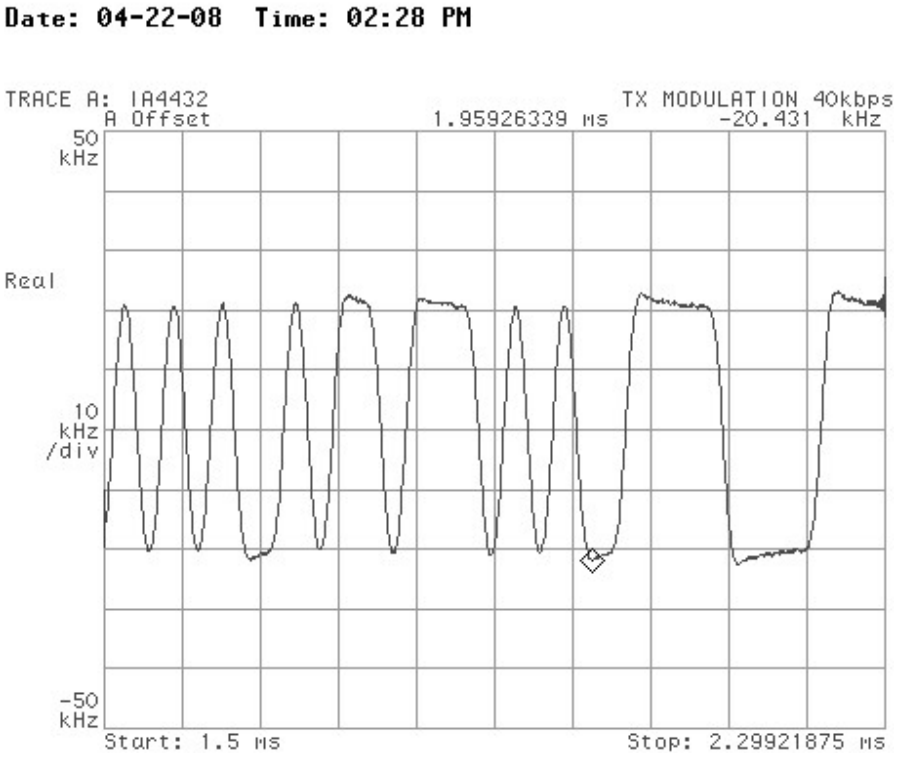


Figure 39: TX Modulation (40kbps, 20khz Deviation)

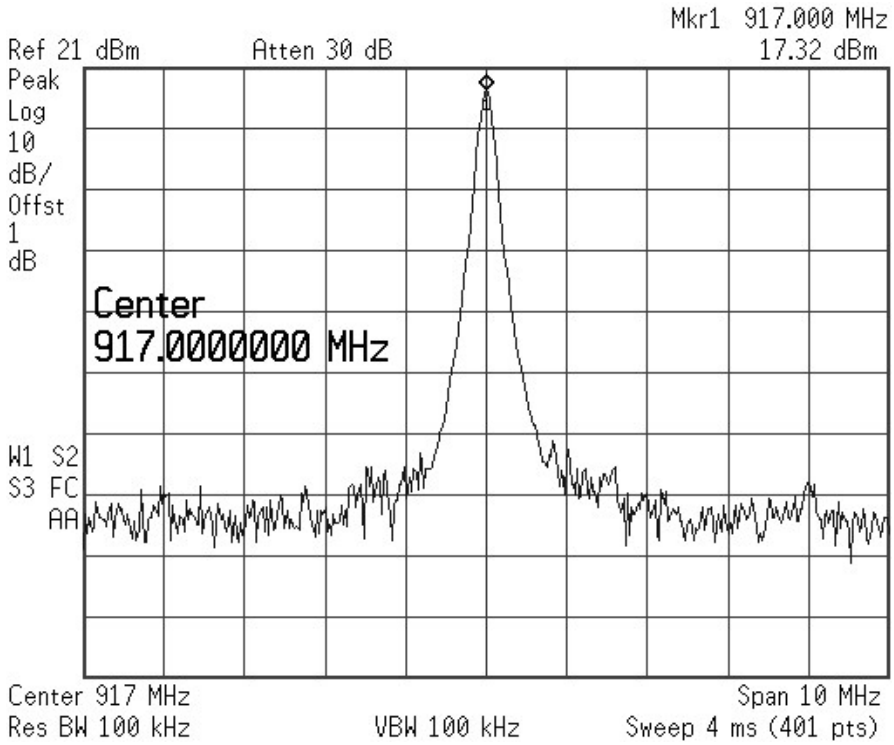


Figure 40: TX Unmodulated Spectrum (917MHz)

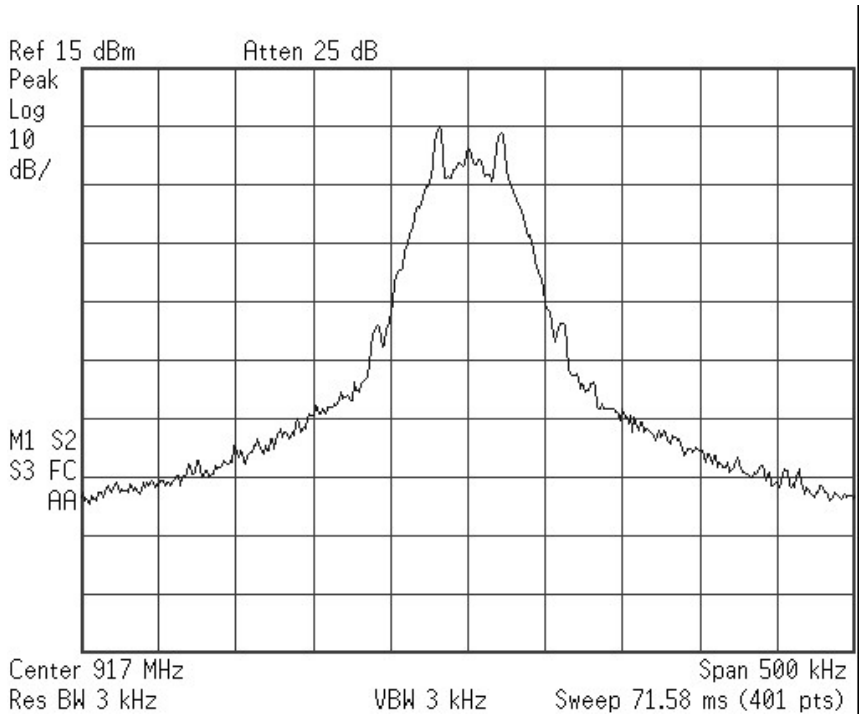


Figure 41: TX Modulated Spectrum (917MHz, 40kbps, 20kHz Deviation, GFSK)

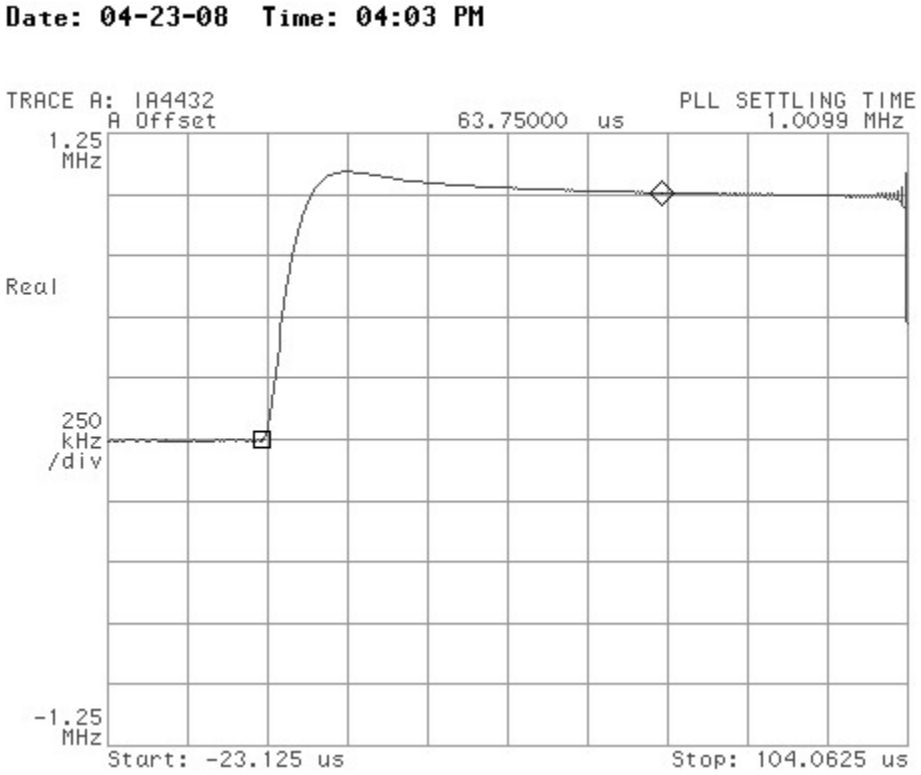


Figure 42: Synthesizer Settling Time for 1MHz Jump settled within 10kHz

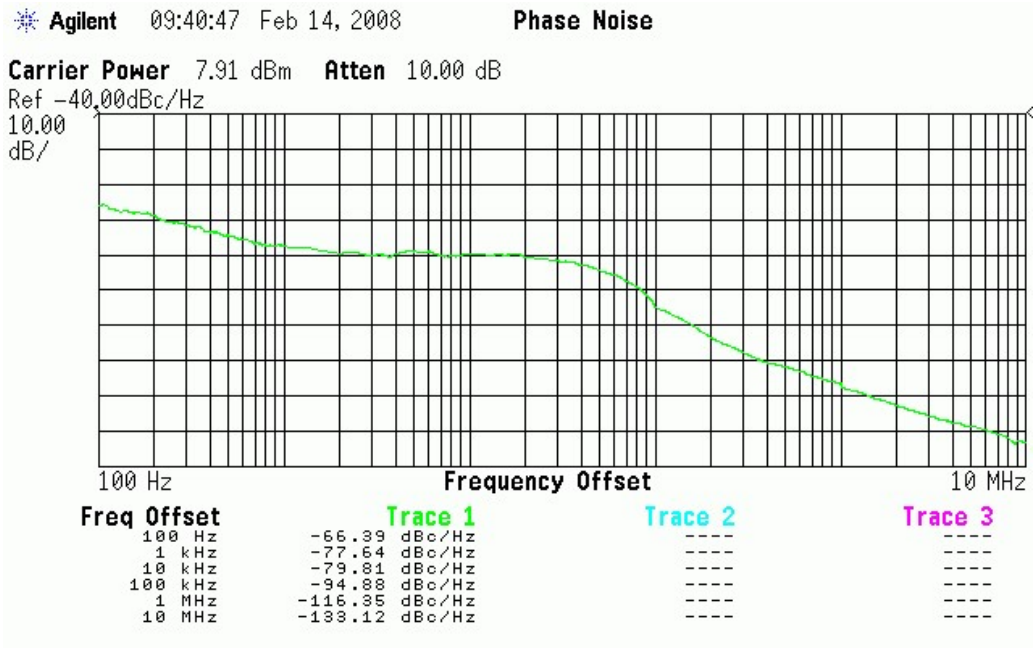


Figure 43: Synthesizer Phase Noise (VCOCURR='11')

13 APPLICATION NOTES

13.1 Crystal Selection

The recommended crystal parameters are given below in the table below:

Table 20: Recommended Crystal Parameters

Frequency	ESR	C_L	C_0	Frequency Accuracy
30MHz	60Ω	12pF	5pF	±20ppm

The internal XTAL oscillator will work over a range for the parameters of ESR, CL, C0, and ppm accuracy. Extreme values may affect the XTAL start-up and sensivit y of the link. For questio ns rega rding the u se of a crys tal paremeters gre atly dev iating f rom th e recommend values listed above, please contact customer support.

The crystal used for engineering evaluation and the reference design is the SIWARD – XTL581200JIG – 30.0MHz – 12.0R.

13.2 Layout Practice

Some general best practice guidelines for PCB layout using the EZRadioPro devices:

-Bypass capacitors should be placed as close as possible to the pin.

-TX/RX matching/layout should mimic reference as much as possible. Failing to do so may cause loss inperformance.

-A solid ground plane is required on the backside of the board under TX/RX matching components

-Crystal should be placed as close as possible to the XIN/XOUT pins and should not have VDD traces running underneath or near it.

-The paddle on the backside of the QFN package needs solid grounding and good soldered connection

-Use GND stitch vias liberally throughout the board, especially underneath the paddle.

13.3 Matching Network Design

13.3.1 RX LNA Matching

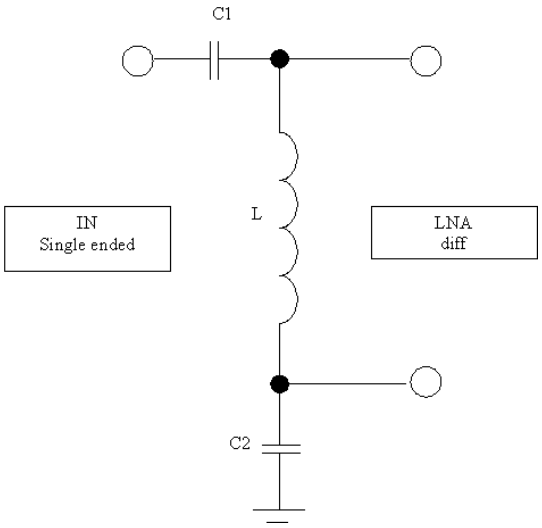


Table 21: RX Matching for Different Bands

Freq Band	C1	L	C2
950 MHz	8.2 pF	10.0 nH	2.7 pF
915 MHz	8.2 pF	10.0 nH	3.3 pF
868 MHz	6.8 pF	11.0 nH	3.0 pF
433 MHz	8.2 pF	36.0 nH	4.7 pF
315 MHz	8.2 pF	56.0 nH	5.6 pF

13.3.2 TX PA Matching and Filtering

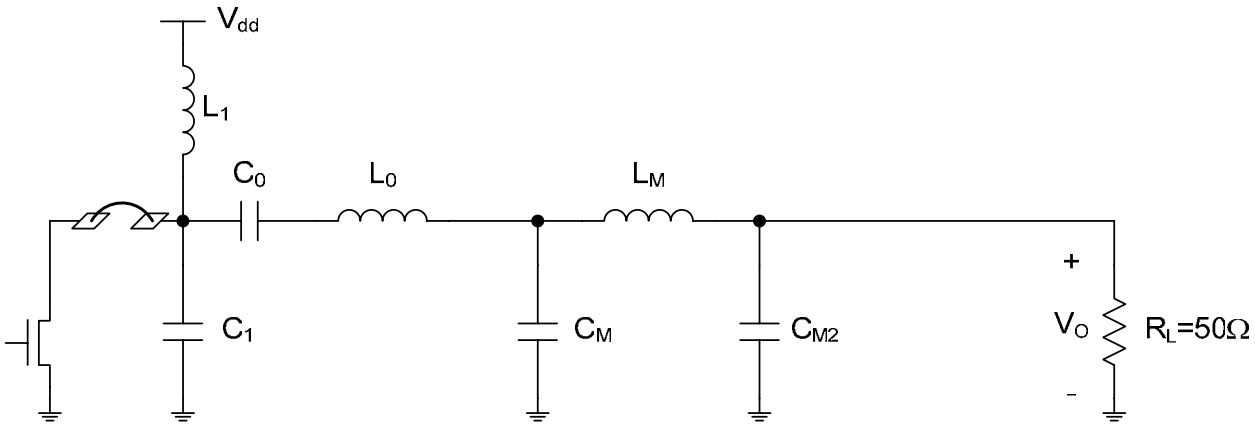
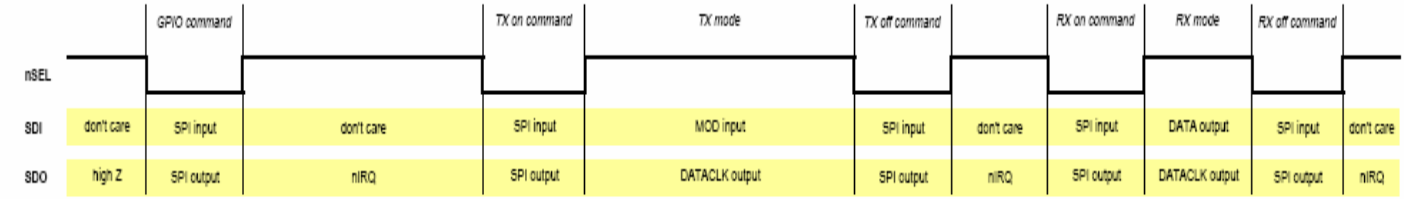


Table 22: TX Matching and Filtering for Different Bands

Freq Band	L1	C0	L0	CM	LM	CM2	LM2
950 MHz	100.0 nH	15.0 pF	12.0 nH	3.6 pF	18.0 nH	3.6 pF	8.2 nH
915 MHz	100.0 nH	22.0 pF	12.0 nH	3.6 pF	18.0 nH	3.0 pF	8.2 nH
868 MHz	100.0 nH	22.0 pF	12.0 nH	3.6 pF	18.0 nH	3.0 pF	10.0 nH
433 MHz	120.0 nH	15.0 pF	36.0 nH	8.2 pF	30.0 nH	12.0 pF	18.0 nH
315 MHz	150.0 nH	15.0 pF	47.0 nH	15.0 pF	39.0 nH	15.0 pF	30.0 nH

13.4 Microcontroller Connection

If the FIFO is not desired to be used and minimizing microcontroller pins is important in the application then the SPI interfance pins may be used in the following fashion to send/read the data from the transceiver. If it is desired to use the chip in this mode, please contact customer support for further instructions.



14 REFERENCE MATERIAL

14.1 Complete Register Table and Descriptions

Table 23: Complete Register Map and Descriptions

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
00	R	Device Type	0	0	0	dt[4] dt	[3] dt	[2]	dt[1] dt	[0]	08h
01 R		Device Version	0	0	0	vc[4]	vc[3]	vc[2]	vc[1]	vc[0]	01h
02 R		Device Status	*ffovfl f*	*funfl*	*rxffem*	*headerr*	*freqerr*	*lockdet*	*cps[1]*	*cps[0]*	-
03	R	Interrupt Status 1	*ifferr itx*	*ffafull*	*itxffaem*	*irxffafull iex*	*t*	*ipksent*	*ipkvalid*	*icrcerror*	-
04	R	Interrupt Status 2	*iswdet ipreaval*		*ipreainval*	*irssi*	*iwut*	*ilbd*	*ichiprdy*	*ipor*	-
05	R/W	Interrupt Enable 1	enfferr	entxffafull	entxffaem	enrxf fafull	enext	enpksent	enpkvalid	encrcerror	00h
06	R/W	Interrupt Enable 2	enswdet	enpreaval	enpreainval	enrssi	enwut	enlbd	enchiprdy	enpor	01h
07	R/W	Operating & Function Control 1	swres	enlbd	enwt	x32ksel	txon	rxon	pllon	xton	01h
08	R/W	Operating & Function Control 2	antdiv[2]	antdiv[1] ant	div[0]	rxmpk	autotx	enldm	ffclrrx	ffclrtx	00h
09	R/W	Crystal Oscillator Load Capacitance		xlc[6]	xlc[5]	xlc[4]	xlc[3]	xlc[2]	xlc[1]	xlc[0]	40h
0A	R/W	Microcontroller Output Clock			clkt[1] clkt	[0]	enlfc	mclk[2]	mclk[1]	mclk[0]	06h
0B R/	W	GPIO0 Configuration	gpio0drv[1]	gpio0drv[0]	pup0	gpio0[4]	gpio0[3]	gpio0[2]	gpio0[1]	gpio0[0]	00h
0C R/	W	GPIO1 Configuration	gpio1drv[1]	gpio1drv[0]	pup1	gpio1[4]	gpio1[3]	gpio1[2]	gpio1[1]	gpio1[0]	00h
0D R/	W	GPIO2 Configuration	gpio2drv[1]	gpio2drv[0]	pup2	gpio2[4]	gpio2[3]	gpio2[2]	gpio2[1]	gpio2[0]	00h
0E	R/W	I/O Port Configuration		*extitst[2] e*	*xtitst[1]*	*extitst[0]*	itsdo dio2		dio1	dio0	00h
0F R/	W	ADC Configuration	adcstart / *adcdone*	adcsel[2]	adcsel[1]	adcsel[0]	adcref[1]	adcref[0]	adcgain[1]	adcgain[0]	00h
10	R/W	ADC Sensor Amplifier Offset					adcoffs[3]	adcoffs[2]	adcoffs[1]	adcoffs[0]	00h
11 R		ADC Value	*adc[7] a*	*dc[6]*	*adc[5]*	*adc[4]*	*adc[3]*	*adc[2]*	*adc[1]*	*adc[0]*	-
12	R/W	Temperature Sensor Control	tsrange[1]	tsrange[0]	entsoffs	entstrim t	strim[3] t	strim[2]	tstrim[1] t	strim[0]	20h
13	R/W	Temperature Value Offset	tvoffs[7]	tvoffs[6]	tvoffs[5]	tvoffs[4] t	voffs[3] t	voffs[2]	tvoffs[1] t	voffs[0]	00h
14	R/W	Wake-Up Timer Period 1			wtr[3]	wtr[2]	wtr[1]	wtr[0]	wtd[1]	wtd[0]	00h
15	R/W	Wake-Up Timer Period 2	wtm[15]	wtm[14]	wtm[13]	wtm[12]	wtm[11]	wtm[10]	wtm[9]	wtm[8]	00h
16	R/W	Wake-Up Timer Period 3	wtm[7]	wtm[6]	wtm[5]	wtm[4]	wtm[3]	wtm[2]	wtm[1]	wtm[0]	00h
17	R	Wake-Up Timer Value 1	*wtv[15]*	*wtv[14]*	*wtv[13] wt*	*v[12] wt*	*v[11] wt*	*v[10]*	*wtv[9]*	*wtv[8]*	-
18	R	Wake-Up Timer Value 2	*wtv[7] wtv*	*[6]*	*wtv[5]*	*wtv[4]*	*wtv[3]*	*wtv[2]*	*wtv[1]*	*wtv[0]*	-

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
19	R/W	Low-Duty Cycle Mode Duration	ldc[7]	ldc[6]	ldc[5]	ldc[4]	ldc[3]	ldc[2]	ldc[1]	ldc[0]	00h
1A	R/W	Low Battery Detector Threshold				lbdt[4]	lbdt[3]	lbdt[2]	lbdt[1]	lbdt[0]	14h
1B	R	Battery Voltage Level	*0*	*0*	*0*	*vbat[4] v*	*bat[3] v*	*bat[2]*	*vbat[1] v*	*bat[0]*	-
1C	R/W	IF Filter Bandwidth	bypdec3	ndec[2]	ndec[1]	ndec[0]	filset[3]	filset[2]	filset[1]	filset[0]	16h
1D	R/W	AFC Loop Gearshift Override		enafc	afcgearh[2]	afcgearh[1]	af cgearh[0]	afcgearl[2]	afcgearl[1]	afcgearl[0]	41h
1E	R/W	AFC Timing Control			shwait[2]	shwait[1]	shwait[0]	lgwait[2]	lgwait[1]	lgwait[0]	1Ch
1F	R/W	Clock Recovery Gearshift Override		rxready	crfast[2]	crfast[1]	crfast[0]	crslow[2]	crslow[1]	crslow[0]	13h
20	R/W	Clock Recovery Oversampling Ratio	rxosr[7]	rxosr[6]	rxosr[5]	rxosr[4]	rxosr[3]	rx osr[2]	rxosr[1]	rxosr[0]	30h
21	R/W	Clock Recovery Offset 2	rxosr[10]	rxosr[9]	rxosr[8]	X	ncoff[19]	ncoff[18]	ncoff[17]	ncoff[16]	02h
22	R/W	Clock Recovery Offset 1	ncoff[15]	ncoff[14]	ncoff[13]	ncoff[12]	ncoff[11]	ncoff[10]	ncoff[9]	ncoff[8]	AAh
23	R/W	Clock Recovery Offset 0	ncoff[7]	ncoff[6]	ncoff[5]	ncoff[4]	ncoff[3]	ncoff[2]	ncoff[1]	ncoff[0]	ABh
24	R/W	Clock Recovery Timing Loop Gain 1						crgain[10]	crgain[9]	crgain[8]	02h
25	R/W	Clock Recovery Timing Loop Gain 0	crgain[7]	crgain[6]	crgain[5]	crgain[4]	crgain[3]	crgain[2]	crgain[1]	crgain[0]	53h
26	R	Received Signal Strength Indicator rssi[	7]	rssi[6]	rssi[5]	rssi[4]	rssi[3]	rssi[2]	rssi[1]	rssi[0]	-
27 R/	W	RSSI Threshold for Clear Channel Indicator	rssith[7]	rssith[6]	rssith[5]	rssit h[4]	r ssith[3]	rssit h[2]	rssith[1]	rssit h[0]	00h
28	R/W	Reserved 1	X	X	X X X X				X	X	00h
29	R	Antenna Diversity Register 1	*adrssi1[7]*	*adrssia[6]*	*adrssia[5]*	*adrssia[4]*	*adrssia[3]*	*adrssia[2]*	*adrssia[1]*	*adrssia[0]*	-
2A	R	Antenna Diversity Register 2	*adrssib[7]*	*adrssib[6]*	*adrssib[5]*	*adrssib[4]*	*adrssib[3]*	*adrssib[2]*	*adrssib[1]*	*adrssib[0]*	-
30	R/W	Data Access Control	enpacrx	lsbfrst	crcdonly	autophdet	enpactx	encrc	crc[1]	crc[0]	1Dh
31	R	EzMAC status	0	0	pksrch	pkrx	pkvalid	crcerror	pktx	pksent	-
32	R/W	Header Control 1	enbcast[1]	enbcast[1]	enbcast[1]	enbcast[0]	hdch[3]	hdch[2]	hdch[1]	hdch[0]	0Ch
33	R/W	Header Control 2		txhdlen[2]	txhdlen[1]	txhdlen[0]	f ixpklen	synclen[1]	synclen[0]	prealen[8]	22h
34 R/	W	Preamble Length	prealen[7]	prealen[6]	prealen[5]	preal en[4]	prealen[3]	prealen[2]	prealen[1]	prealen[0]	07h
35 R/	W	Preamble Detection Control	preath[4]	preat h[3]	preath[2]	preath[1]	preath[0]	preach[2]	preach[1]	preach[0]	40h
36	R/W	Sync Word 3	sync[31]	sync[30]	sync[29]	sync[28]	sync[27]	sync[26]	sync[25]	sync[24]	2Dh
37	R/W	Sync Word 2	sync[23]	sync[22]	sync[21]	sync[20]	sync[19]	sync[18]	sync[17]	sync[16]	D4h
38	R/W	Sync Word 1	sync[15]	sync[14]	sync[13]	sync[12]	sync[11]	sync[10]	sync[9]	sync[8]	00h
39	R/W	Sync Word 0	sync[7]	sync[6]	sync[5]	sync[4]	sync[3]	sync[2]	sync[1]	sync[0]	00h
3A	R/W	Transmit Header 3	txhd[31]	txhd[30]	txhd[29]	t xhd[28]	t xhd[27]	t xhd[26]	txhd[25]	txhd[24]	00h

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
3B	R/W	Transmit Header 2	txhd[23]	txhd[22]	txhd[21] t	xhd[20] t	xhd[19] t	xhd[18]	txhd[17]	txhd[16]	00h
3C	R/W	Transmit Header 1	txhd[15]	txhd[14]	txhd[13] t	xhd[12] t	xhd[11] t	xhd[10]	txhd[9]	txhd[8]	00h
3D	R/W	Transmit Header 0	txhd[7]	txhd[6]	txhd[5] t	xhd[4] t	xhd[3] t	xhd[2]	txhd[1]	txhd[0]	00h
3E	R/W	Transmit Packet Length	pklen[7]	pklen[6]	pklen[5]	pklen[4]	pklen[3]	pklen[2]	pklen[1]	pklen[0]	00h
3F	R/W	Check Header 3	chhd[31]	chhd[30]	chhd[29]	chhd[28]	chhd[27]	chhd[26]	chhd[25]	chhd[24]	00h
40	R/W	Check Header 2	chhd[23]	chhd[22]	chhd[21]	chhd[20]	chhd[19]	chhd[18]	chhd[17]	chhd[16]	00h
41	R/W	Check Header 1	chhd[15]	chhd[14]	chhd[13]	chhd[12]	chhd[11]	chhd[10]	chhd[9]	chhd[8]	00h
42	R/W	Check Header 0	chhd[7]	chhd[6]	chhd[5]	chhd[4]	chhd[3]	chhd[2]	chhd[1]	chhd[0]	00h
43	R/W	Header Enable 3	hden[31]	hden[30]	hden[29]	hden[28]	hden[27]	hden[26]	hden[25]	hden[24]	FFh
44	R/W	Header Enable 2	hden[23]	hden[22]	hden[21]	hden[20]	hden[19]	hden[18]	hden[17]	hden[16]	FFh
45	R/W	Header Enable 1	hden[15]	hden[14]	hden[13]	hden[12]	hden[11]	hden[10]	hden[9]	hden[8]	FFh
46	R/W	Header Enable 0	hden[7]	hden[6]	hden[5]	hden[4]	hden[3]	hden[2]	hden[1]	hden[0]	FFh
47	R	Received Header 3	rxhd[31]	rxhd[30]	rxhd[29]	rxhd[28]	rxhd[27]	rxhd[26]	rxhd[25]	rxhd[24]	-
48 R		Received Header 2	rxhd[23]	rxhd[22]	rxhd[21]	rxhd[20]	rxhd[19]	rxhd[18]	rxhd[17]	rxhd[16]	-
49 R		Received Header 1	rxhd[15]	rxhd[14]	rxhd[13]	rxhd[12]	rxhd[11]	rxhd[10]	rxhd[9]	rxhd[8]	-
4A R		Received Header 0	rxhd[7]	rxhd[6]	rxhd[5]	rxhd[4]	rxhd[3]	rxhd[2]	rxhd[1]	rxhd[0]	-
4B	R	Received Packet Length	rxplen[7]	rxplen[6]	rxplen[5]	rxplen[4]	rxplen[3]	rxplen[2]	rxplen[1]	rxplen[0]	-
50	R/W	Analog Test Bus				atb[4]	atb[3]	atb[2]	atb[1]	atb[0]	00h
51	R/W	Digital Test Bus		ensctest	dtb[5] dt	b[4] dt	b[3] dt	b[2]	dtb[1]	dtb[0]	00h
52	R/W	TX Ramp Control		txmod[2]	txmod[1]	txmod[0]	ldoramp[1]	ldoramp[0]	txramp[1]	txramp[0]	20h
53	R/W	PLL Tune Time	pllts[4]	pllts[3]	pllts[2]	pllts[1]	pllts[0]	pllt0[2]	pllt0[1]	pllt0[0]	45h
54	R/W	Reserved 1	X	X	X X X X				X	X	00h
55 R/	W	Calibration Control			*adccaldone*	enrcfcal rccal		vcocaldp	vcocal	skipvco	04h
56 R/	W	Modem Test					preabp ret	clksel	refclkinv	iqswitch	00h
57	R/W	Chargepump Test			cpforceup	cpforcedn	cdconly	cdccur[2]	cdccur[1]	cdccur[0]	00h
58 R/	W	Chargepump Current Trimming / Override	cpcurr[1]	cpcurr[0]	cpcorrov	cpcorr[4]	cpcorr[3]	cpcorr[2]	cpcorr[1]	cpcorr[0]	80h
59	R/W	Divider Current Trimming		fbdivhc	d3trim[1]	d3t rim[0]	d2t rim[1]	d2t rim[0]	d1p5trim[1]	d1p5trim[0]	00h
5A	R/W	VCO Current Trimming		vcocorrov	vcocorr[3]	vcocorr[2]	vcocorr[1]	vcocorr[0]	vcocur[1]	vcocur[0]	03h
5B	R/W	VCO Calibration / Override	vcocalov / *vcdone*	vcocal[6]	vcocal[5]	vcocal[4]	vcocal[3]	vcocal[2]	vcocal[1]	vcocal[0]	00h

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
5C	R/W	Synthesizer Test		*vcotype*	enoloop	dsmod	dsorder[1]	dsorder[0]	dsrst	mod dsrst	0Eh
5D	R/W	Block Enable Override 1	enmix	enlna	enpga	enpa	enbf5	endv32	enbf12	enmx2	00h
5E	R/W	Block Enable Override 2	ends	enldet	enmx3	enbf4	enbf3	enbf11	enbf2	enmx1	00h
5F	R/W	Block Enable Override 3	enfrdv	endv31	endv2	endv1p5	dvbshunt	envco	encp	enbg	00h
60	R/W	Channel Filter Coefficient Address					chfiladd[3]	chf iladd[2]	chfiladd[1]	chfiladd[0]	00h
61	R/W	Channel Filter Coefficient Value			chfilval[5]	chfilval[4]	chf ilval[3]	chfilval[2]	chfilval[1]	chfilval[0]	00h
62	R/W	Crystal Oscillator / Control Test	*pwst[2] p*	*wst[1]*	*pwst[0]*	clkhyst	enbias2x	enamp2x	bufovr	enbuf	24h
63 R/	W	RC Oscillator Coarse Calibration / Override	rccov	rcc[6]	rcc[5]	rcc[4]	rcc[3]	rcc[2]	rcc[1]	rcc[0]	00h
64 R/	W	RC Oscillator Fine Calibration / Override	rcfov	rcf[6]	rcf [5]	rcf [4]	rcf [3]	rcf [2]	rcf[1]	rcf [0]	00h
65	R/W	LDO Control Override	enspor	enbias	envcoldo	enifldo	enrfldo	enpllldo	endigldo	endigpwdn	81h
66	R/W	Reserved 2	X	X	X X X X				X	X	00h
67	R/W	Deltasigma ADC Tuning 1	adcrst	enrefdac	enadc	adctuneovr	adctune[3]	adctune[2]	adctune[1]	adctune[0]	00h
68	R/W	Deltasigma ADC Tuning 2				envcm	adcoloop	adcref[2]	adcref[1]	adcref[0]	00h
69	R/W	AGC Override 1			agcen	lnagain	pga3	pga2	pga1	pga0	20h
6A	R/W	AGC Override 2		agcslow	lnacomp[3]	lnacomp[2]	lnacomp[1]	lnacomp[0]	pgath[1]	pgath[0]	01h
6B	R/W	GFSK FIR Filter Coefficient Address						firadd[2]	firadd[1]	firadd[0]	00h
6C	R/W	GFSK FIR Filter Coefficient Value			firval[5]	firval[4]	firval[3]	irval[2]	firval[1]	firval[0]	01h
6D R/W		TX Power						txpow[2]	txpow[1]	txpow[0]	03h
6E	R/W	TX Data Rate 1	txdr[15]	txdr[14]	txdr[13]	xdr[12]	xdr[11]	xdr[10]	txdr[9]	txdr[8]	0Ah
6F	R/W	TX Data Rate 0	txdr[7]	txdr[6]	txdr[5]	txdr[4]	txdr[3]	txdr[2]	txdr[1]	txdr[0]	AAh
70	R/W	Modulation Mode Control 1						enmaninv	enmanch	enwhite	04h
71	R/W	Modulation Mode Control 2	trclk[1]	trclk[0]	dtmod[1]	mod[0]	eninv	-	modtyp[1]	modtyp[0]	00h
72	R/W	Frequency Deviation	fd[7]	fd[6]	d[5]	d[4]	d[3]	d[2]	fd[1]	d[0]	43h
73	R/W	Frequency Offset	fo[7]	fo[6]	o[5]	o[4]	o[3]	o[2]	fo[1]	o[0]	00h
74	R/W	Frequency Channel Control							fo[9]	fo[8]	00h
75	R/W	Frequency Band Select		-	hbsel	fb[4]	b[3]	b[2]	fb[1]	b[0]	35h
76	R/W	Nominal Carrier Frequency 1	fc[15]	fc[14]	fc[13]	fc[12]	fc[11]	fc[10]	fc[9]	fc[8]	BBh
77	R/W	Nominal Carrier Frequency 0	fc[7]	fc[6]	c[5]	c[4]	c[3]	c[2]	fc[1]	c[0]	80h
79	R/W	Frequency Hopping Channel Select	fhch[7]	fhch[6]	fhch[5]	fhch[4]	fhch[3]	fhch[2]	fhch[1]	fhch[0]	00h

Address	R / W	Function / Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
7A	R/W	Frequency Hopping Step Size	fhs[7]	fhs[6]	fhs[5]	fhs[4]	fhs[3]	fhs[2]	fhs[1]	fhs[0]	00h
7C	R/W	TX FIFO Control 1			txafthr[5]	txafthr[4]	txafthr[3]	txafthr[2]	txafthr[1]	txafthr[0]	37h
7D	R/W	TX FIFO Control 2			txaethr[5]	txaethr[4] t	xaethr[3]	txaethr[2]	txaethr[1]	txaethr[0]	04h
7E	R/W	RX FIFO Control			rxafthr[5]	rxafthr[4]	rxafthr[3] rxaf	thr[2]	rxafthr[1] rxaf	thr[0]	37h
7F	R/W	FIFO Access	fifod[7]	fifod[6]	fifod[5] f	ifod[4]	fifod[3] f	ifod[2]	fifod[1]	fifod[0]	-

Address: 00h – Device Type Code (DT)

Bit	R/W	Default	Function
[7:5]	R	0	RESERVED
[4:0]	R	01000	**dt[4:0]** = Device Type Code. This internally hardwired code will allow the user to recognize whether this is a Transmitter, Receiver, or a Transceiver. Ara = 01000.

Address: 01h –Version Code (VC)

Bit	R/W	Default	Function
[7:5]	R	0	RESERVED
[4:0]	R	0001	**vc[4:0]** = Version Code. Internally hardwired version code of the chip

Address: 02h – Device Status

Bit	R/W	Default	Function
7	R	-	**ffovfl** = RX/TX FIFO Overflow status.
6	R	-	**ffunfl** = RX/TX FIFO Underflow status.
5	R	-	**rxffem** = RX FIFO Empty status.
4	R	-	**headerr** = Header Error status. The actual received packet has a header check error.
3	R	-	**freqerr** = Frequency Error status. The programmed frequency is outside of the operating range. The actual frequency is saturated to the max/min value.
2	R	-	**lockdet** = Synthesizer Lock Detect status.
[1:0]	R	-	**cps[1:0]** = Chip Power State: 00 – Idle State 01 – RX State 10 – TX State

Address: 03h – Interrupt / Status 1

When any of the following bits change state from '0' to '1' the control block will notify the micro-controller by setting the nIRQ pin LOW = '0' if it is enabled in the Interrupt Enable 1 register. The nIRQ pin will go to HIGH and all the ***enabled*** interrupt bits will be cleared when the microcontroller reads this address. If any of these bits is not enabled in the Interrupt Enable 1 register then it becomes a status signal that can be read anytime in the same location and will not be cleared by reading the register.

Bit	R/W	Default	Function
[7] R		-	**ifferr** = FIFO Underflow/Overflow Error. When set to '1' the TX or RX FIFO has overflowed or underflowed.
[6] R		-	**itxffafull** = TX FIFO Almost Full. When set to '1' the TX FIFO has met its almost full threshold and needs to be transmitted.
[5] R		-	**itxffaem**= TX FIFO Almost Empty. When set to '1' the TX FIFO is almost empty and needs to be filled.
[4] R		-	**irxffafull** = RX FIFO Almost Full. When set to '1' the RX FIFO has met its almost full threshold and needs to be read by the microcontroller
[3] R		-	**iext** = External Interrupt. When set to '1' an interrupt occurred on one of the GPIO's if it is programmed so. The status can be checked in register 0Eh. See GPIOx Configuration section for the details.
[2] R		-	**ipksent** = Packet Sent Interrupt. When set to'1' a valid packet has been transmitted.
[1] R		-	**ipkvalid** = Valid Packet Received. When set to '1' a valid packet has been received.
[0] R		-	**icrcerror** = CRC Error. When set to '1' the cyclic redundancy check is failed.

When does the individual Status bits get Set/Cleared, if not enabled as an Interrupt?

Bit	Status Name	Set/Clear conditions:
[7]	**ifferr**	Set if there is a Tx or RX FIFO Overflow or Underflow. It is cleared only by applying FIFO reset to the specific FIFO that caused the condition.
[6]	**itxffafull**	Will be set when the number of bytes written to TX FIFO is greater than the Almost Full threshold set by SPI. It is automatically cleared when we start transmitting and the FIFO data is read out and the number of bytes left in the FIFO is smaller or equal to the threshold).
[5]	**itxffaem**	Will be set when the number of bytes (not yet transmitted) in TX FIFO is smaller or equal than the Almost Empty threshold set by SPI. It is automatically cleared when we write enough data to TX FIFO so that the number of data bytes not yet transmitted is above the Almost Empty threshold.
[4]	**irxffafull**	Will be set when the number of bytes received (and not yet read-out) in RX FIFO is greater than the Almost Full threshold set by SPI. It is automatically cleared when we read enough data from RX FIFO so that the number of data bytes not yet read is below the Almost Full threshold.
[3]	**iext**	External interrupt source
[2]	**ipksent**	Will go high once a packet is sent all the way through (no TX abort). This status will be cleaned if 1) We leave FIFO mode or 2) In FIFO mode we start a new transmission.
[1]	**ipkvalid**	Goes high once a packet is fully received (no RX abort). It is automatically cleaned once we receive and acknowledge the Sync Word for the next packet.
[0]	**icrcerror**	Goes High once the CRC computed during RX differs from the CRC sent in the packet by the TX. It is cleaned once we start receiving new data in the next packet.

Address: 04h – Interrupt or Status 2

When any of the following bits change state from '0' to '1' the control block will notify the micro-controller by setting the nIRQ pin LOW = '0' if it is enabled in the Interrupt Enable 2 register. The nIRQ pin will go to HIGH and all the ***enabled*** interrupt bits will be cleared when the microcontroller reads this address. If any of these bits is not enabled in the Interrupt Enable 2 register then it becomes a status signal that can be read anytime in the same location and will not be cleared by reading the register.

Bit	R/W	Default	Function
[7] R		-	**iswdet** = Sync Word Detected. When a sync word is detected this bit will be set to 1.
[6] R		-	**ipreaval** = Valid Preamble Detected. When a preamble is detected this bit will be set to 1.
[5] R		-	**ipreainval** = Invalid Preamble Detected. When the preamble is not found within a period of time after the RX is enabled, this bit will be set to 1.
[4] R		-	**irssi** = RSSI. When RSSI level exceeds the programmed thershold this bit will be set to 1.
[3] R		-	**iwut** = Wake-Up-Timer. On the expiration of programmed wake-up timer this bit will be set to 1.
[2] R		-	**ilbd** = Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled.
[1] R		-	**ichiprdy** = Chip Ready (XTAL). When a chip ready event has been detected this bit will be set to 1.
[0] R		-	**ipor** = Power-on-Reset (POR). When the chip detectes a Power on Reset above the desired setting this bit will be set to 1.

When does the individual Status bits get Set/Cleared, if not enabled as an Interrupt?

Bit	Status Name	Set/Clear conditions:
[7]	**iswdet**	Goes high once the Sync Word is detected. Goes low once we are done receiving the current packet.
[6]	**ipreaval**	Goes high once the preamble is detected. Goes low once the sync is detected or the RX wait for the sync times-out.
[5]	**ipreainval**	Self cleaning, user should use this as an interrupt source rather than a status.
[4]	**irssi**	Should remain high as long as the RSSI value is above programmed threshold level
[3]	**iwut**	Wake time timer interrupt. Use as an interrupt, not as a status.
[2]	**ilbd**	Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. Probably the status is cleared once the battery is replaced.
[1]	**ichiprdy**	Chip ready goes high once we enable the xtal, Tx or RX and a settling time for the Xtal clock elapses. The status stay high unless we go back to Idle mode.
[0]	**ipor**	Power on status.

Address: 05h – Interrupt Enable 1

Bit R/W	Default	Function
[7] R/W	0	**enfferr** = Enable FIFO Underflow/Overflow. When set to '1' the FIFO Underflow/Overflow interrupt will be enabled.
[6] R/W	0	**entxffafull** = Enable TX FIFO Almost Full. When set to '1' the TX FIFO Almost Full interrupt will be enabled.
[5] R/W	0	**entxffaem** = Enable TX FIFO Almost Empty. When set to '1' the TX FIFO Almost Empty interrupt will be enabled.
[4] R/W	0	**enrxffafull** = Enable RX FIFO Almost Full. When set to '1' the RX FIFO Almost Full interrupt will be enabled.
[3] R/W	0	**enext** = Enable External Interrupt. When set to '1' the External Interrupt will be enabled.
[2] R/W	0	**enpksent** = Enable Packet Sent. When ipksent ='1' the Packet Sense Interrupt will be enabled.
[1] R/W	0	**enpkvalid** = Enable Valid Packet Received. When ipkvalid = '1' the Valid Packet Received Interrupt will be enabled
[0] R/W	0	**encrcerror** = Enable CRC Error. When set to '1' the CRC Error interrupt will be enabled.

Address: 06h – Interrupt Enable 2

Bit R/W	Default	Function
[7] R	0	**enswdet** = Enable Sync Word Detected. When mpreadet ='1' the Preamble Detected Interrupt will be enabled.
[6] R	0	**enpreaval** = Enable Valid Preamble Detected. When mpreadet ='1' the Valid Preamble Detected Interrupt will be enabled.
[5] R	0	**enpreainval** = Enable Invalid Preamble Detected. When mpreadet ='1' the Invalid Preamble Detected Interrupt will be enabled.
[4] R	0	**enrssi** = Enable RSSI. When set to '1' the RSSI Interrupt will be enabled.
[3] R/W	0	**enwut** = Enable Wake-Up Timer. When set to '1' the Wake-Up Timer interrupt will be enabled.
[2] R/W	0	**enlbd** = Enable Low Battery Detect. When set to '1' the Low Battery Detect interrupt will be enabled.
[1] R/W	1	**enchiprdy** = Enable Chip Ready (XTAL). When set to '1' the Chip Ready interrupt will be enabled.
[0] R/W	1	**enpor** = Enable POR. When set to '1' the POR interrupt will be enabled.

Address: 07h – Operating Mode & Function Control 1

Bit	R/W	Default	Function
7 R/W		0	**swres** = Software Register Reset bit. This bit may be used to reset all SPI registers simultaneously to a DEFAULT state, without the need for sequentially writing to each individual register. The RESET is accomplished by setting swres = '1'. This bit will be automatically cleared.
6	R/W	0	**enlbd** = Enable Low Battery Detect. When this bit is set to '1' the Low Battery Detector circuit and threshold comparison will be enabled.
5 R/W		0	**enwt** = Enable Wake-Up-Timer. When this function will be enabled when enwt = '1'. If the Wake-up-Timer function is enabled it will operate in any mode and notify the microcontroller through the GPIO interrupt when the timer expires.
4	R/W	0	**x32ksel** = 32,768 kHz crystal oscillator select. The source of the 32kHz clock is the watch crystal oscillator instead of the RC oscillator if this bit is set.
3	R/W	0	**txon =** TX on to enable Transmit mode
2	R/W	0	**rxon =** RX on to enable Receiver mode.
1 R/W		0	**pllon =** TUNE Mode (PLL is ON). When pllon = '1' the PLL will remain enabled in Idle State. This will for faster turn-around time at the cost of increased current consumption in Idle State.
0	R/W	1	**xton =** READY Mode (Xtal is ON).

Address: 08h – Operating Mode & Function Control 2

Bit	R/W	Default	Function
[7:5]	R/W	000	**antdiv[2:0] =** Enable Antenna Diversity. The GPIO must be configured for Antenna Diversity for the algorithm to work properly. RX/TX state: GPIO Ant1 / GPIO Ant2 — non RX/TX state: GPIO Ant1 / GPIO Ant2 000 – 1 / 0 — 0 / 0 001 – 0 / 1 — 0 / 0 010 – 1 / 0 — 1 / 1 011 – 0 / 1 — 1 / 1 100 – antenna diversity algorythm — 0 / 0 101 – antenna diversity algorythm — 1 / 1 110 – ant. div. algorythm in beacon mode — 0 / 0 111 – ant. div. algorythm in beacon mode — 1 / 1
4	R/W	0	**rxmpk** = RX Multi Packet. When the chip is selected to use FIFO Mode (dtmod[1:0]) and RX Packet Handling (enpacrx) then it will fill up the FIFO with multiple valid packets if this bit is set, otherwise the transceiver will automatically leaves the RX State after the first valid packet has been received.
3	R/W	0	**autotx** = Automatic Transmission. When autotx = '1' the transceiver will enter automatically TX State when the FIFO is almost full. When the FIFO is empty it will automatically return to the Idle State.
2	R/W	0	**enldm =** Enable Low Duty Cycle Mode. If this bit is set to '1' then the chip turns on the RX regularly. The frequency should be set in the Wake-Up Timer Period register, while the minimum ON time should be set in the Low-Duty Cycle Mode Duration register. The FIFO mode should be enabled also.
1	R/W	0	**ffclrrx** = RX FIFO Clear. Setting ffclrrx='1' will clear the contents of the RX FIFO.
0	R/W	0	**ffclrtx** = TX FIFO Clear. Setting ffclrtx='1' will clear the contents of the TX FIFO.

Address: 09h – 30MHz Crystal Oscillator Load Capacitance

Bit	R/W	Default	Function
7	R	-	RESERVED
[6:0]	R	40h	**xlc[6:0]** = Tuning Capacitance for the 30MHz XTAL

Address: 0Ah – Microcontroller Output Clock

Bit R/W	Default	Function
[7:6] R	-	RESERVED
[5:4] R/W	00	**clkt[1:0] =** Clock Tail. If enlfc = '0' then it can be useful to provide a few extra cycles for the microcontroller to complete its operation. Setting the clkt[1:0] register will provide the addition cycles of the clock before it shuts off. 00 – 0 cycle 01 – 128 cycles 10 – 256 cycles 11 – 512 cycles
3 R/W	0	**enlfc =** Enable Low Frequency Clock. When enlfc = '1' and the chip is in Sleep mode then the 32.768kHz clock will be provided to the Microcontroller no matter what the selection of mclk[2:0] is. For example if mclk[2:0] = '000', 30MHz will be available through the GPIO to output to the Microctroller in all Idle, TX, or RX states. When the chip is commanded to Sleep mode the 30MHz clock will become 32.768kHz.
[2:0] R/W	110	**mclk[2:0] =** Microcontroller Clock. Different clock frequencies may be selected for configurable GPIO clock output. All clock frequencies are created by dividing the XTAL except for the 32kHz clock which comes directly from the 32kHz RC Oscillator. The mclk[2:0] setting is only valid when xton = '1' except the '111'. 000 – 30 MHz 001 – 15 MHz 010 – 10 MHz 011 – 4 MHz 100 – 3 MHz 101 – 2 MHz 110 – 1 MHz 111 – 32.768 kHz

Address: 0Bh – GPIO Configuration 0

Bit	R/W	Default	Function
[7:6]	R	-	RESERVED
5	R/W	0	**pup0 =** Pull-up Resistor enable on GPIO0. When set to '1' the a 200 kohm resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.
[4:0]	R/W	0000	**gpio1[4:0] =** GPIO0pin function select: 00000 – Power-On-Reset (output) 00001 – Wake-Up Timer: '1' when WUT has expired (output) 00010 – Low Battery Detect: '1' when battery is below threshold setting (output) 00011 – Direct Digital Input 00100 – External Interrupt, falling edge (input) 00101 – External Interrupt, rising edge (input) 00110 – External Interrupt, state change (input) 00111 – ADC Analog Input 01000 – Reserved (Analog Test N Intput) 01001 – Reserved (Analog Test P Intput) 01010 – Direct Digital Output 01011 – Reserved (Digital Test Output) 01100 – Reserved (Analog Test N Output) 01101 – Reserved (Analog Test P Output) 01110 – Reference Voltage (output) 01111 – TX Data CLK output to be used in conjunction with TX Data pin (output) 10000 – TX Data input for direct modulation (input) 10001 – External Retransmission Request (input) 10010 – TX State (output) 10011 – TX FIFO Almost Full (output) 10100 – RX Data (output) 10101 – RX State (output) 10110 – RX FIFO Almost Full (output) 10111 – Antenna 1 Switch used for antenna diversity (output) 11000 – Antenna 2 Switch used for antenna diversity (output) 11001 – Valid Preamble Detected (output) 11010 – Invalid Preamble Detected (output) 11011 – Sync Word Detected (output) 11100 – Clear Channel Assessement (output) 11101 – VDD else – GND

Address: 0Ch – GPIO Configuration 1

Bit	R/W	Default	Function
[7:6]	R	-	RESERVED
5	R/W	0	**pup1** = Pull-up Resistor enable on GPIO1. When set to '1' the a 200 kohm resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.
[4:0]	R/W	0000	**gpio1[4:0]** = GPIO1 pin function select: 00000 – Power-On-Reset Inverted (output) 00001 – Wake-Up Timer: '1' when WUT has expired (output) 00010 – Low Battery Detect: '1' when battery is below threshold setting (output) 00011 – Direct Digital Input 00100 – External Interrupt, falling edge (input) 00101 – External Interrupt, rising edge (input) 00110 – External Interrupt, state change (input) 00111 – ADC Analog Input 01000 – Reserved (Analog Test N Intput) 01001 – Reserved (Analog Test P Intput) 01010 – Direct Digital Output 01011 – Reserved (Digital Test Output) 01100 – Reserved (Analog Test N Output) 01101 – Reserved (Analog Test P Output) 01110 – Reference Voltage (output) 01111 – TX Data CLK output to be used in conjunction with TX Data pin (output) 10000 – TX Data input for direct modulation (input) 10001 – External Retransmission Request (input) 10010 – TX State (output) 10011 – TX FIFO Almost Full (output) 10100 – RX Data (output) 10101 – RX State (output) 10110 – RX FIFO Almost Full (output) 10111 – Antenna 1 Switch used for antenna diversity (output) 11000 – Antenna 2 Switch used for antenna diversity (output) 11001 – Valid Preamble Detected (output) 11010 – Invalid Preamble Detected (output) 11011 – Sync Word Detected (output) 11100 – Clear Channel Assessement (output) 11101 – VDD else – GND

Address: 0Dh – GPIO Configuration 2

Bit	R/W	Default	Function
[7:6]	R	-	RESERVED
5	R/W	0	**pup2** = Pull-up Resistor enable on GPIO2. When set to '1' the a 200 kohm resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.
[4:0]	R/W	0000	**gpio2[4:0]** = GPIO2 pin function select: 00000 – Microcontroller Clock (output) 00001 – Wake-Up Timer: '1' when WUT has expired (output) 00010 – Low Battery Detect: '1' when battery is below threshold setting (output) 00011 – Direct Digital Input 00100 – External Interrupt, falling edge (input) 00101 – External Interrupt, rising edge (input) 00110 – External Interrupt, state change (input) 00111 – ADC Analog Input 01000 – Reserved (Analog Test N Intput) 01001 – Reserved (Analog Test P Intput) 01010 – Direct Digital Output 01011 – Reserved (Digital Test Output) 01100 – Reserved (Analog Test N Output) 01101 – Reserved (Analog Test P Output) 01110 – Reference Voltage (output) 01111 – TX Data CLK output to be used in conjunction with TX Data pin (output) 10000 – TX Data input for direct modulation (input) 10001 – External Retransmission Request (input) 10010 – TX State (output) 10011 – TX FIFO Almost Full (output) 10100 – RX Data (output) 10101 – RX State (output) 10110 – RX FIFO Almost Full (output) 10111 – Antenna 1 Switch used for antenna diversity (output) 11000 – Antenna 2 Switch used for antenna diversity (output) 11001 – Valid Preamble Detected (output) 11010 – Invalid Preamble Detected (output) 11011 – Sync Word Detected (output) 11100 – Clear Channel Assessement (output) 11101 – VDD else – GND

Address: 0Eh – I/O Port Configuration

Bit	R/W	Default	Function
7	R	0	RESERVED
6	R	0	**extitst[2]** = External Interrupt Status. If the GPIO2 is programmed to be external interrupt sources then the status can be read here.
5	R	0	**extitst[1]** = External Interrupt Status. If the GPIO1 is programmed to be external interrupt sources then the status can be read here.
4	R	0	**extitst[0]** = External Interrupt Status. If the GPIO0 is programmed to be external interrupt sources then the status can be read here.
3	R/W	0	**itsdo** = Interrupt Request Output on the SDO Pin. nIRQ output is present on the SDO pin if this bit is set and the nSEL input is inactive (high).
2	R/W	0	**dio2** = Direct I/O for GPIO2. If the GPIO2 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO2 is configured to be a direct input then the value of the pin can be read here.
1	R/W	0	**dio1** = Direct I/O for GPIO1. If the GPIO1 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO1 is configured to be a direct input then the value of the pin can be read here.
0	R/W	0	**dio0** = Direct I/O for GPIO0. If the GPIO0 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO0 is configured to be a direct input then the value of the pin can be read here.

Address: 0Fh – ADC Configuration

Bit	R/W	Default	Function
7	R/W	0	**adcstart / adcdone** = ADC Measurement Start bit. Reading this bit gives '1' if the ADC measurement cycle has been finished.
[6:4]	R/W	00	**adcsel[2:0]** = ADC Input Source selection. The internal 8 bit ADC input source can be selected as follows: 000 – Internal Temperature Sensor 001 – GPIO0, single-ended 010 – GPIO1, single-ended 011 – GPIO2, single-ended 100 – GPIO0(+) - GPIO1(-), differential 101 – GPIO1(+) - GPIO2(-), differential 110 – GPIO0(+) - GPIO2(-), differential 111 – GND
[3:2]	R/W	00	**adcref[1:0]** = ADC Reference Voltage selection. The reference voltage of the internal 8 bit ADC can be selected as follows: 0X – bandgap voltage (1.2V) 10 – VDD / 3 11 – VDD / 2
[1:0]	R/W	000	**adcgain[1:0]** = ADC Sensor Amplifier Gain selection. The full scale range of the internal 8 bit ADC in differential mode (see adcsel) can be set as follows: adcref[0] = 0: FS = 0.014 * (adcgain[1:0] + 1) * VDD adcref[0] = 1: FS = 0.021 * (adcgain[1:0] + 1) * VDD

Address: 10h – ADC Sensor Amplifier Offset

The offset can be calculated as Offset = adcoffs[2:0] * V_{DD} / 1000; MSB = adcoffs[3] = Sign bit

Bit	R/W	Default	Function
[7:4]	R	-	RESERVED
[3:0]	R/W	00	**adcoffs[3:0]** = ADC Sensor Amplifier Offset. See formula above.

Address: 11h – ADC Value

Bit	R/W	Default	Function
[7:0]	R	-	**adc[7:0]** = Internal 8 bit ADC Output Value.

Address: 12h – Temperature Sensor Calibration

Bit	R/W	Default	Function
[7:6]	R/W	00	**tsrange[1:0]** = Temperature Sensor Range selection (FS range is 0..1024mV) 00 – -40°C .. 64°C (full operating range), with 0.5°C resolution (1 LSB in the 8 bit ADC) 01 – -40°C .. 85°C, with 1°C resolution (1 LSB in the 8 bit ADC) 11 – 0°C .. 85°C, with 0.5°C resolution (1 LSB in the 8 bit ADC) 10 – -40°F .. 216°F, with 1°F resolution (1 LSB in the 8 bit ADC)
5	R/W	1	**entsoffs** = Temperature Sensor Offset to convert from K to ◦C.
4	R/W	0	**entstrim** = Temperature Sensor Trim enable
[3:0]	R/W	0	**tstrim[3:0]** = Temperature Sensor Trim value

Address: 13h – Temperature Value Offset

Bit	R/W	Default	Function
[7:0]	R/W	00	**tvoffs[7:0**] = Temperature Value Offset. This value is added to the measured temperature value. (MSB, tvoffs[8]: sign bit)

Address: 14h – Wake-Up Timer Period 1

The period of the wake-up timer can be calculated as T_{WUT} = (32 * M * 2^{R-D}) / 32.768 [ms]

Bit	R/W	Default	Function
[7:6]	R/W	-	RESERVED
[5:2]	R/W	0	**wtr[3:0]** = Wake Up Timer Exponent (R) value. See formula above.
[1:0]	R/W	0	**wtd[1:0]** = Wake Up Timer Exponent (D) value. See formula above.

Address: 15h – Wake-Up Timer Period 2

Bit	R/W	Default	Function
[7:0]	R/W	0	**wtm[15:8]** = Wake Up Timer Mantissa (M) value. See formula above.

Address: 16h – Wake-Up Timer Period 3

Bit	R/W	Default	Function
[7:0]	R/W	0	**wtm[7:0]** = Wake Up Timer Mantissa (M) value. See formula above.

Address: 17h – Wake-Up Timer Value 1

Bit	R/W	Default	Function
[7:0]	R	-	**wtm[15:8]** = Wake Up Timer Current Mantissa (M) value. See formula above.

Address: 18h – Wake-Up Timer Value 2

Bit	R/W	Default	Function
[7:0]	R	-	**wtm[7:0]** = Wake Up Timer Current Mantissa (M) value. See formula above.

Address: 19h – Low-Duty Cycle Mode Duration

The period of the low-duty cycle ON time can be calculated as T_{LDC_ON} = (32 * LDC * 2^{R-D}) / 32.768 [ms] R and D values are the same as in the wake-up timer setting in register 14h.

Bit	R/W	Default	Function
[7:0]	R/W	0	**ldc[7:0]** = Low-Duty Cycle Mode Duration (LDC). See formula above

Address: 1Ah – Low Battery Detector Threshold

The threshold can be calculated as $V_{threshold}$ = (1.675 + LBDT * 50 mV) $\pm$ 25 mV

Bit	R/W	Default	Function
[7:5]	R	-	RESERVED
[4:0]	R/W	10100	**lbdt[4:0]** = Low Battery Detector Threshold. This threshold is compared to Battery Voltage Level. If the Battery Voltage is less than the threshold the Low Battery Interrupt is set. Default = 2V. See formula above.

Address: 1Bh – Battery Voltage Level

Bit	R/W	Default	Function
[7:5]	R	-	RESERVED
[4:0] R		-	**vbat[4:0]** = Battery Voltage Level. The battery voltage is converted by a 5 bit ADC. In Sleep Mode the register is updated in every 1 s. In other states it measures continouosly.

Address: 1Ch – IF Filter Bandwidth

$$BW = (Rb + 2 \cdot Fd) \cdot k \cdot (1 + MC)$$

Where BW is the required -3dB filter bandwidth of the receiver in kHz, *Rb* is the bit rate in kbps, *Fd* is the frequency deviation of the received GFSK/FSK signal, *MC* is Manchester Coding parameter (*MC* is 1 when enabled, *MC* is 0 when disabled) and *k* is a correction factor depending if GFSK or FSK is received.

- *k* = 1 for FSK
- *k* = 0.9 for GFSK with default Gaussian filter settings (BT = 0.5)

ndec_exp can be calculated from Fd:

$$8\mathrm{Fd} < \frac{500kHz}{2^{ndec\_\exp}} < 16\mathrm{Fd}$$

(Fd = frequency deviation, see Register 72h)

$$filset = 10\ln\left[\frac{Bw \cdot 2^{ndec\_\exp}}{500kHz}\right] + 17.3$$

Bit R/W	Default	Function
7 R/W	0	**bypdec3 –** If set to “1” then the decimate by 3 in the RX Modem will be bypassed
[6:4] R/W	001	**ndec_exp[2:0]** = IF Filter decimation rates
[3:0] R/W	0110	**filset[3:0] =** IF Filter coefficient sets ; defauts are for Rb = 40kbps and Fd = 20kHz so Bw = 80kHz

Address: 1Dh – AFC Loop Gearshift Override

Bit R/W	Default	Function
7 R/W	0	RESERVED
6 R/W	1	**enafc** = AFC enable
[5:3] R/W	000	**afcgearh[2:0]** = AFC High Gear Setting
[2:0] R/W	001	**afcgearl[2:0]** = AFC Low Gear Setting

Address: 1Eh – AFC Timing Control

Bit R/W	Default	Function
[7:6] R	-	RESERVED
[5:3] R/W	3	**shwait[2:0]** = short wait periods after AFC correction used before preamble is detected (unit is $2*T_{bit}$)
[2:0] R/W	4	**lgwait[2:0]** = long wait periods after correction used after preamble detected (unit is $2*T_{bit}$)

Address: 1Fh – Clock Recovery Gearshift Override

Bit R/W	Default	Function
7 R/W	0	RESERVED
6 R/W	0	**rxready** = improves receiver noise immunity when in direct mode. It is recommended to set this bit after preamble is detected. When in FIFO mode this bit should be set to "0" since noise immunity is controlled automatically.
[5:3] R/W	010	**crfast[2:0]** = Clock Recovery Fast Gearshift value
[2:0] R/W	011	**crslow[2:0]** = Clock Recovery Slow Gearshift value

Address: 20h – Clock Recovery Oversampling Rate

The oversampling rate can be calculated as

$$rxosr = \frac{500}{2^{ndec\_\exp-3} \cdot Rb \cdot (1+MC)}$$

Bit R/W		Default	Function
[7:0]	R/W	30h	**rxosr[7:0]** = Oversampling Rate, 3 LSBs are the fraction default = 0011 0000 = 6 clock cycles per data bit

Address: 21h – Clock Recovery Offset 2

The offset can be calculated as

$$ncoff = \frac{RX\_DR \cdot 2^{20+ndec\_\exp}}{500}$$

The default values for register 20h to 23h gives 41.7 kbps RX_DR.

Bit R/W		Default	Function
[7:5] R/W		0	**rxosr[10:8]** = Oversampling Rate, upper bits
4 R/W		0	RESERVED
[3:0] R/W		0010	**ncoff[19:16]** = NCO offset. See formula above.

Address: 22h – Clock Recovery Offset 1

Bit R/W		Default	Function
[7:0]	R/W	AAh	**ncoff[15:8]** = NCO offset. See formula above.

Address: 23h – Clock Recovery Offset 0

Bit R/W		Default	Function
[7:0]	R/W	ABh	**ncoff[7:0]** = NCO offset. See formula above.

Address: 24h – Clock Recovery Timing Loop Gain 1

The loop gain can be calculated as crgain = 2^{16} / (rxosr * h * P), where the modulation index h = 2 * FD / RX_DR.

Bit R/W		Default	Function
[5:3]	R/W	0	RESERVED
[2:0] R/W		010	**crgain[10:8]** = Clock Recovery Timing Loop Gain

Address: 25h – Clock Recovery Timing Loop Gain 0

Bit R/W		Default	Function
[7:0] R/W		53h	**crgain[7:0]** = Clock Recovery Timing Loop Gain

Address: 26h – Received Signal Strength Indicator

Bit	R/W	Default	Function
[7:0]	R	0	**rssi[7:0]** = Received Signal Strength Indicator value

Address: 27h – RSSI Threshold for Clear Channel Indicator

Bit	R/W	Default	Function
[7:0]	R/W	0	**rssith[7:0]** = RSSI Threshold. Interrupt is set if the RSSI value is a bove this threshold.

Address: 28h – Antenna Diversity 1

Bit	R/W	Default	Function
[7:0]	R	0	**adrssi1[7:0]** = Measured RSSI value on antenna 1

Address: 29h – Antenna Diversity 2

Bit	R/W	Default	Function
[7:0]	R	0	**adrssi2[7:0]** = Measured RSSI value on antenna 2

Address: 30h – Data Access Control

Bit R/W	Default	Function
7 R/W	1	**enpacrx** = Enable Packet RX Handling. If FIFO Mode (dtmod='10') is being used automatic packet handling may be enabled. Setting enpacrx='1' will enable automatic packet handling in the RX path. Register 30-4D allow for various configurations of the packet structure. Setting enpacrx='0' will not do any packet handling in the RX path. It will only receive everything after the sync word and fill up the RX FIFO.
6 R/W	0	**lsbfrst** = LSB First enable. The LSB of the data will be transmitted/received first if this bit is set.
5 R/W	0	**crcdonly** = CRC Data Only enable When this bit is set to '1' the CRC is calculated on and check against the packet data fields only.
4 R/W	0	**autophdet** = Auto Phase Detection enable. Automatic Manchester phase detection during RX if this bit is set.
3 R/W	1	**enpactx** = Enable Packet TX Handling. If FIFO Mode (dtmod='10') is being used automatic packet handling may be enabled. Setting enpactx='1' will enable automatic packet handling in the TX path. Register 30-4D allow for various configurations of the packet structure. Setting enpactx='0' will not do any packet handling in the TX path. It will only transmit what is loaded to the FIFO.
2 R/W	1	**encrc** = CRC enable. Cyclic Redundancy Check generation is enabled if this bit is set.
[1:0] R/W	01	**crc[1:0]** = CRC polynomial selection. 00 – CCITT 01 – CRC-16 10 – IEC-16 11 – Biacheva

Address: 31h – EzMAC Status

Bit	R/W	Default	Function
[7:6]	R	0	RESERVED
5	R	0	**pksrch** = Packet Searching. When pksrch = '1' the radio is searching for a valid packet.
4	R	0	**pkrx** = Packet Receiving. When pkrx = '1' the radio is currently receiving a valid packet.
3	R	0	**pkvalid** = Valid Packet Received. When a pkvalid = '1' a valid packet has been received by the receiver. (Same bit as in register 03, but reading it does not reset the IRQ)
2	R	0	**crcerror** = CRC Error. When crcerror = '1' a Cyclic Redundancy Check error has been detected. (Same bit as in register 03, but reading it does not reset the IRQ)
1	R	0	**pktx** = Packet Transmitting. When pktx = '1' the radio is currently transmitting a packet.
0	R	0	**pksent** = Packet Sent. A pksent = '1' a packet has been sent by the radio. (Same bit as in register 03, but reading it does not reset the IRQ)

Address: 32h – Header Control 1

Bit	R/W	Default	Function
[7:4]	R/W	0	**bcen[3:0]** = Broadcast Address (FFh) Check enable. If it is enabled together with Header Byte Check then the header check is OK if the incoming header byte equals with the appropriate check byte *or* FFh). One hot encoding. 0000 – No broadcast address enable. 0001 – Broadcast address enable for header byte 0. 0010 – Broadcast address enable for header byte 1. 0011 – Broadcast address enable for header bytes 0 & 1. 0100 – …
[3:0]	R/W	1100	**hdch[3:0]** = Received Header bytes to be checked against the Check Header bytes. One hot encoding. The receiver will use hdch[2:0] to know the position of the Header Bytes. 0000 – No Received Header check 0001 – Received Header check for byte 0. 0010 – Received Header check for bytes 1. 0011 – Received header check for bytes 0 & 1. 0100 – …

Address: 33h – Header Control 2

Bit R/W	Default	Function
7 R	0	RESERVED
[2:1] R/W	010	**hdlen[2:0]** = Transmit/Receive Header Length. Length of header used if packet handler is enabled for TX (enpactx) or for RX (enpacrx). Headers are sent or received in descending order. 000 – No TX header 001 – Header 3 010 – Header 3 and 2 011 – Header 3 and 2 and 1 100 – Header 3 and 2 and 1 and 0
3 R/W	0	**fixpklen** = Fix Transmit/Receive Packet Length. When fixpklen = '1' the packet length (pklen[7:0]) is not included in the packet structure. When fixpklen = '0' the packet length is included in the packet.
[2:1] R/W	01	**synclen[1:0]** = Synchronization Word Length. The value in this register corresponds to the number of bytes used in the Synchronization Word. The synchronization word bytes are transmitted in descending order. 00 – Synchronization Word 3 01 – Synchronization Word 3 and 2 10 – Synchronization Word 3 and 2 and 1 11 – Synchronization Word 3 and 2 and 1 and 0
0 R/W	0	**prealen[8]** = MSB of Preamble Length. See register Preamble Length.

Address: 34h – Preamble Length

Bit R/W	Default	Function
[7:0] R/W	07h	**prealen[7:0]** = Preamble Length. The value in the prealen[8:0] register + 1 corresponds to the number of nibbles (4 bits) in the packet. For example prealen[8:0] = '00 0001000' corresponds to a preamble length of 32 bits (8*4bits) or 4 Bytes. The maximum preamble length is prealen[8:0] = '111111111' which corresponds to a 255 Bytes Preamble. Writing a value of 0 to this register will have the same effect as 1 and one nibble will be sent.

Address: 35h – Preamble Detection Control 1

Bit R/W	Default	Function
[7:3] R/W	0100	**preath[4:0]** = Number of nibbles processed during detection.
[2:0] R/W	000	**preach[2:0]** = Number of non-consecutive bit errors allowed during detection.

Address: 36h – Synchronization Word 3

Bit R/W	Default	Function
[7:0] R/W	2Dh	**sync[31:24]** = Synchronization Word 3. 4th byte of the synchronization word.

Address: 37h – Synchronization Word 2

Bit	R/W	Default	Function
[7:0]	R/W	D4h	**sync[23:16]** = Synchronization Word 2. 3rd byte of the synchronization word.

Address: 38h – Synchronization Word 1

Bit	R/W	Default	Function
[7:0]	R/W	0	**sync[15:8]** = Synchronization Word 1. 2nd byte of the synchronization word.

Address: 39h – Synchronization Word 0

Bit	R/W	Default	Function
[7:0]	R/W	0	**sync[7:0]** = Synchronization Word 0. 1st byte of the synchronization word.

Address: 3Ah – Transmit Header 3

Bit	R/W	Default	Function
[7:0]	R/W	0	**txhd[31:24]** = Transmit Header 3. 4th byte of the header to be transmitted.

Address: 3Bh – Transmit Header 2

Bit	R/W	Default	Function
[7:0]	R/W	0	**txhd[23:16]** = Transmit Header 2. 3rd byte of the header to be transmitted.

Address: 3Ch – Transmit Header 1

Bit	R/W	Default	Function
[7:0]	R/W	0	**txhd[15:8]** = Transmit Header 1. 2nd byte of the header to be transmitted.

Address: 3Dh – Transmit Header 0

Bit	R/W	Default	Function
[7:0]	R/W	0	**txhd[7:0]** = Transmit Header 0. 1st byte of the header to be transmitted.

Address: 3Eh –Transmit Packet Length

Bit	R/W	Default	Function
[7:0]	R/W	0	**pklen[7:0]** – Packet Length. The value in the pklen[7:0] register corresponds directly to the number of bytes in the Transmit Packet. For example pklen[7:0] = '00001000' corresponds to a packet length of 8 Bytes. The maximum packet length is pklen[7:0] = '11111111', a 255 byte packet. If a '0' is written no data bytes will be sent in the packet structure.

Address: 3Fh – Check Header 3

Check Header bytes 3 to 0 are checked against the corresponding bytes in the Received Header if the check is enabled in the Header Control Register (31h).

Bit	R/W	Default	Function
[7:0]	R/W	0	**chhd[31:24]** = Check Header 3. 4th byte of the check header.

Address: 40h – Check Header 2

Bit	R/W	Default	Function
[7:0]	R/W	0	**chhd[23:16]** = Check Header 2. 3rd byte of the check header.

Address: 41h – Check Header 1

Bit	R/W	Default	Function
[7:0]	R/W	0	**chhd[15:8]** = Check Header 1. 2nd byte of the check header.

Address: 42h – Check Header 0

Bit	R/W	Default	Function
[7:0]	R/W	0	**chhd[7:0]** = Check Header 0. 1st byte of the check header.

Address: 43h –Header Enable 3

Header Enable bytes 3 to 0 control which bits of the Check Header bytes are checked against the corresponding bits in the Received Header. Only those bits are compared where the enable bits are set to 1.

Bit	R/W	Default	Function
[7:0]	R/W	0	**hden[31:24]** = Header Enable 3. 4th byte of the check header.

Address: 44h – Header Enable 2

Bit	R/W	Default	Function
[7:0]	R/W	0	**hden[23:16]** = Header Enable 2. 3rd byte of the check header.

Address: 45h – Header Enable 1

Bit	R/W	Default	Function
[7:0]	R/W	0	**hden[15:8]** = Header Enable 1. 2nd byte of the check header.

Address: 46h – Header Enable 0

Bit	R/W	Default	Function
[7:0]	R/W	0	**hden[7:0]** = Header Enable 0. 1st byte of the check header.

Address: 47h – Received Header 3

Bit	R/W	Default	Function
[7:0]	R	0	**rxhd[31:24]** = Received Header 3. 4th byte of the received header.

Address: 48h – Received Header 2

Bit	R/W	Default	Function
[7:0]	R	0	**rxhd[23:16]** = Received Header 2. 3rd byte of the received header.

Address: 49h – Received Header 1

Bit	R/W	Default	Function
[7:0]	R	0	**rxhd[15:8]** = Received Header 1. 2nd byte of the received header.

Address: 4Ah – Received Header 0

Bit	R/W	Default	Function
[7:0]	R	0	**rxhd[7:0]** = Received Header 0. 1st byte of the received header.

Address: 4Bh – Received Packet Length

Bit	R/W	Default	Function
[7:0]	R	0	**rxplen[7:0]** = Length byte of the received header.

Address: 50h – Analog Test Bus Select

Bit	R/W	Default	Function
[7:5]	R/W	0	RESERVED
[4:0]	R/W	0	**atb[4:0]** = Analog Test Bus. The selection of internal analog testpoints that are muxed onto TESTp and TESTn.

Internal analog signals available on the Analog Test Bus:

atb[4:0]	GPIOx	GPIOx
1	MixIp Mix	In
2	MixQp Mix	Qn
3	PGA_Ip PG	A_In
4	PGA_QP PG	A_Qn
5	ADC_vcm	ADC_vbn
6	ADC_refmid	ADC_vbiasp
7	ADC_vcm	ADC_vcmb
8	ADC_ipoly10u	ADC_ref
9	ADC_refdac_p ADC_refd	ac_m
10	ADC_Res1i_p	ADCRes1i_m
11	ADC_Res1q_p	ADC_Res1q_m
12	ADC_Res2i_p	ADCRes2i_m
13	ADC_Res2q_p	ADC_Res2q_m
14	ADC_Res3i_p	ADCRes3i_m
15	ADC_Res3q_p	ADC_Res3q_m
16	spare	spare
17	ADC_RES_CAL_cap ADC_RES_CAL	_res
18	ICP_Test PLL_IBG_0	5
19	PLL_VBG VSS_VCO	
20	Vctrl_Test PLL_IPTAT_0	5
21	PA_vbias spar	e
22	DIGBG DIGV	FB
23	IFBG	IFVFB
24	PLLBG	PLLVReg
25	IBias10u	IBias5u
26	32KRC_Ucap 32KRC_U	res
27	ADC8_VIN	ADC8_VDAC
28	LBDcomp	LBDcompref
29	TSBG	TSVtemp
30	RFBG RFVRE	G
31	VCOBG V	COVREG

Address: 51h – Digital Test Bus Select

Bit	R/W	Default	Function
7	R/W	0	RESERVED
6	R/W	0	**ensctest** = Scan Test Enable. When set to '1' then GPIO0 will be the ScanEn input.
[5:0]	R/W	0	**dtb[5:0]** = Digital Test Bus. GPIO must be configured to Digital Test Mux Output

Internal digital signals available on the Digital Test Bus:

dtb[4:0]	GPIO0	Signal	GPIO1	Signal	GPIO2	Signal
0	wkup_clk_32k	wake-up 32kHz clock	rbase_en	first divided clock	clk_base	timebase clock
1	wkup_clk_32k	wake-up 32kHz clock	wake_up	wake-up event	tm1sec	1 sec timebase
2	ts_adc_en	aux. ADC enable	adc_rdy_n	aux. ADC conversion ready	adc_done	aux. ADC measurement done
3	cont_lbd	low battery continouos mode	lbd_on	low battery ON signal	lbd	unfiltered output of LBD
4	div_clk_g	gated divided clock	uc_clk	microcontroller clock	ckout_rcsel	slow clock selected
5	en_div_sync	clock divider enable (sync'ed)	en_ckout	clock out enable	en_ckout_s	clock out enable (sync'ed)
6	osc30_en	oscillator enable	osc30_bias2x	oscillator bias control	xok	chip ready
7	xok	chip ready	zero_cap	cap. load zero	osc30_buff_en	buffer enable
8	tsadc_needed	aux. ADC enable	ext_retran	ext. retransmission request	tx_mod_gpio	TX modulation inpit
9	gpio_0_oen_n	GPIO0 output enable	gpio_0_aen	GPIO0 analog selection	gpio_0_aden	GPIO0 ADC input line enable
10	int_ack1	interrupt acknowledge 1	int_ack2	interrupt acknowledge 2	int_store	interrupt latch closed
11	ext_int2	ext. interrupt from GPIO2	irq_bit8	combined external status	msk_bit8	combined masked ext. int.
12	sdo_aux_sel	SDO aux. function select	sdo_aux	SDO aux. signal	nirq_aux_sel	nIRQ aux. function select
13	trdata_on_sdi	TX/RX data on SDI	tx_mod	TX modulation input	tx_clk_out	TX clock output
14	start_full_sync	RC osc. full calibration start	start_fine_sync	RC osc. fine calibration start	xtal_req	crystal req. for RC osc. cal.
15	coarse_rdy	RC osc. coarse cal. ready	fine_rdy	RC osc. fine cal. ready	xtal_req_sync	sync'ed crystal request
16	vco_cal_rst_s_n	VCO calibration reset	vco_cal	VCO calibration is running	vco_cal_done	VCO calibration done
17	vco_cal_en	VCO calibration enable	en_ref_cnt	reference counter enable	en_freq_cnt_s	frequency counter enable
18	vco_cal_en	VCO calibration enable	pos_diff	positive difference to goal	en_freq_cnt_s	frequency counter enable
19	dsm_clk_mux	DSM multiplexed clock	pll_fb_clk_tst	PLL feedback clock	pll_ref_clk_tst	PLL reference clock
20	dsm[0]	delta-sigma output	dsm[1]	delta-sigma output	dsm[2]	delta-sigma output
21	dsm[3]	delta-sigma output	pll_fbdiv15		dsm_rst_s_n	delta-sigma reset
22	pll_en	PLL enable: TUNE state	pllt0_ok	PLL initial settling OK	pllts_ok	PLL soft settling OK
23	ch_freq_req	frequency change request	pllts_ok	PLL soft settling OK	vco_cal_done	VCO calibration done
24	vco_cal_en	VCO calibration enable	pll_vbias_shunt_en	VCO bias shunt enable	prog_req	frequency recalculation req.
25	bandgap_en	bandgap enable	frac_div_en	fractional divider enable	buff3_en	buffer3 enable
26	pll_pfd_up	PFD up signal	pll_pfd_down	PFD down signal	pfd_up_down	PFD output change (XOR'ed)
27	pll_lock_detect	PLL lock detect	pll_en	PLL enable: TUNE state	pllt0_ok	PLL initial settling OK
28	pll_en	PLL enable: TUNE state	pll_lock_detect	PLL lock detect	pllts_ok	PLL soft settling OK
29	pwst[0]	internal power state	pwst[1]	internal power state	pwst[2]	internal power state

Internal digital signals available on the Digital Test Bus (continued from the previous page):

dtb[4:0]	GPIO0	Signal	GPIO1	Signal	GPIO2	Signal
30	xok	chip ready: READY state	pll_en	PLL enable: TUNE state	tx_en	TX enable: TX state
31	ts_en	temperature sensor enable	auto_tx_on	automatic TX ON	tx_off	TX OFF
32	ch_freq_req	frequency change request	return_tx	return from TX	pk_sent	packet sent
33	retran_req	retransmission request	tx_ffpt_store	TX FIFO pointer store	tx_ffpt_restore	TX FIFO pointer restore
34	pa_on_trig	PA ON trigger	dly_5us_ok	5 us delay expired	mod_dly_ok	modulator delay expired
35	tx_shdwn	TX shutdown	ramp_start	modulator ramp down start	ramp_done	modulator ramp down ended
36	pk_sent_dly	delayed packet sent	tx_shdwn_done	TX shutdown done	pa_ramp_en	PA ramp enable
37	tx_en	TX enable: TX state	ldo_rf_precharge	RF LDO precharge	pa_ramp_en	PA ramp enable
38	pa_on_trig	TX enable: TX state	dp_tx_en	packet handler (TX) enable	mod_en	modulator enable
39	reg_wr_en	register write enable	reg_rd_en	register rdead enable	addr_inc	register address increment
40	dp_tx_en	packet handler (TX) enable	data_start	start of TX data	pk_sent	packet has been sent
41	data_start	start of TX data	tx_out	packet handler TX data out	pk_sent	packet has been sent
42	ramp_done	ramp is done	data_start	start of TX data	pk_tx	packet is being transmitted
43	tx_ffaf	TX FIFO almost full	tx_fifo_wr_en	TX FIFO write enable	tx_ffem_tst	internal TX FIFO empty
44	clk_mod	modulator gated 10MHz clock	tx_clk	TX clock from NCO	rd_clk_x8	read clock = tx_clk / 10
45	mod_en	modulator enable	ramp_start	start modulator ramping down	ramp_done	modulator ramp done
46	data_start	data input start from PH	ook_en	OOK modulation enble	ook	OOK modulation
47	prog_req	freq. channel update request	freq_err	wrong freq. indication	dsm_rst_s_n	dsm sync. reset
48	mod_en	modulator enable	tx_rdy	TX ready	tx_clk	TX clock from NCO
49	dp_rx_en	packet handler (RX) enable	prea_valid	valid preamble	pk_srch	packet is being searched
50	pk_srch	packet is being searched	sync_ok	sync. word has been detected	rx_data	packet handler RX data input
51	pk_rx	packet is being received	sync_ok	sync. word has been detected	pk_valid	valid packet received
52	sync_ok	sync. word has been detected	crc_error	CRC error has been detected	hdch_error	header error detected
53	direct_mode	direct mode	rx_ffaf	RX FIFO almost full	rx_fifo_rd_en	RX FIFO read enable
54	bit_clk	bit clock	prea_valid	valid preamble	rx_data	demodulator RX data output
55	prea_valid	valid preamble	prea_inval	invalid preamble	ant_div_sw	antenna switch (algorythm)
56	sync_ok	sync. word has been detected	bit_clk bit	clock	rx_data	demodulator RX data output
57	clk_demod	demodulator gated 30MHz clk	adc_lsb_i	ADC I channel data LSB demod_t	st[0]	demodulator test
58	prea_valid	valid preamble	demod_tst[2]	demodulator test	demod_tst[1]	demodulator test
59	agc_smp_clk	AGC sample clock	win_h_tp	window comparator high	win_l_tp	window comparator low dly'd
60	agc_smp_clk	AGC sample clock	win_h_dly_tp	window comparator high	win_l_dly_tp	window comparator low dly'd
61	ldc_on	active low duty cycle	pll_en	PLL enable: TUNE state	rx_en	RX enable: RX state
62	ldc_on	active low duty cycle	no_sync_det	no sync word detected	prea_valid	valid preamble
63	adc_en	ADC enable	adc_refdac_en	ADC reference DAC enable	adc_rst_n	combined ADC reset

Address: 52h –TX Ramp Control

Bit R/W	Default	Function
7 R/W	0	RESERVED
[6:4] R/W	010	**txmod[2:0] =** TX Modulation Delay. The time delay between PA enable and the beginning of the TX modulation to allow for PA ramp-up. It can be set from 0 µs to 28 µs in 4 µs steps.
[3:2] R/W	00	**ldoramp[2:0] =** TX LDO Ramp Time. The RF LDO is used to help ramp the PA to prevent VCO pulling and spectral splatter. 00 – 5 µs 01 – 10 µs 10 – 15 µs 11 – 20 µs
[1:0] R/W	00	**txramp[1:0]** = TX ramp Time. The PA is ramped up slowly to prevent VCO pulling and spectral splatter. This register sets the time the PA is ramped up. 00 – 5 µs 01 – 10 µs 10 – 15 µs 11 – 20 µs

Address: 53h – PLL Tune Time

The total settling time (cold start) of the PLL after the calibration can be calculated as $T_{CS} = T_S + T_O$.

Bit R/W		Default	Function
[7:3]	R/W	01000	**pllts[4:0]** = PLL Soft Settling Time (T_S). This register will set the settling time for the PLL from a previous locked frequency in Tune mode. The value is configurable between 0 µs and 310 µs, in 10 µs intervals. The default plltime corresponds to 80 µs. See formula above.
[2:0]	R/W	101	**pllt0** = PLL Settling Time (T_O). This register will set the time allowed for PLL settling after the calibrations are completed. The value is configurable between 0 µs and 70 µs, in 10 µs steps. The default pllt0 corresponds to 50 µs. See fomula above.

Address: 54h – Reserved 1

Bit R/W	Default	Function
[7:0] R/W	0	RESERVED

Address: 55h – Calibration Control

Bit R/W	Default	Function
[7:6] R	-	RESERVED
5 R	-	**adccaldone** = Delta-sigma ADC Calibration Done. Reading this bit gives '1' if the calibration process has been finished.
4 R/W	0	**enrcfcal** = RC Oscillator Fine Calibration enable. If this bit is set to '1' then the RC oscillator performs fine calibration in every app. 30 s.
3 R/W	0	**rccal** = RC Calibration Force. If setting rccal='1' will automatically perform a forced calibration of the 32kHz RC Oscillator. The RC OSC will automatically be calibrated if the Wake-Up-Timer is enabled or if in the Wake-on-Receiver state. The calibration takes 2ms. The 32kHz RC oscillator must be enabled to perform a calibration. Setting this signal from a '0' to '1' will initiate the calibration. This bit is cleared automatically.
2 R/W	1	**vcocaldp** = VCO Calibration Double Precision enable. When this bit is set to '1' then the VCO calibration measures longer thus calibrates more precisely.
1 R/W	0	**vcocal** = VCO Calibration Force. If in Idle Mode and pllon='1', setting vcocal='1' will force a one time calibration of the synthesizer VCO. This bit is cleared automatically.
0 R/W	0	**skipvco** = Skip VCO Calibration. Setting skipvco='1' will skip the VCO calibration when going from the Idle state to the TX or RX state.

Address: 56h – Modem Test

Bit R/W	Default	Function
[7:4] R/W	0	RESERVED
3 R/W	0	**preabp** = Bypass Preamble Detection.
2 R/W	0	**refclksel** = Delta-sigma Reference Clock Source Selection (1: 10MHz, 0: PLL)
1 R/W	0	**refclkinv** = Delta-sigma Reference Clock Inversion enable
0 R/W	0	**iqswitch** = I&Q Channel Switch enable.

Address: 57h – Charge Pump Test

Bit R/W	Default	Function
[7:6] R/W	0	RESERVED
5 R/W	0	**cpforceup** = Charge Pump Force Up
4 R/W	0	**cpforcedn** = Charge Pump Force Down
3 R/W	0	**cdconly** = Charge Pump DC Offset Only
[2:0] R/W	0	**cdcurr[2:0]** = Charge Pump DC Current selection

Address: 58h – Charge Pump Current Trimming / Override

Bit	R/W	Default	Function
[7:6]	R/W	10	**cpcurr[1:0]** = Charge Pump Current (Gain Setting). Changing these bits will change the BW of the PLL. The default setting is adequate for all data rates.
5	R/W	0	**cpcorrov** = Charge Pump Correction Override enable
[4:0]	R/W	NA	**cpcorr[4:0]** = Charge Pump Correction value

Address: 59h – Divider Current Trimming / Delta-Sigma Test

Bit	R/W	Default	Function
7	R	-	RESERVED
6	R/W	0	**fbdivhc** = Feedback (fractional) Divider High Current enable (+5uA)
[5:4]	R/W	0	**d3trim[1:0]** = Divider 3 Current Trim value
[3:2]	R/W	0	**d2trim[1:0]** = Divider 2 Current Trim value
[1:0]	R/W	0	**d1p5trim[1:0]** = Divider 1.5 (div-by-1.5) Current Trim value

Address: 5Ah – VCO Current Trimming

Bit	R/W	Default	Function
7	R	-	RESERVED
6	R/W	0	**vcocorrov** = VCO Current Correction override
[5:2]	R/W	0	**vcocorr[3:0]** = VCO Current Correction value
[1:0]	R/W	11	**vcocur[1:0]** = VCO Current Trim value

Address: 5Bh – VCO Calibration / Override

Bit	R/W	Default	Function
7	R/W	0	**vcocalov** / **vcdone** = VCO Calibration Override / Done. When vcocalov='0' the internal VCO Calibration results may be viewed by reading the vcocal register. When vcocalov='1' the VCO results may be overridden externally through the SPI by writing to the vcocal register. Reading this bit gives '1' if the calibration process has been finished.
[6:0]	R/W	0	**vcocal[6:0]** = VCO Calibration Results

Address: 5Ch – Synthesizer Test

Bit R/W	Default	Function
7 R	-	RESERVED
6 R	-	**vcotype** = VCO Type. 0 – basic, constant K 1 – single varactor, changing K
5 R/W	0	**enoloop** = Open Loop Mode enable
4 R/W	0	**dsmod** = Delta-Sigma Modulus 0 – 64 000 1 – 65 536
[3:2] R/W	11	**dsorder[1:0]** = Delta-Sigma Order 00 – 0 order 01 – 1st order 10 – 2nd order 11 – Mash 111
1 R/W	1	**dsrstmode** = Delta-Sigma Reset Mode
0 R/W	0	**dsrst** = Delta-Sigma Reset

Address: 5Dh – Block Enable Override 1

Bit R/W		Default	Function
7	R/W	0	**enmix** = Mixer enable override
6	R/W	0	**enlna** = LNA enable override
5	R/W	0	**enpga** = PGA enable override
4	R/W	0	**enpa** = Power Amplifier enable override
3	R/W	0	**enbf5** = Buffer 5 enable override
2	R/W	0	**endv32** = Divider 3_2 enable override
1	R/W	0	**enbf12** = Buffer 1_2 enable override
0	R/W	0	**enmx2** = Multiplexer 2 enable override

Address: 5Eh – Block Enable Override 2

Bit	R/W	Default	Function
7	R/W	0	**ends** = Delta-Sigma enable override
6	R/W	0	**enldet** = Lock Detect enable (direct control, not override!)
5	R/W	0	**enmx3** = Mutiplexer 3 enable override
4	R/W	0	**enbf4** = Buffer 4 enable override
3	R/W	0	**enbf3** = Buffer 3 enable override
2	R/W	0	**enbf11** = Buffer 1_1 enable override
1	R/W	0	**enbf2** = Buffer 2 enable override
0	R/W	0	**enmx1** = Multiplexer enable override

Address: 5Fh – Block Enable Override 3

Bit R/W		Default	Function
7	R/W	0	**enfrdv** = Fractional Divider enable override
6	R/W	0	**endv31** = Divider 3_1 enable override
5	R/W	0	**endv2** = Divider 2 enable override
4	R/W	0	**endv1p5** = Divider 1.5 (div-by-1.5) enable override
3	R/W	0	**dvbshunt** = VCO Bias Shunt disable override
2	R/W	0	**envco** = VCO enable override
1	R/W	0	**encp** = Charge Pump enable override
0	R/W	0	**enbg** = Bandgap enable override

Address: 60h – Channel Filter Coefficient Address

Bit R/W		Default	Function
[7:4] R/W		0	RESERVED
[3:0] R/W		000	**chfiladd[3:0]** = Channel Filter Coefficient Look-up Table Address. The address for channel filter coefficients used in the RX path.

Address: 61h – Channel Filter Coefficient Value

Bit R/W	Default	Function
[7:6] R/W	0	RESERVED
[5:0] R/W	0	**chfilval[5:0]** = Filter Coefficient Value in the look-up table addressed by the chfiladd[3:0]

Address: 62h – Crystal Oscillator / Power-On-Reset Control

Bit R/W	Default	Function
[7:6] R	-	**pwst[1:0]** = Internal Power States of the chip 00 – low power (stand-by / sleep / sensor) 01 – ready 11 – tune 10 – TX
5 R/W	1	**enspor** = Smart POR enable
4 R/W	0	**clkhyst** = Clock Hysteresis Setting
3 R/W	0	**enbias2x** = 2 times higher bias current enable
2 R/W	1	**enamp2x** = 2 times higher amplification enable
1 R/W	0	**bufovr** = Output Buffer Enable Override If set to '1' then the enbuf bit controls the output buffer. 0 – output buffer is controlled by the state machine 1 – output buffer is controlled by the enbuf bit
0 R/W	0	**enbuf** = Output Buffer Enable This bit is active only if the bufovr bit is set to '1'.

Address: 63h – RC Oscillator Coarse Calibration / Override

Bit R/W	Default	Function
7 R/W	0	**rccov** = RC Oscillator Coarse Calibration Override. When rccov='0' the internal Coarse Calibration results may be viewed by reading the rcccal register. When rccov='1' the Coarse results may be overridden externally through the SPI by writing to the rcccal register.
[6:0] R/W	0	**rcc[6:0]** = RC Oscillator Coarse Calibration Override Value / Results

Address: 64h – RC Oscillator Fine Calibration / Override

Bit	R/W	Default	Function
7	R/W	0	**rcfov** = RC Oscillator Fine Calibration Override. When rcfov='0' the internal Fine Calibration results may be viewed by reading the rcfcal register. When rcfov='1' the Fine results may be overridden externally through the SPI by writing to the rcfcal register.
[6:0]	R/W	0	**rcf[6:0]** = RC Oscillator Coarse Calibration Override Value / Results

Address: 65h – LDO Control Override

Bit	R/W	Default	Function
7	R/W	0	RESERVED
6	R/W	0	**enbias** = Bias enable
5	R/W	0	**envcoldo** = VCO LDO enable
4	R/W	0	**enifldo** = IF LDO enable
3	R/W	0	**enrfldo** = RF LDO enable
2	R/W	0	**enpllldo** = PLL LDO enable
1	R/W	0	**endigldo** = Digital LDO enable
0	R/W	1	**endigpwdn** = Digital Power Domain Powerdown enable in Idle mode

Address: 66h – Reserved 2

Bit	R/W	Default	Function
[7:0]	R	-	RESERVED

Address: 67h – Delta-sigma ADC Tuning 1

Bit	R/W	Default	Function
7	R/W	0	**adcrst** = delta-sigma ADC reset
6	R/W	0	**enrefdac** = delta-sigma ADC reference DAC enable override
5	R/W	0	**enadc** = delta-sigma ADC enable override
4	R/W	0	**adctuneovr** = resonator RC calibration value override enable
[3:0]	R/W	0	**adctune[3:0]** = resonator RC calibration value

Address: 68h – Delta-sigma ADC Tuning 2

Bit	R/W	Default	Function
[7:6]	R	-	RESERVED
4	R/W	0	**envcm** = delta-sigma ADC VCM enable override
3	R/W	0	**adcoloop** = delta-sigma ADC open loop enable
[2:0]	R/W	0	**adcref[2:0]** = delta-sigma ADC reference voltage 000 – 0.5 V 001 – 0.6 V 010 – 0.7 V … 111 – 1.2 V

Address: 69h – AGC Override 1

Bit	R/W	Default	Function
[7:6]	R/W	0	RESERVED
5	R/W	1	**agcen** = Automatic Gain C ontrol en able When this bit is set then the re sult of the control can be read out from bits [4:0], otherwise the gain can be controlled manually by writing into bits [4:0].
4	R/W	0	**lnagain** = LNA Gain select 0 – min. gain = 5 dB 1 –max. gain = 25 dB
[3:0]	R/W	0	**pga[3:0]** = PGA Gain Override value 000 – 0 dB 001 – 3 dB 010 – 6 dB ... 101 – 24 dB max.

Address: 6Ah – AGC Override 2

Bit	R/W	Default	Function
7	R/W	0	RESERVED
6	R/W	0	**agcslow** = AGC Slow Gain Increase enable. When this bit is set then the AGC loop will slow down the gain increase in the receiver. The speed of the gain reduction is not affected.
[5:2]	R/W	0	**lnacomp[3:0]** = LNA Gain Comp ensation, used for smo othing RSSI valu e when LNA gain is switched.
[1:0]	R/W	01	**pgath[1:0]** = window comparator reference voltage adjust in the PGA

Address: 6Bh – GFSK FIR Filter Coefficient Address

Bit	R/W	Default	Function
[7:3]	R	-	RESERVED
[2:0]	R/W	000	**firadd[2:0]** = GFSK FIR Filter Coefficient Look-up Table Address. The address for Gaussian filter coefficients used in the TX path. The default GFSK setting is for BT =0.5. It is not needed to change or load the GFSK Coefficients if BT=0.5 is satisfactory for the system. 000 – i_coe0 (Default =d1) 001 – i_coe1 (Default =d3) 010 – i_coe2 (Default =d6) 011 – i_coe3 (Default =d10) 100 – i_coe4 (Default =d15) 101 – i_coe5 (Default =d19) 110 – i_coe6 (Default =d20)

Address: 6Ch – GFSK FIR Filter Coefficient Value

Bit	R/W	Default	Function
[7:6]	R/W	0	RESERVED
[5:0]	R/W	1	**firval[5:0]** = FIR Coefficient Value in the look-up table addressed by the firadd[2:0]. The default coefficient can be read or modified.

Address: 6Dh – TX Power

Bit	R/W	Default	Function
[7:3]	R	-	RESERVED
[1:0]	R/W	11	**txpow[1:0]** = TX Output Power. The output power is configurable from +20 to +11dBm in ~3dB steps. txpow[1:0]='11' corresponds to +20dBm and '00' to +11dBm.

Address: 6Eh – TX Data Rate 1

The data rate can be calculated as $TX\_DR = 10^3 * txdr[15:0] / 2^{16}$ [kbit/s]

Bit	R/W	Default	Function
[7:0]	R/W	0Ah	**txdr[15:8]** = Data Rate upper byte. See formula above.

Address: 6Fh – TX Data Rate 0

Bit	R/W	Default	Function
[7:0]	R/W	AAh	**txdr[7:0]** = Data Rate lower byte. See formula above. Defaults = 40 kbps

Address: 70h – Modulation Mode Control 1

Bit	R/W	Default	Function
[7:3]	R	0	RESERVED
2	R/W	1	**enmaninv** = Manchester Data Inversion is enabled if this bit is set.
1	R/W	0	**enmanch** = Manchester Coding is enabled if this bit is set.
0	R/W	0	**enwhite** = Data Whitening is enabled if this bit is set.

Address: 71h – Modulation Mode Control 2

Bit	R/W	Default	Function
[7:6]	R/W	0	**trclk[1:0]** = TX Data Clock Configuration. 00 – No TX Data CLK is available (asynchronous mode) 01 – TX Data CLK is available via the GPIO (one of the GPIO's should be programmed as well) 10 – TX Data CLK is available via the SCK pin 11 – TX Data CLK is available via the nIRQ pin
[5:4]	R/W	0	**dtmod[1:0]** = Modulation Source 00 – Direct Mode using TX_Data function via the GPIO pin (one of the GPIO's should be programmed accordingly as well) 01 – Direct Mode using TX_Data function via the SDI pin (only when nSEL is high) 10 – FIFO Mode 11 – PN9 (internally generated)
3	R/W	0	**eninv** = Invert TX and RX Data
[2:0]	R/W	0	**modtyp[2:0]** = Modulation Type 000 – Unmodulated carrier 001 – OOK 010 – FSK 011 – GFSK (enable TX Data CLK (trclk[1:0]) when direct mode is used)

Address: 72h – Frequency Deviation

The frequency deviation can be calculated: Fd = 625 Hz * fd[7:0]

Bit	R/W	Default	Function
[7:0]	R/W	43h	**fd[7:0]** = Frequency Deviation Setting. See formula above.

Address: 73h – Frequency Offset

The frequency offset can be calculated: Offset = 156.25 Hz * (hbsel + 1) * fo[7:0] . fo[9:0] is a 2's complement value.

Bit	R/W	Default	Function
[7:0]	R/W	00h	**fo[7:0]** = Frequency Offset Setting.

Address: 74h – Frequency Channel Control

Bit	R/W	Default	Function
[7:1]	R	0	RESERVED
[1:0]	R/W	0	**fo[9:8]** = Upper bits of the Frequency Offset Setting. fo[9] is the sign bit.

Address: 75h – Frequency Band Select

Bit	R/W	Default	Function
7	R	0	RESERVED
6	R/W	0	**sbsel** = Side Band Select.
5	R/W	1	**hbsel** = High Band Select. Setting hbsel = '1' will choose the freqency range from 480-930MHz (High Bands). Setting hbsel = '0' will choose the freqency range from 240-479.9MHz (Low Bands).
[4:0]	R/W	10101	**fb[4:0]** = Frequency Band Select. Every increment corresponds to a 10MHz Band for the Low Bands and a 20MHz Band for the High Bands. Setting fb[4:0]='00000' corresponds to the 240-250MHz Band for hbsel='0' and the 480-500MHz Band for hbsel='1'. Setting fb[4:0]='00001' corresponds to the 250-260MHz Band for hbsel='0' and the 500-520MHz Band for hbsel='1'.

Address: 76h – Nominal Carrier Frequency

The RF carrier frequency can be calculated as:

$$f_{carrier} = (f_b+24+(f_c+f_o) / 64000) * 10000 * (hbsel+1) + (f_{hch} * f_{hs} * 10) \ [kHz],$$

where parameters f_c, f_o, f_b and hb_sel come from registers 73h–77h. Parameters f_{hch} and f_{hs} come from register 79h and 7Ah.

Bit	R/W	Default	Function
[7:0]	R/W	BBh	**fc[15:8]** = Nominal Carrier Frequency Setting. See formula above.

Address: 77h – Nominal Carrier Frequency

Bit	R/W	Default	Function
[7:0]	R/W	80h	**fc[7:0]** = Nominal Carrier Frequency Setting. See formula above.

Address: 79h –Frequency Hopping Channel Select

Bit	R/W	Default	Function
[7:0]	R/W	0	**fhch[7:0]** = Frequency Hopping Channel number.

Address: 7Ah –Frequency Hopping Step Size

Bit	R/W	Default	Function
[7:0]	R/W	0	**fhs[7:0]** Frequency Hopping Step Size in 10kHz increments. See formula for the nominal carrier frequency at register 76h.

Address: 7Ch – TX FIFO Control 1

Bit	R/W	Default	Function
[7:6]	R/W	0	RESERVED
[5:0]	R/W	110111	**txafthr[5:0]** = TX FIFO Almost Full Threshold

Address: 7Dh – TX FIFO Control 2

Bit R/W	Default	Function
[7:6] R/W	0	RESERVED
[5:0] R/W	000100	**txfaethr[5:0]** = TX FIFO Almost Empty Threshold

Address: 7Eh – RX FIFO Control

Bit R/W	Default	Function
[7:6] R/W	0	RESERVED
[5:0] R/W	110111	**rxafthr[5:0]** = RX FIFO Almost Full Threshold

Address: 7Fh – FIFO Access

Bit R/W	Default	Function
[7:0] R/W	NA	**fifod[7:0]** = A write (R/W='1') to this address will begin a burst write to the TX FIFO. The FIFO will be loaded in the same manner as a Burst SPI Write but the SPI address will not be incremented. To conclude the TX FIFO Write the SEL pin should be brought HIGH. A Read (R/W='0') to this address will begin a burst read of the RX FIFO, in the same manner.

RELATED PRODUCTS AND DOCUMENTS

Integration Associates, Inc.
110 Pioneer Way, Unit L
Mountain View, California 94041
Tel: 650.969.4100
Fax: 650.969.4582
www.integration.com
marketing@integration.com
wireless.support@integration.com
P840