

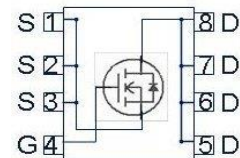
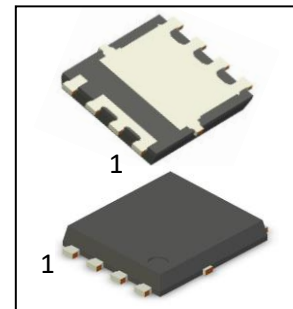
**OptiMOS™ - 6 Power-Transistor**

**Product Summary**

$V_{DS}$	40	V
$R_{DS(on),max}$	0.8	mΩ
$I_D$	120	A

**Features**

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal Level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

**PG-TDSON-8-43**


Type	Package	Marking
IAUC120N04S6N008	<a href="#">PG-TDSON-8-43</a>	6N04N008

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current <sup>1)</sup>	$I_D$	$V_{GS}=10V$ , Chip Limitation <sup>1,2)</sup>	314	A
		$V_{GS}=10V$ , DC current <sup>3)</sup>	120	
		$T_a=85\text{ °C}$ , $V_{GS}=10V$ , $R_{thJA}$ on 2s2p <sup>2,4)</sup>	43	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	480	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D=60A$ , $R_{G,min}=25\Omega$	400	mJ
Avalanche current, single pulse	$I_{AS}$	$R_{G,min}=25\Omega$	60	A
Gate source voltage	$V_{GS}$	-	$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	150	W
Operating and storage temperature	$T_j, T_{stg}$	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Thermal characteristics<sup>2)</sup></b>						
Thermal resistance, junction - case	$R_{thJC}$	-	-	-	1.0	K/W
Thermal resistance, junction - ambient <sup>4)</sup>	$R_{thJA}$	-	-	23.3	-	

**Electrical characteristics, at  $T_j=25^\circ\text{C}$ , unless otherwise specified**

### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=90\mu A$	2.2	2.6	3.0	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	$\mu A$
		$V_{DS}=40V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	-	25	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=7V, I_D=60A$	-	0.80	1.1	$m\Omega$
		$V_{GS}=10V, I_D=60A$	-	0.68	0.8	
Gate resistance <sup>2)</sup>	$R_G$		-	0.9	-	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	5371	7150	pF
Output capacitance	$C_{oss}$		-	1626	2170	
Reverse transfer capacitance	$C_{rss}$		-	66	100	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=120A, R_G=3.5\Omega$	-	9	-	ns
Rise time	$t_r$		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	22	-	
Fall time	$t_f$		-	11	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=32V, I_D=120A,$ $V_{GS}=0 \text{ to } 10V$	-	22	30	nC
Gate to drain charge	$Q_{gd}$		-	16	24	
Gate charge total	$Q_g$		-	83	110	
Gate plateau voltage	$V_{plateau}$		-	4.1	-	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25^\circ C$	-	-	120	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$		-	-	480	
Diode forward voltage	$V_{SD}$	$V_{GS}=0V, I_F=60A,$ $T_J=25^\circ C$	-	0.8	1.1	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=20V, I_F=120A,$ $di_F/dt=100A/\mu s$	-	60	-	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	73	-	nC

<sup>1)</sup> Practically the current is limited by overall system design including customer specific PCB.

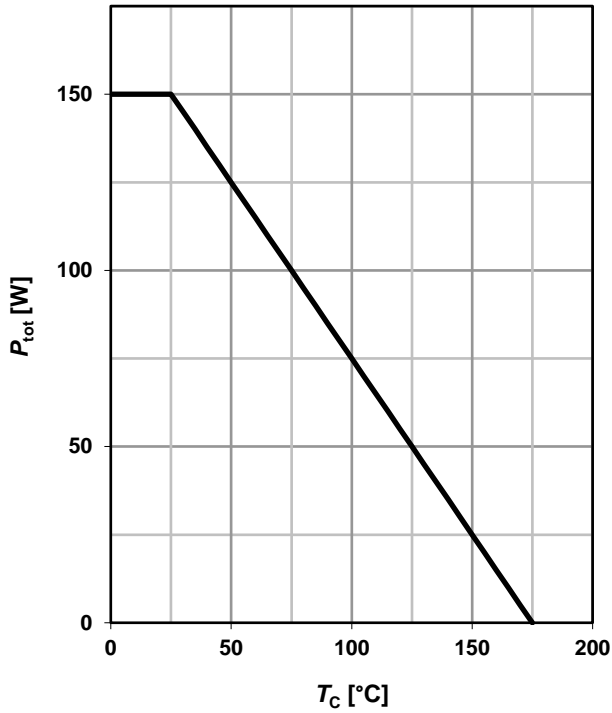
<sup>2)</sup> The parameter is not subject to production testing - specified by design.

<sup>3)</sup> The product can operate at specified current based on best practice to minimize electromigration at the solder joint. For rare events and inrush currents the value may be exceeded.

<sup>4)</sup> Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

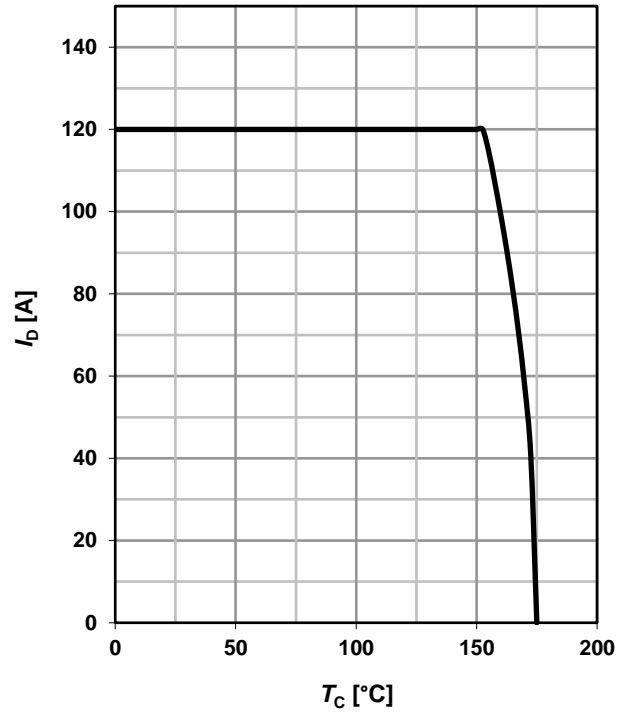
### 1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



### 2 Drain current

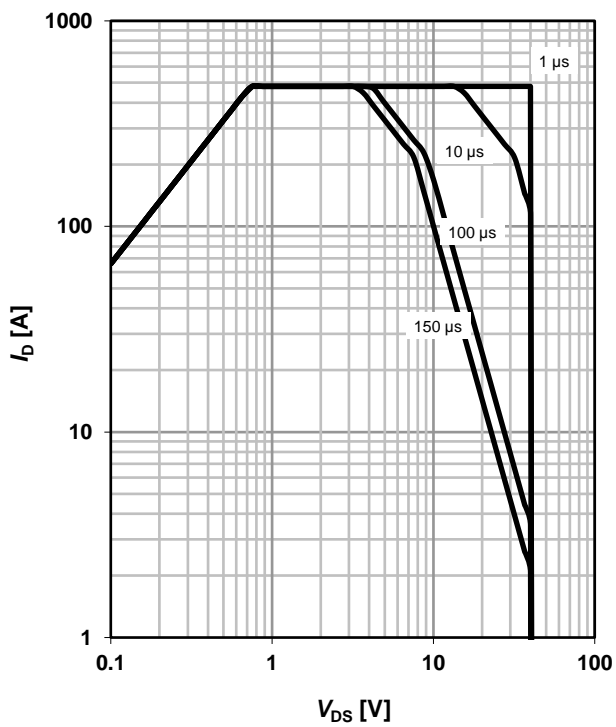
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$



### 3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

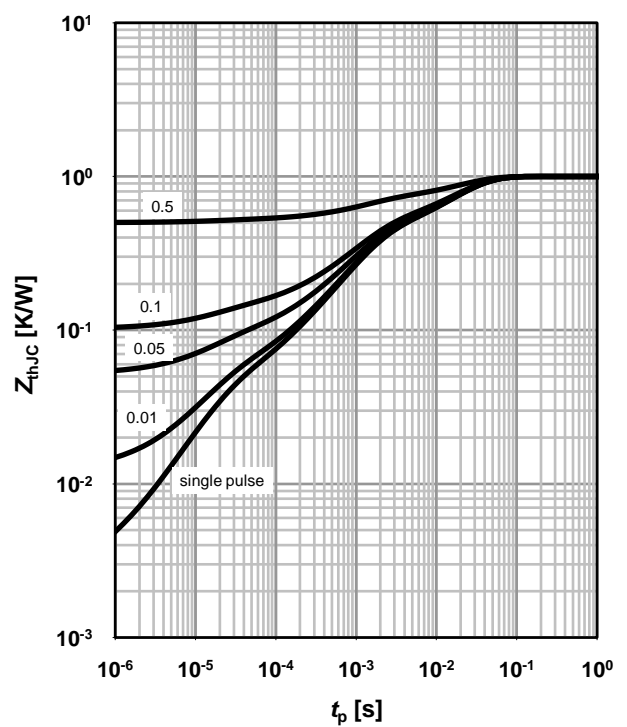
parameter:  $t_p$



### 4 Max. transient thermal impedance

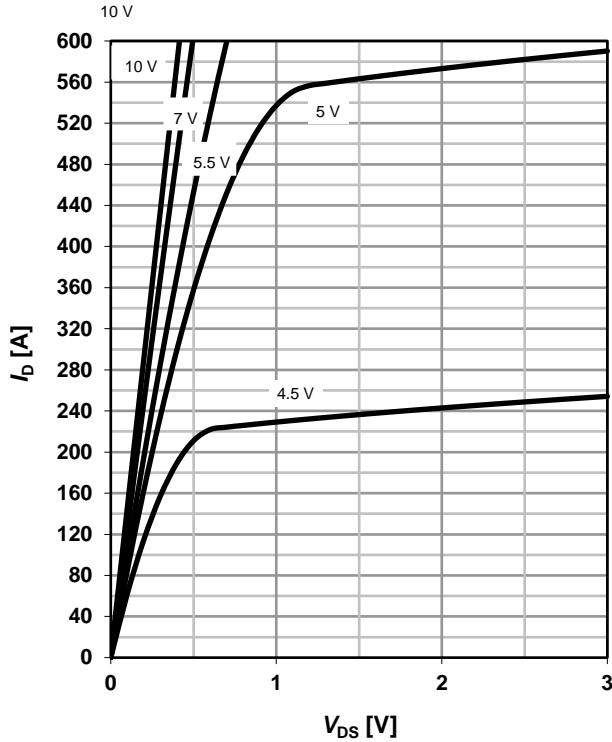
$$Z_{\text{thJC}} = f(t_p)$$

parameter:  $D = t_p/T$

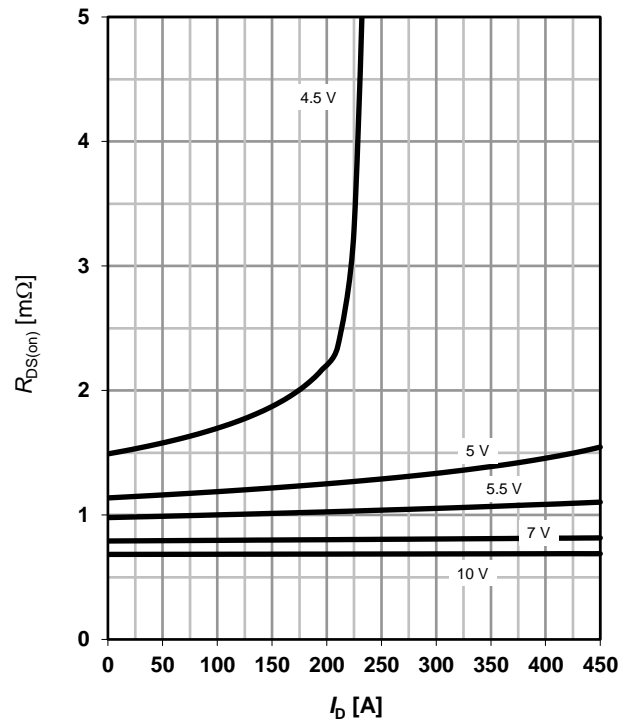


**5 Typ. output characteristics**

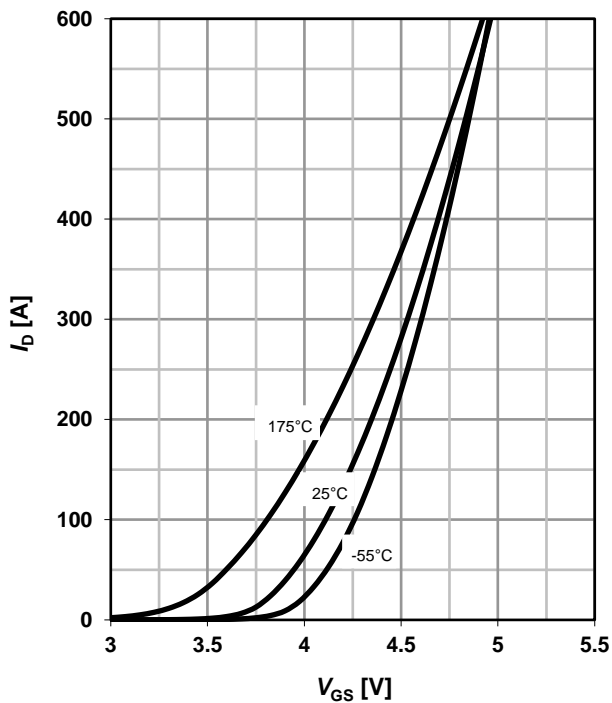
$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

 parameter:  $V_{GS}$ 

**6 Typ. drain-source on-state resistance**

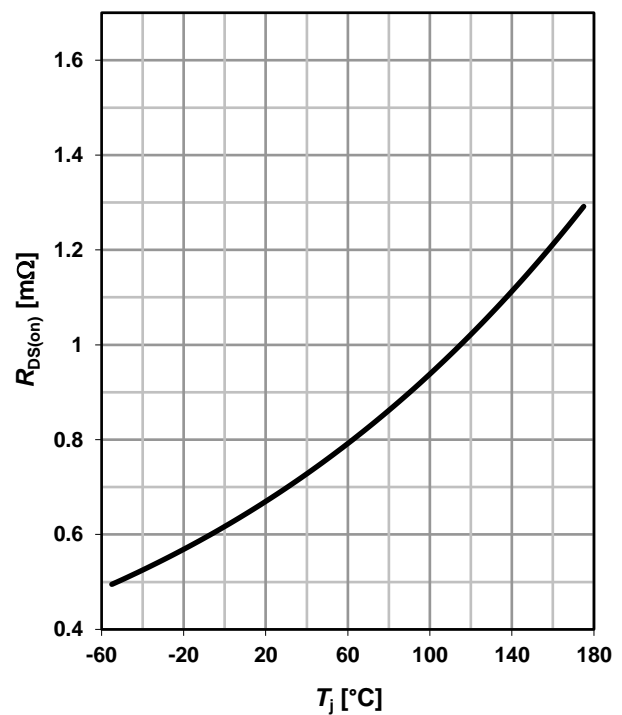
$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

 parameter:  $V_{GS}$ 

**7 Typ. transfer characteristics**

$$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$$

 parameter:  $T_j$ 

**8 Typ. drain-source on-state resistance**

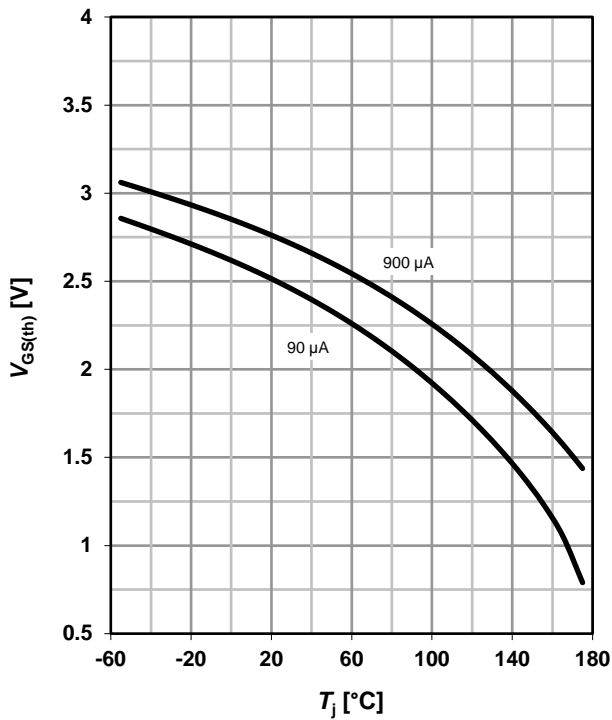
$$R_{DS(on)} = f(T_j); I_D = 60\text{ A}; V_{GS} = 10\text{ V}$$



**9 Typ. gate threshold voltage**

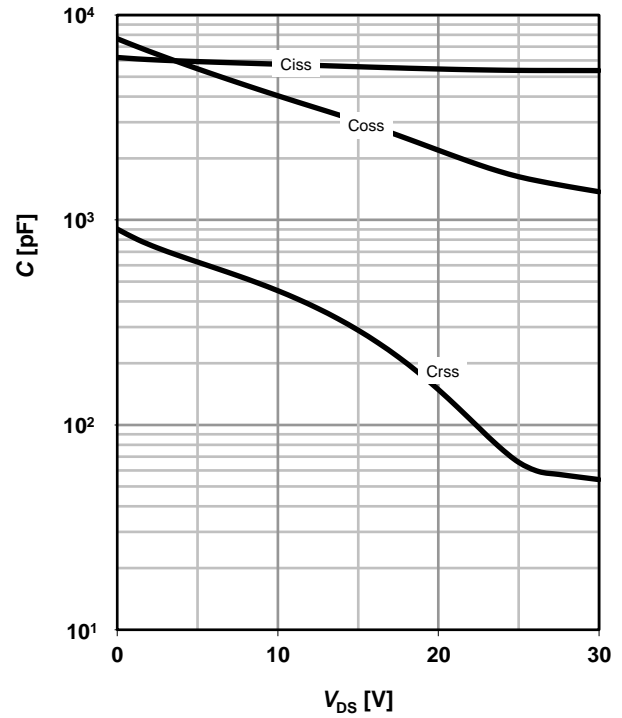
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter:  $I_D$



**10 Typ. capacitances**

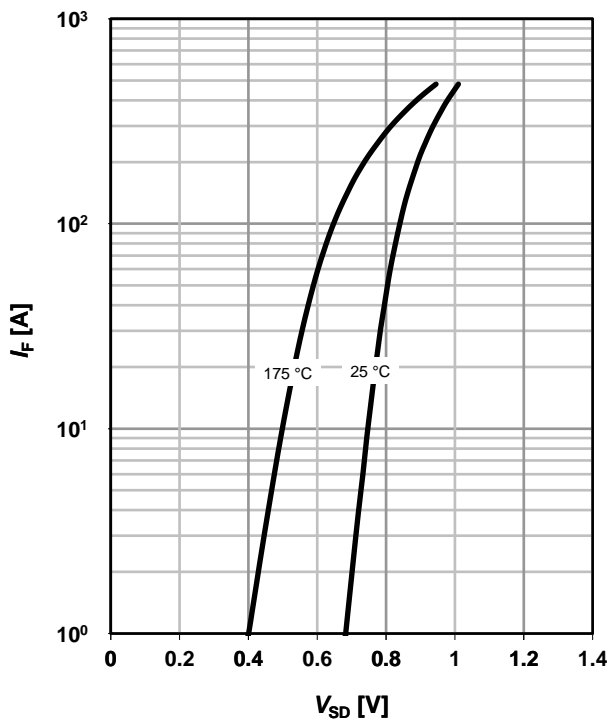
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



**11 Typical forward diode characteristics**

$I_F = f(V_{SD})$

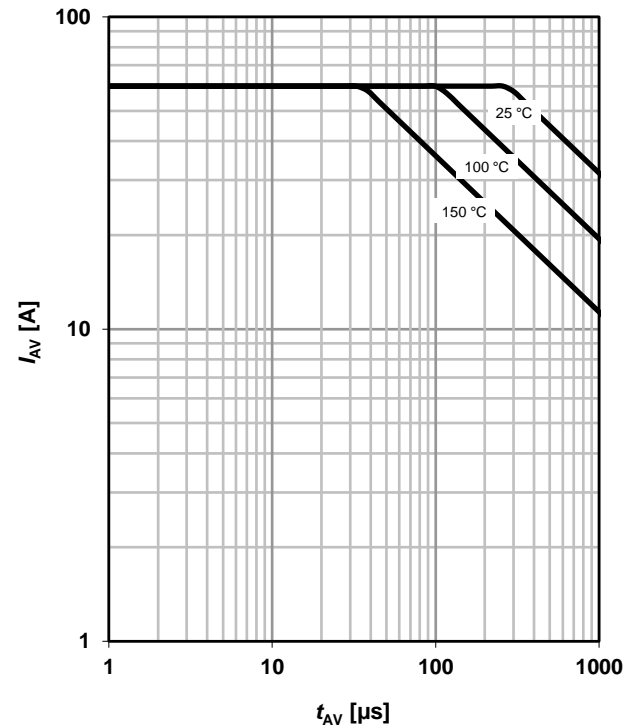
parameter:  $T_j$



**12 Avalanche characteristics**

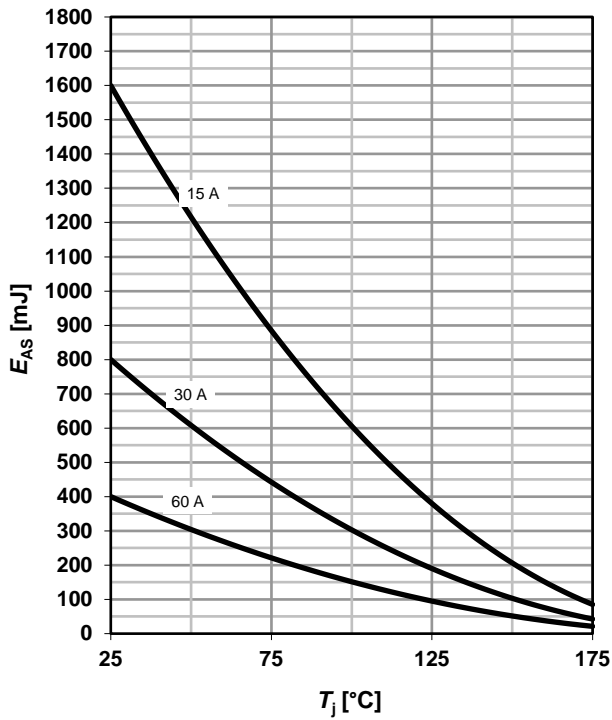
$I_{AS} = f(t_{AV})$

parameter:  $T_{j(start)}$

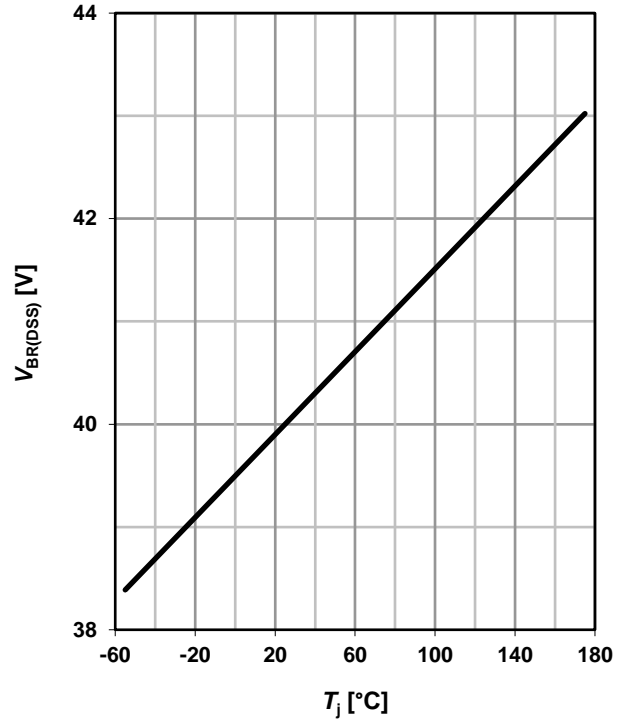


**13 Avalanche energy**

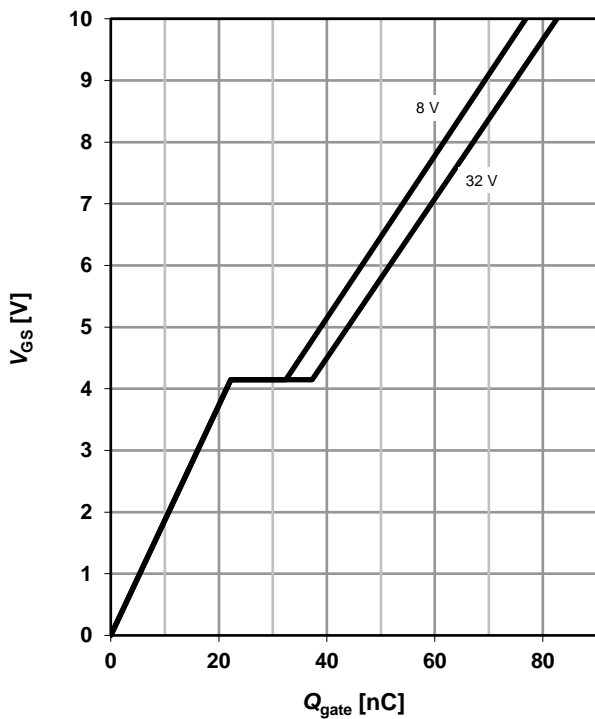
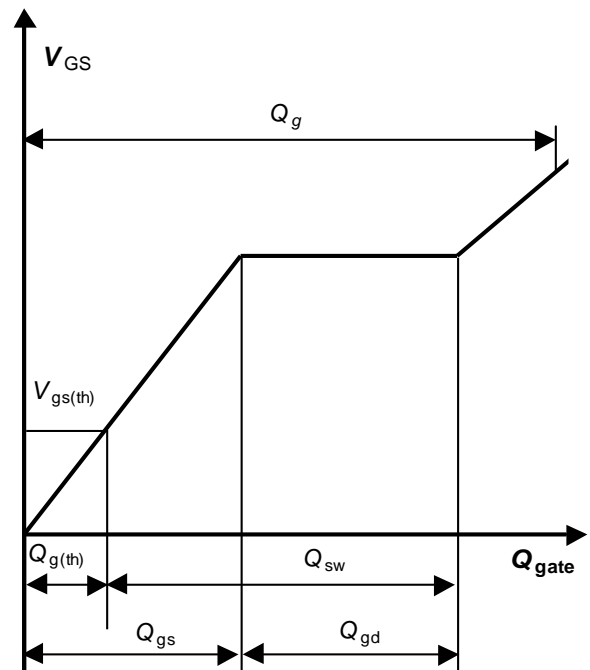
$$E_{AS} = f(T_j)$$


**14 Drain-source breakdown voltage**

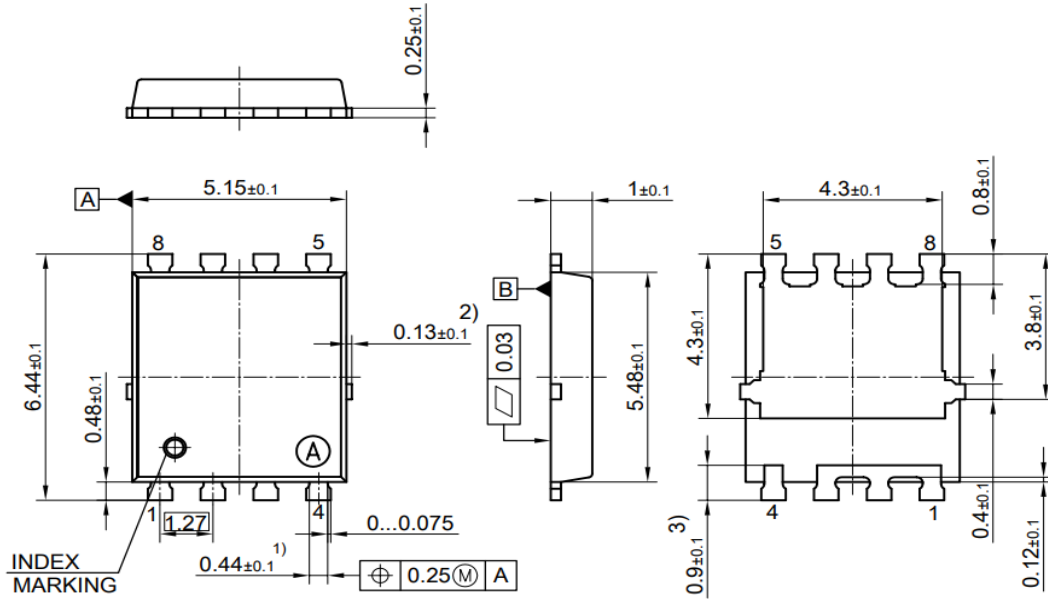
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$


**15 Typ. gate charge**

$$V_{GS} = f(Q_{gate}); I_D = 40 \text{ A pulsed}$$

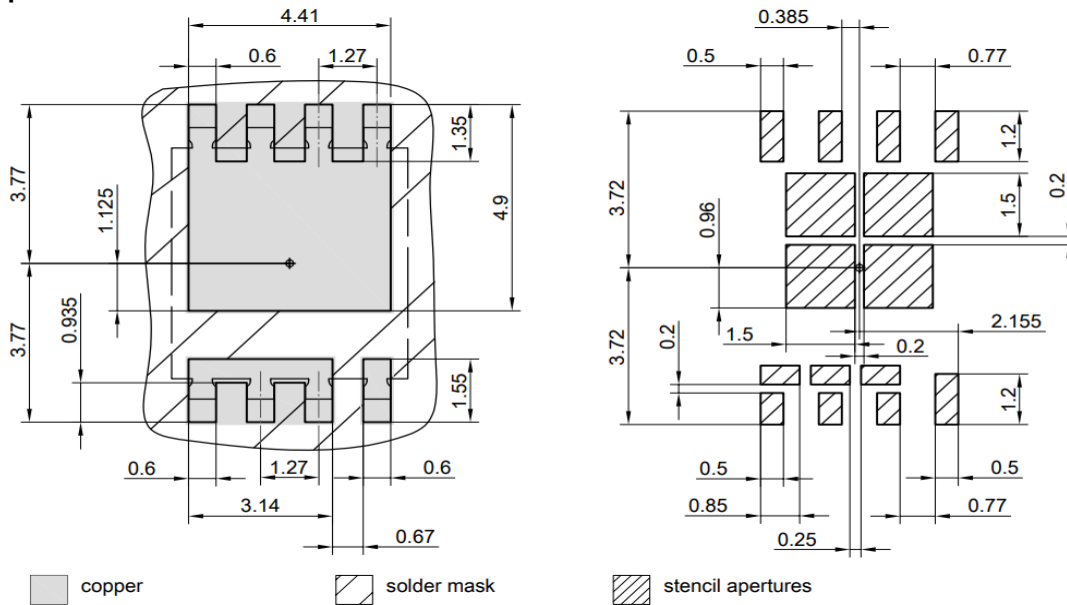
 parameter:  $V_{DD}$ 

**16 Gate charge waveforms**


PG-TDSON-8: Outline

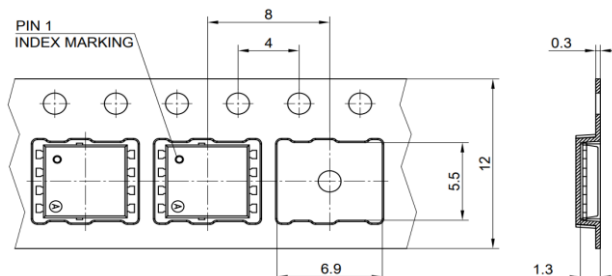


- 1) EXCLUDE MOLD FLASH
  - 2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
  - 3) LEAD LENGTH UP TO ANTI FLASH LINE
  - 4) ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
- ALL DIMENSIONS ARE IN UNITS MM  
 THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [ ]

Footprint



Dimensions in mm  
 Packaging





**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

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Version	Date	Changes
Revision 1.0	24.08.2020	Final Datasheet