

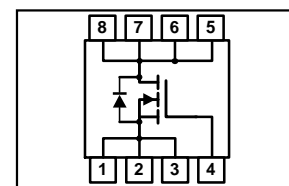
Automotive MOSFET

OptiMOS™-5 Power-Transistor



Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested



Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	60	V
$R_{DS(on)}$	7.4	mΩ
I_D (chip limited)	60	A

Type	Package	Marking
IAUC60N06S5N074	PG-TDSON-8-33	5N06N074



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Maximum ratings

at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$V_{GS}=10\text{ V}$, Chip limitation ^{1,2)}	60	A
		$V_{GS}=10\text{V}$, DC current	60	
		$T_a=85\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,4)}	15	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$, $t_p=100\text{ }\mu\text{s}$	168	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=30\text{ A}$	40	mJ
Avalanche current, single pulse	I_{AS}	–	60	A
Gate source voltage	V_{GS}	–	± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	52	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	–	–	55/175/56	

Thermal characteristics²⁾

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	–	2.9	K/W
Thermal resistance, junction - ambient ⁴⁾	R_{thJA}	–	–	24.8	–	

Electrical characteristics

 at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$	60	–	–	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=19\text{ }\mu\text{A}$	2.2	2.8	3.4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	–	–	1	μA
		$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=100\text{ °C}^{2)}$	–	–	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=7\text{ V}$, $I_D=15\text{ A}$	–	7.5	9.0	m Ω
		$V_{GS}=10\text{ V}$, $I_D=30\text{ A}$	–	6.0	7.4	
Gate resistance ²⁾	R_G	–	–	1.3	–	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics²⁾						
Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$	-	1124	1461	pF
Output capacitance	C_{oss}		-	284	369	
Reverse transfer capacitance	C_{rss}		-	14	21	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=30\text{ A}, R_G=3.5\ \Omega$	-	3.7	-	ns
Rise time	t_r		-	2.3	-	
Turn-off delay time	$t_{d(off)}$		-	5.4	-	
Fall time	t_f		-	3.0	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=30\text{ V}, I_D=30\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	5.0	6.5	nC
Gate to drain charge	Q_{gd}		-	2.9	4.3	
Gate charge total	Q_g		-	15.4	20.0	
Gate plateau voltage	$V_{plateau}$		-	4.6	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ °C}$	-	-	60	A
Diode pulse current ²⁾	$I_{S,pulse}$	$T_C=25\text{ °C}, t_p=100\ \mu\text{s}$	-	-	168	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=30\text{ A}, T_j=25\text{ °C}$	-	0.8	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=30\text{ V}, I_F=50\text{ A}, di_f/dt=100\text{ A}/\mu\text{s}$	-	27	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	16.8	-	nC

¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

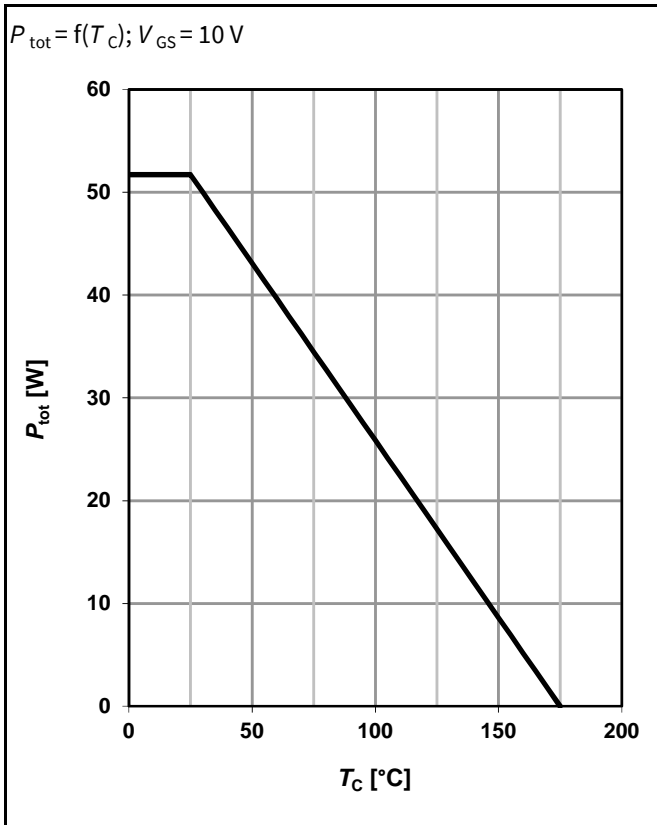
²⁾ The parameter is not subject to production testing – specified by design.

³⁾ Current is limited by the package.

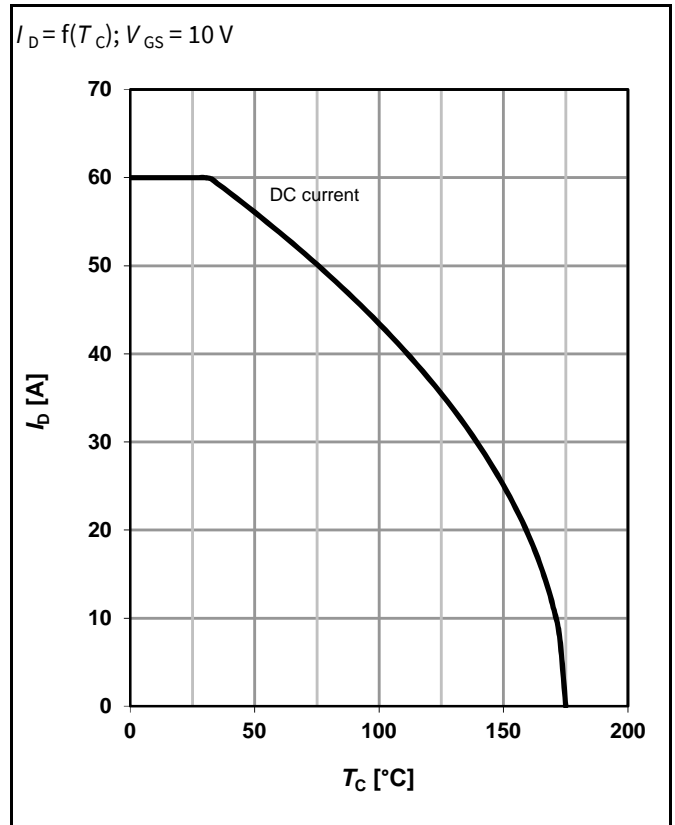
⁴⁾ Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

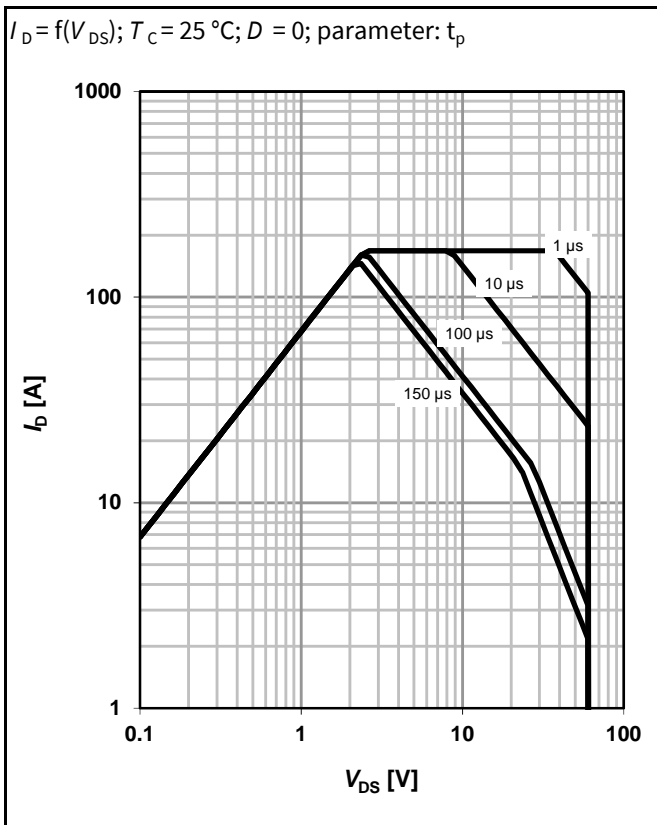
1 Power dissipation



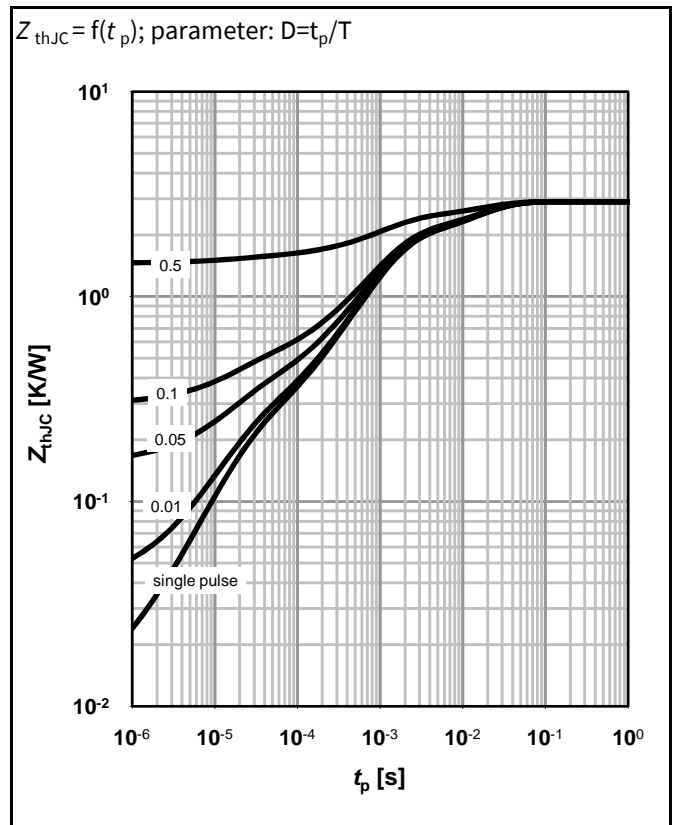
2 Drain current



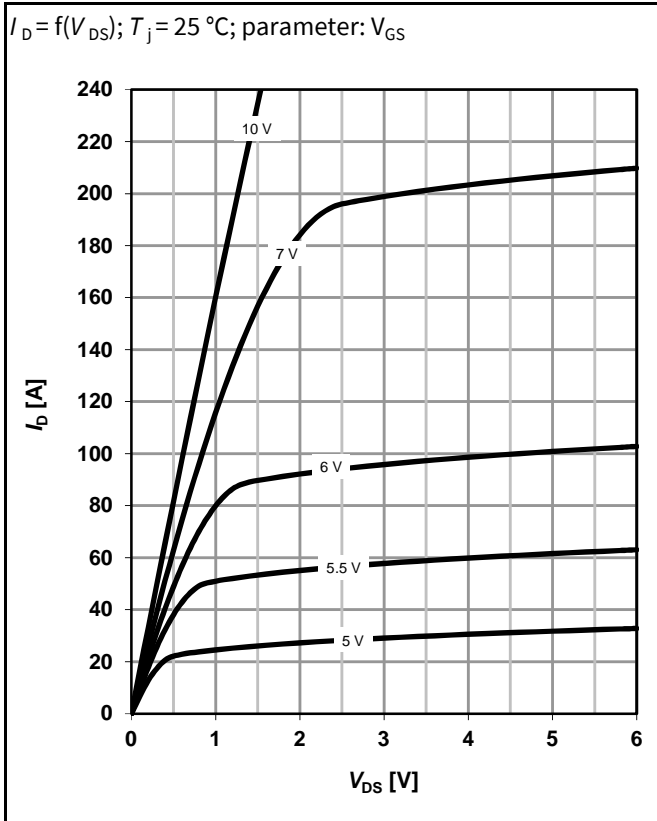
3 Safe operating area



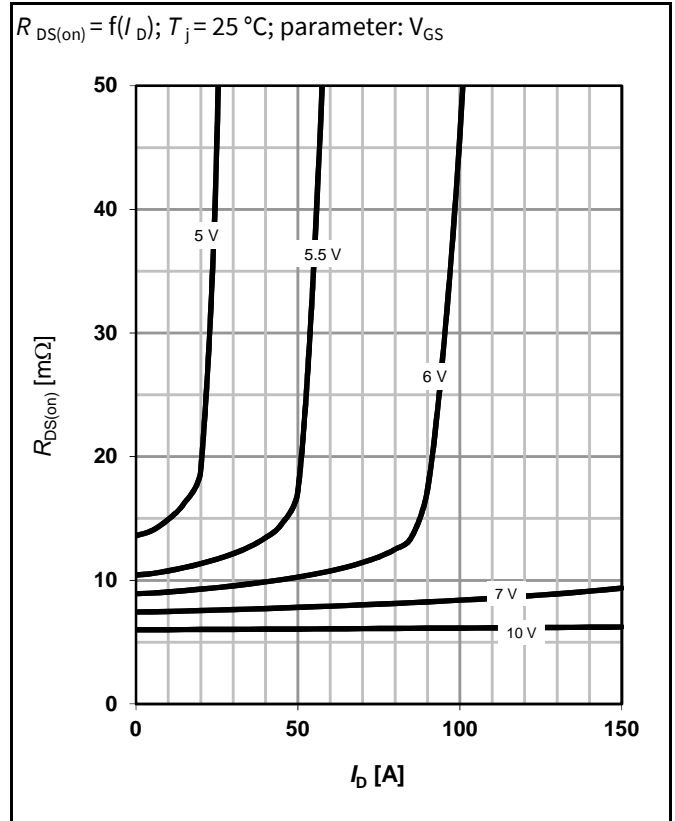
4 Max. transient thermal impedance



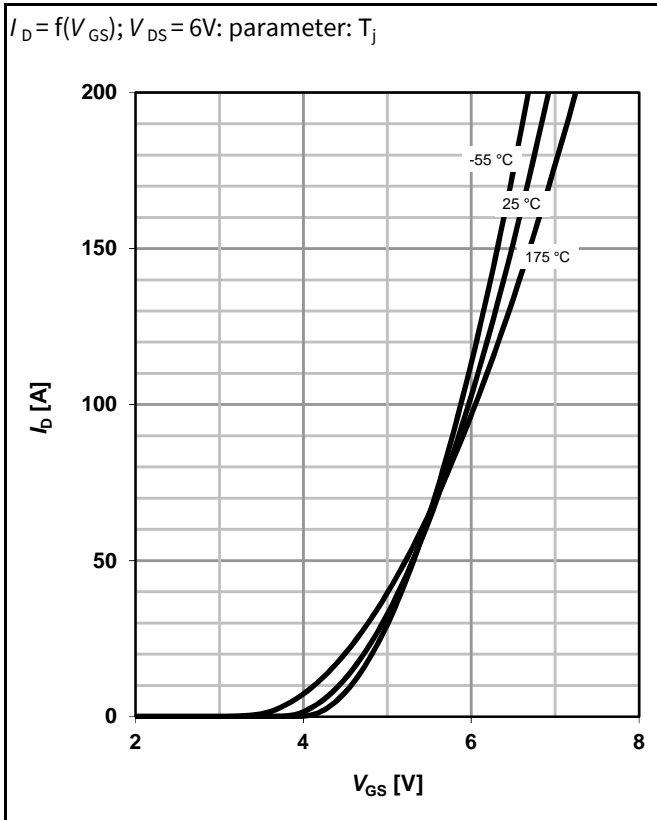
5 Typ. output characteristics



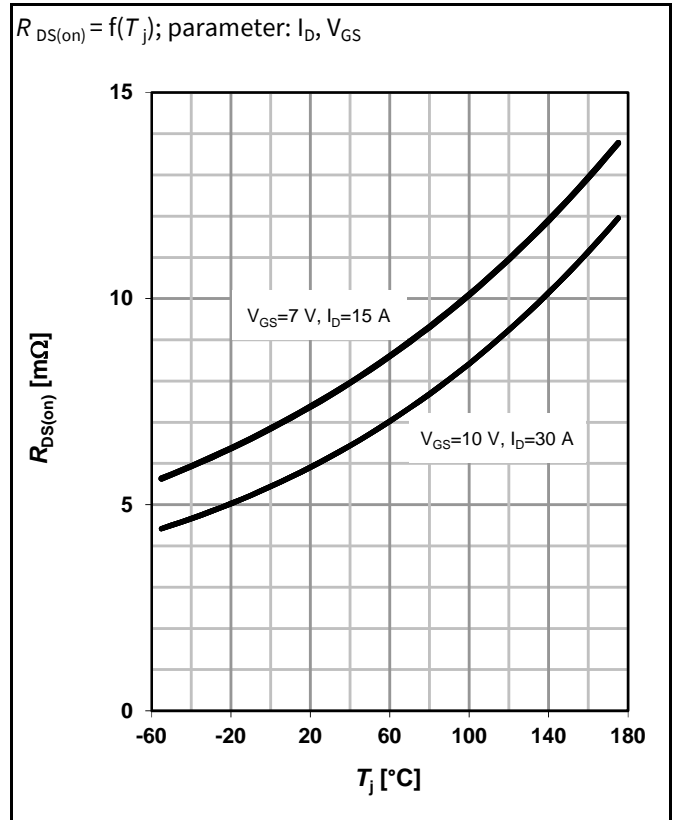
6 Typ. drain-source on-state resistance



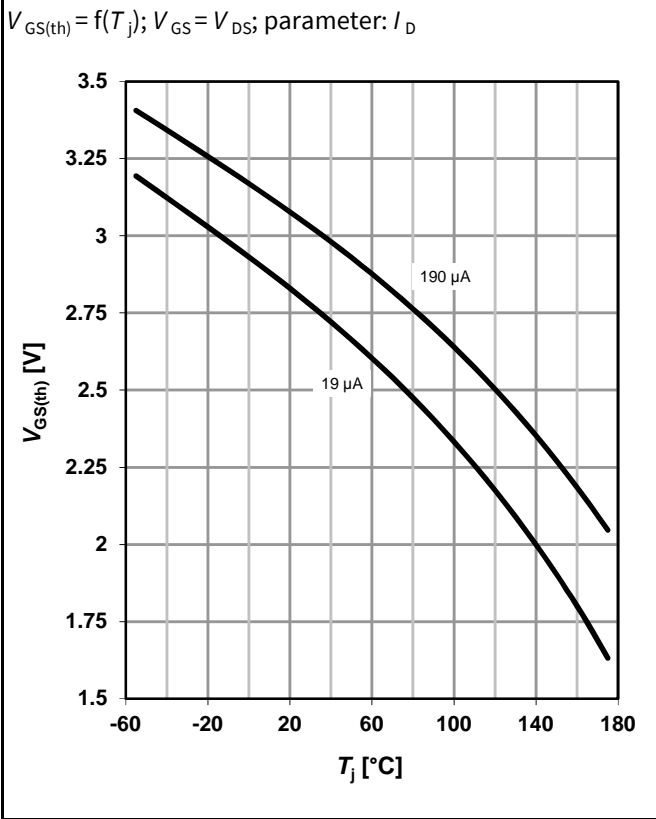
7 Typ. transfer characteristics



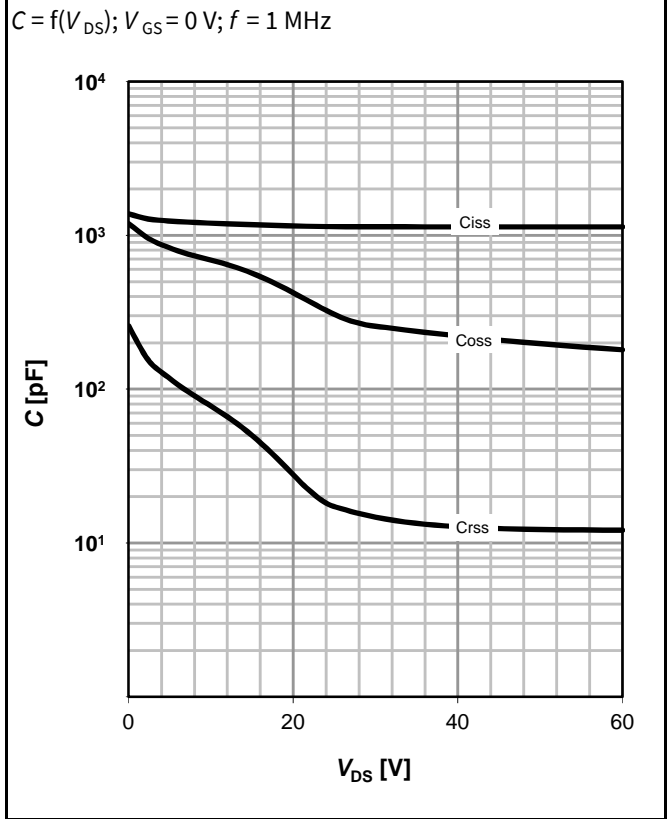
8 Typ. drain-source on-state resistance



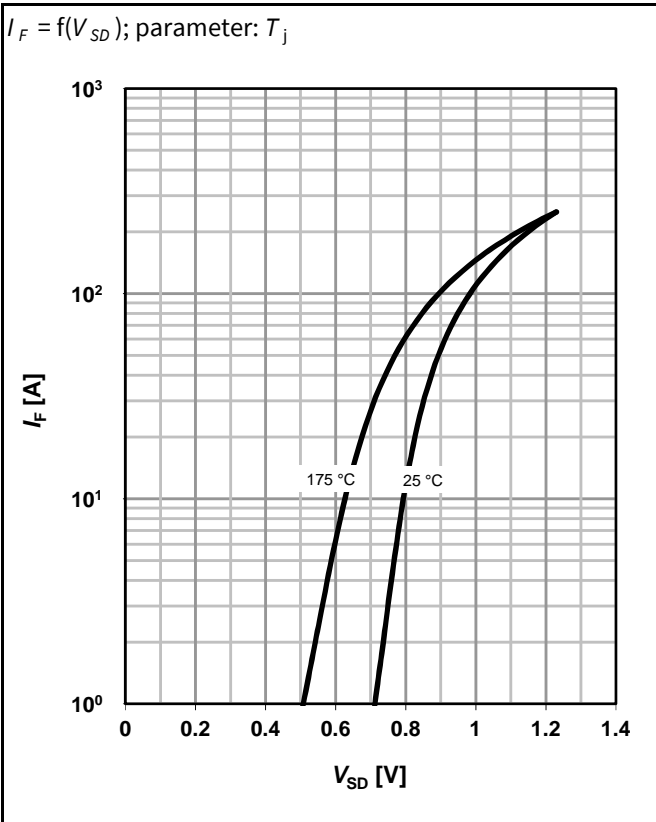
9 Typ. gate threshold voltage



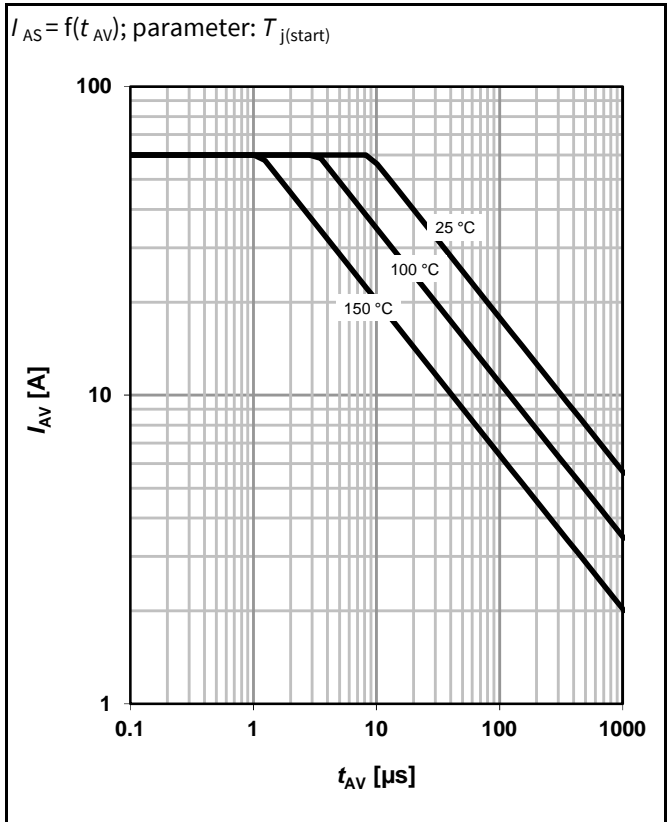
10 Typ. capacitances



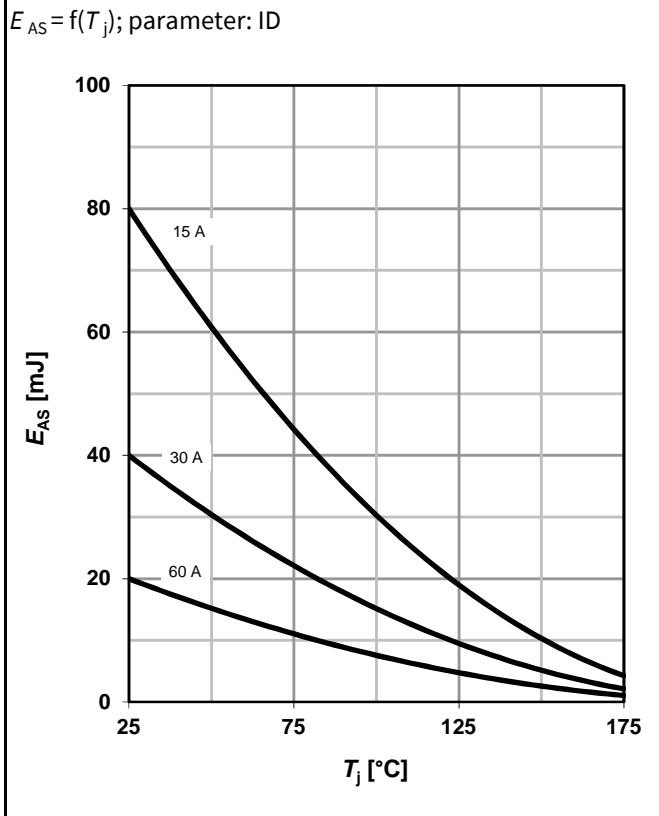
11 Typical forward diode characteristics



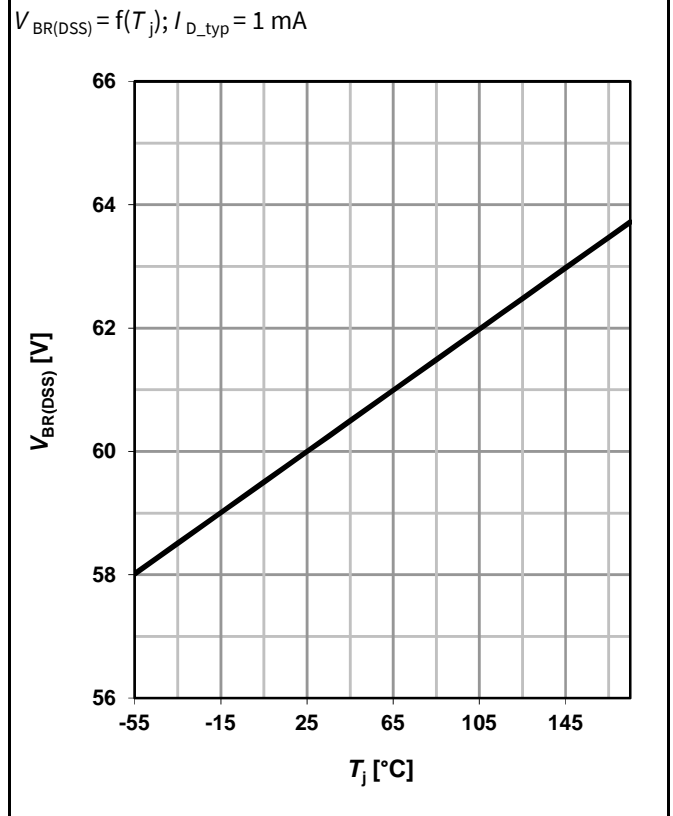
12 Typ. avalanche characteristics



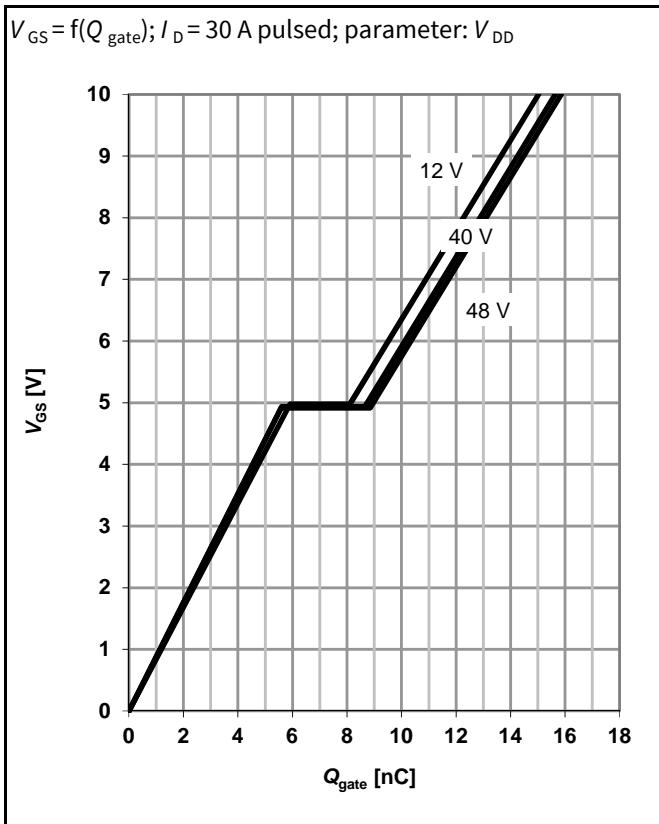
13 Typical avalanche energy



14 Drain-source breakdown voltage



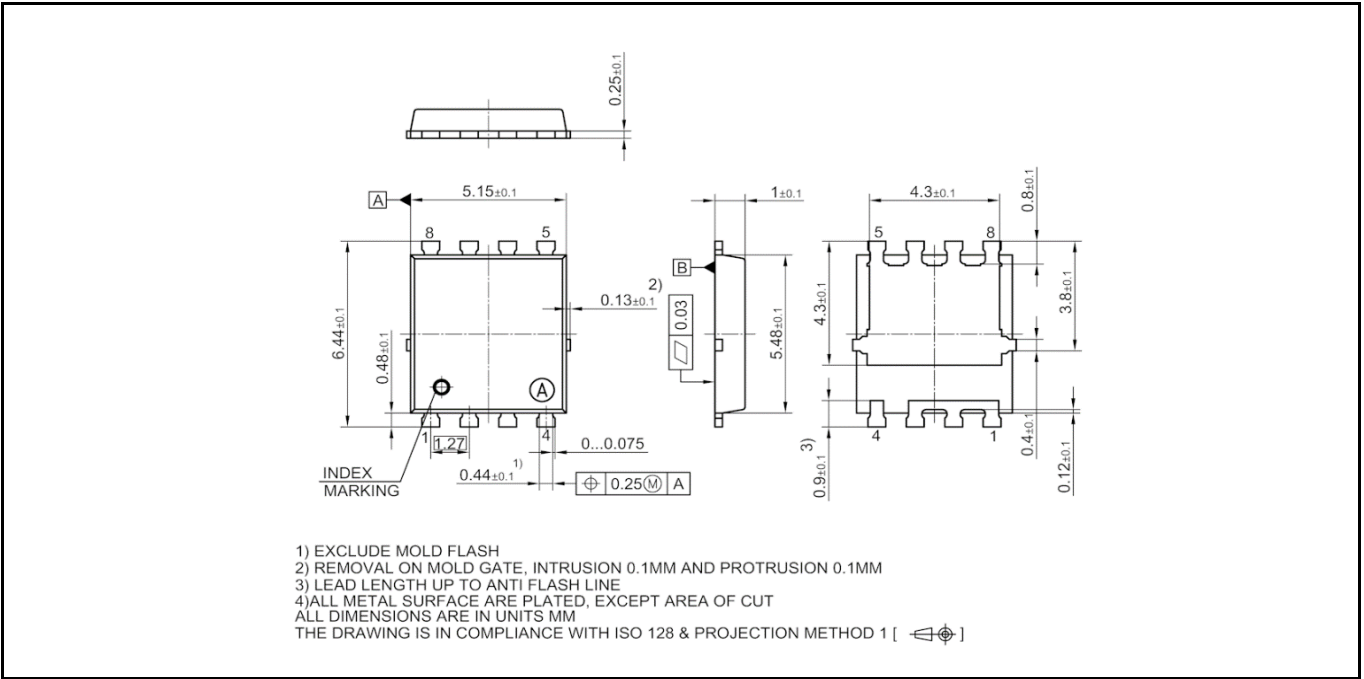
15 Typ. gate charge



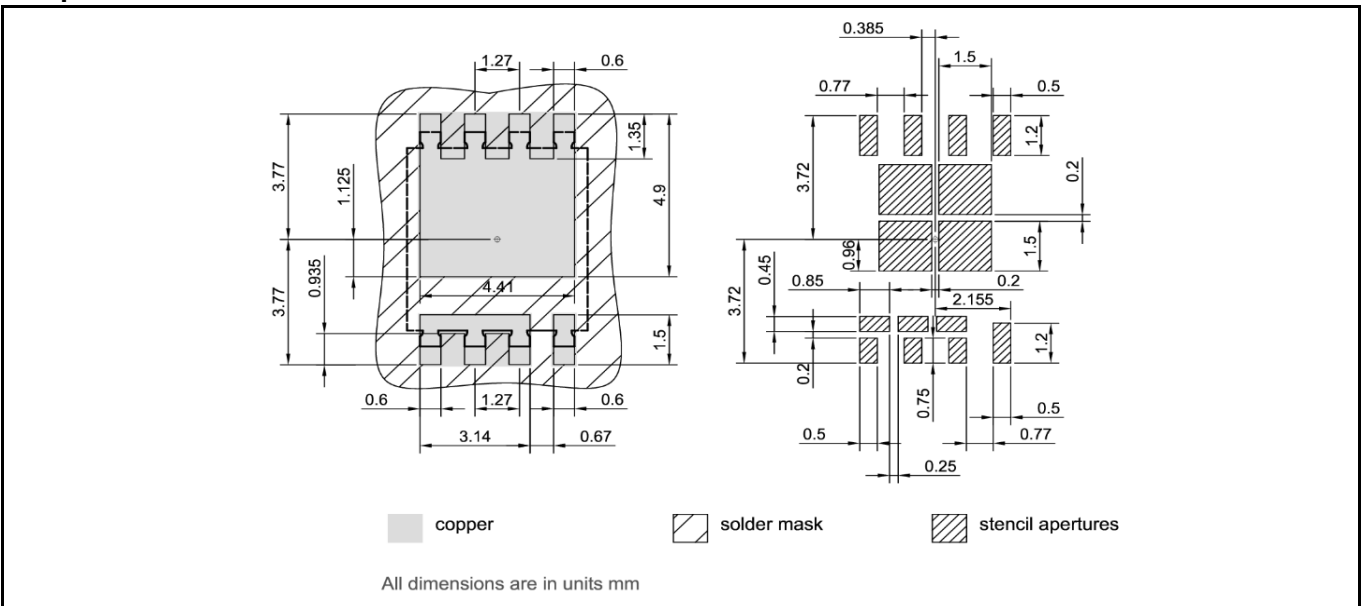
16 Gate charge waveforms



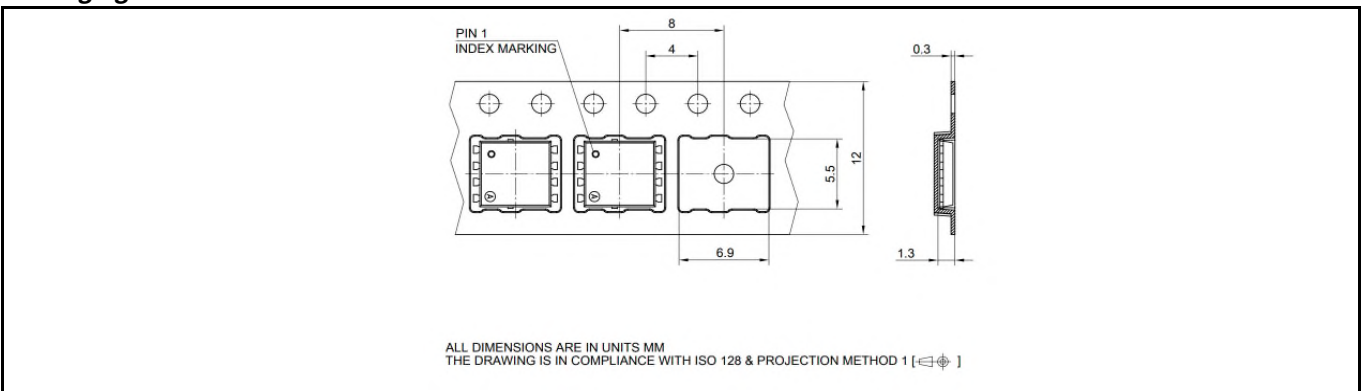
Package Outline



Footprint



Packaging



Revision History

Revision	Date	Changes
Revision 1.0	04.05.2021	final data sheet
Revision 1.1	14.02.2022	update image of pin layout (page 1)

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