

## Automotive MOSFET

## OptiMOS™ 5 Power-Transistor



## Features

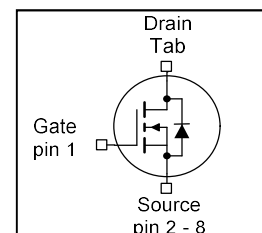
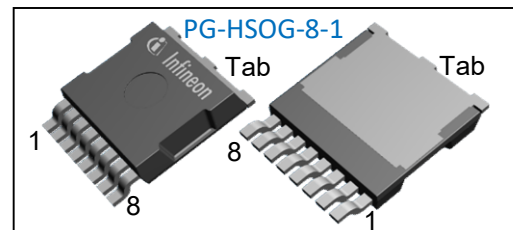
- OptiMOS™ power MOSFET for automotive applications
- N-channel – enhancement mode – normal level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% avalanche tested

## Potential applications

General automotive applications.

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



## Product Summary

$V_{DS}$	60	V
$R_{DS(on)}$	0.78	m $\Omega$
$I_D$ (chip limited)	504	A

Type	Package	Marking
IAUTN06S5N008G	PG-HSOG-8-1	5N06N008



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## Maximum ratings

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}$ , Chip limitation <sup>1,2)</sup>	504	A
		$V_{GS}=10\text{ V}$ , DC current <sup>3)</sup>	350	
		$T_a=100\text{ °C}$ , $V_{GS}=10\text{ V}$ , $R_{thJA}$ on 2s2p <sup>2,4)</sup>	59	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$ , $t_p=100\text{ }\mu\text{s}$	1940	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D=175\text{ A}$	940	mJ
Avalanche current, single pulse	$I_{AS}$	–	350	A
Gate source voltage	$V_{GS}$	–	$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	358	W
Operating and storage temperature	$T_j, T_{stg}$	–	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	–	–	55/175/56	

## Thermal characteristics<sup>2)</sup>

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	$R_{thJC}$	–	–	–	0.42	K/W
Thermal resistance, junction - ambient <sup>4)</sup>	$R_{thJA}$	–	–	14.8	–	

## Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$	60	–	–	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=275\text{ }\mu\text{A}$	2.2	2.6	3.0	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$	–	0.1	1	$\mu\text{A}$
		$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=100\text{ °C}^{2)}$	–	10	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=7\text{ V}$ , $I_D=50\text{ A}$	–	0.76	0.89	m $\Omega$
		$V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$	–	0.64	0.78	
Gate resistance <sup>2)</sup>	$R_G$	–	–	1.8	–	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Dynamic characteristics<sup>2)</sup></b>						
Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$	-	15600	20280	pF
Output capacitance	$C_{oss}$		-	3200	4160	
Reverse transfer capacitance	$C_{rss}$		-	110	165	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=100\text{ A}, R_G=3.5\ \Omega$	-	42	-	ns
Rise time	$t_r$		-	58	-	
Turn-off delay time	$t_{d(off)}$		-	111	-	
Fall time	$t_f$		-	86	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=30\text{ V}, I_D=100\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	64	83	nC
Gate to drain charge	$Q_{gd}$		-	36	54	
Gate charge total	$Q_g$		-	210	273	
Gate plateau voltage	$V_{plateau}$		-	4.1	-	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25\text{ °C}$	-	-	504	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	$T_C=25\text{ °C}, t_p=100\ \mu\text{s}$	-	-	1940	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_J=25\text{ °C}$	-	0.82	0.92	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=30\text{ V}, I_F=50\text{ A}, di_f/dt=100\text{ A}/\mu\text{s}$	-	57	86	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	64	128	

<sup>1)</sup> Practically the current is limited by the overall system design including the customer-specific PCB.

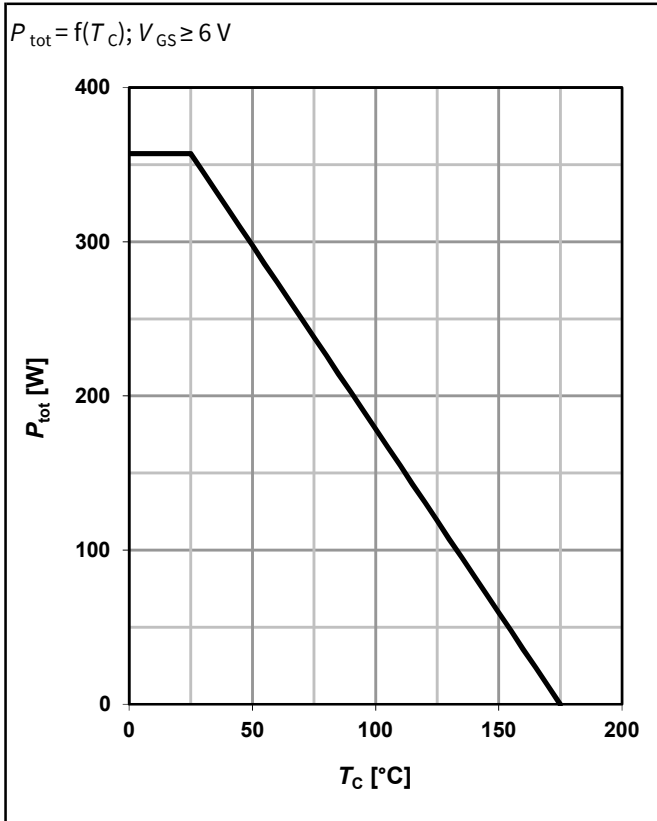
<sup>2)</sup> The parameter is not subject to production testing – specified by design.

<sup>3)</sup> Current is limited by package.

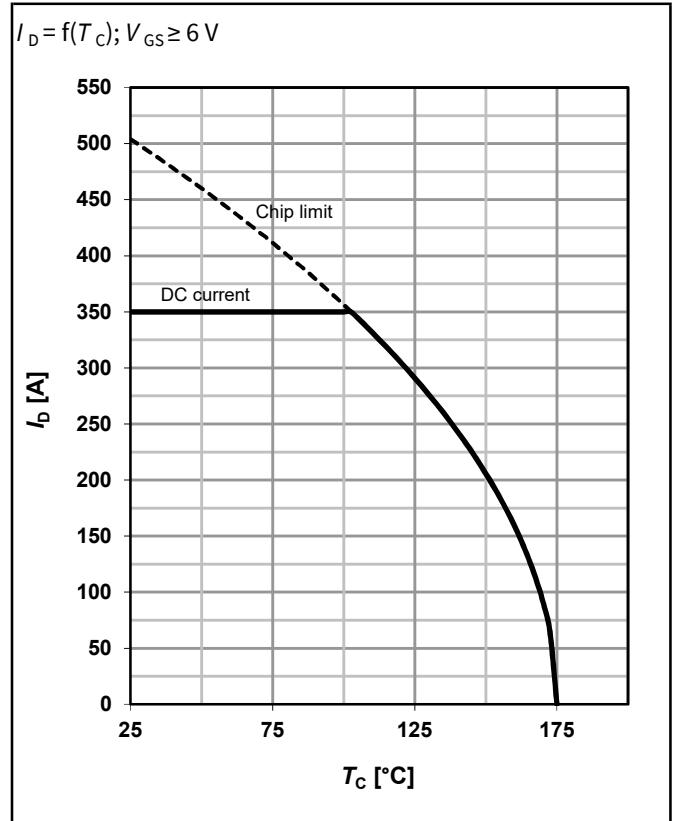
<sup>4)</sup> Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

## Electrical characteristics diagrams

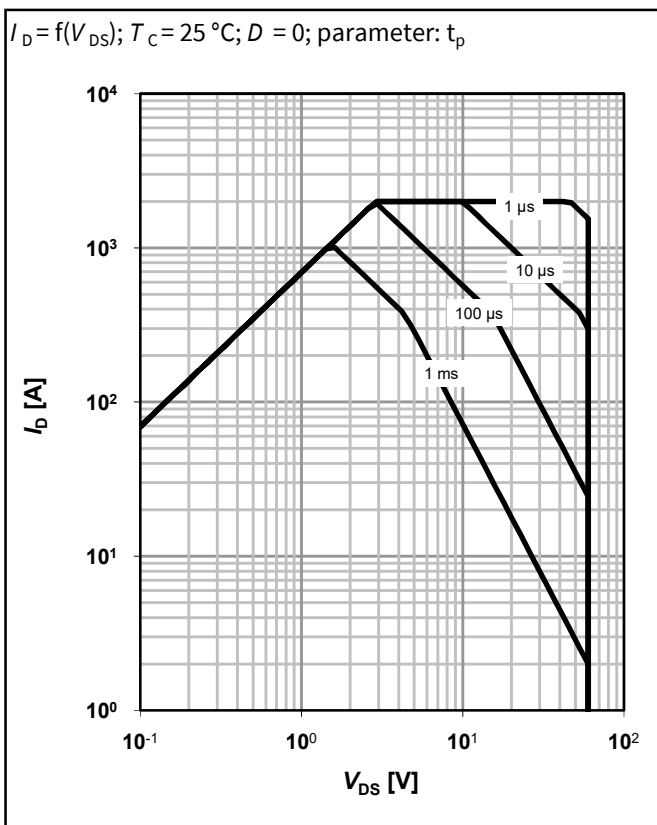
### 1 Power dissipation



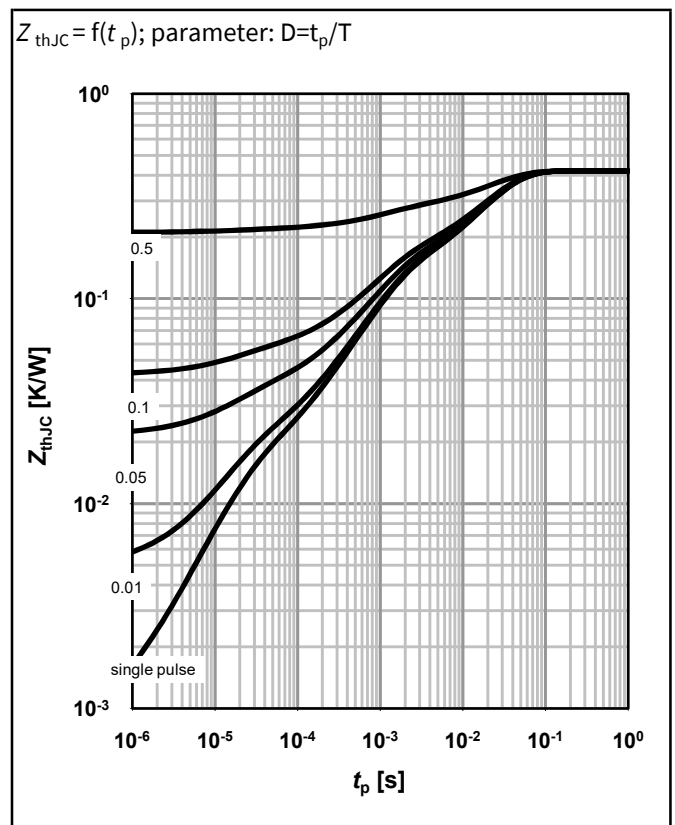
### 2 Drain current



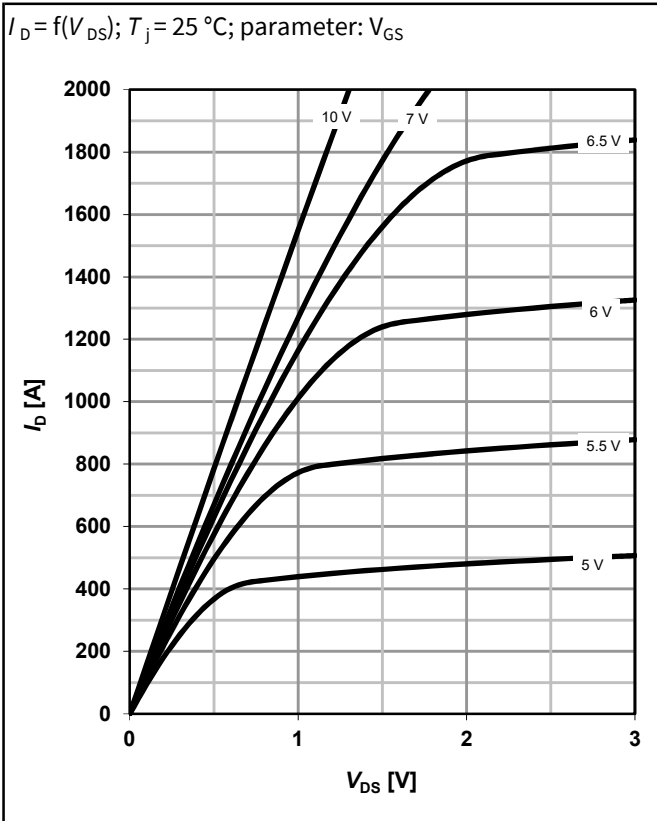
### 3 Safe operating area



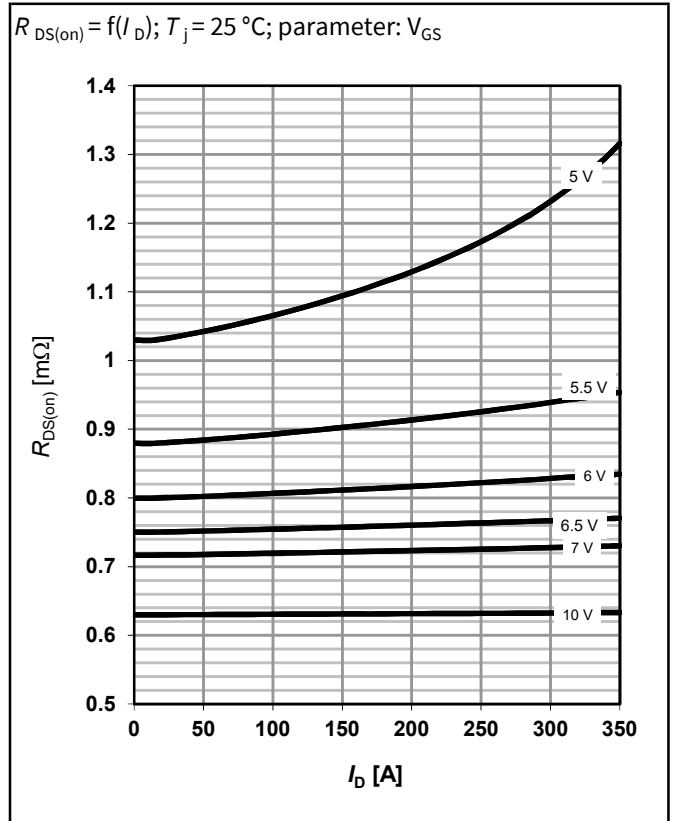
### 4 Max. transient thermal impedance



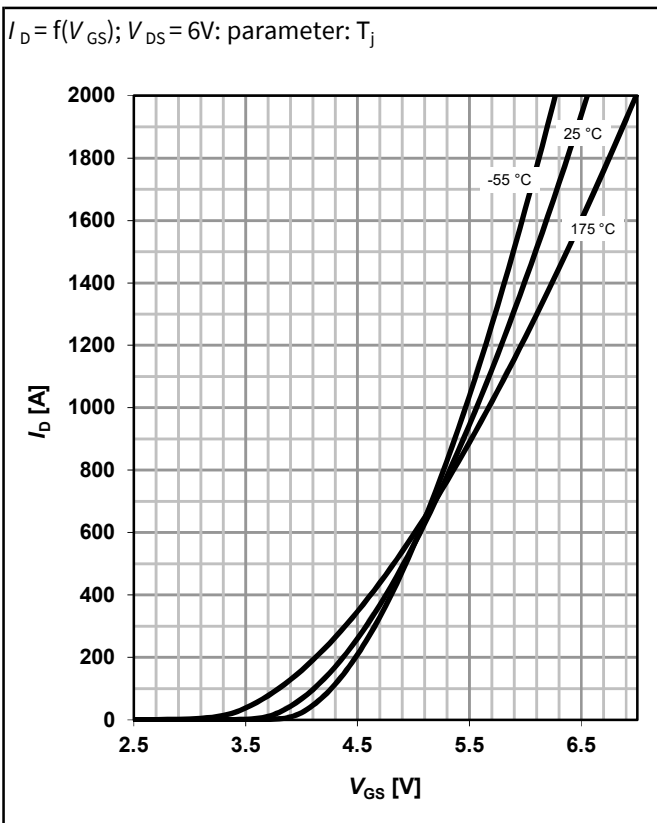
5 Typ. output characteristics



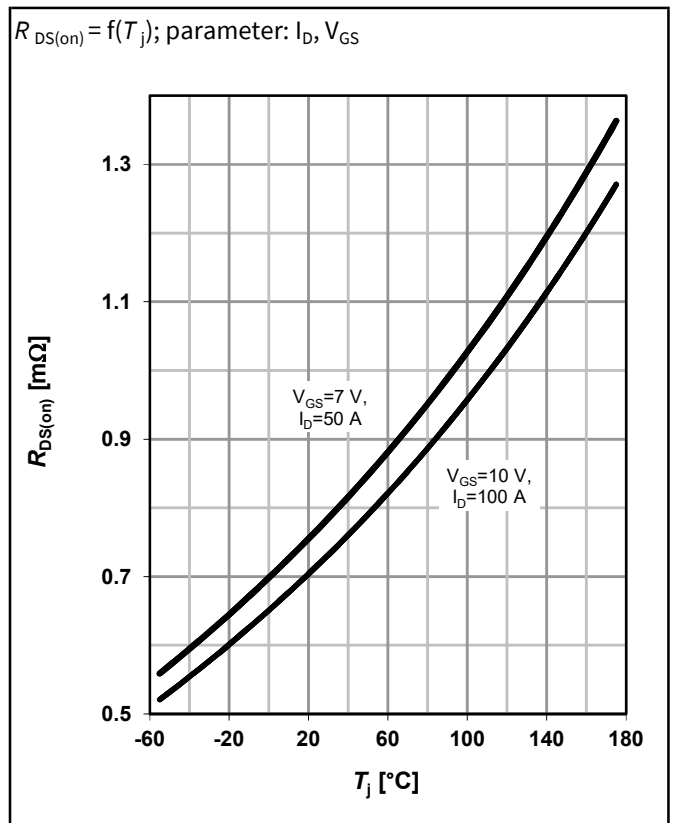
6 Typ. drain-source on-state resistance



7 Typ. transfer characteristics

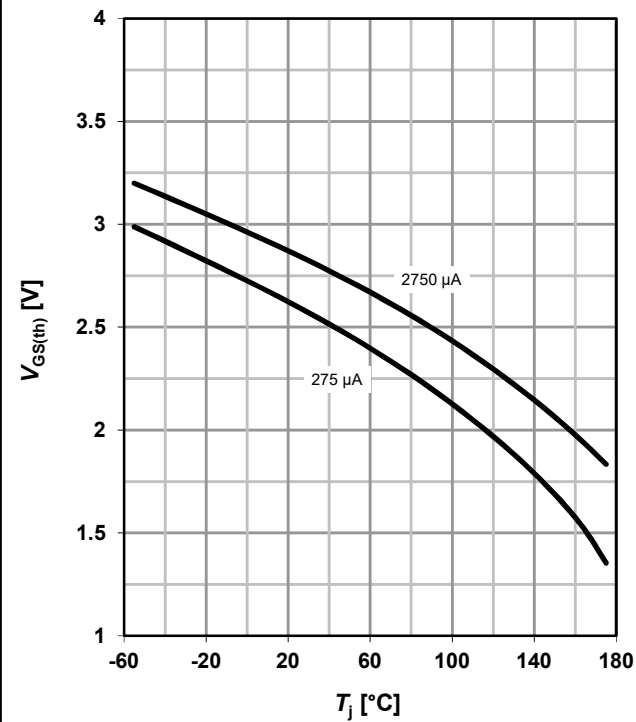


8 Typ. drain-source on-state resistance



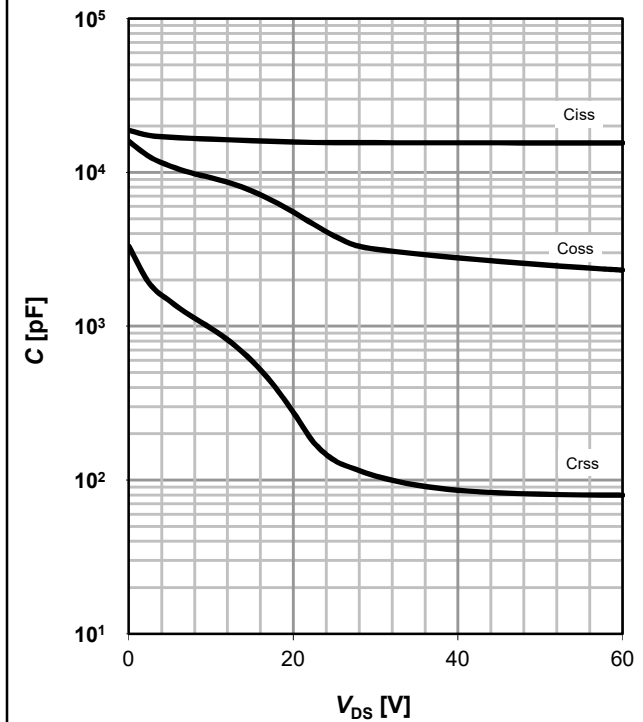
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; \text{parameter: } I_D$



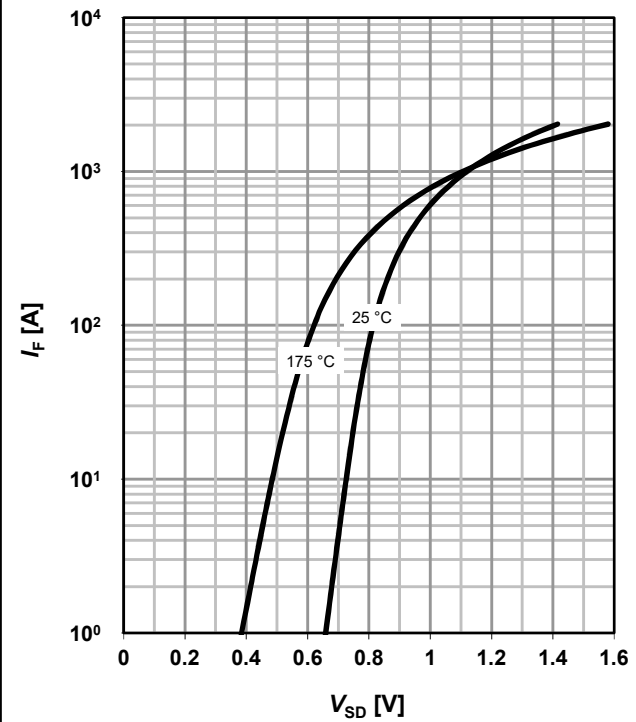
10 Typ. capacitances

$C = f(V_{DS}); V_{GS} = 0 V; f = 1 \text{ MHz}$



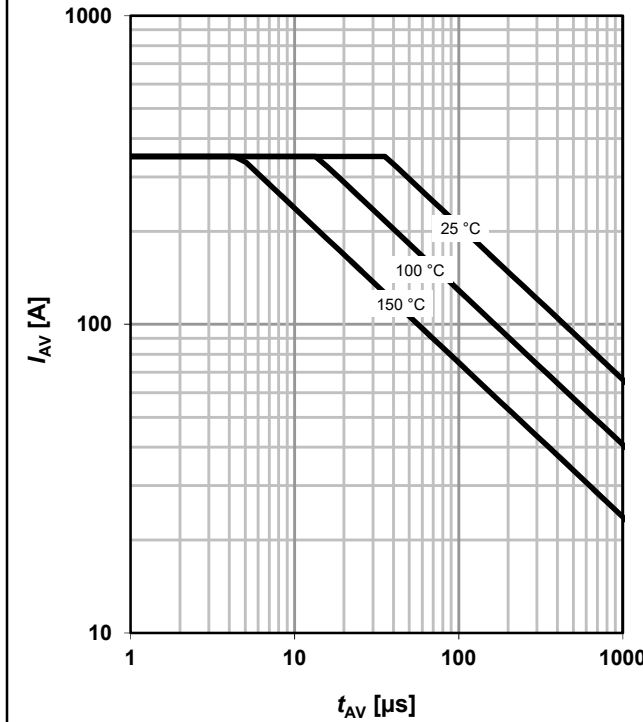
11 Typical forward diode characteristics

$I_F = f(V_{SD}); \text{parameter: } T_j$



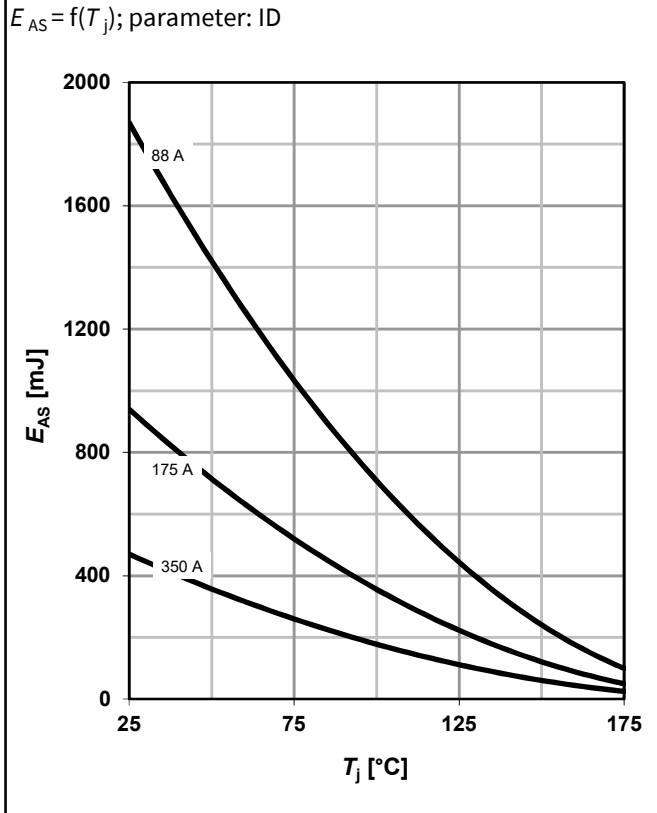
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV}); \text{parameter: } T_{j(start)}$

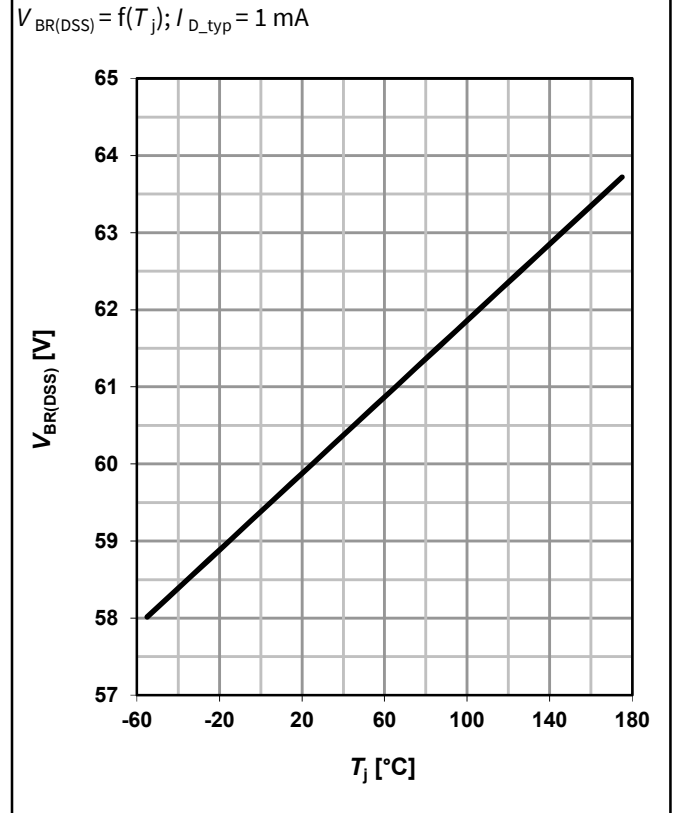




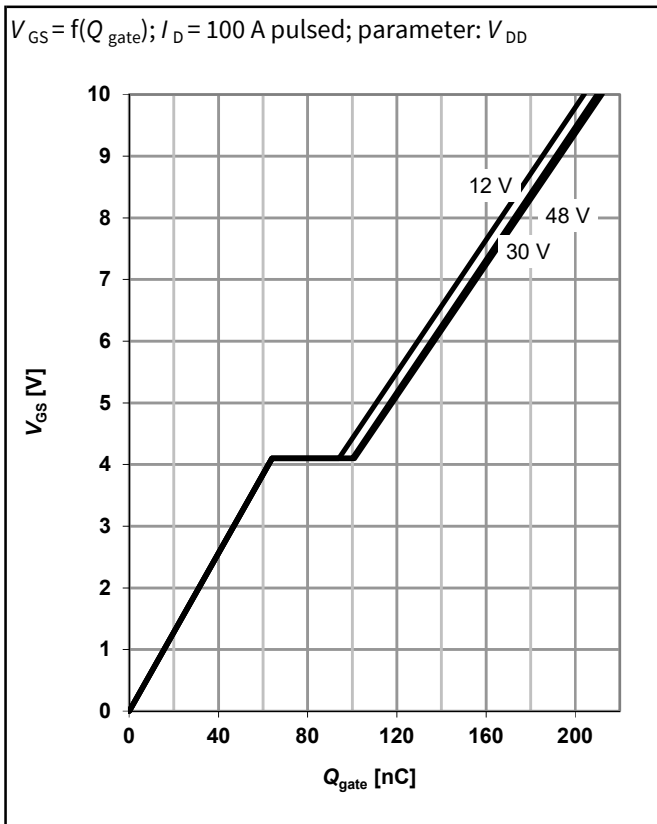
### 13 Typical avalanche energy



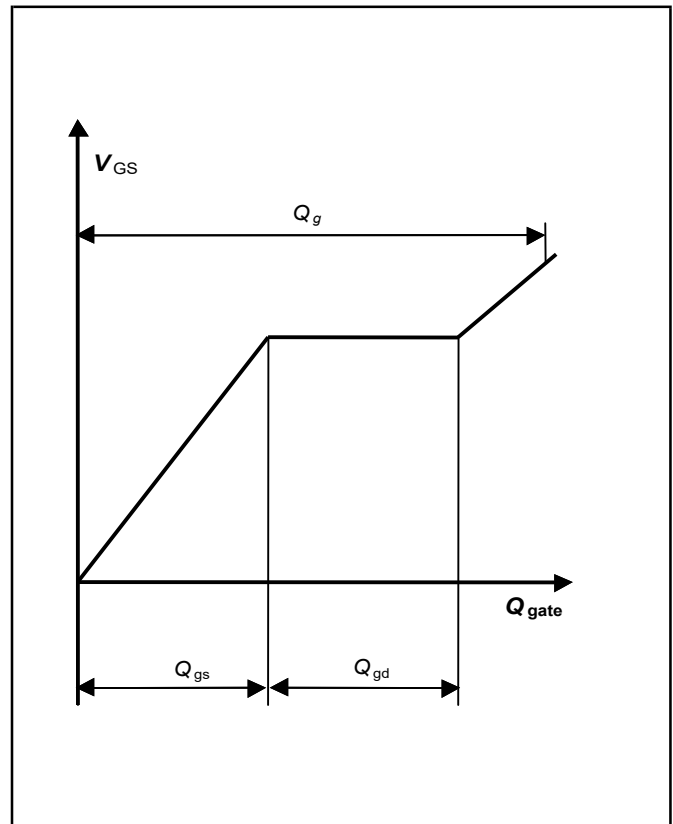
### 14 Drain-source breakdown voltage



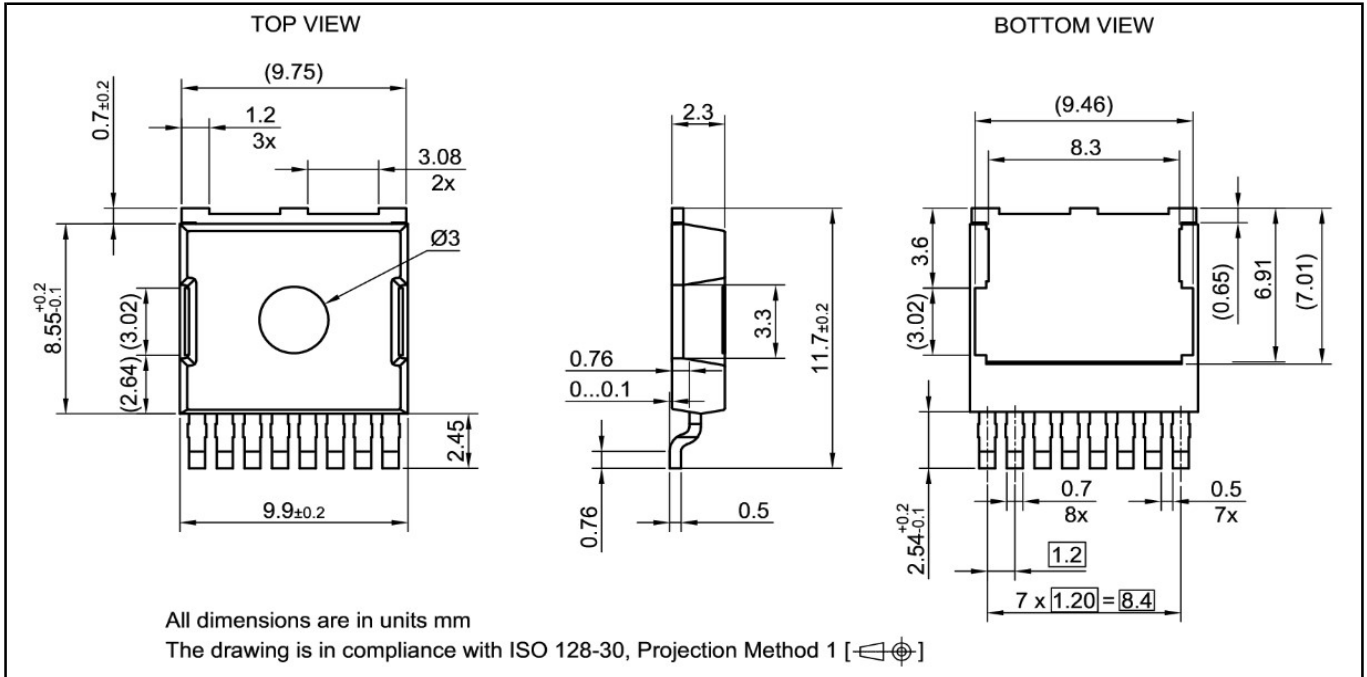
### 15 Typ. gate charge



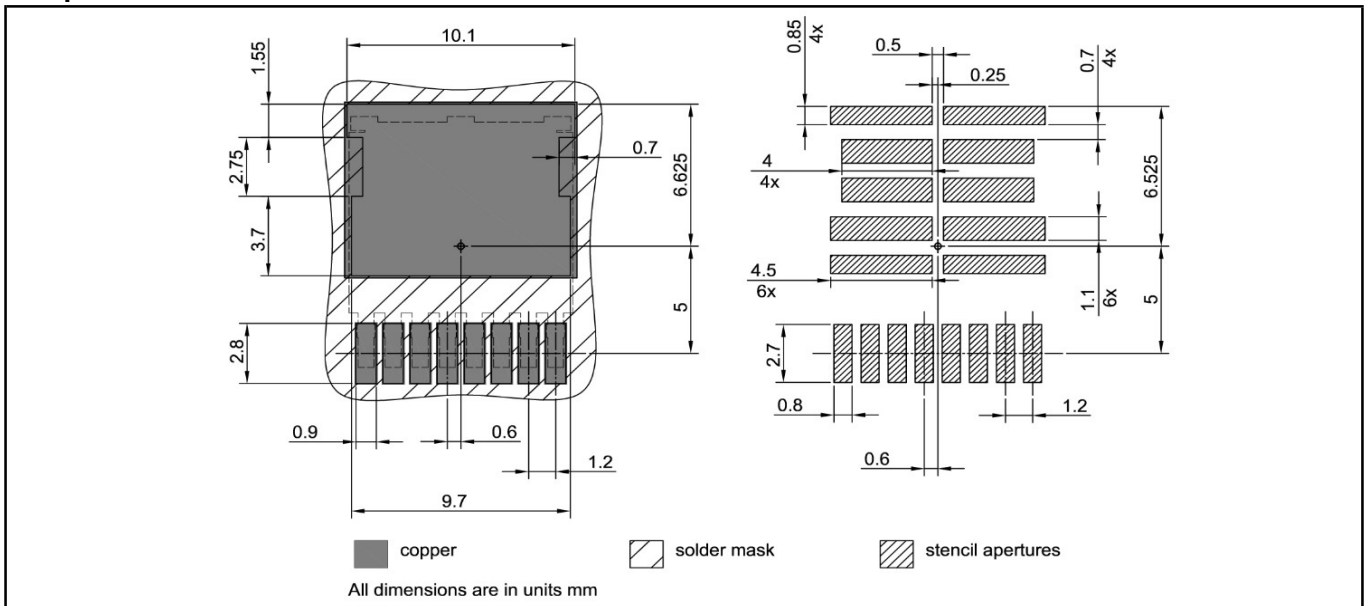
### 16 Gate charge waveforms



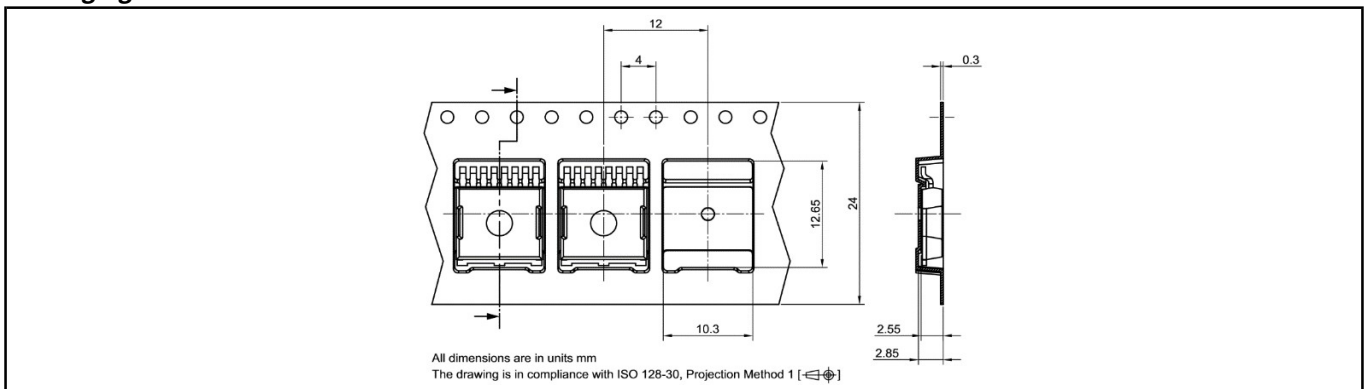
## Package Outline



## Footprint



## Packaging





**Revision History**

Revision	Date	Changes
Revision 1.0	2023-02-07	Final data sheet

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