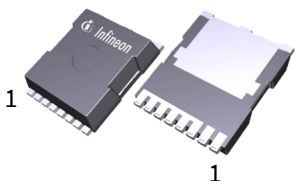
Automotive MOSFET

OptiMOS™ 5 Power-Transistor

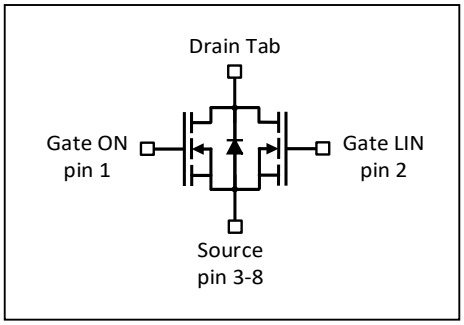
RoHS Infineon Automotive Quality AEC Qualified

PG-HSOF-8-2



Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- Linear FET (LINFET) and low $R_{DS(on)}$ FET (ONFET) in one package
- Dedicated gate pins for both MOSFETs (Dual Gate)
- Linear FET with enhanced SOA and paralleling characteristics for linear operation
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested
- MSL1 up to 260°C peak reflow



Potential applications

- Power distribution and battery management (electronic fuses and disconnect switches)
- In-rush current limitation (capacitor charging, motor surge current)
- Slow switching to minimize voltage transients and EMI (electrical catalyst heater)
- Drain-source voltage clamping (dissipation of inductive energy, over-voltage protection)

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product summary

V_{DS}	80	V
$R_{DS(on),max}$	1.15	mΩ
I_D (chip limited)	410	A

Type	Package	Marking
IAUTN08S5N012L	PG-HSOF-8-2	5N0812L

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Maximum ratings

at T_j = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Drain current	I_D	$V_{GS,LIN} = V_{GS,ON}$ = 10 V, T_c = 25 °C, chip limitation[1,2)]	410	A
		$V_{GS,LIN} = V_{GS,ON}$ = 10 V, T_c = 25 °C, DC current[3)]	300	
		$V_{GS,LIN} = V_{GS,ON}$ = 10 V, T_c = 85 °C, R_{thja} on 2s2p[2,4)]	52	
Pulsed drain current	$I_{D,pulse}$	$V_{GS,LIN} = V_{GS,ON}$ = 10 V, T_c = 25 °C, t_p = 100 µs[2)]	1505	
Avalanche energy, single pulse[2)]	E_{AS}	I_D = 150 A	820	mJ
Avalanche current, single pulse	I_{AS}	–	300	A
Gate source voltage, LINFET	$V_{GS,LIN}$	–	± 20	V
Gate source voltage, ONFET	$V_{GS,ON}$	–	± 20	V
Power dissipation	P_{tot}	T_C = 25 °C, $V_{GS,LIN} = V_{GS,ON}$ = 10 V	375	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C

Thermal characteristics[2)]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	–	0.40	K/W
Thermal resistance, junction - ambient[3)]	R_{thJA}	–	–	14.8	–	

Electrical characteristics

at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Static characteristics						
Drain-source breakdown voltage	$V_{(Br)DSS}$	$V_{GS,ON} = V_{GS,LIN} = 0$ V, $I_D = 1$ mA	80	–	–	V
Current limit precision	$I_{D(lim)}$	$V_{DS} = 6$ V, $V_{GS,ON} = 0$ V, $V_{GS,LIN} = 5.6$ V	15	39	57	A
		$V_{DS} = 6$ V, $V_{GS,ON} = 0$ V, $V_{GS,LIN} = 6.2$ V	35	65	87	A
		$V_{DS} = 48$ V, $V_{GS,ON} = 0$ V, $V_{GS,LIN} = 5.6$ V	25	48	66	A
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS,LIN}$, $V_{GS,ON} = 0$ V, $I_D = 22$ µA	2.5	2.9	3.3	V
		$V_{DS} = V_{GS,ON} = V_{GS,LIN}$, $I_D = 275$ µA	2.5	2.9	3.3	
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 80$ V, Tj = 25 °C, $V_{GS,ON} = V_{GS,LIN} = 0$ V	–	–	1	µA
		$V_{DS} = 50$ V, Tj = 85 °C, $V_{GS,ON} = V_{GS,LIN} = 0$ V[2)]	–	–	20	
Gate-source leakage current LINFET	$I_{GSS,LIN}$	$V_{GS,LIN} = 20$ V	–	–	100	nA
Gate-source leakage current ONFET	$I_{GSS,ON}$	$V_{GS,ON} = 20$ V	–	–	100	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS,ON} = V_{GS,LIN} = 6$ V, $I_D = 75$ A	–	1.30	1.80	mΩ
		$V_{GS,ON} = V_{GS,LIN} = 10$ V, $I_D = 100$ A	–	1.00	1.15	
		$V_{GS,ON} = 0$ V, $V_{GS,LIN} = 6$ V, $I_D = 3.75$ A	–	11.0	16.0	
		$V_{GS,ON} = 0$ V, $V_{GS,LIN} = 10$ V, $I_D = 5$ A	–	6.0	9.0	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance ON- and LINFET	$C_{iss,ON+LIN}$	$V_{GS,ON} = V_{GS,LIN} = 0$ V, $V_{DS} = 40$ V, $f = 1$ MHz, refers to pins Gate ON and Gate LIN short-circuited	–	11800	15340	pF
Output capacitance ON- and LINFET	$C_{oss,ON+LIN}$		–	2100	2730	
Reverse transfer capacitance ON- and LINFET	$C_{rss,ON+LIN}$		–	91	137	
Input capacitance LINFET	$C_{iss,LIN}$	$V_{GS,ON} = V_{GS,LIN} = 0$ V, $V_{DS} = 40$ V, $f = 1$ MHz, refers to pin Gate LIN	–	1200	1560	
Output capacitance LINFET	$C_{oss,LIN}$		–	2100	2730	
Reverse transfer capacitance LINFET	$C_{rss,LIN}$		–	16	24	
Gate charge characteristics[2]						
Gate to source charge ON- and LINFET	$Q_{gs,ON+LIN}$	$V_{DD} = 40$ V, $I_D = 100$ A, $V_{GS,ON} = V_{GS,LIN} = 0$ to 10 V	–	51	66	nC
Gate to drain charge ON- and LINFET	$Q_{gd,ON+LIN}$		–	44	66	
Gate charge total ON- and LINFET	$Q_{g,ON+LIN}$		–	178	231	
Gate to source charge LINFET	$Q_{gs,LIN}$	$V_{DD} = 40$ V, $I_D = 5$ A, $V_{GS,LIN} = 0$ to 10 V, $V_{GS,ON} = 0$ V	–	5.2	6.8	
Gate to drain charge LINFET	$Q_{gd,LIN}$		–	4.7	7.1	
Gate charge total LINFET	$Q_{g,LIN}$		–	19	24	
Reverse diode						
Diode continous forward current[2]	I_S	$T_C = 25$ °C	–	–	300	A
Diode pulse current[2]	$I_{S,pulse}$	$T_C = 25$ °C, $t_p = 100$ µs	–	–	1505	
Diode forward voltage	V_{SD}	$I_F = 100$ A, $T_j = 25$ °C	–	0.8	1.1	V
Reverse recovery time[2]	t_{rr}	$V_R = 40$ V, $I_F = 50$ A, $di_F/dt = 100$ A/µs	–	86	–	ns
Reverse recovery charge[2]	Q_{rr}		–	177	–	nC

[1] Current is limited by the overall system design and the customer-specific PCB.

[2] The parameter is not subject to production testing – specified by design.

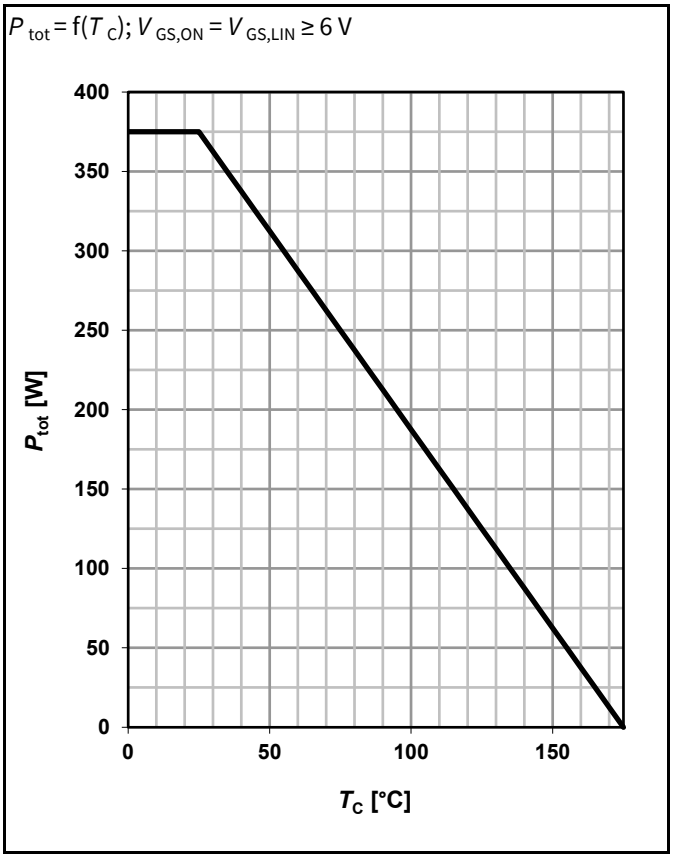
[3] Current is limited by the bond wires.

[4] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

Electrical characteristics diagrams

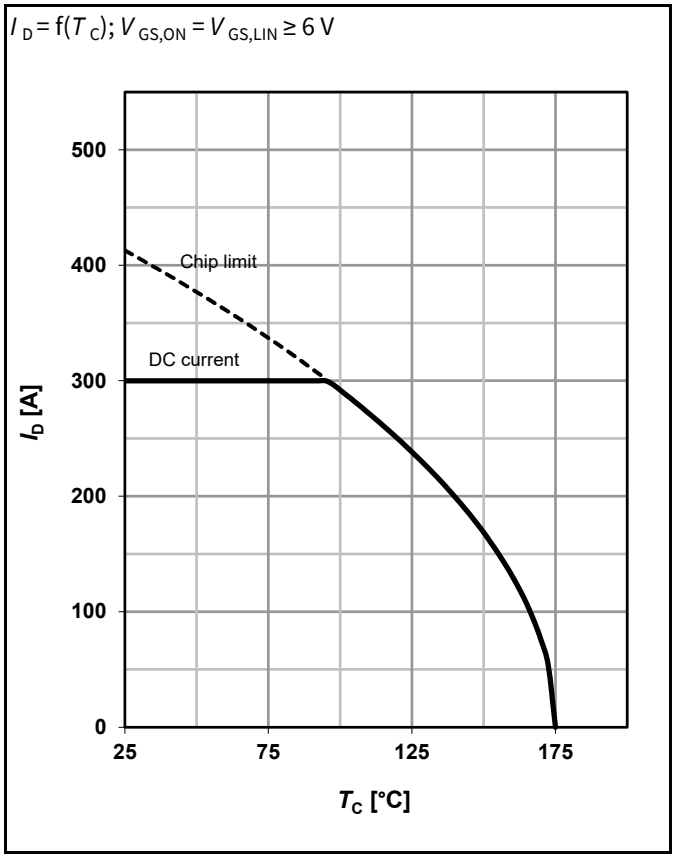
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS,ON} = V_{GS,LIN} \geq 6$ V



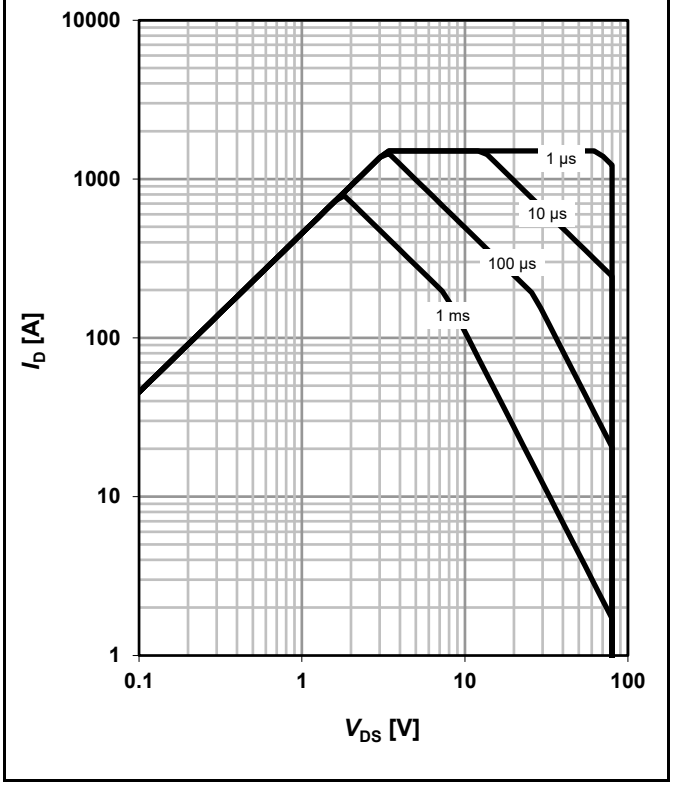
2 Drain current

$I_D = f(T_C)$; $V_{GS,ON} = V_{GS,LIN} \geq 6$ V



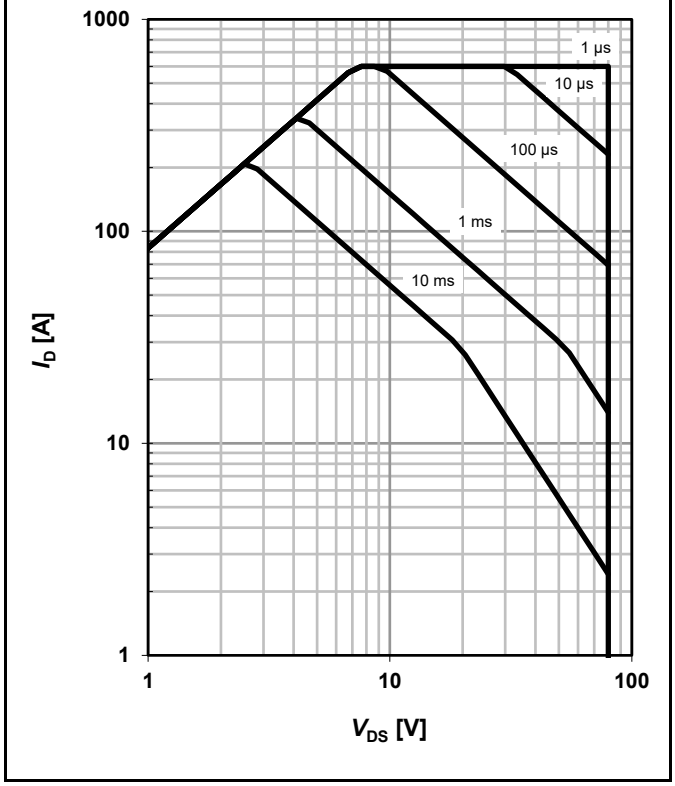
3 Safe operating area ONFET and LINFET

$I_D = f(V_{DS})$; $T_C = 25$ °C; $V_{GS,LIN} = V_{GS,ON}$; $D = 0$; parameter: t_p



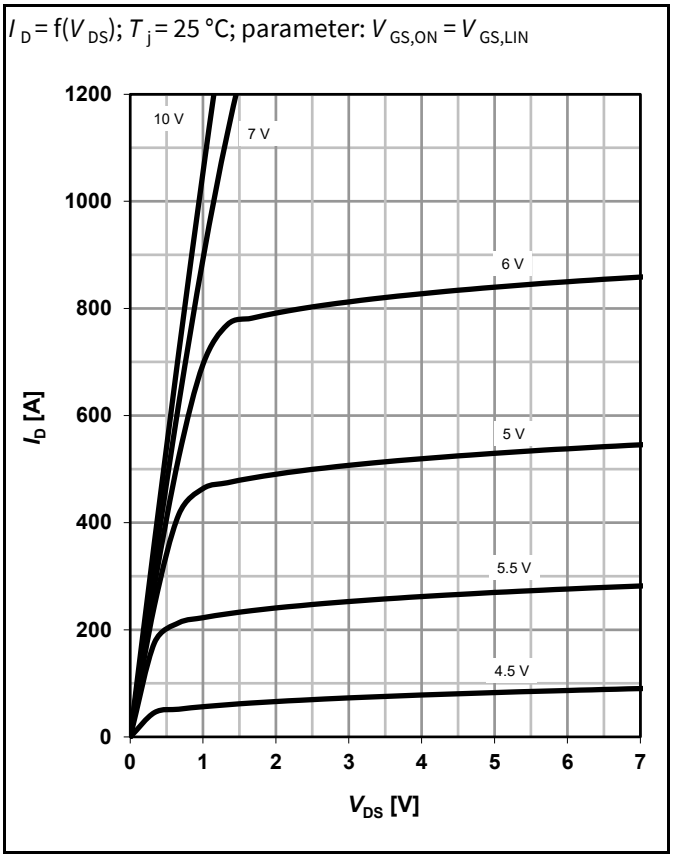
4 Safe operating area LINFET

$I_D = f(V_{DS})$; $T_C = 25$ °C; $V_{GS,ON} = 0$ V; D = 0; parameter: t_p



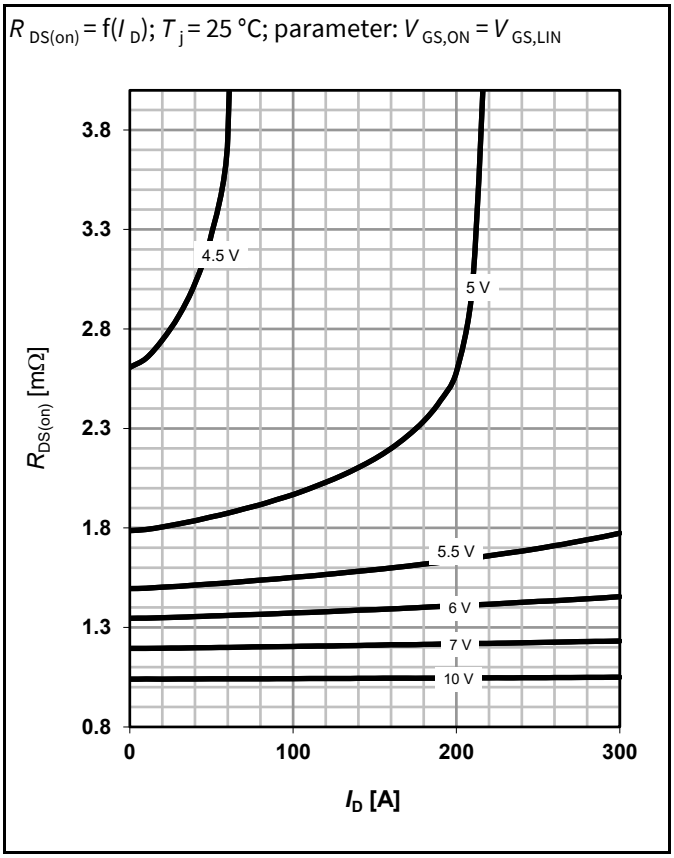
5 Typ. output characteristics ONFET and LINFET

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: $V_{GS,ON} = V_{GS,LIN}$



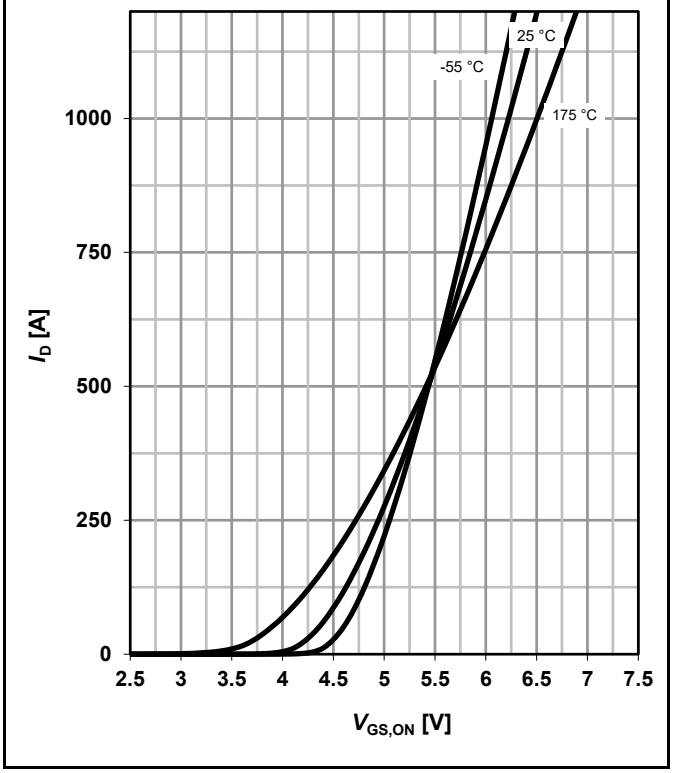
6 Typ. drain-source on-state resistance ONFET and LINFET

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: $V_{GS,ON} = V_{GS,LIN}$



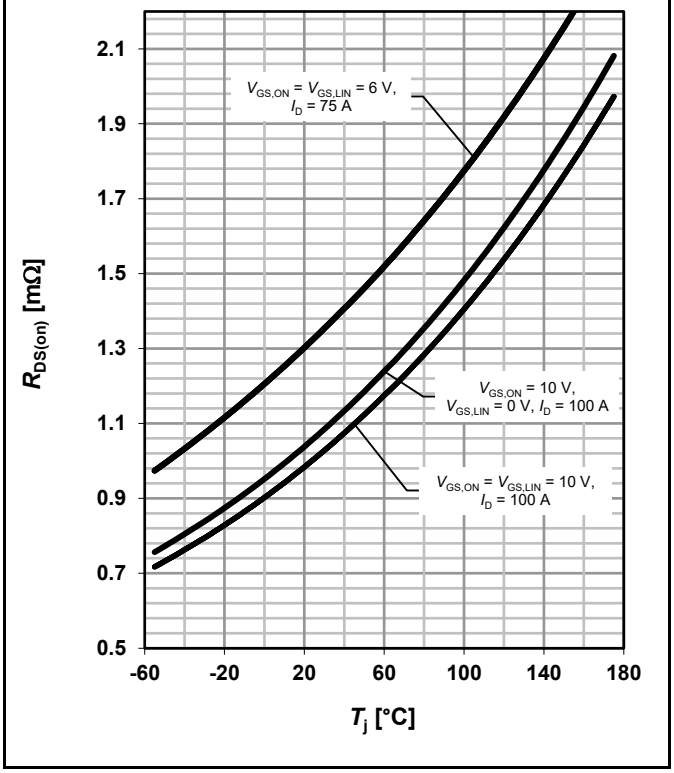
7 Typ. transfer characteristics ONFET and LINFET

$I_D = f(V_{GS,ON})$; $V_{DS} = 6$ V; $V_{GS,ON} = V_{GS,LIN}$; parameter: T_j

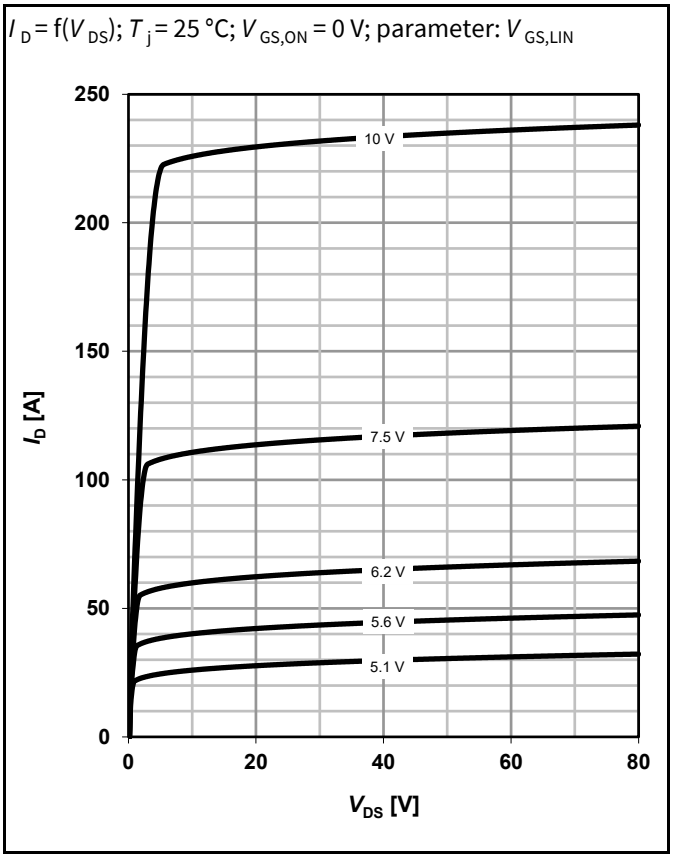


8 Typ. drain-source on-state resistance ONFET and LINFET

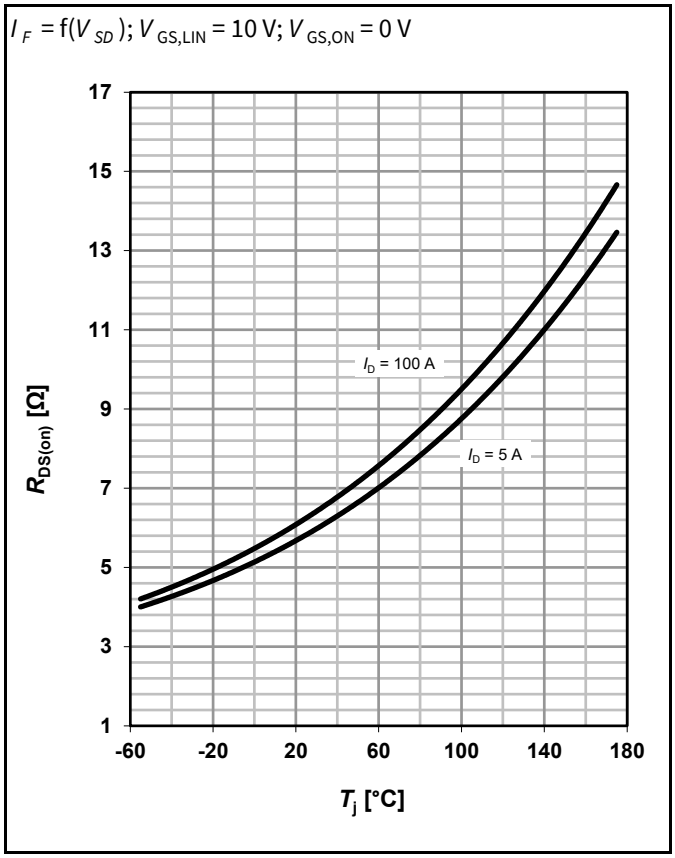
$R_{DS(on)} = f(T_j)$; parameter: I_D, $V_{GS,ON}$, $V_{GS,LIN}$



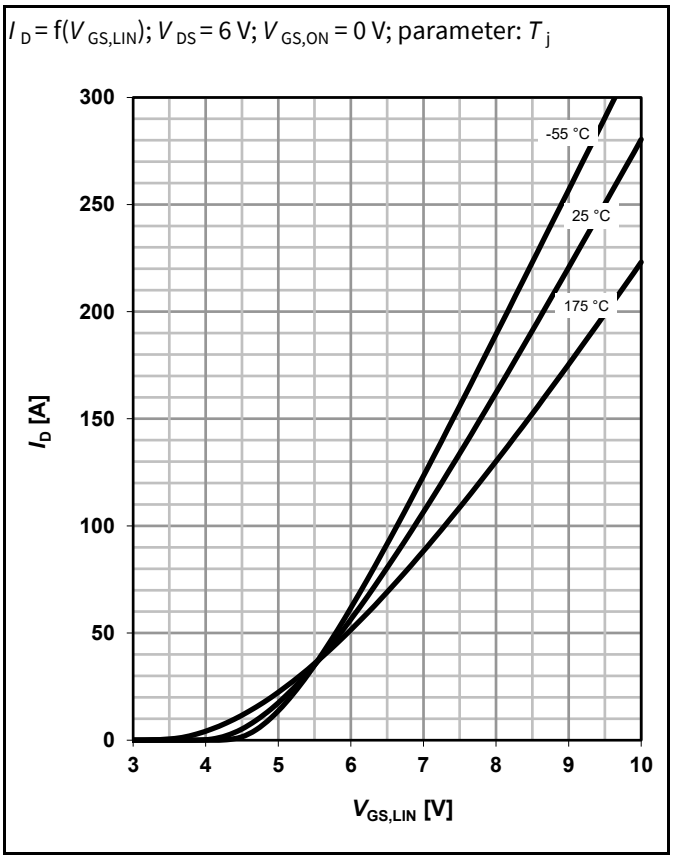
9 Typ. output characteristics LINFET



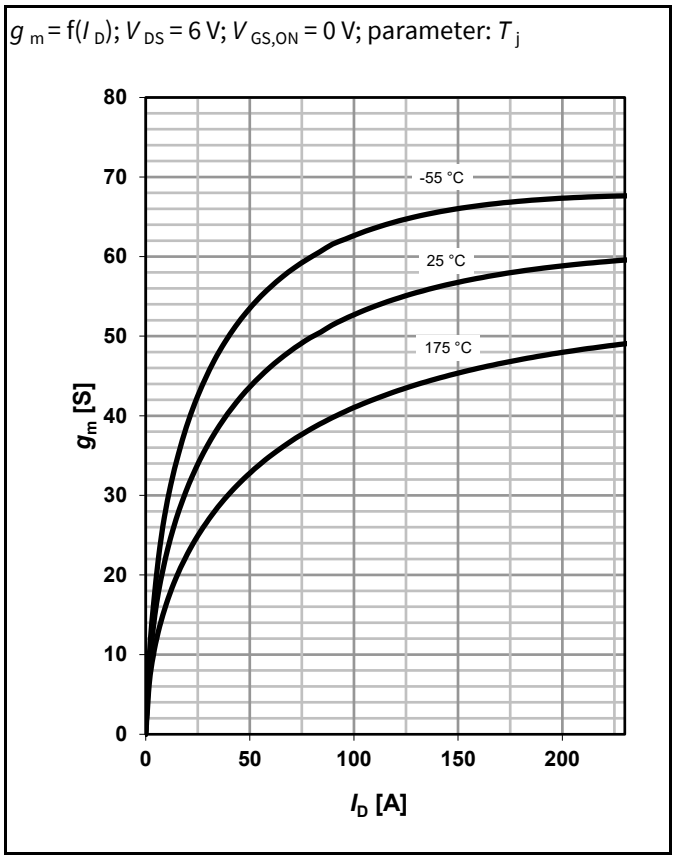
10 Typ. drain-source on-state resistance LINFET



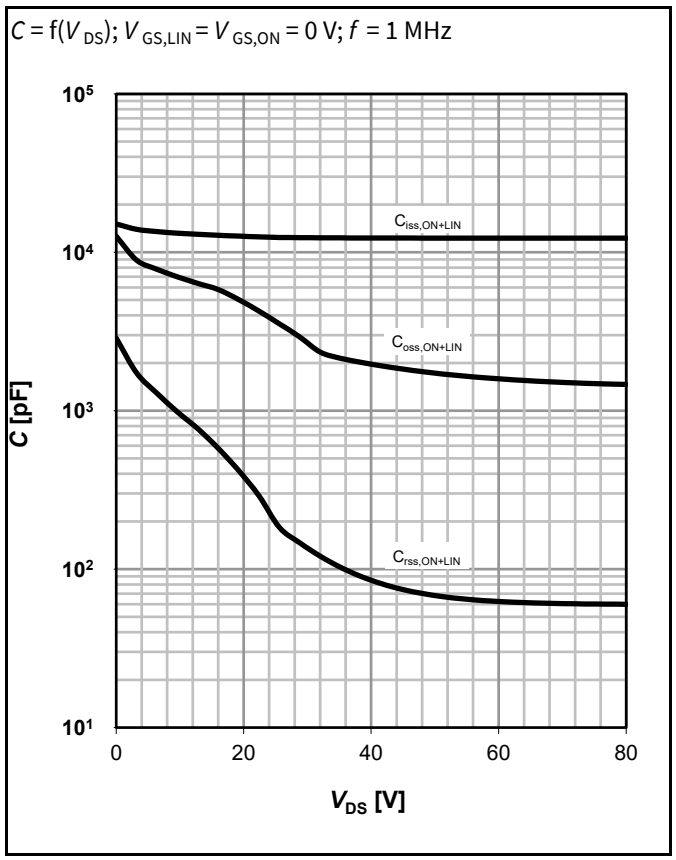
11 Typ. transfer characteristics LINFET



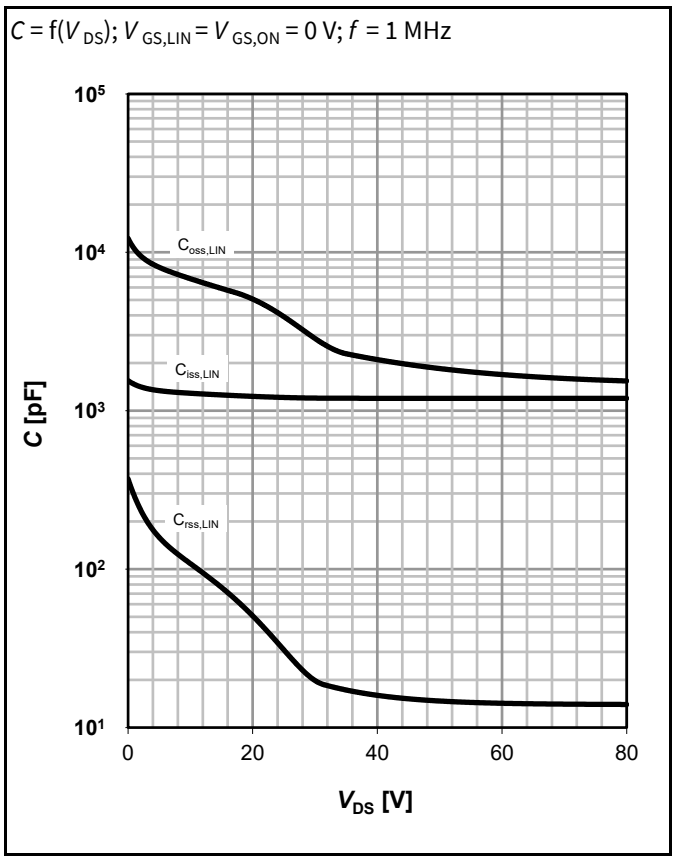
12 Typ. transconductance LINFET



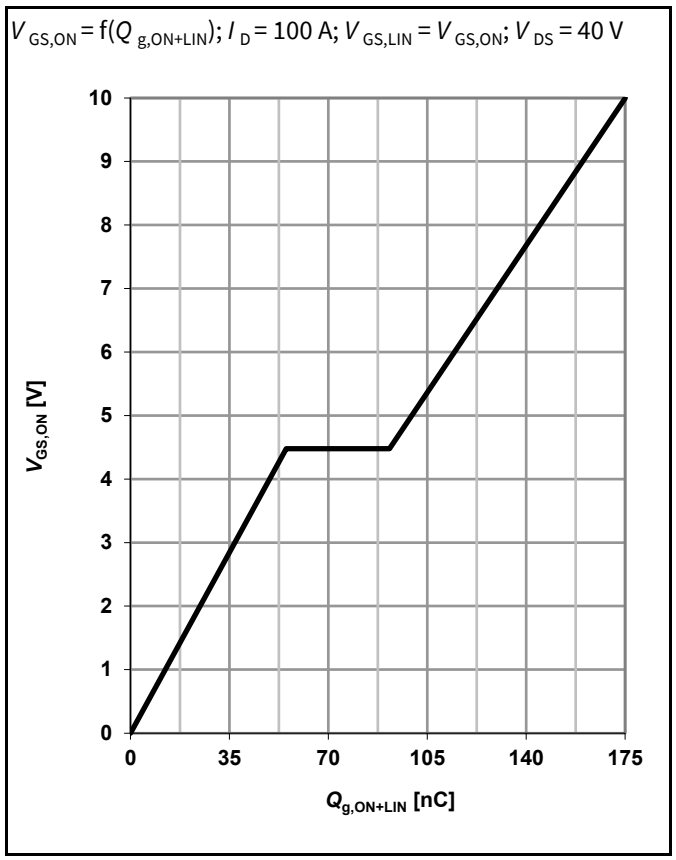
13 Typ. capacitances ONFET and LINFET



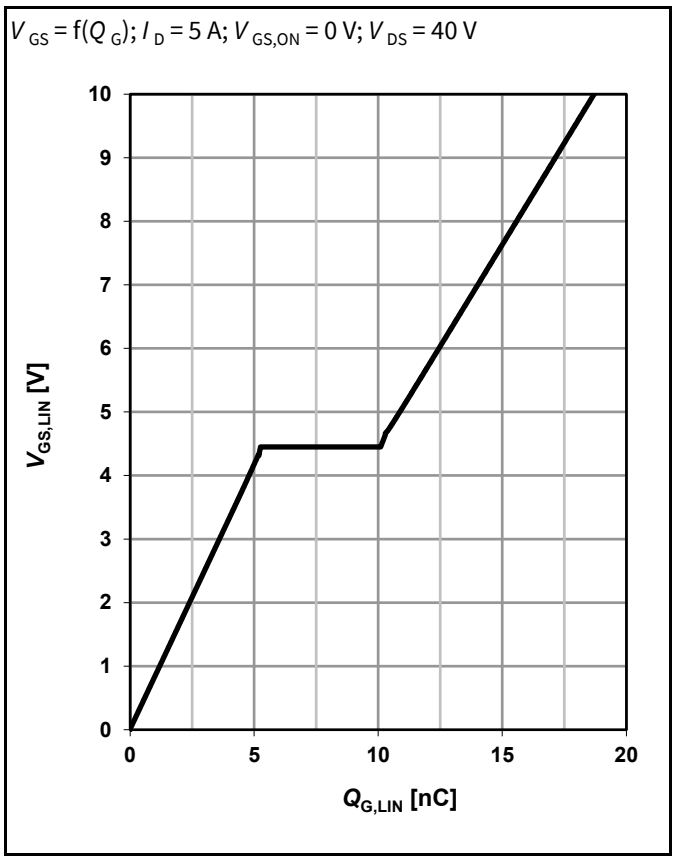
14 Typ. capacitances LINFET



15 Typ. gate charge ONFET and LINFET

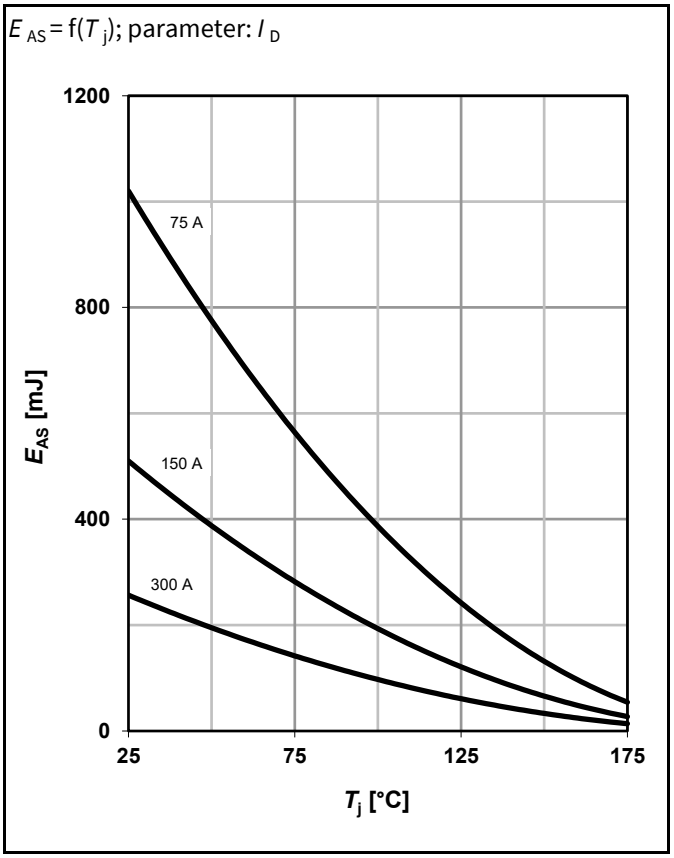


16 Typ. gate charge LINFET



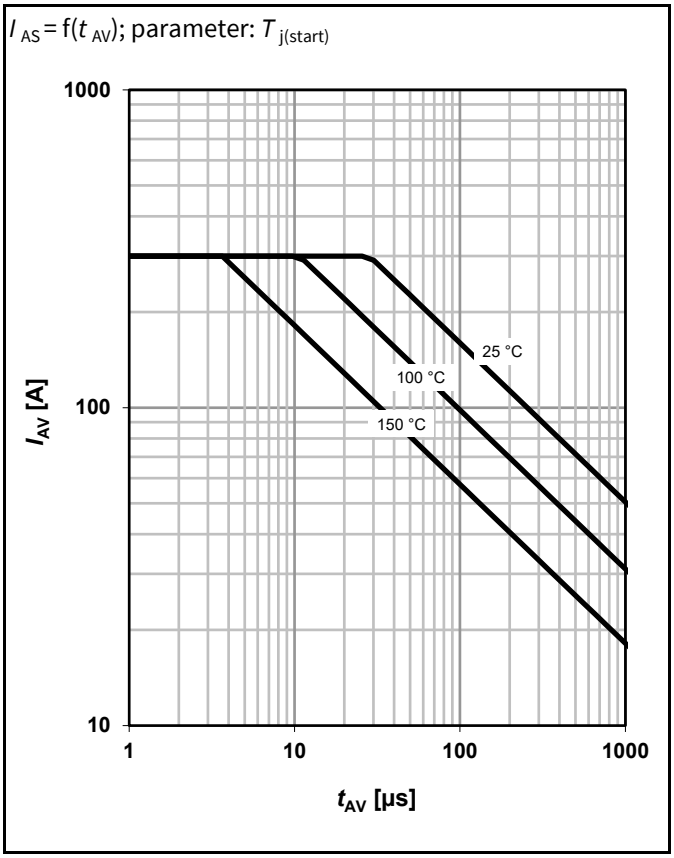
17 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: I_D



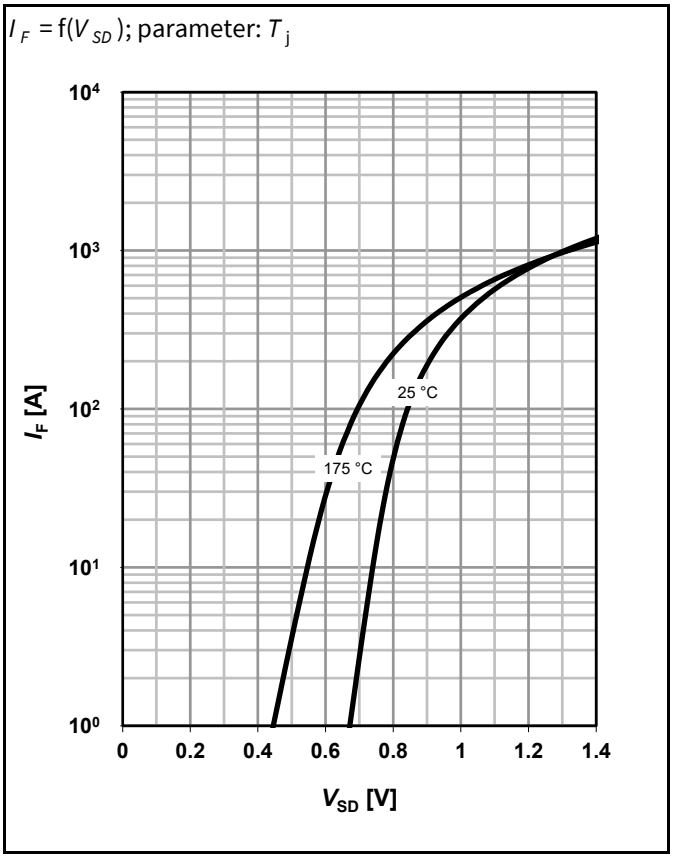
18 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



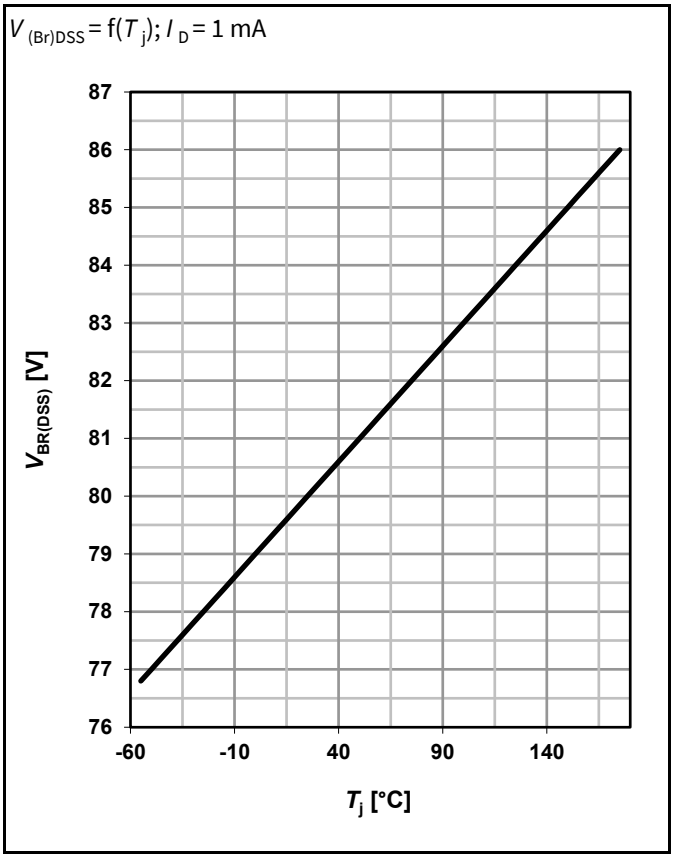
19 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



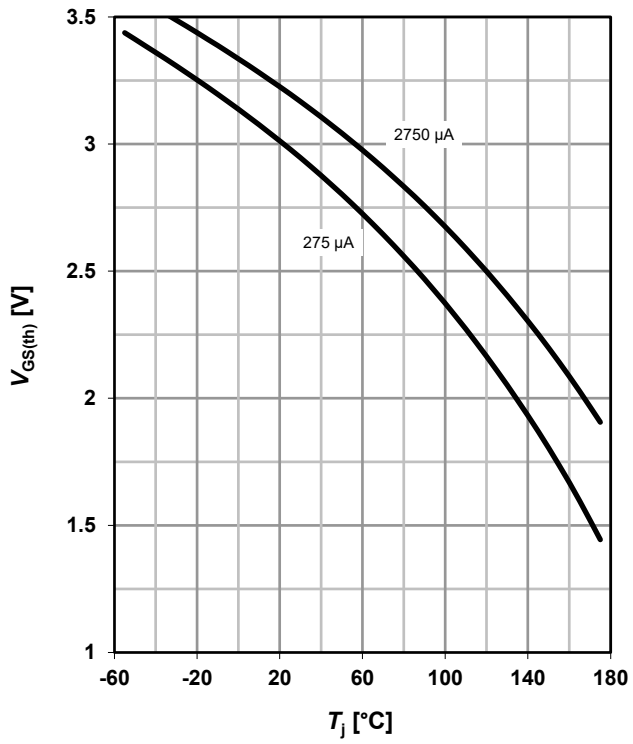
20 Drain-source breakdown voltage

$V_{(Br)DSS} = f(T_j)$; $I_D = 1$ mA



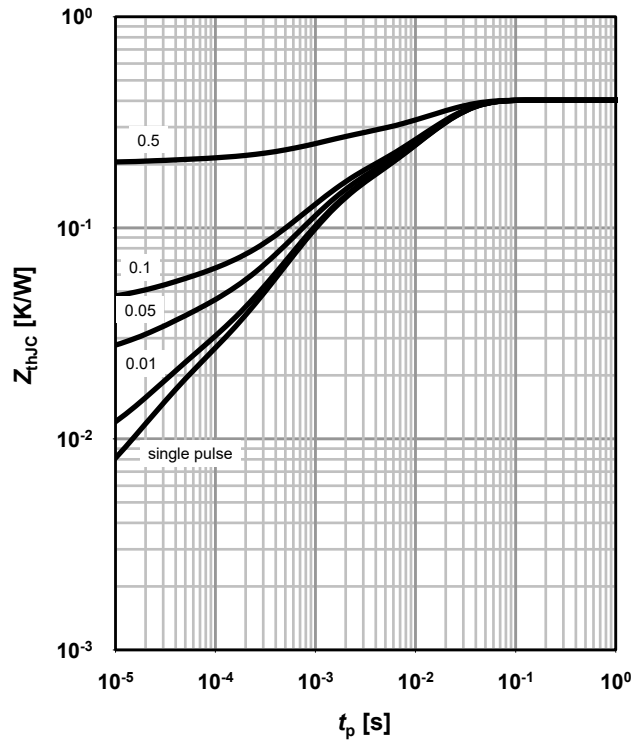
21 Typ. gate threshold voltage ONFET and LINFET

$V_{GS(th)} = f(T_j)$; $V_{GS,LIN} = V_{GS,ON} = V_{DS}$; parameter: I_D

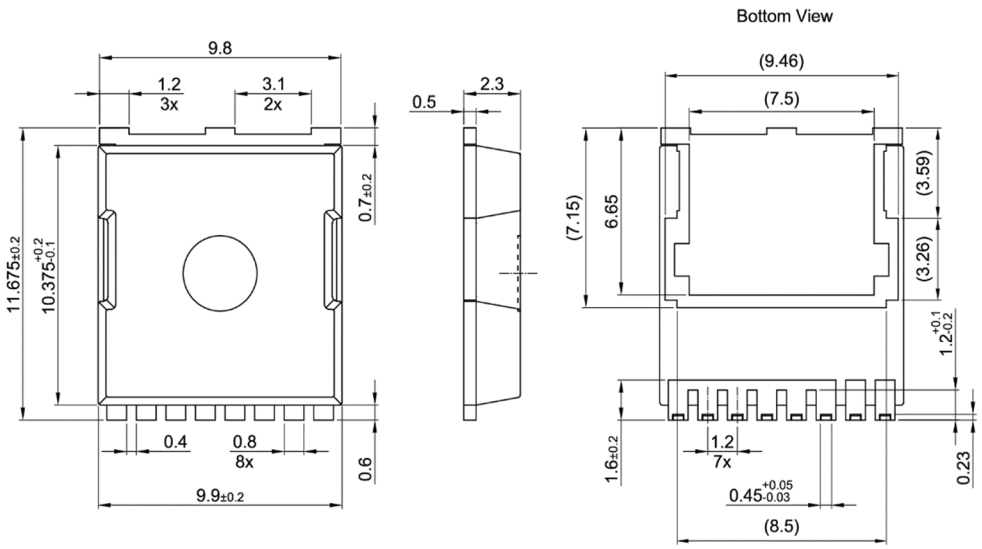


22 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$; parameter: $D = t_p/T$

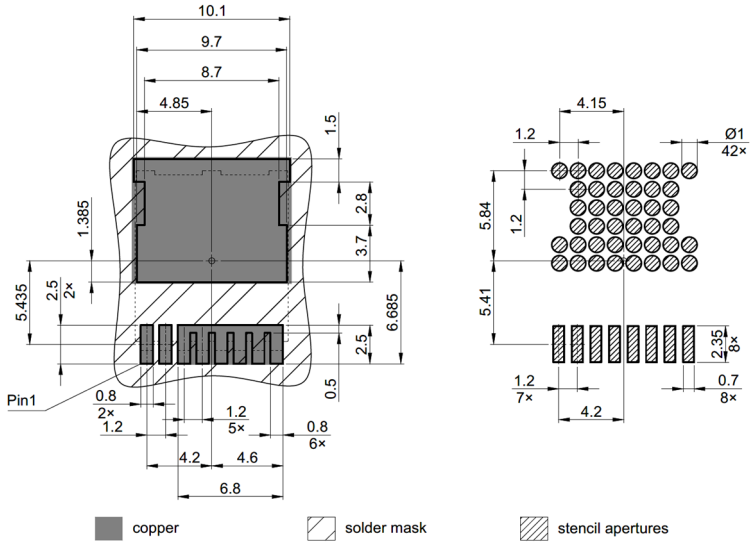


Package outline



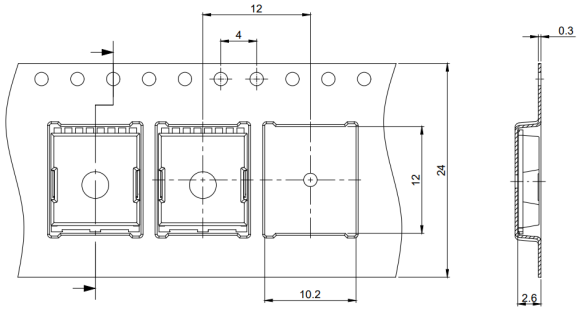
Lead length up to anti flash profile, mold flashes excluded
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⇹]

Footprint



All dimensions are in units mm
All pads are solder mask defined

Packaging



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⇹]

Revision History

Revision	Date	Changes
Rev 1.0	2024-02-28	Final Data Sheet

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