IDTech Customer's Acceptance Specification

TO: LG Electronics Inc.

Accepted By: Date :

Customer's Acceptance Specification

Type 15.0 UXGA Color TFT/LCD Module
Model Name:IAUX14P

Document Control Number : CAS I-914P-L01

Issued By : T. TOKUDA   **Date: December 5,2002**

Sales Support
International Display Technology

IDTech Customer's Acceptance Specification

i Contents

Customer's Acceptance Specification

ii　Record of Revision

Date	Document Revision	Page	Summary
December 5,2002	CAS I-914P-L01	All	First Edition for LG Electronics Inc. Based on Engineering Spec. OEM I-914P-01.
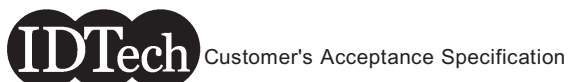
IDTech Customer's Acceptance Specification
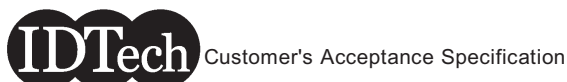
1.0 Handling Precautions

- If any signals or power lines deviate from the power on/off sequence, it may cause shorten the life of the LCD module.
- The LCD panel and the CFL are made of glass and may break or crack if dropped on a hard surface, so please handle them with care.
- CMOS-ICs are included in the LCD panel. They should be handled with care, to prevent electrostatic discharge.
- Do not press the reflector sheet at the back of the LCD module to any directions.
- Do not stick the adhesive tape on the reflector sheet at the back of the LCD module.
- Please handle care when mount in the system cover. Mechanical damage for lamp cable and for lamp connector may cause safety problems.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.5, IEC60950 or UL60950), or be applied exemption conditions of flammability requirements (4.7.3.4, IEC60950 or UL60950) in an end product.
- The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL60950).
- The fluorescent lamp in the liquid crystal display(LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Never apply detergent or other liquid directly to the screen.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth; do not use solvents or abrasives.
- Do not touch the front screen surface in your system, even bezel.

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Customer's Acceptance Specification

2.0 General Description
This specification applies to the Type 15.0 Color TFT/LCD Module 'IAUX14P'.
This module is designed for a display unit of notebook style personal computer.
The screen format and electrical interface are intended to support the UXGA (1600(H) x 1200(V)) screen.
Support color is native 262K colors(RGB 6-bit data driver).
All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.
This module does not contain an inverter card for backlight.

2.1 Characteristics

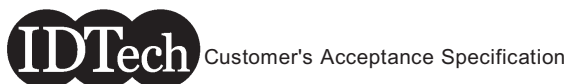The following items are characteristics summary on the table under 25 degree C condition:

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	381
Pixels H x V	1600(x3) x 1200
Active Area [mm]	304.8(H) x 228.6(V)
Pixel Pitch [mm]	0.1905(per one triad) x 0.1905
Pixel Arrangement	R,G,B Vertical Stripe
Weight [grams]	690 Typ., 725 Max.
Physical Size [mm]	317.3(W) x 242.0(H) x 7.2(D) Typ./7.5(D) Max.
Display Mode	Normally Black
Support Color	Native 262K colors(RGB 6-bit data driver)
White Luminance [cd/m^2] (center)	200 Typ.
Contrast Ratio	400 : 1 Typ.
Optical Rise Time + Fall Time [msec]	60 Typ., 150 Max.
Nominal Input Voltage VDD [Volt]	+3.3 Typ.
Power Consumption [Watt](VDD)	2.9 Typ., 3.8 Max.
Lamp Power Consumption [Watt]	4.5 Typ.,(W/o inverter loss) 5.0 Max.,(W/o inverter loss)
Typical Power Consumption [Watt]	7.4 Typ., 8.8 Max.(W/o inverter loss)
Electrical Interface	8 pairs LVDS(Even/Odd R/G/B Data(6bit), 3sync signals, Clock)
Temperature Range [degree C] Operating Storage (Shipping)	0 to +50 -20 to +60

IDTech Customer's Acceptance Specification
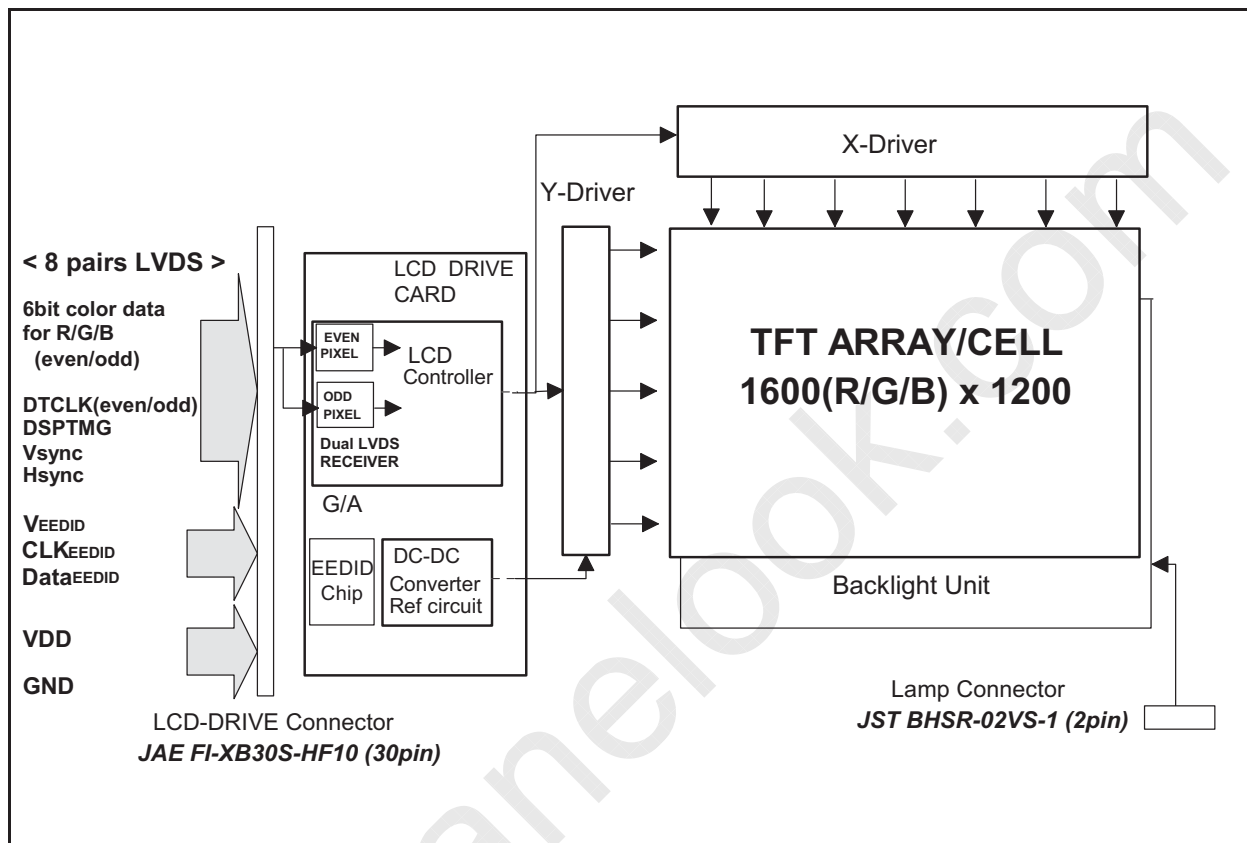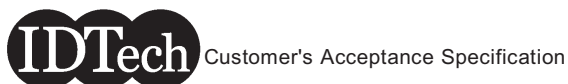
2.2 Functional Block Diagram

The following diagram shows the functional block of this Type 15.0 Color TFT/LCD Module.
The first LVDS port transmits even pixels while the second LVDS port transmits odd pixels.

Customer's Acceptance Specification

3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	V	
Input Signal Voltage	VIN	-0.3	VDD+0.3	V	
CFL Ignition Voltage	Vs	-	+1,600	Vrms	**(Note 2)**
CFL Current	ICFL	-	8	mAms	
CFL Peak Inrush Current	ICFLP	-	20	mA	
Operating Temperature	TOP	0	+50	deg.C	**(Note 1)**
Operating Relative Humidity	HOP	8	95	%RH	**(Note 1)**
Storage Temperature	TST	-20	+60	deg.C	**(Note 1)**
Storage Relative Humidity	HST	5	95	%RH	**(Note 1)**
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Rectangle wave

Note :
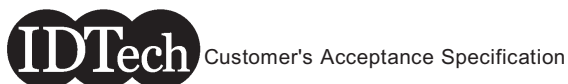
1. Maximum Wet-Bulb should be 39 degree C and No condensation.
2. Duration : 50msec Max. Ta=0 degree C

IDTech Customer's Acceptance Specification
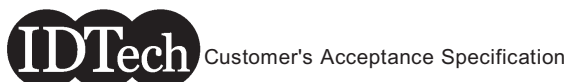
4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K≥10	Horizontal (Right)	85	-
	(Left)	85	-
K:Contrast Ratio	Vertical (Upper)	85	-
	K≥10 (Lower)	85	-
Contrast ratio		400	-
Response Time (ms)	Rising	30	-
	Falling	30	-
Color Chromaticity (CIE)	Red x	0.569	$\pm$0.030
	Red y	0.332	$\pm$0.030
	Green x	0.312	$\pm$0.030
	Green y	0.544	$\pm$0.030
	Blue x	0.149	$\pm$0.030
	Blue y	0.132	$\pm$0.030
	White x	0.313	$\pm$0.030
	White y	0.329	$\pm$0.030
White Luminance (cd/m^2)		200 Typ.	170 Min.

IDTech Customer's Acceptance Specification

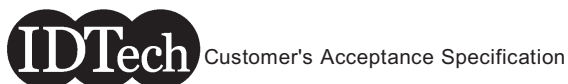The following is the note for the Optical Characteristics:
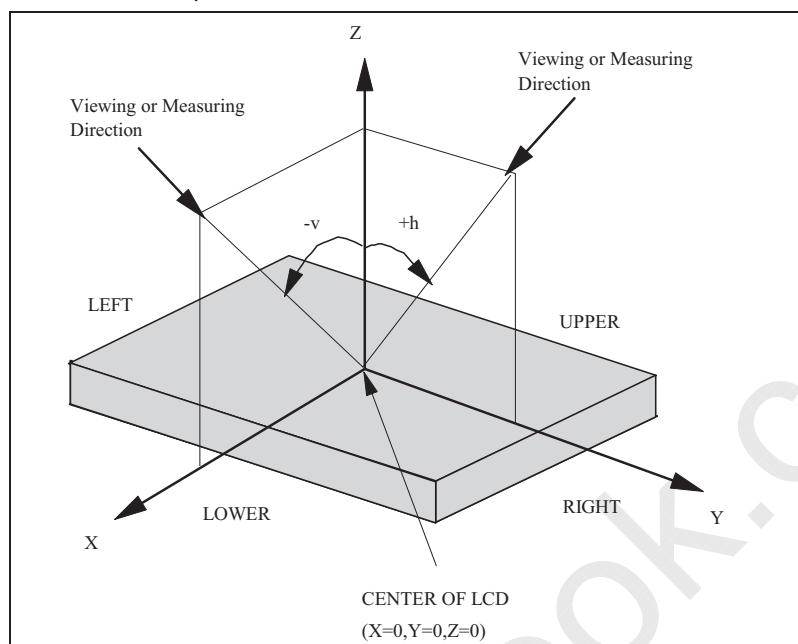
w Chromaticity and White Balance are defined as the C.I.E. 1931 x,y coordinates at the center of LCD. The Standard Equipments are as shown below table.

Item	Standard Equipment
Viewing Angle	MCPD-7000 by Ohtsuka Elec
Contrast	MCPD-7000 by Ohtsuka Elec
Response Time	BM5A by TOPCON OPTICAL Co.,Ltd.
White Luminance	MCPD-7000 by Ohtsuka Elec
Luminance Uniformity	MCPD-7000 by Ohtsuka Elec
Chromaticity	MCPD-7000 by Ohtsuka Elec
White Balance	MCPD-7000 by Ohtsuka Elec

The measurement is to be done after 30 minutes of Power-on of BackLight.
Unless otherwise specified, the ambient conditions are as following.

Ambient Temperature   :   25 + 2   (degreeC)
Ambient Humidity   :   25 - 85   (%)
Atmospheric Pressure   :   86.0 - 104.0   (kPa)

IDTech Customer's Acceptance Specification

4.1 Luminance Uniformity

When the backlight is on with all pels in the unselected state (white), the luminance uniformity is defined as follows;

Average luminance is defined as follows.

$$\text{Average Luminance} = \frac{L1 + L2 + L3 + L4 + L5}{5}$$

Luminance variation is measured by dividing the maximum luminance values of the 13 or 5 test points by the minimum luminance of the 13 or 5 test points.

$$\text{Luminance Uniformity} \quad \frac{\text{Maximum Luminance 13 Points (L1-L13)}}{\text{Minimum Luminance 13 Points (L1-L13)}} \leqq 1.65$$

$$\text{Luminance Uniformity} \quad \frac{\text{Maximum Luminance 5 Points (L1-L5)}}{\text{Minimum Luminance 5 Points (L1-L5)}} \leqq 1.25$$

Figure. Average luminance and Luminance uniformity test points
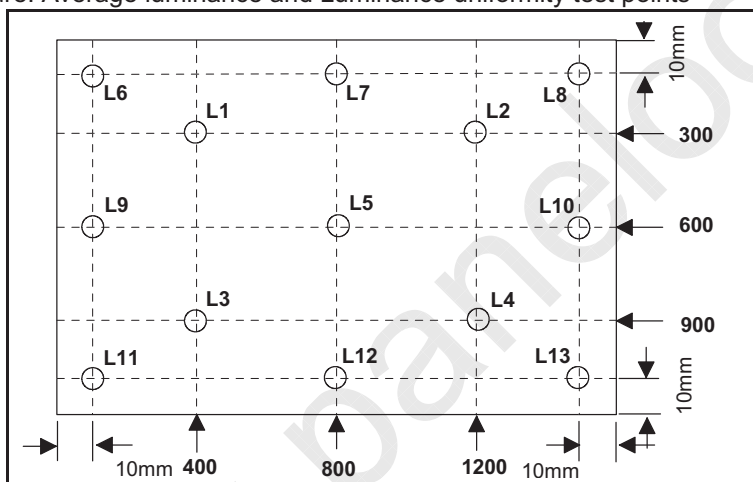
IDTech Customer's Acceptance Specification

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	JAE
Type / Part Number	FI-XB30S-HF10
Mating Receptacle Manufacture	JAE
Mating Receptacle/Part Number	FI-X30M

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

December 5,2002　　　　　　　　　　CAS I-914P-L01

IDTech Customer's Acceptance Specification

5.2 Interface Signal Connector

Pin #	Signal Name
1	GND
2	VDD
3	VDD
4	V_{EEDID} (Note 2,3)
5	Reserved (Note 1)
6	CLK_{EEDID} (Note 2,4)
7	$Data_{EEDID}$ (Note 2,4)
8	ReIN0-
9	ReIN0+
10	GND
11	ReIN1-
12	ReIN1+
13	GND
14	ReIN2-
15	ReIN2+

Pin #	Signal Name
16	GND
17	ReCLKIN-
18	ReCLKIN+
19	GND
20	RoIN0-
21	RoIN0+
22	GND
23	RoIN1-
24	RoIN1+
25	GND
26	RoIN2-
27	RoIN2+
28	GND
29	RoCLKIN-
30	RoCLKIN+

Note :
1. 'Reserved' pins are not allowed to connect any other line.
2. This LCD Module complies with "VESA ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA STANDARD Release A, Revision 1" and supports "EEDID version 1.3".
   This module uses Serial EEPROM BR24C02FV (ROHM) or compatible as a EEDID function.
3. V_{EEDID} power source shall be the current limited circuit which has not exceeding 1A. (Reference Document : "Enhanced Display Data Channel (E-DDC^{TM}) Proposed Standard", VESA)
4. Both CLK_{EEDID} line and $Data_{EEDID}$ line are pulled-up with 10K ohm resistor to V_{EEDID} power source line at LCD panel, respectively.

Voltage levels of all input signals are LVDS compatible (except VDD,EEDID). Refer to "Signal Electrical Characteristics for LVDS", for voltage levels of all input signals.

IDTech Customer's Acceptance Specification

5.3 Interface Signal Description

The LVDS receiver equipped in this LCD module is compatible with ANSI/TIA/TIA-644 standard.

PIN #	SIGNAL NAME	Description
1	GND	Ground
2	VDD	+3.3V Power Supply
3	VDD	+3.3V Power Supply
4	V_{EEDID}	EEDID 3.3V Power Supply
5	Reserved	Reserved
6	CLK_{EEDID}	EEDID Clock
7	$Data_{EEDID}$	EEDID Data
8	ReIN0-	Negative LVDS differential data input (Even R0-R5, G0)
9	ReIN0+	Positive LVDS differential data input (Even R0-R5, G0)
10	GND	Ground
11	ReIN1-	Negative LVDS differential data input (Even G1-G5, B0-B1)
12	ReIN1+	Positive LVDS differential data input (Even G1-G5, B0-B1)
13	GND	Ground
14	ReIN2-	Negative LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
15	ReIN2+	Positive LVDS differential data input (Even B2-B5, HSYNC, VSYNC, DSPTMG)
16	GND	Ground
17	ReCLKIN-	Negative LVDS differential clock input (Even)
18	ReCLKIN+	Positive LVDS differential clock input (Even)
19	GND	Ground
20	RoIN0-	Negative LVDS differential data input (Odd R0-R5, G0)
21	RoIN0+	Positive LVDS differential data input (Odd R0-R5, G0)
22	GND	Ground
23	RoIN1-	Negative LVDS differential data input (Odd G1-G5, B0-B1)
24	RoIN1+	Positive LVDS differential data input (Odd G1-G5, B0-B1)
25	GND	Ground
26	RoIN2-	Negative LVDS differential data input (Odd B2-B5)
27	RoIN2+	Positive LVDS differential data input (Odd B2-B5)
28	GND	Ground
29	RoCLKIN-	Negative LVDS differential clock input (Odd)
30	RoCLKIN+	Positive LVDS differential clock input (Odd)

Note :

1. Input signals of odd and even clock shall be the same timing.
2. The module uses a 100ohm resistor between positive and negative data lines of each receiver input.
3. Even : First Pixel data Odd : Second Pixel Data

Customer's Acceptance Specification

SIGNAL NAME	Description
+RED 5 +RED 4 +RED 3 +RED 2 +RED 1 +RED 0 (EVEN/ODD)	RED Data 5 (MSB) RED Data 4 RED Data 3 RED Data 2 RED Data 1 RED Data 0 (LSB) Red-pixel Data: Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0 (EVEN/ODD)	GREEN Data 5 (MSB) GREEN Data 4 GREEN Data 3 GREEN Data 2 GREEN Data 1 GREEN Data 0 (LSB) Green-pixel Data: Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0 (EVEN/ODD)	BLUE Data 5 (MSB) BLUE Data 4 BLUE Data 3 BLUE Data 2 BLUE Data 1 BLUE Data 0 (LSB) Blue-pixel Data: Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK (EVEN/ODD)	Data Clock: The typical frequency is 81MHz. The signal is used to strobe the pixel +data and the +DSPTMG
+DSPTMG	Display Timing: When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync: This signal is synchronized with -DTCLK. Both active high/low signals are acceptable.
HSYNC	Horizontal Sync: This signal is synchronized with -DTCLK. Both active high/low signals are acceptable.
VDD	Power Supply
GND	Ground
V_{EEDID}	EEDID Power Supply
CLK_{EEDID}	EEDID Clock
$Data_{EEDID}$	EEDID Data

Note : Output signals except V_{EEDID} ,CLK_{EEDID} and $Data_{EEDID}$ from any system shall be Hi-Z state when VDD is off. VSYNC should start with active high (positive pulse) signal from when VDD is supplied and its polarity should not be changed.
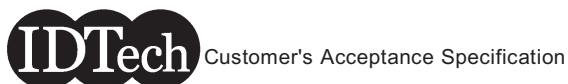
IDTech Customer's Acceptance Specification

5.3.1 E-EDID
E-EDID detail in this LCD module is in the following table.

Address (hex)	Description	Data (hex)	Remark
00 - 07	Header	00 FF FF FF FF FF FF 00	Header, Fixed
08 - 09	ID Manufacturer Name	24 94	"IDT"
0A - 0B	ID Product code	D2 22	Product code "8914"
0C - 0F	ID Serial Number	01 01 01 01	Unused
10	Week of Manufacture	00	Unused
11	Year of Manufacture	00	Unused
12 - 13	EDID Structure Version/Revision	01 02	Ver1.2
14 - 18	Basic Display Parameters/Features	80 1E 17 78 0A	
19 - 22	Color Characteristics	CD 75 91 55 4F 8B 26 21 50 54	
23 - 25	Established Timings	00 00 00	Unused
26 - 35	Standard Timing Identification	A9 40 01 01 01 01 01 01 01 01 01 01 01 01 01 01	
36 - 47	Detailed Timing/Monitor Description #1	48 3F 40 30 62 B0 32 40 40 C0 13 00 31 E5 10 00 00 18	VESA 1600x1200 @ 60Hz, Negative H/V-sync polarity
48 - 59	Detailed Timing/Monitor Description #2	00 00 00 0F 00 3B 3D 4A 4C 11 00 0A 20 20 20 20 20 01	Video timing min/max parameters,EDID version=1
5A - 6B	Detailed Timing/Monitor Description #3	00 00 00 FE 00 49 44 54 45 43 48 0A 20 20 20 20 20 20	Supplier Name "IDTECH"
6C - 7D	Detailed Timing/Monitor Description #4	00 00 00 FE 00 49 41 55 58 31 34 50 0A 20 20 20 20 20	Monitor Name "IAUX14P"
7E	Extension Flag	00	No extension
7F	Checksum	86	

IDTech Customer's Acceptance Specification

5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

The LVDS receiver equipped in this LCD module is compatible with ANSI/TIA/TIA-644 standard.

Table. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Differential Input High Threshold	Vth			+100	mV	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100			mV	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100		600	mV	
Common Mode Voltage	Vcm	1.0	1.2	1.4	V	Vth - Vtl = 200mV
Common Mode Voltage Offset	∆Vcm	-50		+50	mV	Vth - Vtl = 200mV

Note:
- Input signals shall be low or Hi-Z state when VDD is off.
- All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD (see Figure "Measurement system").

Figure. Voltage Definitions

Customer's Acceptance Specification
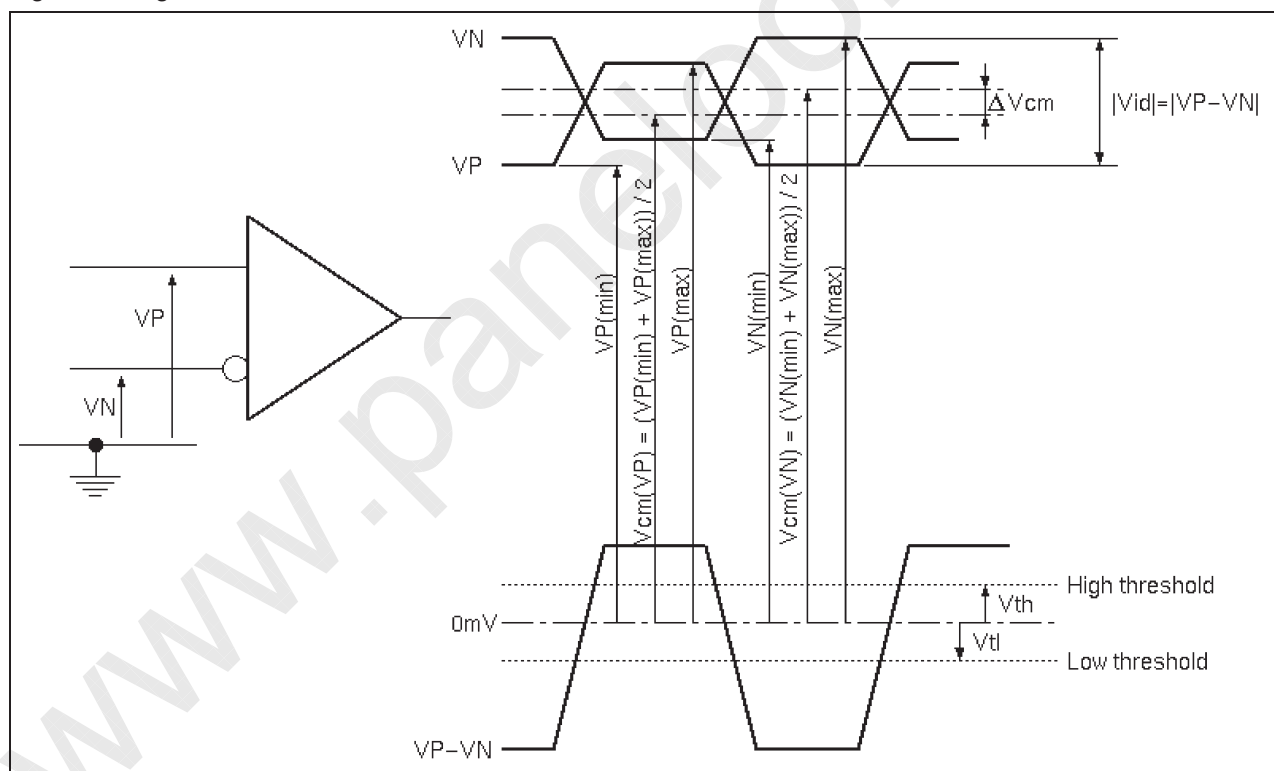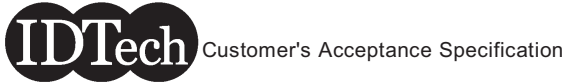
Figure. Measurement system
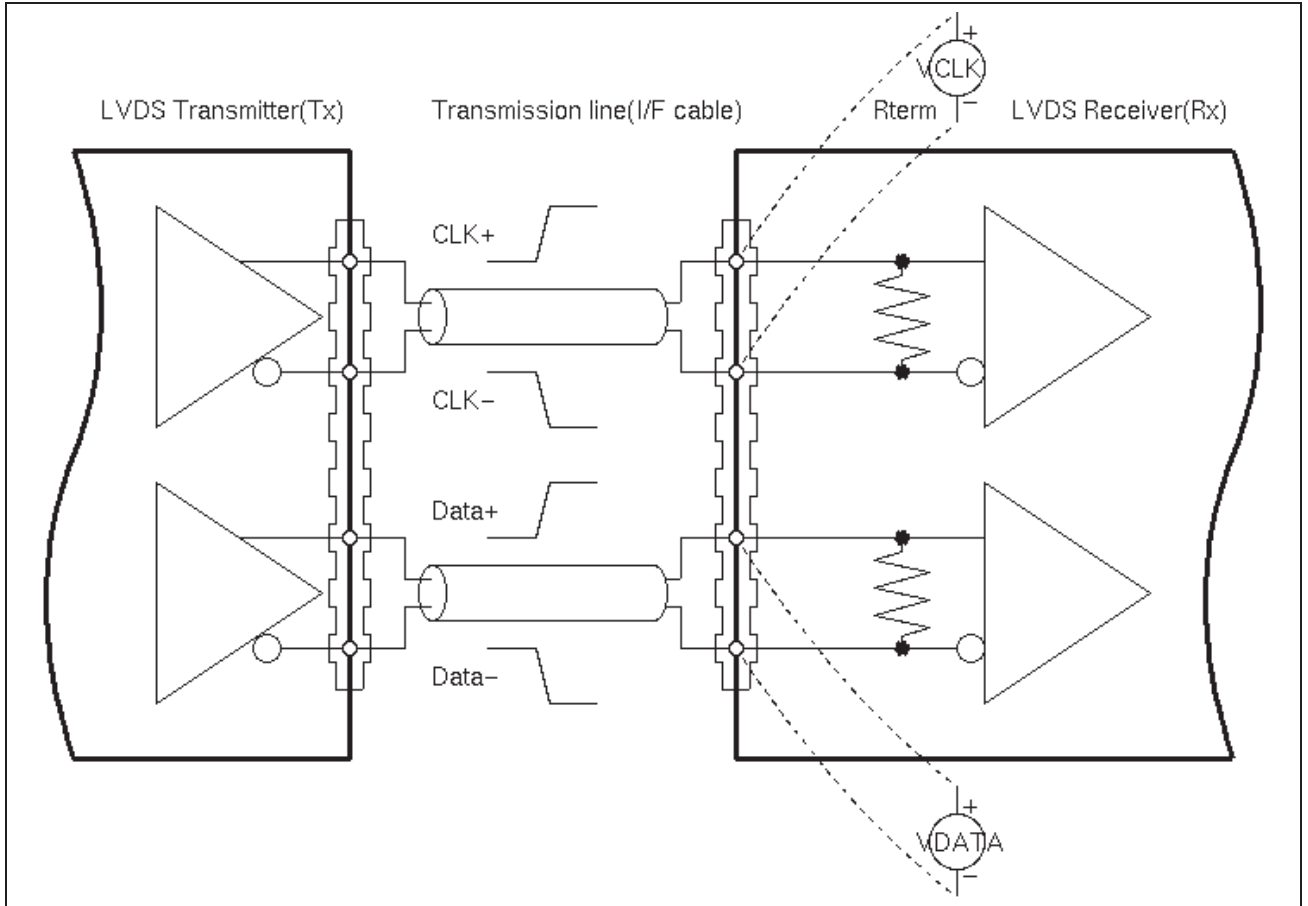
IDTech Customer's Acceptance Specification

Table. Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency	fc	53.0	81.0	83.0	MHz	
Cycle Time	tc	12.0	12.3	18.9	ns	
Data Setup Time(Note 1)	Tsu	500			ps	fc = 81MHz, tCCJ < 50ps,
Data Hold Time(Note 2)	Thd	500			ps	Vth-Vtl = 200mV, Vcm = 1.2V, ΔVcm = 0
Cycle-to-cycle jitter(Note 3)	tCCJ	-150		+150	ps	fc = 81MHz
Cycle Modulation Rate(Note 4)	tCJavg			20	ps/clk	fc = 81MHz

Note 1: All values are at VDD=3.3V, Ta=25 degree C.
Note 2: See figure "Timing Definition" and "Timing Definition(detail A)" for definition.
Note 3: Jitter is the magnitude of the change in input clock period.
Note 4: This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles.
This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

Figure. Timing Definition (Even)

December 5,2002   CAS I-914P-L01   18/35

Customer's Acceptance Specification
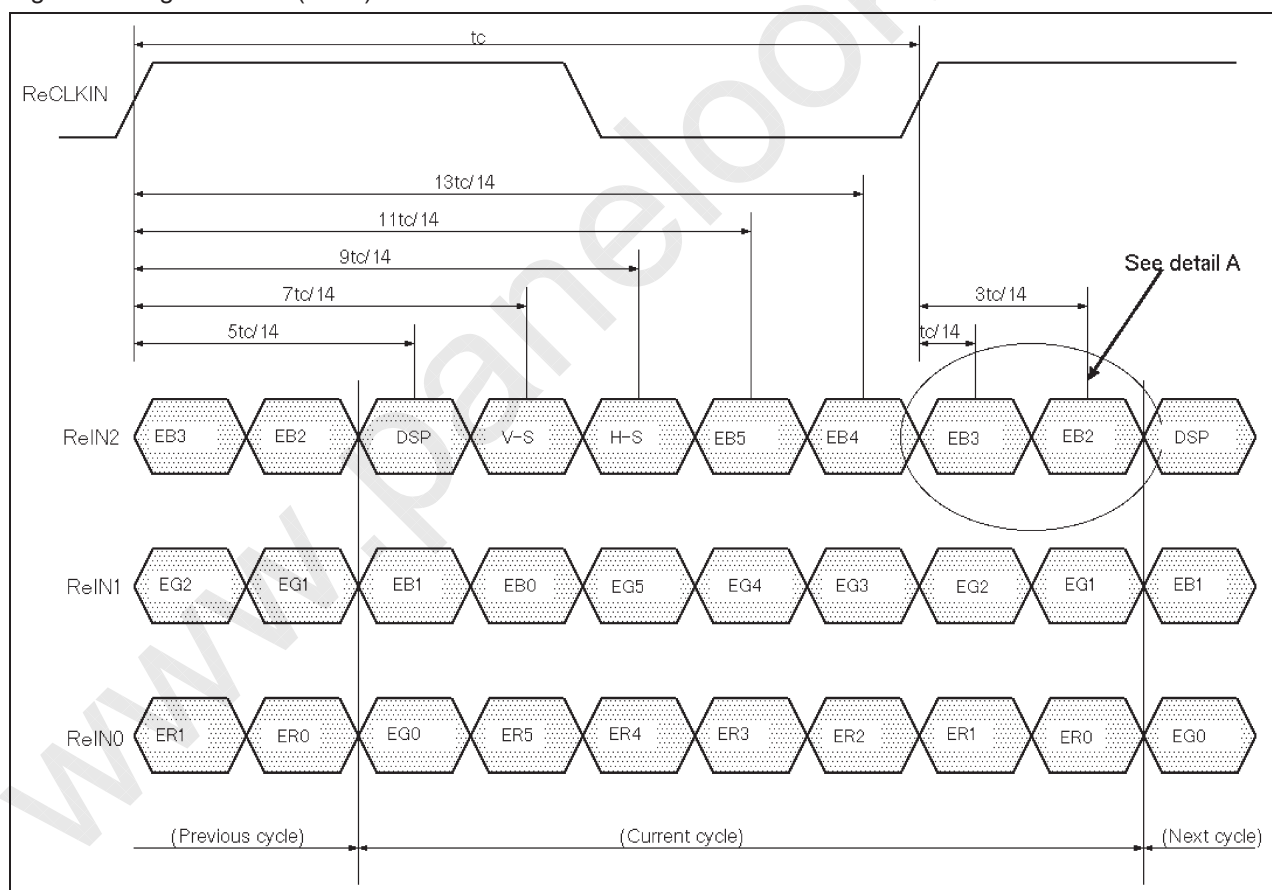
Figure. Timing Definition (Odd)

December 5,2002　　　　　　　　　　　CAS I-914P-L01　　　　　　　　　　　19/35

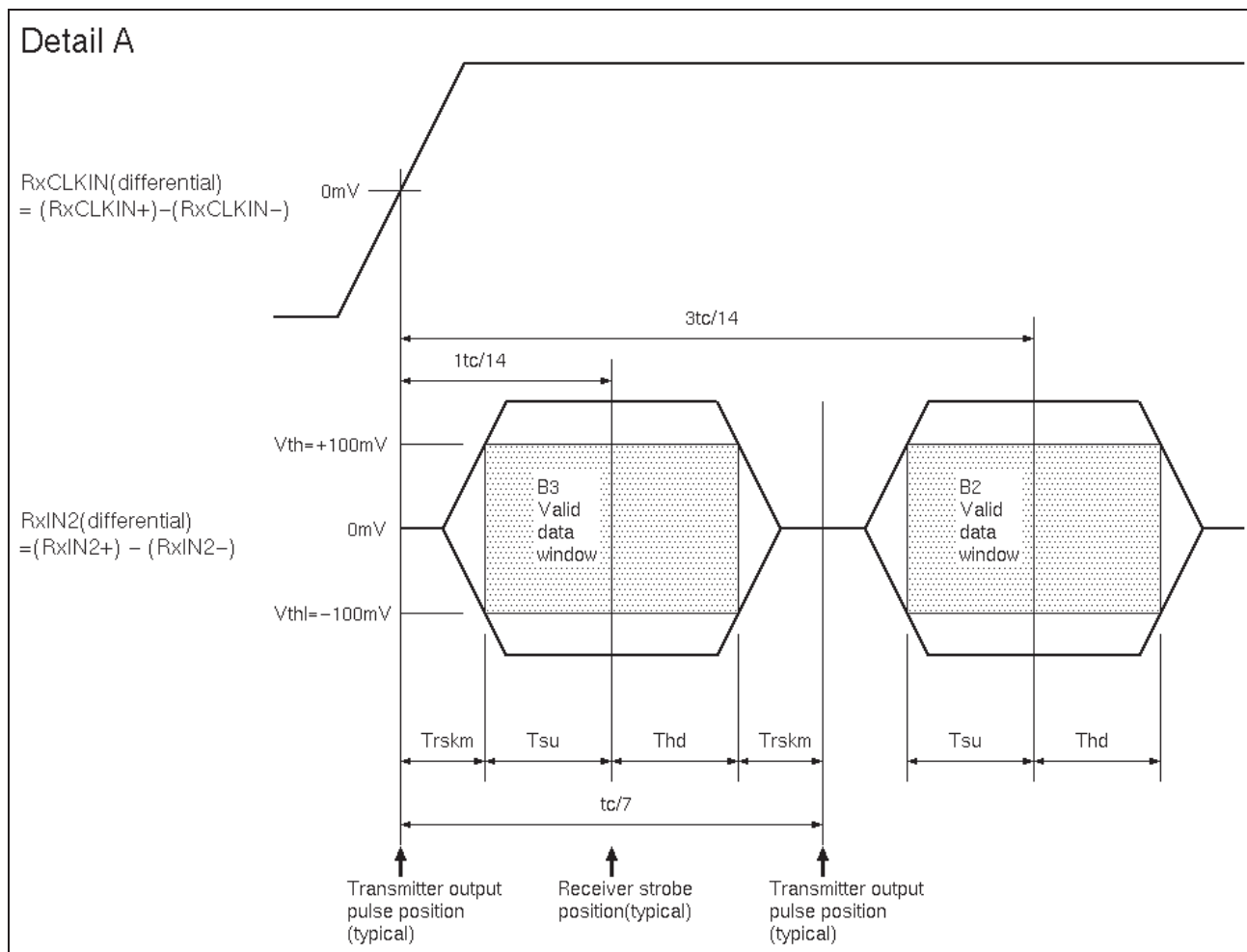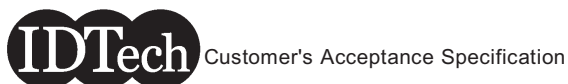IDTech Customer's Acceptance Specification
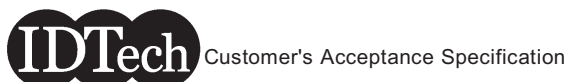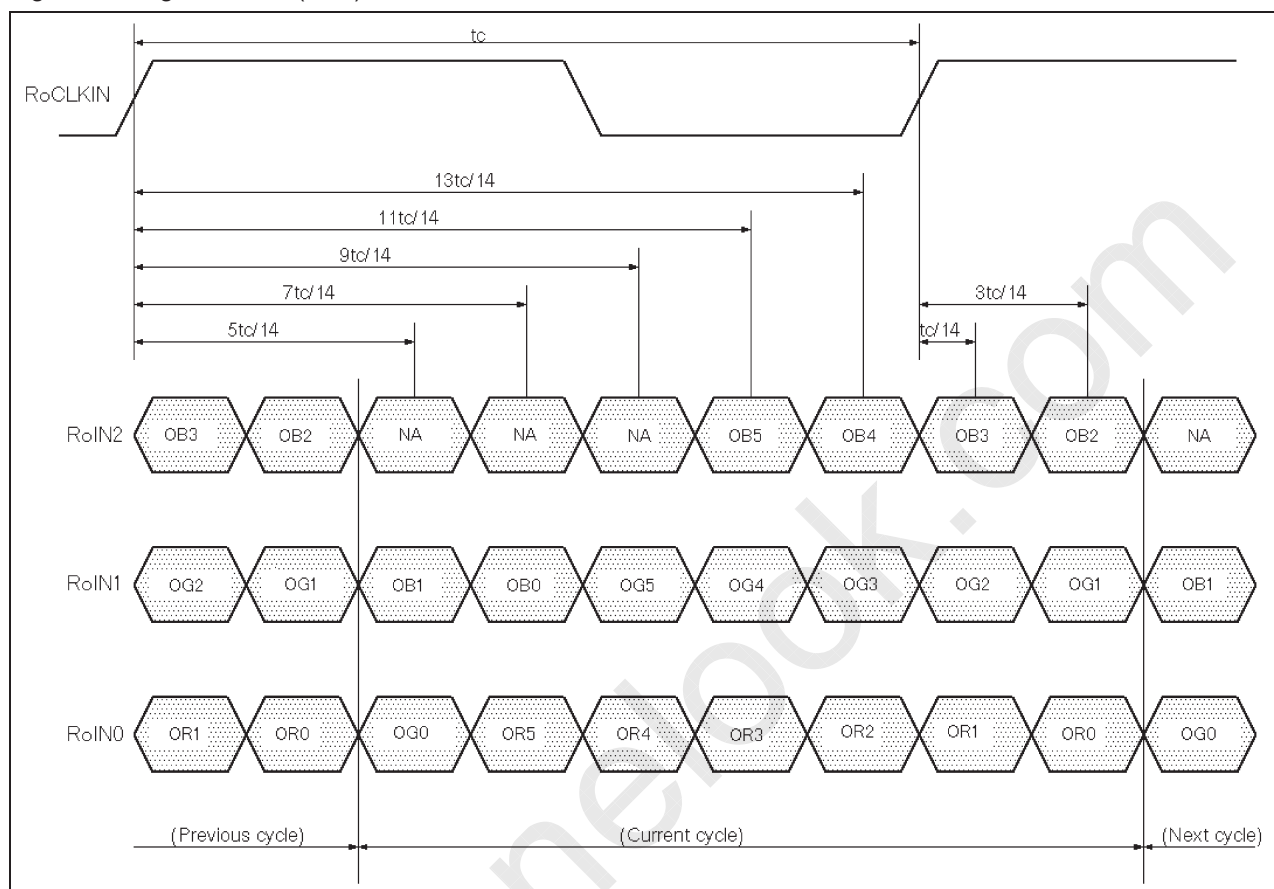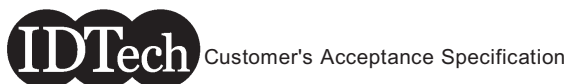
Figure. Timing Definition(detail A)

Note: Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.
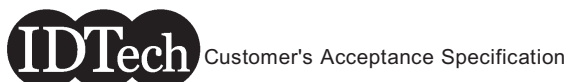
IDTech Customer's Acceptance Specification

5.4.2 LVDS Receiver Internal Circuit

Below figure shows the internal block diagram of the LVDS receiver.
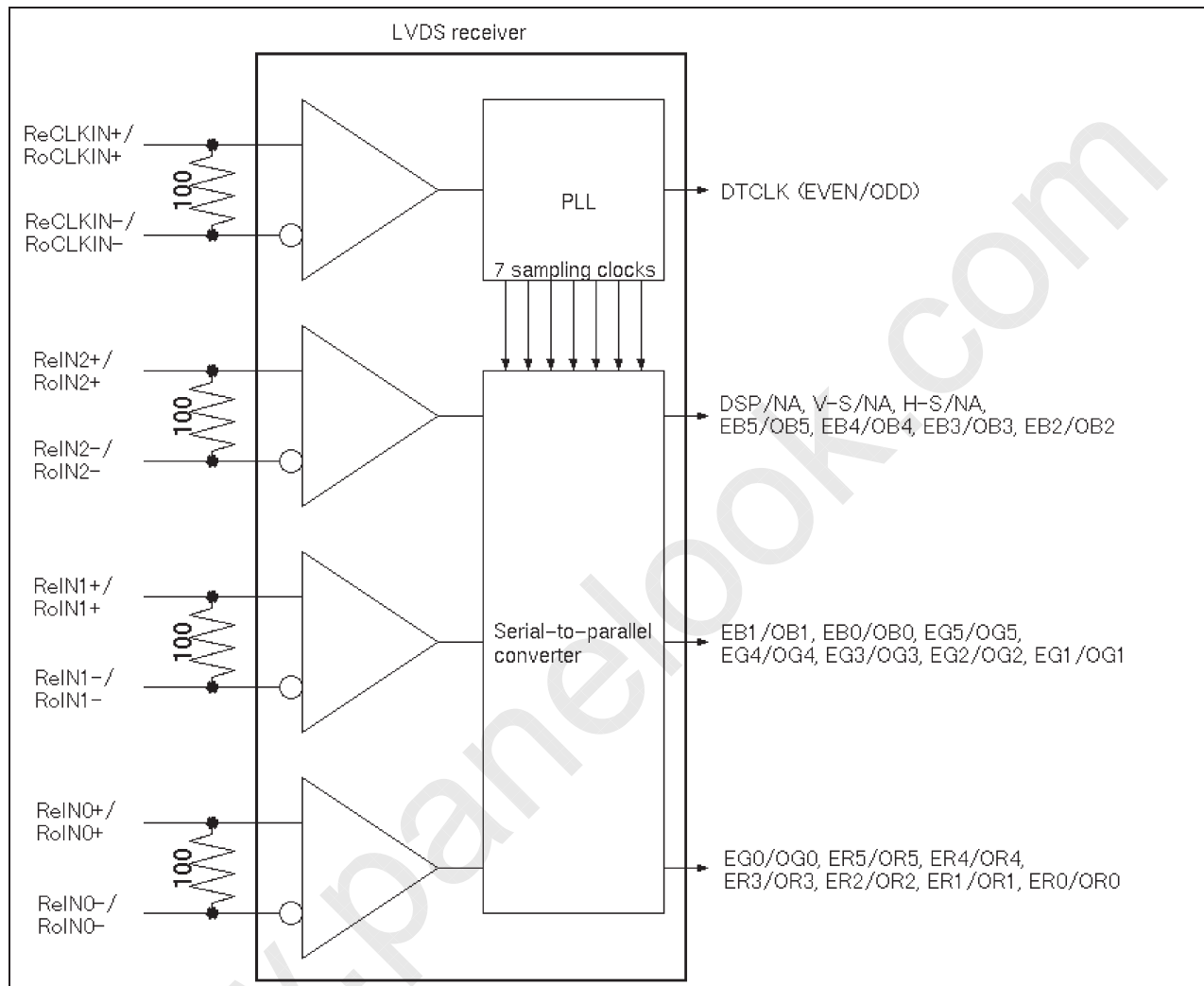
5.4.3 Recommended Guidelines for Motherboard PCB Design and Cable Selection

Following the suggestions below will help to achieve optimal results.

- Use controlled impedance media for LVDS signals. They should have a matched differential impedance of 100ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from LVDS signals.
- For cables, twisted pair, twinax, or flex circuit with close coupled differential traces are recommended.
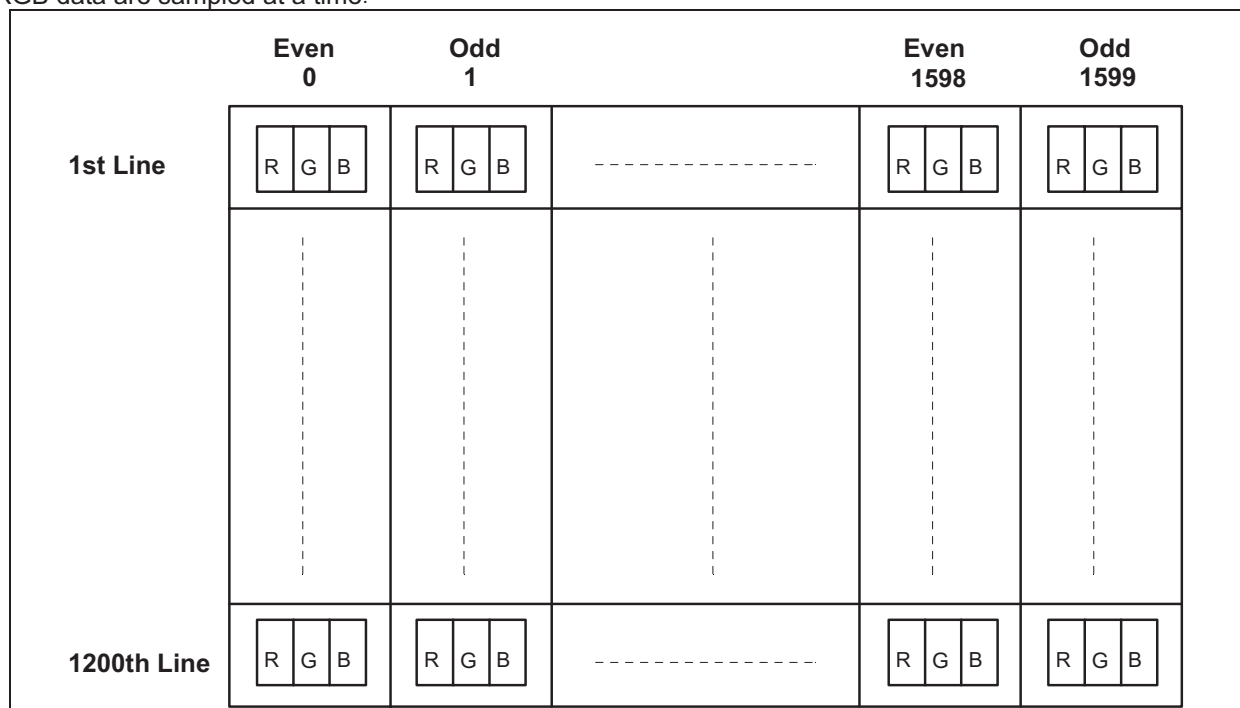
Customer's Acceptance Specification

5.5 Signal for Lamp Connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

Customer's Acceptance Specification
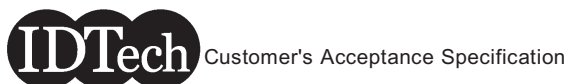
6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image. Even and odd pair of RGB data are sampled at a time.

IDTech Customer's Acceptance Specification

7.0 Parameter guide line for CFL Inverter

PARAMETER	MIN	DP-1	MAX	UNITS	CONDITION
White Luminance	-	200	-	cd/m^2	(Ta=25 deg.C)
CFL current(ICFL)	3.0	7.65	8.0	mArms	(Ta=25 deg.C)
CFL Frequency(FCFL)	40		60	KHz	(Ta=25 deg.C) **(Note 1)**
CFL Ignition Voltage(Vs)	1,500	-	-	Vrms	(Ta= 0 deg.C) **(Note 3)**
CFL Voltage (Reference)(VCFL)	-	590	-	Vrms	(Ta=25 deg.C) **(Note 2)**
CFL Power consumption(PCFL)	-	4.5	5.0	W	(Ta=25 deg.C) **(Note 2)**

Note 1: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 2: Calculated value for reference (ICFL x VCFL = PCFL).

Note 3: CFL inverter should be able to give out a power that has a generating capacity of over 1,500 voltage. Lamp units need 1,500 voltage minimum for ignition.

Note 4: DP-1(Design Point-1) is recommended Design Point.

　　*1 All of characteristics listed are measured under the condition using the Test inverter.

　　*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

　　*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

　　*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

　　*5 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

　　*6 It should be employed the inverter which has 'Duty Dimming', if ICFL is less than 4[mA].

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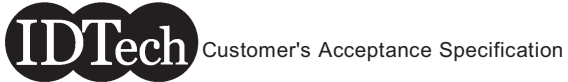
The following chart is Luminance versus Lamp Power for your reference.
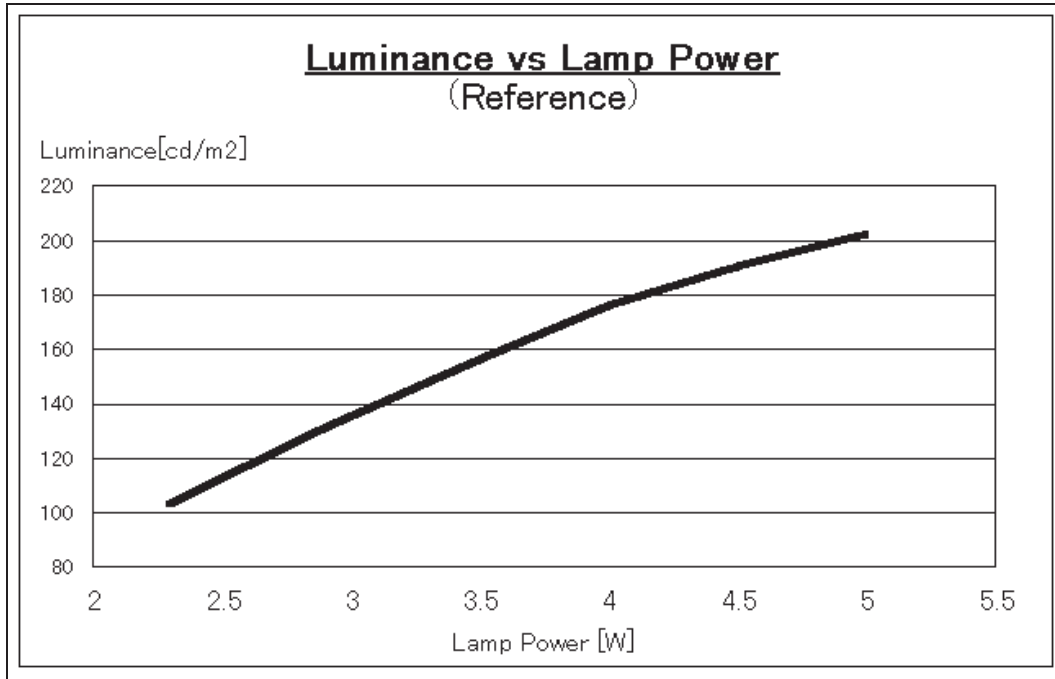
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8.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86(Texas Instruments) or equivalent.

8.1 Timing Characteristics

Signal	Item	Symbol	MIN.	TYP.	MAX.	Unit
DTCLK	Freqency	Fdck	53.0	81.0	83.0	[MHz]
		Tck	12.0	12.3	18.9	[ns]
+V-Sync	Frame Rate	Fv	-	60.0	-	[Hz]
		Tv	-	16.67	-	[ms]
		Nv	1208	1250	2046	[lines]
	V-Active Level	Tva	13.33	40.0	839.8	[us]
		Nva	1	3	63	[lines]
	V-Back Porch	Nvb	6	46	125	[lines]
	V-Front Porch	Nvf	1	1	125	[lines]
+DSPTMG	V-Line	m		1200		[lines]
+H-Sync	Scan Rate	Fh	-	75.0	-	[KHz]
		Th	-	13.33	-	[us]
		Nh	1024	1080	2046	[Tck]
	H-Active Level	Tha		1.185		[us]
		Tha	8	96	255	[Tck]
	H-Back Porch	Thb	8	152	511	[Tck]
	H-Front Porch	Thf	8	32		[Tck]
+DSPTMG	Display	Thd		9.877		[us]
+DATA	Data Even/Odd	n		1600		[dots]

Note: Both positive Hsync and positive Vsync polarity is recommended.

Disp Timing Period (Th, Nh) must be constant by each every line.
If Disp timing are not constant due to Spread Spectrum, the following expression has to be satisfied.

DeltaDT x Tvblk < 300 [Tck]

DTmax : Disp Timing Period MAX [Tck]
DTmin : Disp Timing Period MIN [Tck]
DeltaDT = DTmax - DTmin
Tvblk : V Blanking [lines]
Tck : DTCLK

When there are invalid timing, Display appears black pattern.
Synchronous Signal Defects and enter Auto Refresh for LCD Module protection Mode.

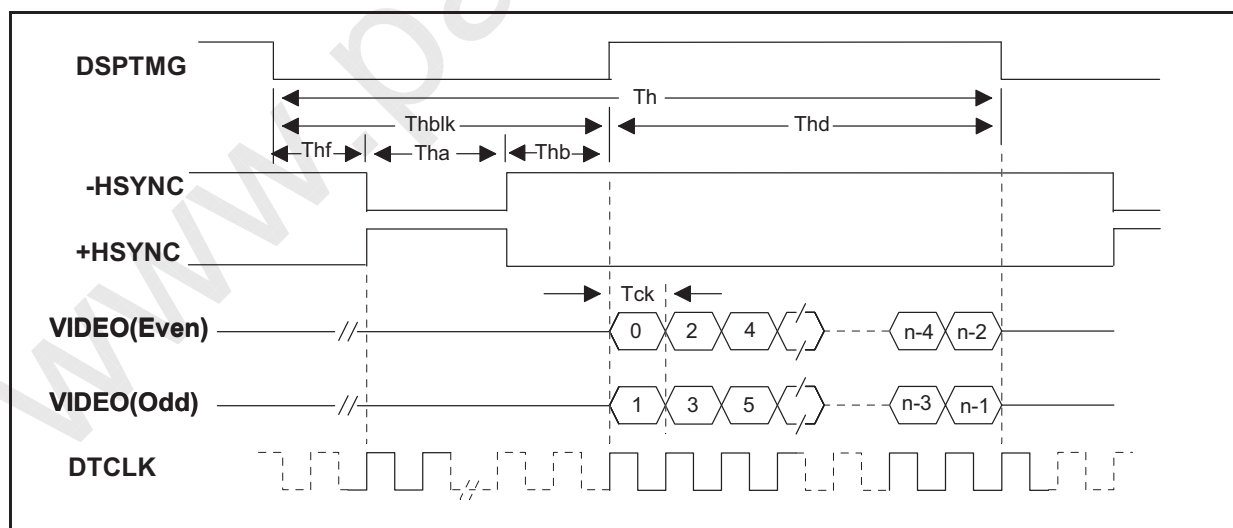Customer's Acceptance Specification

8.2 Timing Definition

Vertical Timing

Support mode	Tvblk Vertical Blanking	m Active Field	Tvf VSYNC Front Porch	Tv,Nv Frame Time	Tva VSYNC Width	Tvb VSYNC Back Porch
1600 x 1200 at 60Hz (H line rate : 13.3 us)	0.667 ms (50 lines)	16.000 ms (1200 lines)	0.013 ms (1 line)	16.667 ms (1250 lines)	0.040 ms (3 lines)	0.613 ms (46 lines)
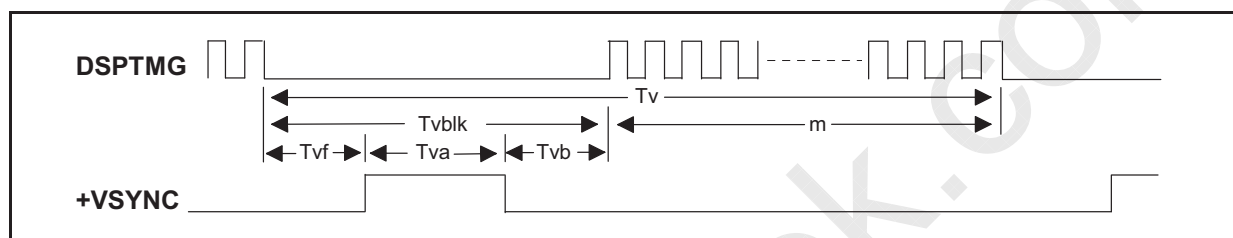
Horizontal Timing

Support mode	Thblk Horizontal Blanking	Thd Active Field	Thf HSYNC Front Porch	Th,Nh H Line Time	Tha HSYNC Width	Thb HSYNC Back Porch
1600 x 1200 Dotclock : 162.000 MHz (81.000MHz x2)	3.457 us (560 dots)	9.877 us (1600 dots)	0.395 us (64 dots)	13.333 us (2160 dots)	1.185 us (192 dots)	1.877 us (304 dots)

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9.0 Power Consumption

Input power specifications are as follows;

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	V	Load Capacitance 68uF
PDD	VDD Power			3.8	W	MAX Pattern **VDD=3.6V**
PDD	VDD Power		2.9		W	All White Pattern **VDD=3.3V**
IDD	VDD Current			1,250	mA	MAX Pattern **VDD=3.0V**
IDD	VDD Current		880		mA	All White Pattern **VDD=3.3V**
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	

Note : Max Pattern: Sub-pixel checker

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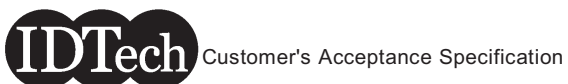
10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.
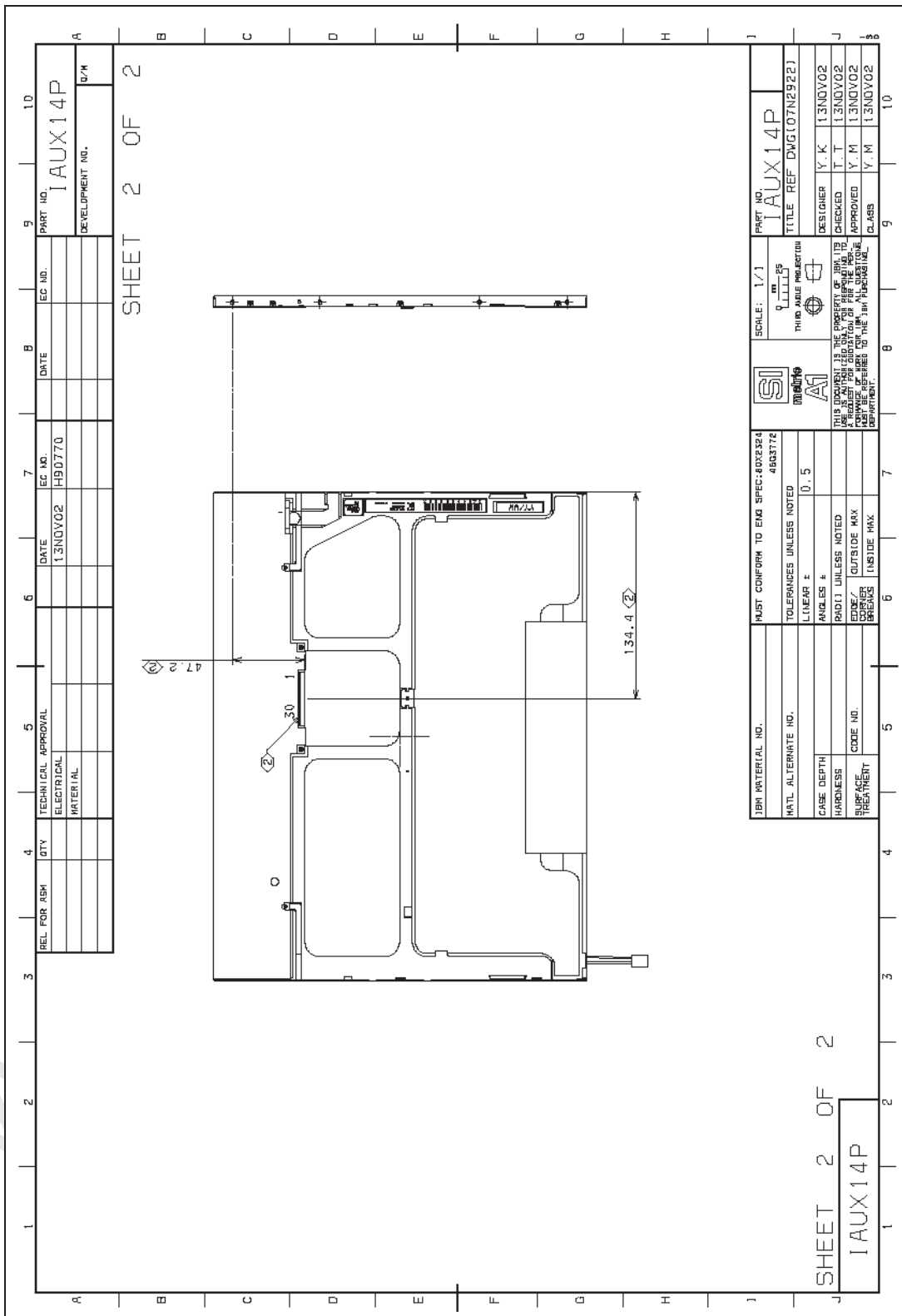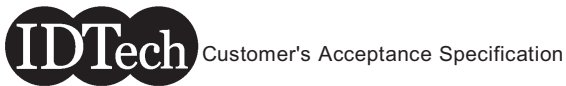
December 5,2002   CAS I-914P-L01

IDTech Customer's Acceptance Specification
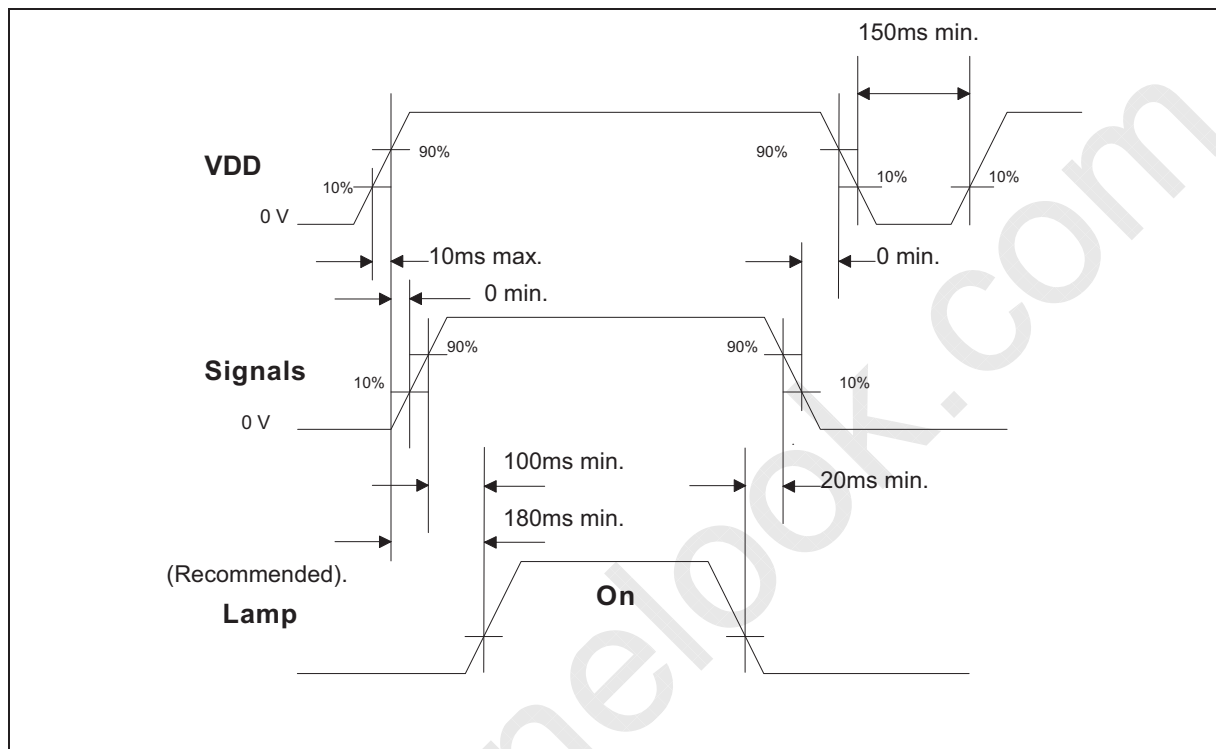
11.0 Mechanical Characteristics
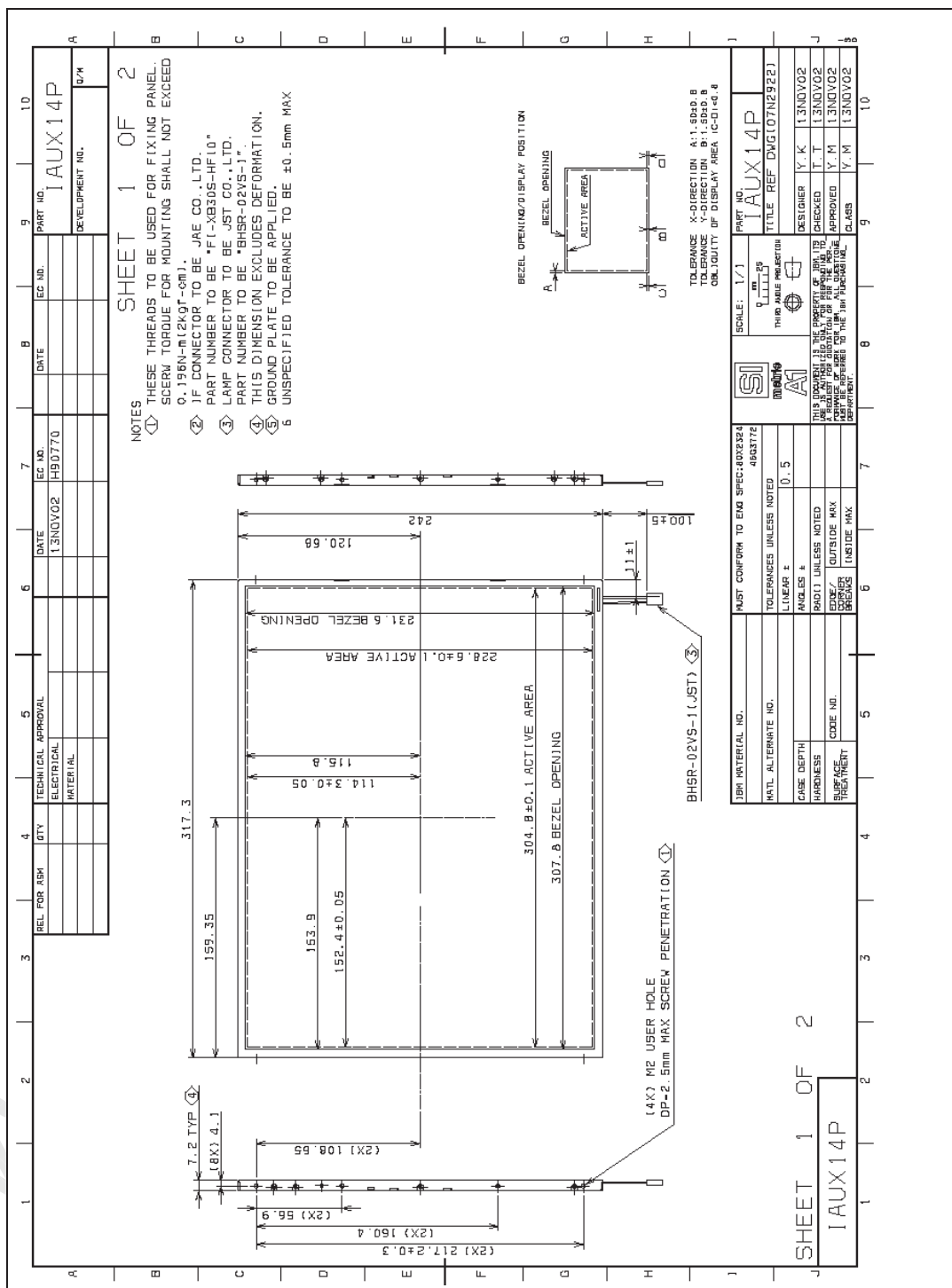
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Customer's Acceptance Specification

## 12.0   National Test Lab Requirement

The display module is authorized to Apply the UL Recognized Mark.

Conditions of Acceptability

Conditions of Acceptability - When installed on the end-product, consideration shall be given to the following;

1.   This component has been judged on he basis of he required spacings in the Standard for Safety of Information Technology Equipment, CAS/CSA C22.2 No. 60950-00 *UL 60950, Third Edition, which are based on the IEC 60950, Third Edition, which would cover the component itself if submitted for Listing.

2.   The unit is supplied by Limited Power Sources.

3.   The terminals and connectors are suitable for factory wiring only.

4.   The terminals and connectors have not been evaluated for field wiring.

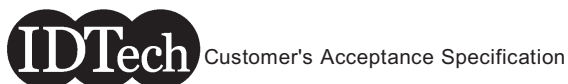5.   A suitable Electrical and Fire enclosure shall be provided.

Panel back should be separated from source of fire at least 13 mm of air or solid barrier of material of

Flammability Class V-1.

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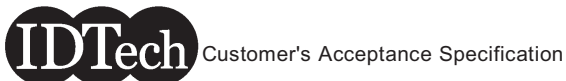
13.0 Packaging Specification

The packaging of the LCD meets 75 cm drop test.
The following is the drawing of the package.

December 5,2002   CAS I-914P-L01   33/35

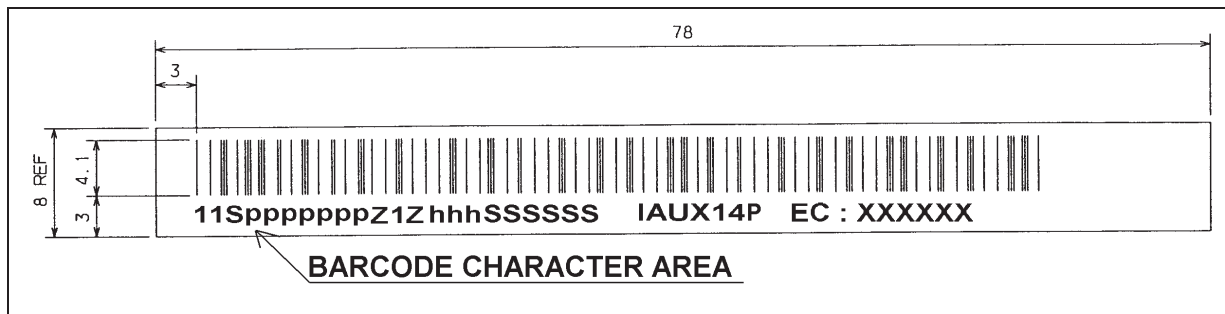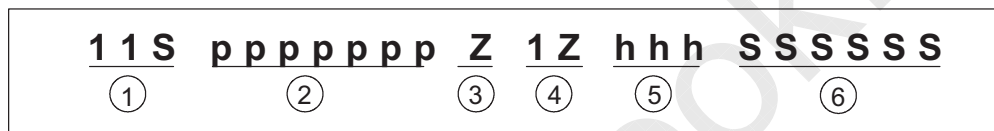IDTech Customer's Acceptance Specification
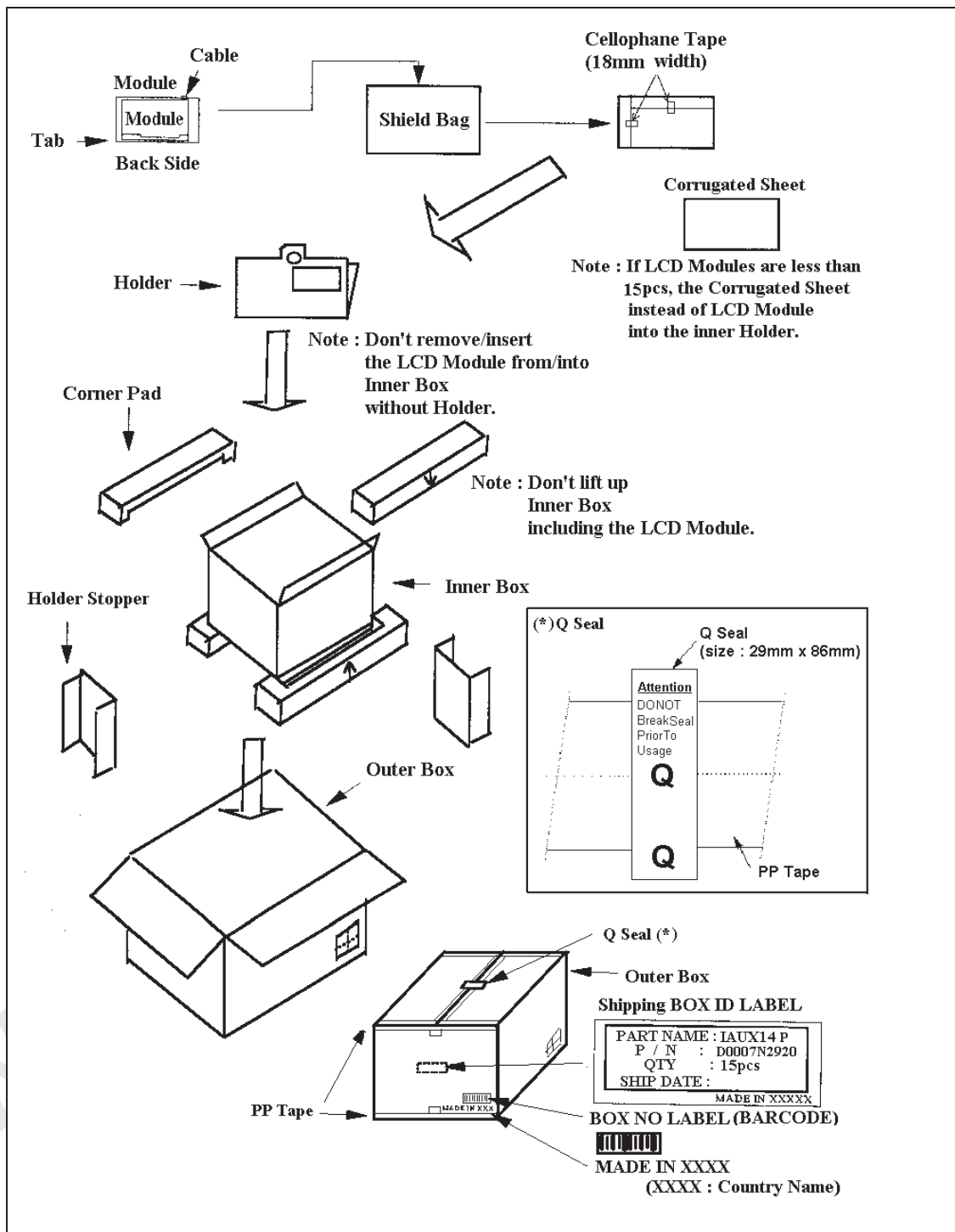
14.0   Label

There are labels on the rear side of the Module.

Serial Number Label

BARCODE CHARACTER AREA

① 11S = FIXED
Starting identifier which is common to component level serial numbers.

② Seven digit IBM part number Assigned by the IBM laboratory releasing the part

③ Z = FIXED
Automatically given when using the 11S-Z format

④ 1Z = FIXED
Location code

⑤ hhh = Header code
(Depend on EC Level and Manufacturing Location)
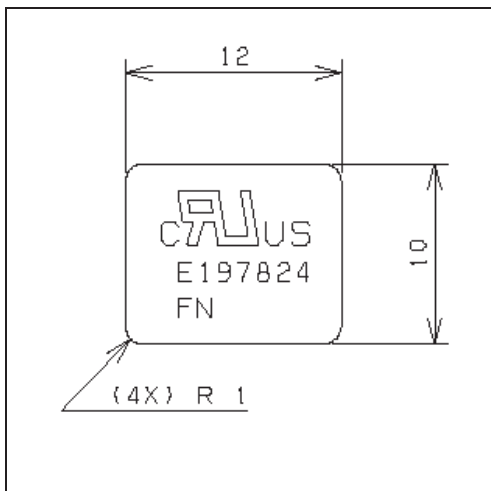
⑥ SSSSSS = Serial Number

Date Label

YY and WW of the Week Code stand for the Year and the Week of the Year of manufacturing of the Module respectively.

December 5,2002   CAS I-914P-L01   34/35
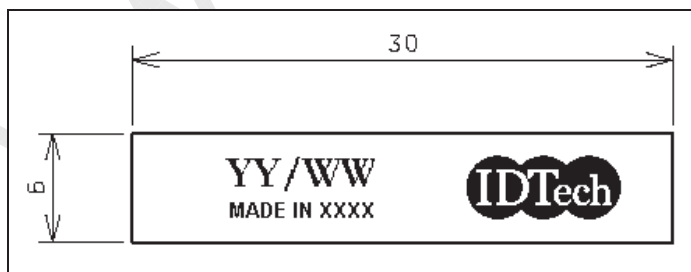
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UL Label

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December 5,2002　　　　　　　　　　CAS I-914P-L01　　　　　　　　　　35/35