IDTech Engineering Specification

Engineering Specification

Type 12.1 XGA Color TFT/LCD Module
Model Name:IAXG01M

Document Control Number : OEM I-901M-03

Note:Specification is subject to change without notice. Consequently it is better to contact to International Display Technology before proceeding with the design of your product incorporating this module.

Product Development
International Display Technology

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ii Record of Revision

Date	Document Revision	Page	Summary
December 21,2001	OEM I-901M-01	All	First Edition for customer. Based on Internal Spec. EC H30861 as of December 11,2001.
January 16,2002	OEM I-901M-02	21 22	Based on Internal Spec. EC H30861. To update the following items. • Min. value of CFL Current • Max. value of CFL Frequency • Min. value of CFL Ignition voltage • Note To update Luminance versus Lamp Power.
May 28,2002	OEM I-901M-03	6 23 27,28	To update Weight. To update Min. value of Frame Rate. To update Reference Drawings.

1.0 Handling Precautions

- If any signals or power lines deviate from the power on/off sequence, it may cause shorten the life of the LCD module.
- The LCD panel and the CFL are made of glass and may break or crack if dropped on a hard surface, so please handle them with care.
- CMOS-ICs are included in the LCD panel. They should be handled with care, to prevent electrostatic discharge.
- Do not press the reflector sheet at the back of the LCD module to any directions.
- Do not stick the adhesive tape on the reflector sheet at the back of the LCD module.
- Please handle care when mount in the system cover. Mechanical damage for lamp reflector, for lamp cable and for lamp connector may cause safety problems.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.5, IEC60950 or UL60950), or be applied exemption conditions of flammability requirements (4.7.3.4, IEC60950 or UL60950) in an end product.
- The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL60950).
- The fluorescent lamp in the liquid crystal display(LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Never apply detergent or other liquid directly to the screen.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth; do not use solvents or abrasives.
- Do not touch the front screen surface in your system, even bezel.
- Gently wipe the covers and the screen with a soft cloth.

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- The information contained herein may be changed without prior notice. It is therefore advisable to contact International Display Technology before proceeding with the design of equipment incorporationg this product.

2.0 General Description

This specification applies to the Type 12.1 Color TFT/LCD Module 'IAXG01M'.
This module is designed for a display unit of notebook style personal computer.
The screen format and electrical interface are intended to support the XGA(1024(H) x 768(V)) screen.
Support color is native 262K colors(RGB 6-bit data driver).
All input signals are LVDS(Low Voltage Differential Signaling) interface compatible.
This module does not contain an inverter card for backlight.

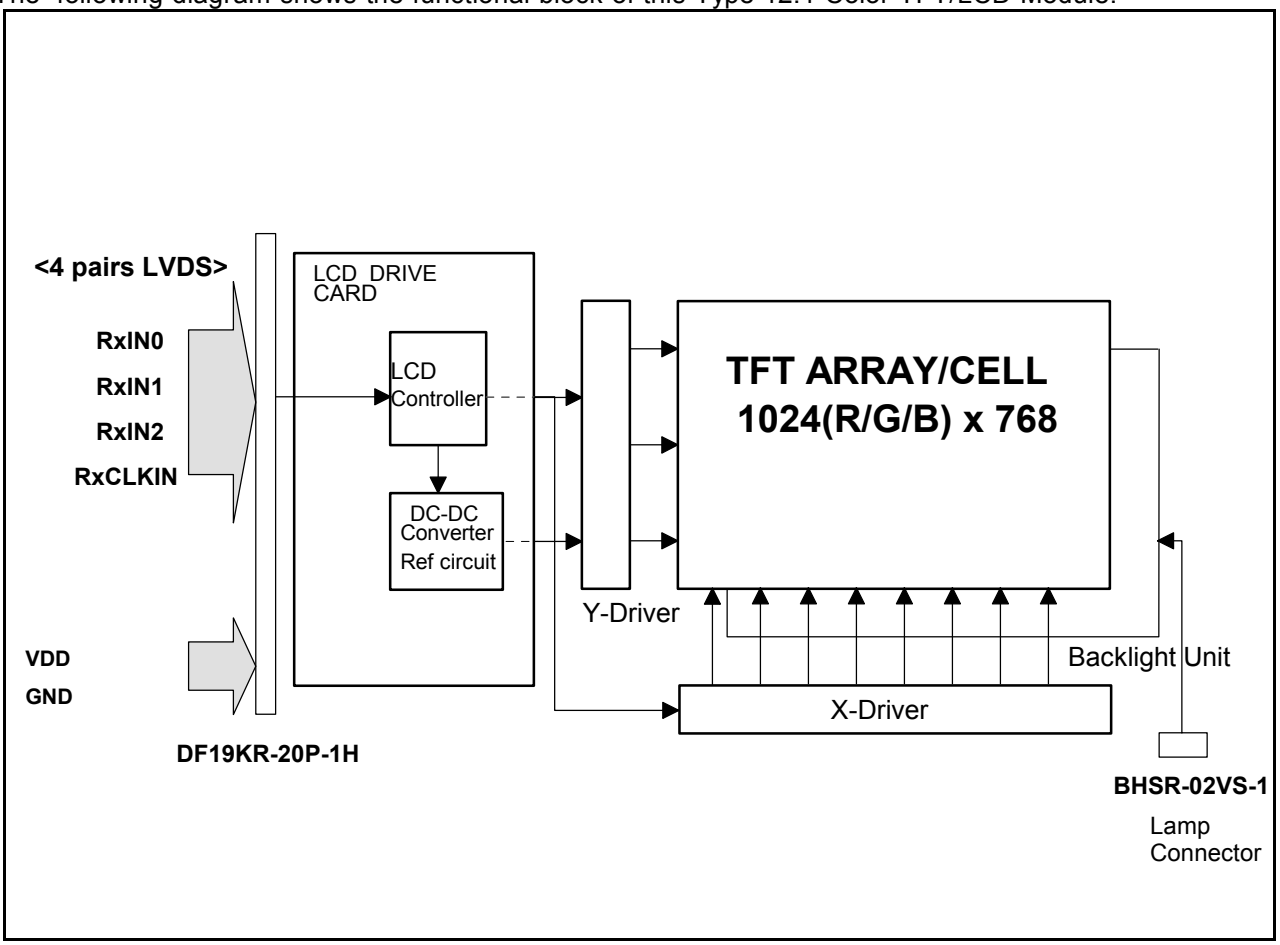
2.1 Characteristics

The following items are characteristics summary on the table under 25 degree C condition:

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	307.2
Pixels H x V	1024(x3) x 768
Active Area [mm]	245.76(H) x 184.32(V)
Pixel Pitch [mm]	0.240(per one triad) x 0.240
Pixel Arrangement	R,G,B Vertical Stripe
Weight [grams]	295 Typ.
Physical Size [mm]	261.0(W) x 198.0(H) x 5.0(D) Typ.
Display Mode	Normally White
Support Color	Native 262K colors(RGB 6-bit data driver)
White Luminance [cd/m^2] (center)	150 Typ.
Contrast Ratio	250 : 1 Typ.
Optical Rise Time / Fall Time [msec]	30 Typ., 50 Max.
Nominal Input Voltage VDD [Volt]	+3.3 Typ.
Power Consumption [Watt]	4.6 Typ. (All Black Pattern)
Electrical Interface	4 pairs LVDS(Even/Odd R/G/B Data(6bit), 3sync signals, Clock)
Temperature Range [degree C] Operating Storage (Shipping)	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of this Type 12.1 Color TFT/LCD Module.



3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	V	
Input Signal Voltage	VIN	-0.3	VDD+0.3	V	
CFL Ignition Voltage	Vs	-	+1,500	Vrms	**(Note 2)**
CFL Current	ICFL	-	7	mAms	
CFL Peak Inrush Current	ICFLP	-	20	mA	
Operating Temperature	TOP	0	+50	deg.C	**(Note 1)**
Operating Relative Humidity	HOP	8	95	%RH	**(Note 1)**
Storage Temperature	TST	-20	+60	deg.C	**(Note 1)**
Storage Relative Humidity	HST	5	95	%RH	**(Note 1)**
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Rectangle wave

Note :

1. Maximum Wet-Bulb should be 39 degree C and No condensation.
2. Duration : 50msec Max. Ta=0 degree C

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K≧10 (Left) Vertical (Upper) K≧10 (Lower)	40 40 15 30	- - - -
Contrast ratio		250	-
Response Time	Rising	30	-
(ms)	Falling	30	-
Color	Red x	0.577	-
Chromaticity	Red y	0.338	-
(CIE)	Green x	0.310	-
	Green y	0.554	-
	Blue x	0.158	-
	Blue y	0.124	-
	White x	0.313	-
	White y	0.329	-
White Luminance (cd/m^2)		150 Typ. (Center)	

5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	HIROSE
Type / Part Number	DF19KR-20P-1H
Mating Receptacle/Part Number	DF19G-20S-1F (FPC Type) DF19G-20S-1C (Cable Type)

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	BHSR-02VS-1
Mating Type / Part Number	SM02B-BHSS-1

5.2 Interface Signal Connector

Pin#	Signal	Pin#	Signal
1	GND	11	GND
2	GND	12	RxIN1+
3	Reserved	13	RxIN1-
4	Reserved	14	GND
5	GND	15	RxIN0+
6	RxCLKIN+	16	RxIN0-
7	RxCLKIN-	17	GND
8	GND	18	GND
9	RxIN2+	19	VDD
10	RxIN2-	20	VDD

Note:

- 'Reserved' pins are not allowed to connect any other line.
- Voltage levels of all input signals are LVDS compatible (except VDD,). Refer to "Signal Electrical Characteristics for LVDS", for voltage levels of all input signals.

5.3 Interface Signal Description

Signal Name	Description
RxIN0+, RxIN0-	LVDS differential data input (Red0-Red5, Green0)
RxIN1+, RxIN1-	LVDS differential data input (Green1-Green5,Blue0-Blue1)
RxIN2+, RxIN2-	LVDS differential data input (Blue2-Blue5, HSync, VSync, DSPTMG)
RxCLKIN+, RxCLKIN-	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Note :

- The module uses a 100ohm resistor between positive and negative data lines of each receiver input.
- Input signals shall be low or Hi-Z state when VDD is off

SIGNAL NAME	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) **Red-pixel Data**	Each red pixel's brightness data consists of these 6 bits pixel data.
+GREEN 5 +GREEN 4 +GREEN 3 +GREEN 2 +GREEN 1 +GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) **Green-pixel Data**	Each green pixel's brightness data consists of these 6 bits pixel data.
+BLUE 5 +BLUE 4 +BLUE 3 +BLUE 2 +BLUE 1 +BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) **Blue-pixel Data**	Each blue pixel's brightness data consists of these 6 bits pixel data.
-DTCLK	**Data Clock**	The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals.
DSPTMG	**Display Timing**	This signal is strobed at te falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	**Vertical Sync**	The signal is synchronized to -DTCLK .
HSYNC	**Horizontal Sync**	The signal is synchronized to -DTCLK .

Note : Output signals from any system shall be low or Hi-Z state when VDD is off.

5.4 Interface Signal Electrical Characteristics

5.4.1 Signal Electrical Characteristics for LVDS Receiver

Table. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Differential Input High Threshold	Vth			+100	mV	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100			mV	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100		600	mV	
Common Mode Voltage	Vcm	1.0	1.2	1.4	V	Vth - Vtl = 200mV
Common Mode Voltage Offset	ΔVcm	-50		+50	mV	Vth - Vtl = 200mV

Note:

- Input signals shall be low or Hi-Z state when VDD is off.
- All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD (see Figure "Measurement system").

Figure. Voltage Definitions

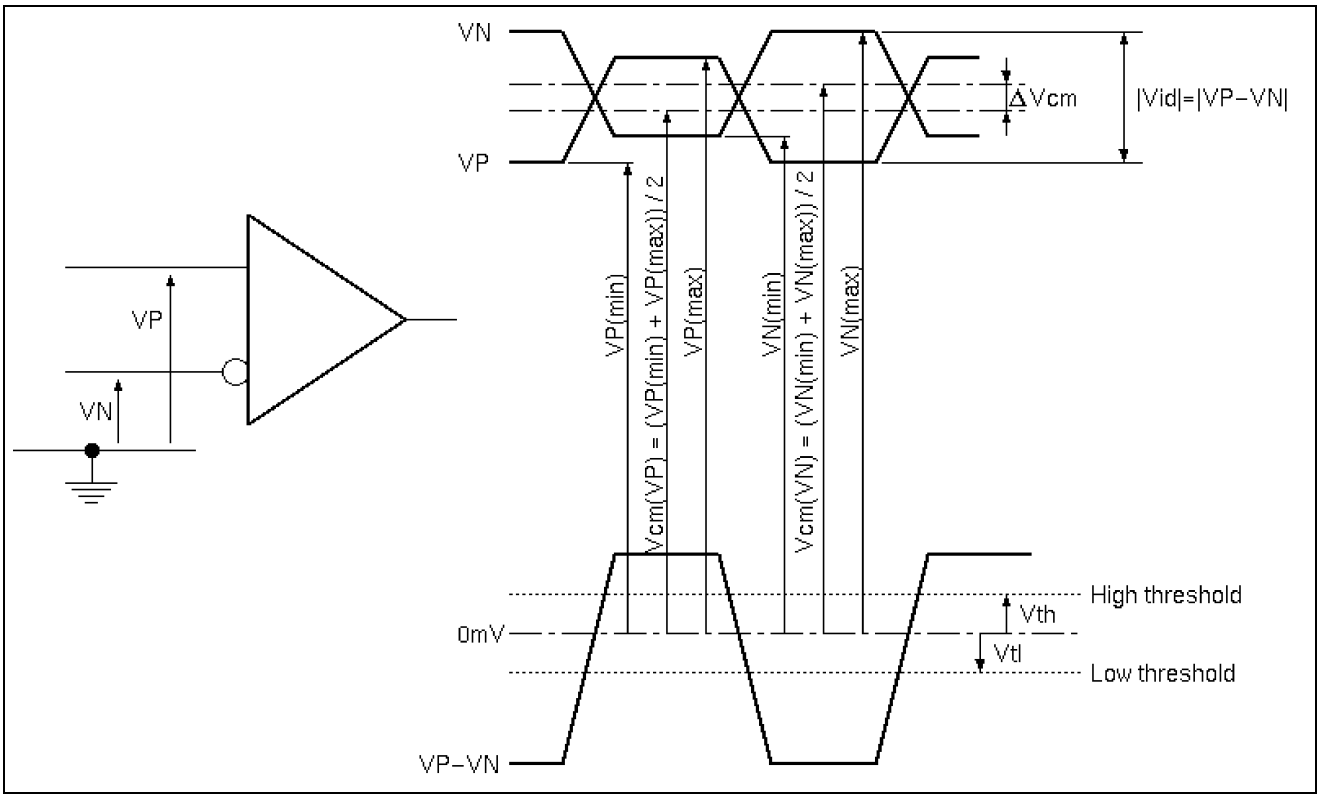


Figure. Measurement system

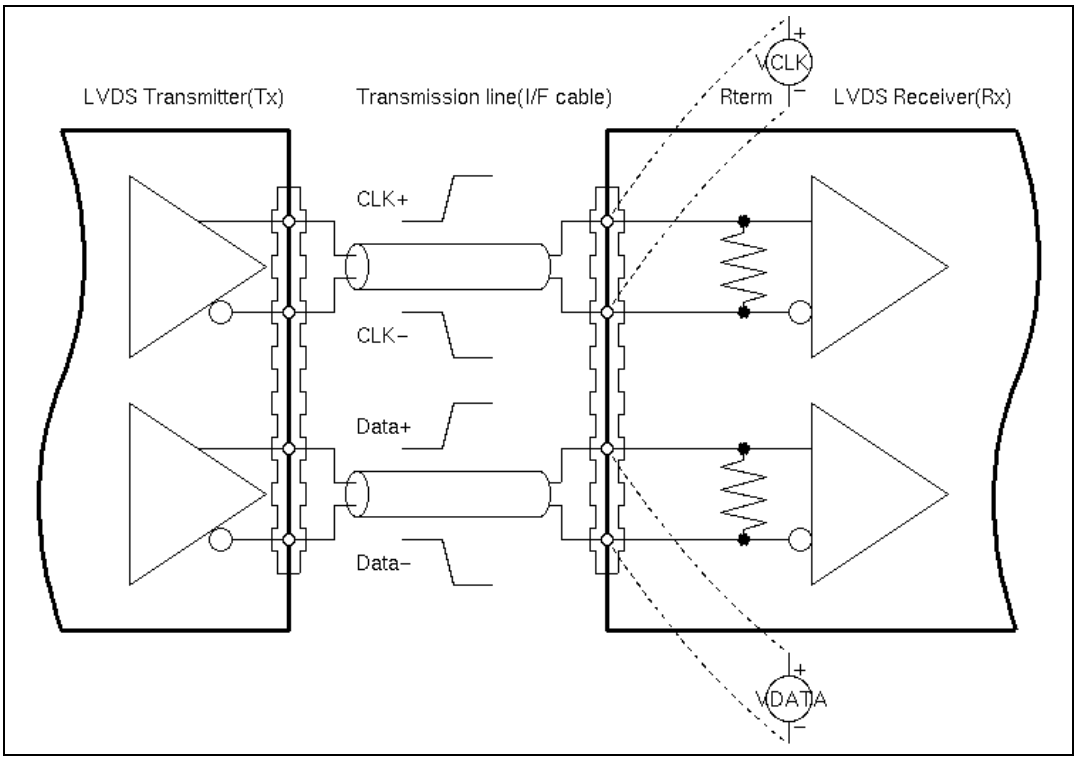


Table. Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Clock Frequency	fc	50	65	67	MHz	
Cycle Time	tc	14.93	15.38	20.00	ns	
Data Setup Time**(Note 2)**	Tsu	500			ps	fc = 65MHz, tCCJ < 50ps, Vth-Vtl = 400mV, Vcm = 1.2V, ΔVcm = 0
Data Hold Time**(Note 2)**	Thd	500			ps	
Cycle-to-cycle jitter**(Note 3)**	tCCJ	-150		+150	ps	
Cycle Modulation Rate**(Note 4)**	tCJavg			20	ps/clk	

Note :

1. All values are at VDD=3.3V, Ta=25 degree C.
2. See figure "Timing Definition" and "Timing Definition(detail A)" for definition.
3. Jitter is the magnitude of the change in input clock period.
4. This specification defines maximum average cycle modulation rate in peak-to-peak transition within any 100 clock cycles.
   This specification is applied only if input clock peak jitter within any 100 clock cycles is greater than 300ps.

Figure. Timing Definition (Even)

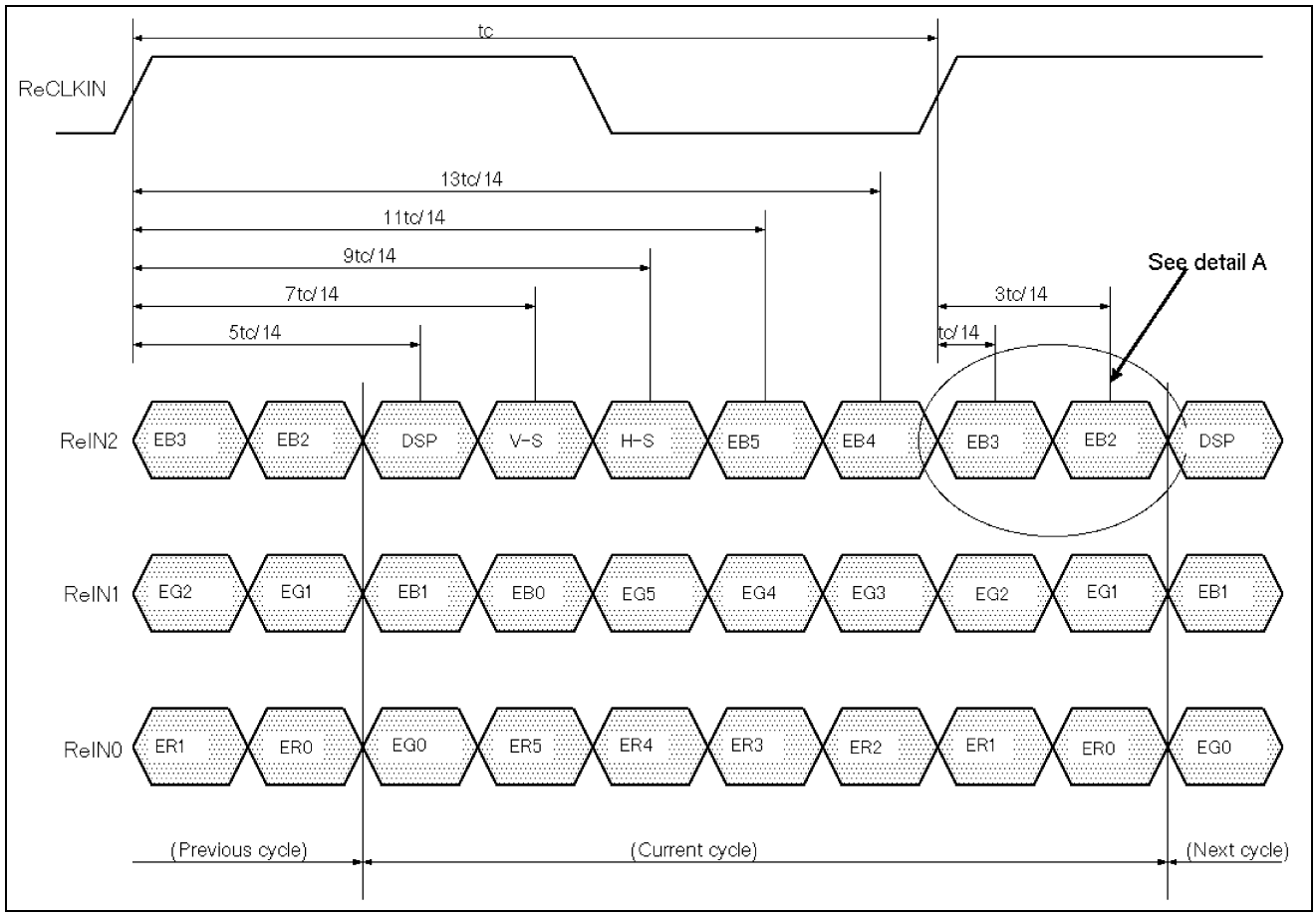


Figure. Timing Definition (Odd)

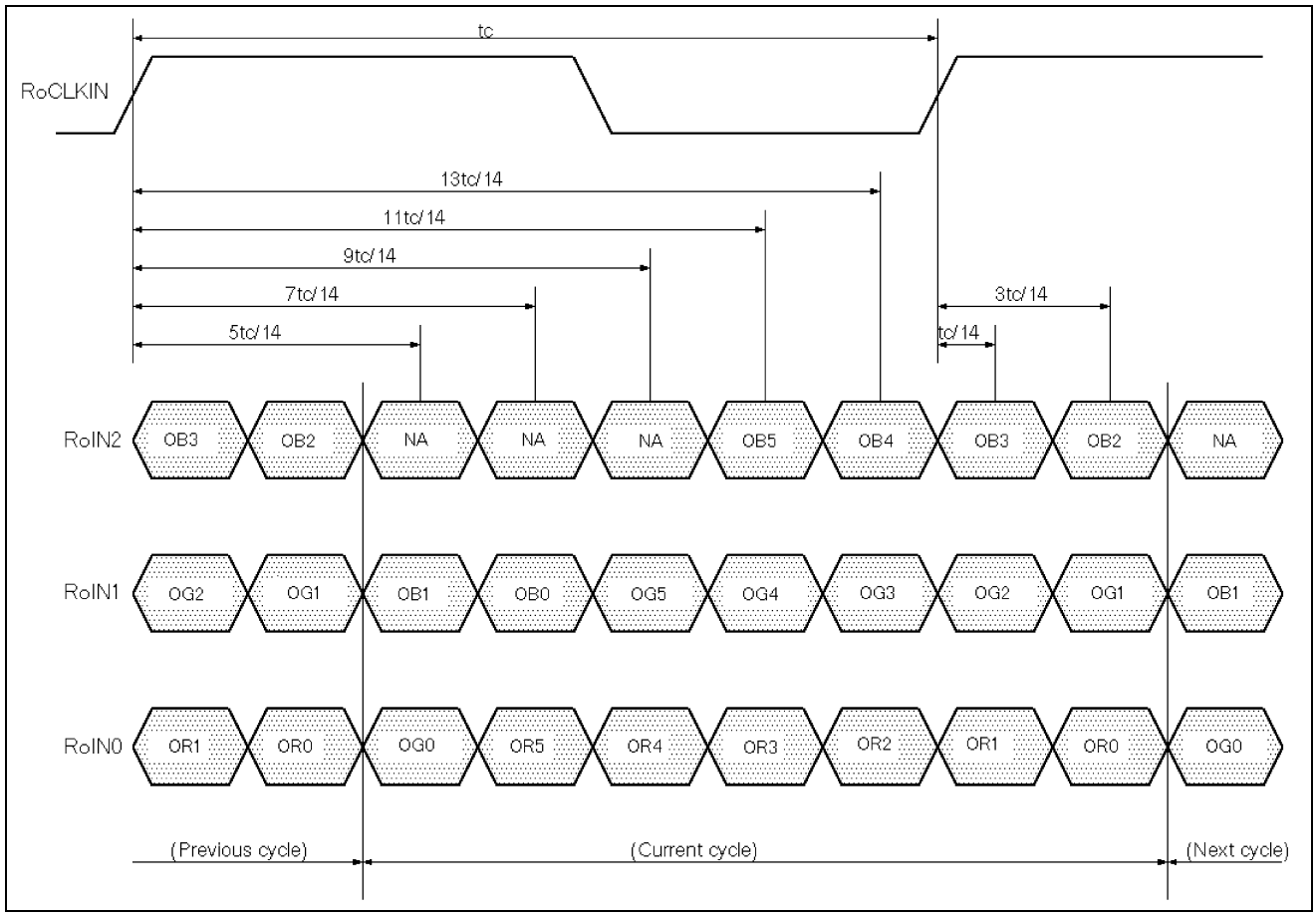
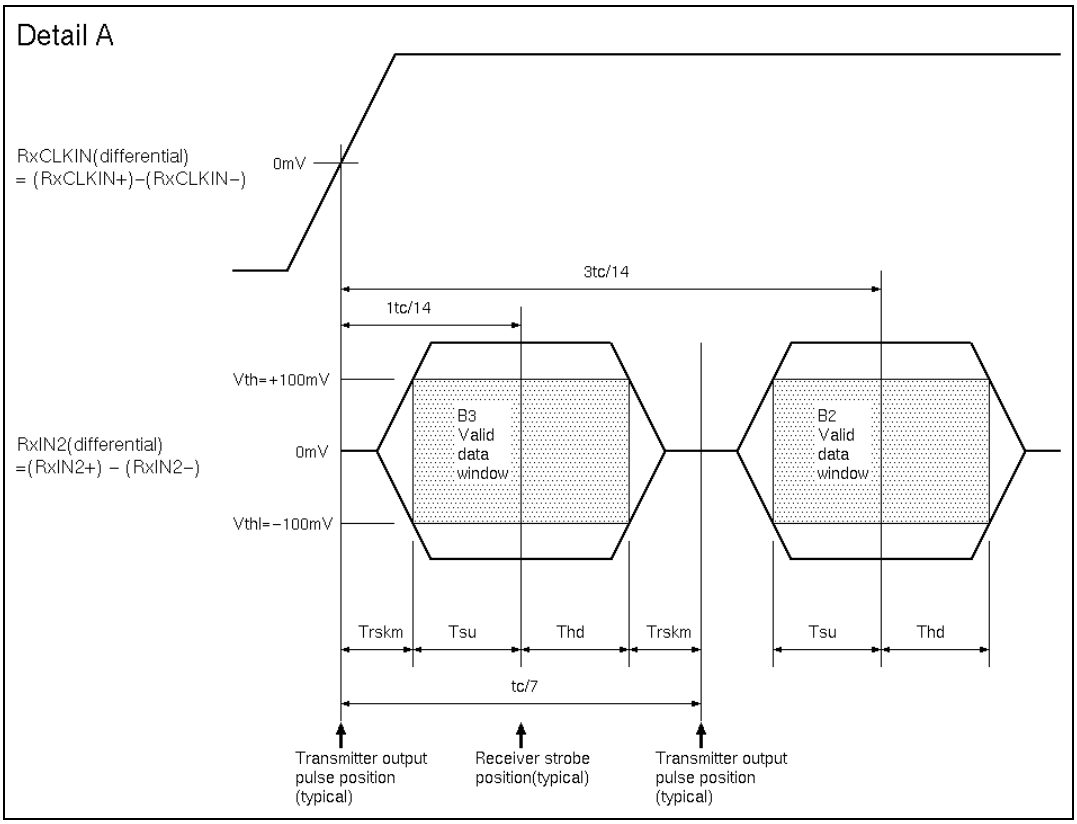


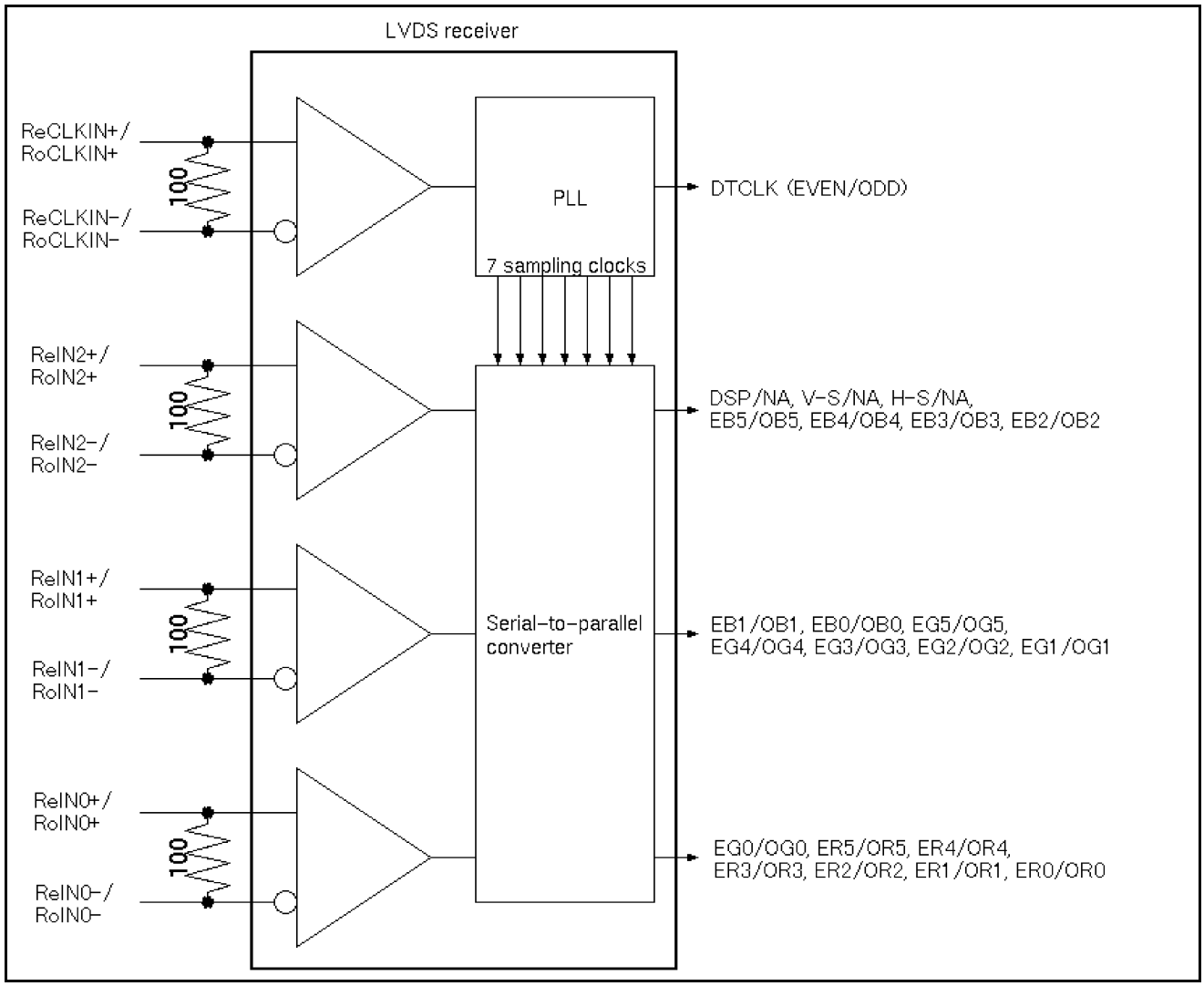
Figure. Timing Definition(detail A)



Note: Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

5.4.2 LVDS Receiver Internal Circuit

The following figure shows the internal block diagram of the LVDS receiver.
This LCD module equips termination resistors for LVDS link.



5.4.3 Recommended Guidelines for Motherboard PCB Design and Cable Selection

Following the suggestions below will help to achieve optimal results.

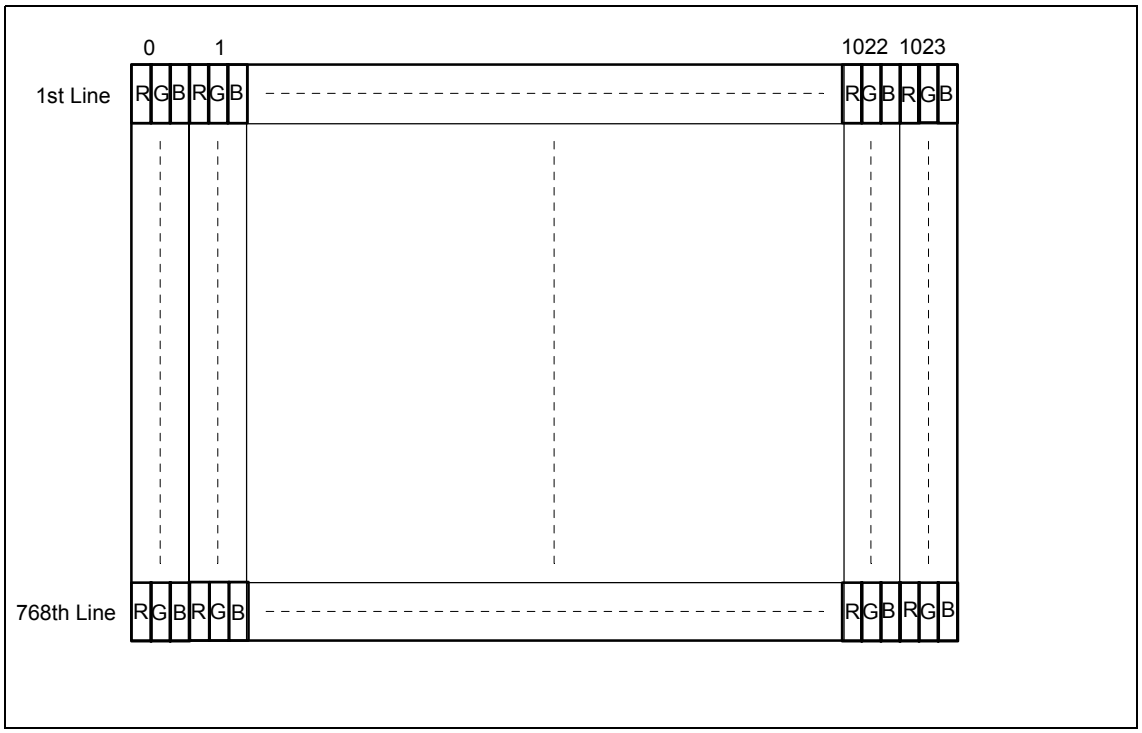
- Use controlled impedance media for LVDS signals. They should have a matched differential impedance of 100ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TTL signals from LVDS signals.
- For cables, twisted pair, twinax, or flex circuit with close coupled differential traces are recommended.

5.5 Signal for Lamp Connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp Low Voltage

6.0 Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format image.



7.0 Parameter guide line for CFL Inverter

SYMBOL	PARAMETER	MIN	D.P-1 (Note1)	D.P-2 (Note2)	MAX	UNITS	CONDITION
(L63)	White Luminance (Center) (5 points average)	 - -	 95 90	 150 140	 - -	 [cd/m^2] [cd/m^2]	Ta=25[deg. C]
ICFL	CFL current	2.0	3.5	6.0	7.0	[mArms]	Ta=25[deg. C] **Note3, 4**(*7, *8)
ICFLP	CFL Peak Inrush Current				20	[mA]	Ta=25[deg. C] **Note3, 4**(*7)
FCFL	CFL Frequency	40			70	[kHz]	Ta=25[deg. C] **Note 1, 4**(*5)
Vinv	Inverter Ignition Voltage	1,350				[Vrms]	Ta=0[deg. C] **Note 3**
VCFL	CFL Voltage (Reference)		655	560		[Vrms]	Ta=25[deg. C] **Note 2**
PCFL	CFL Power consumption		2.3	3.4		[W]	Ta=25[deg. C] **Note 2, 4**(*6)

Note 1: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 2: Calculated value for reference (ICFL x VCFL = PCFL).

Note 3: CFL inverter should be able to give out a power that has a generating capacity of over 1,350 voltage. Lamp units need 1,350 voltage minimum for ignition.

Note 4: DP-1(Design Point-1) and DP-2(Design Point-2) are recommended Design Point.

*1 All of characteristics listed are measured under the condition using the Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

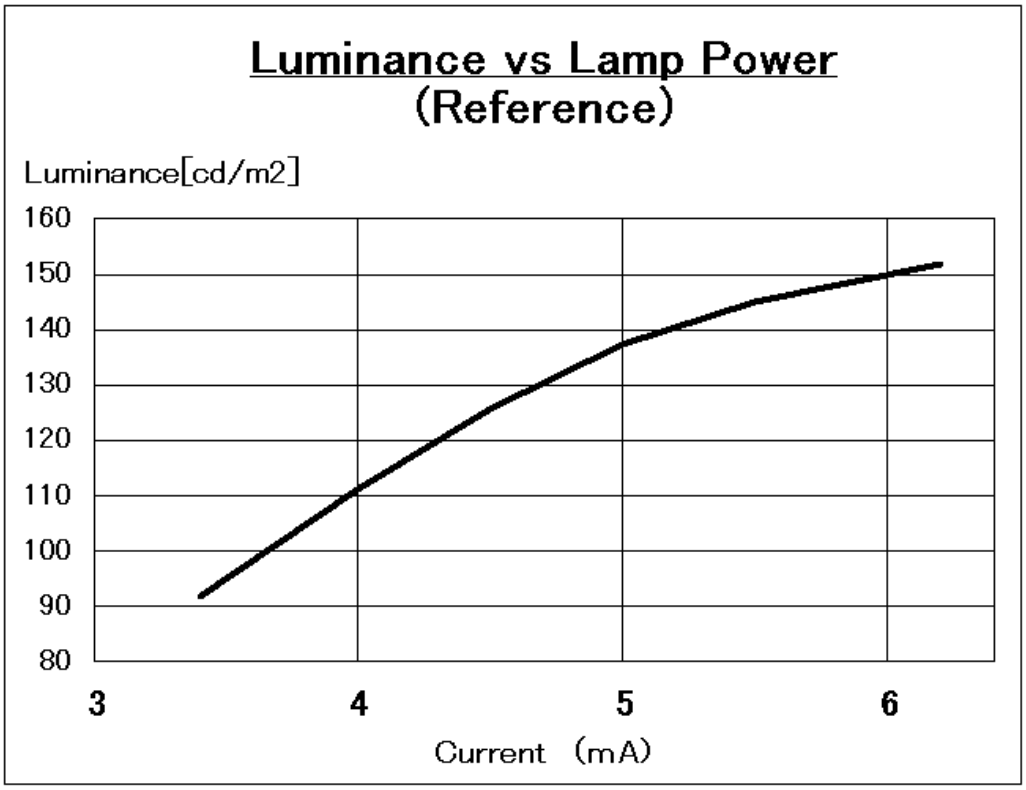
*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

*7 It should be employed the inverter which has 'Duty Dimming', if ICFL is less than 4[mA].

*8 ICFL = (ICFL Peak) x (Duty Dimming Rate)

The following chart is Luminance versus Lamp Power for your reference.



8.0 Interface Timings

Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS86(Texas Instruments) or equivalent.

8.1 Timing Characteristics

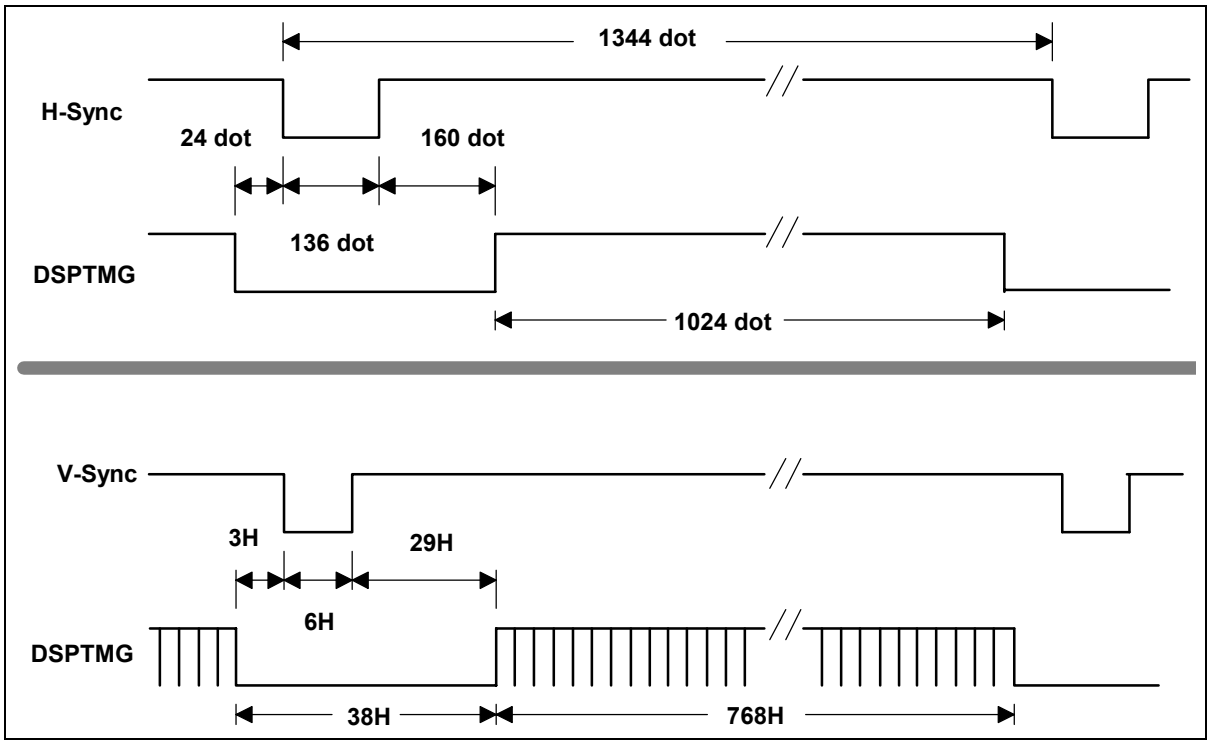
Timing Characteristics

Symbol		MIN	TYP	MAX	Unit	Note
fdck	DTCLK Frequency	50.00	65.00	67.00	MHz	
tck	DTCLK cycle time	14.93	15.38	20.00	nsec	
tx	X total time	1324	1344	2047	tck	
tacx	X active time	1024	1024	1024	tck	
Hsync	H frequency		48.363		KHz	
Hsw	H-Sync width	8	136		tck	
Hbp	H back porch	8	160		tck	
Hfp	H front porch	0	24		tck	
ty	Y total time	779	806	1023	tx	
tacy	Y active time	768	768	768	tx	
Vsync	Frame rate	55	60	61	Hz	
Vw	V-sync Width	1	6		tx	
Vfp	V-sync front porch	1	3		tx	
Vbp	V-sync back porch	9	29	63	tx	1

Note:

1. Vbp should be static
2. When there are invalid timing, Display appears black pattern.
   Synchronous Signal Defects and enter Auto Refresh for LCD Module protection Mode.

8.2 Timing Definition



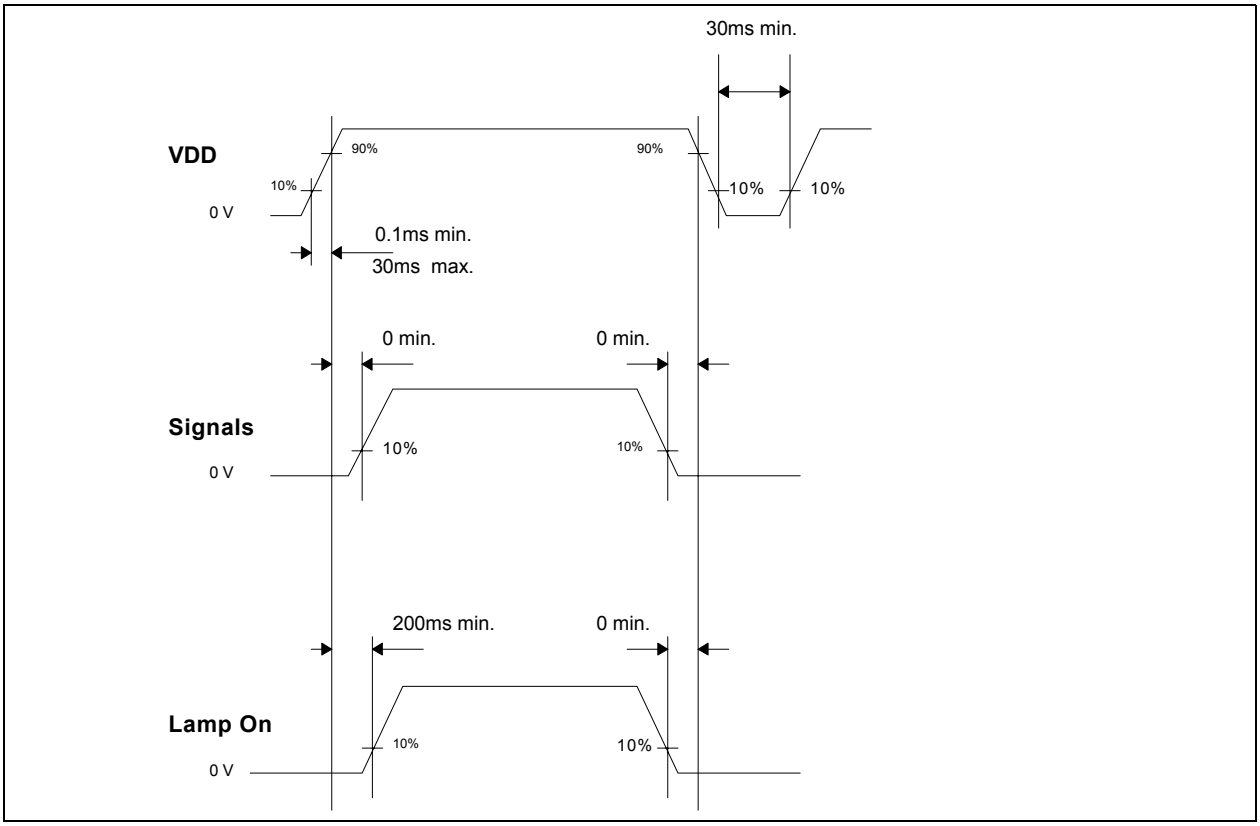
9.0 Power Consumption

Input power specifications are as follows;

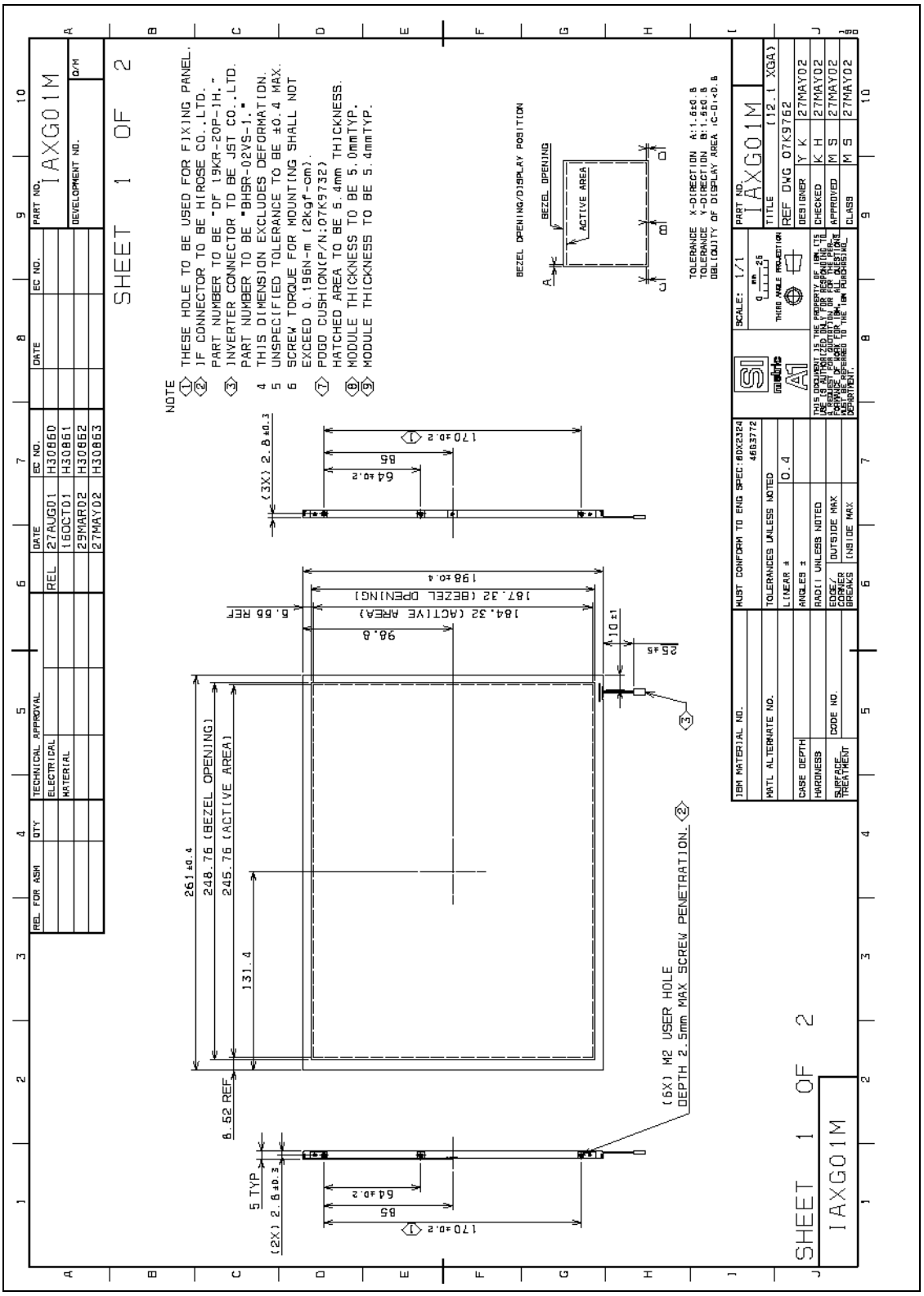
SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[V]	Load Capacitance 20 uF
PDD	VDD Power			1.6	[W]	MAX. Pattern, VDD=3.3[V]
PDD	VDD Power		1.2		[W]	All Black Pattern, VDD=3.3[V]
IDD	VDD Current			480	[mA]	MAX Pattern, VDD=3.3[V]
IDD	VDD Current		360		[mA]	All Black Pattern, VDD=3.3[V]
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	

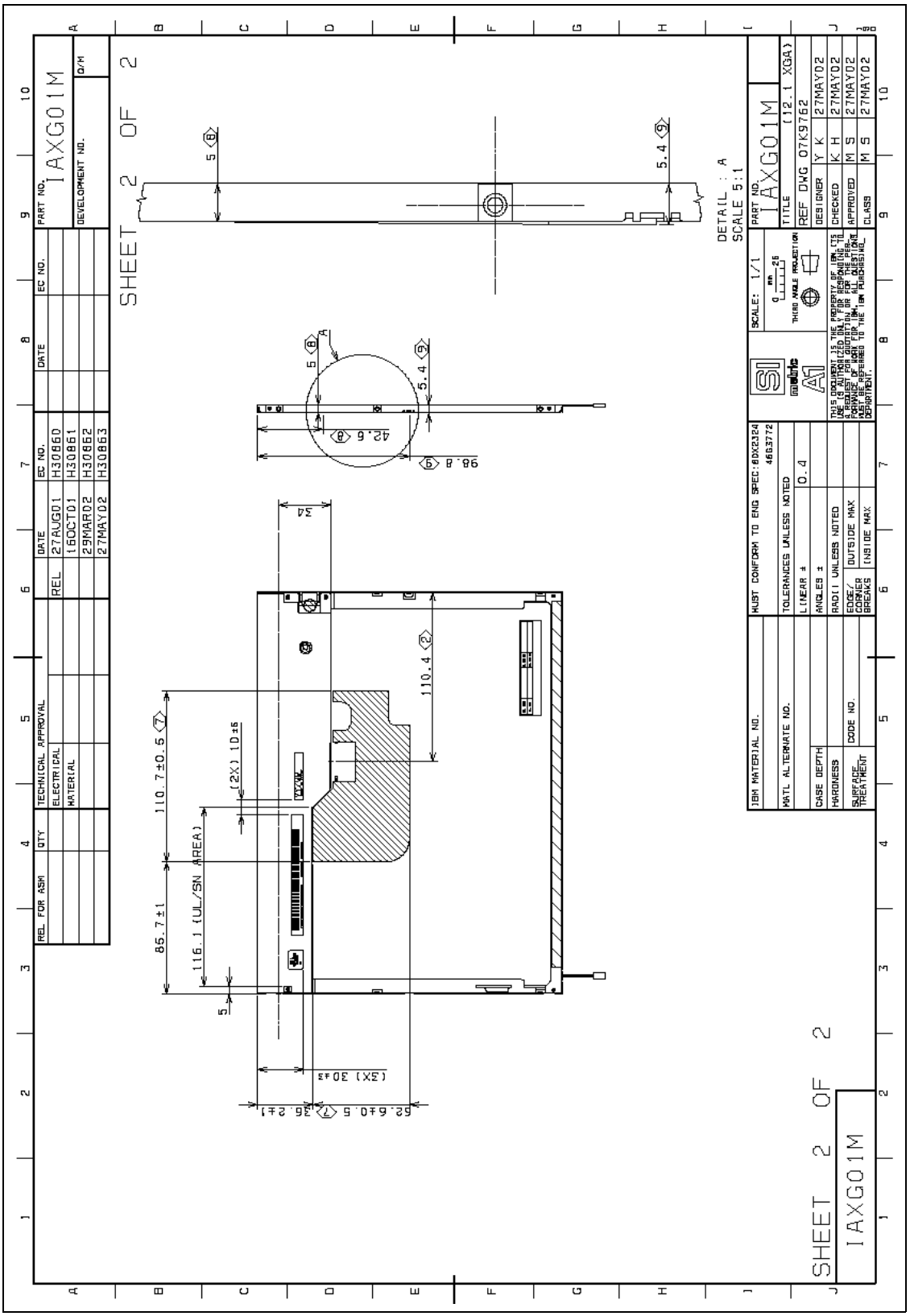
10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off .



11.0 Mechanical Characteristics





12.0 National Test Lab Requirement

The display module is satisfied all requirements for compliance to

UL60950 3rd. Ed.	U.S.A. Information Technology Equipment

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