

## Preliminary STB032xx and STB034xx Digital Set-Top Box Integrated Controllers

### Features

#### Overall

- High-End Set-Top Box technology
- Four major subsystems integrated with IBM® on-chip CoreConnect™ structure.
- Maximum MIPS for OS and application tasks
- Simplified driver and software development
- Scalable, flexible, and extendible
- 108 MHz/150 MIPS and 162 MHz/225 MIPS versions available
- 3.3 V and 2.5 V power supplies
- IBM CMOS SA-12E (0.25 µm) process technology
- 304-pin PBGA package

#### MPEG-2 Digital Audio/Video Subsystem

- MPEG-2 Video Decoder
- MPEG-2 Audio Decoder
- MPEG-2 Transport/DVB Descrambler
- Dolby® Digital Audio<sup>1</sup> support on selected parts
- Macrovision Copy Protection on selected parts
- Display Controller
- Digital Encoder (DENC) with six outputs
- Anti-Flicker Filter

#### PowerPC 405™ Host Processor: PPC405B3 CPU

- 16KB Instruction, 8KB Data caches
- Universal Interrupt Controller

#### Memory Subsystem

- DMA Controller
- Cross-Bar Switch
- External Bus Interface Unit (EBIU)
- IDE interface
- Two SDRAM Controllers

#### Peripheral Subsystem

- General Purpose Timers (GPTs)
- Pulse Width Modulators
- 1284 Parallel Port
- Two Smart Card controllers
- Two I<sup>2</sup>C Interfaces
- 16550 Serial Communications Port
- Infrared Serial Communications Port
- General Purpose Input/Output (GPIO)
- Serial Controller Port
- Modem Serial Interface/Digital Audio Input

### Description

IBM STB03xxx Digital Set-Top Box Integrated Controller family are highly integrated silicon devices specifically developed for digital set-top box (STB) applications using industry-leading IBM CMOS SA-12E (0.25 µm) process technology.

The STB03xxx is part of the second generation of IBM products for digital STB applications. PowerPC processing and peripheral I/O architecture provide a high level of performance and functionality when used in audio and video subsystems. The resulting STB technology is full-functioned and easy to use.

The STB03xxx minimizes host processor intervention to maximize MIPS for operating system and application tasks. Most of the features required in the back end of typical midrange and high-end STBs are integrated. Driver and software development is facilitated while preserving scalability, flexibility, and extendibility.

Architecturally, the devices consist of four subsystems interconnected and tuned using CoreConnect, the IBM multiple-bus, on-chip interconnect structure:

1. PowerPC host processor
2. Digital audio/video
3. Memory interface
4. Peripheral

These high performance subsystems are suited to advanced interactive STBs with demanding software requirements including web browsers and Java™.

1. This implementation has not yet completed the evaluation process by Dolby Laboratories and is offered subject to obtaining approval. A Dolby Digital Audio license is required from Dolby Laboratories.



## Ordering Information

Part Number	Performance (est.)	Clock Speed	Audio	Copy Protection
IBM39STB03200PBB09C	150 MIPS	108 MHz	MPEG	None
IBM39STB03201PBB09C				Macrovision <sup>2</sup>
IBM39STB03210PBB09C			MPEG/Dolby Digital <sup>1</sup>	None
IBM39STB03211PBB09C				Macrovision <sup>2</sup>
IBM39STB03400PBB06C	225 MIPS	162 MHz	MPEG	None
IBM39STB03401PBB06C				Macrovision <sup>2</sup>
IBM39STB03410PBB06C			MPEG/Dolby Digital <sup>1</sup>	None
IBM39STB03411PBB06C				Macrovision <sup>2</sup>

1. These parts include Dolby Digital enabling software and require the user to obtain a license from Dolby Laboratories Licensing Corporation. Please see "Dolby Digital Licensing" on page 3.

2. These parts support Macrovision Copy Protection and require that a license be in effect between the purchaser and Macrovision Corporation. Please see "Macrovision Licensing" on page 3.

## Conventions and Notation

Throughout this document, standard IBM notation is used, meaning that bits and bytes are numbered in ascending order from left to right. Thus, for a 4-byte word, bit 0 is the most significant bit and bit 31 is the least significant bit.

Overbars, e.g.  $\overline{\text{TxEnb}}$ , designate signals that are active low.

Numeric notation is as follows:

Hexadecimal values are in single quotes and preceded by "x" or "X." For example: x'0B00'.

Binary values are spelled out (zero and one) or appear in single quotes and preceded by a "b."  
 For example: b'10101'.

Settings of a bit or field are binary numbers but are often displayed in tabular form without quotes or the preceding "b."

For example:

- 00 : 30 frames per second
- 01 : 15 frames per second
- 11 : 10 frames per second



## Licensing Requirements

### Dolby Digital Licensing

Dolby Digital audio enabling software is provided with the IBM39STB0321x and IBM39STB0341x products.

Dolby is a trademark of the Dolby Laboratories. Supply of this implementation of Dolby Technology does not convey a license or imply a right under any patent, or any other Industrial or Intellectual Property Right of Dolby Laboratories, to use this implementation in any end-user or ready-to-use final product. Companies planning to use this implementation in products must obtain a license from Dolby Laboratories Licensing Corporation before designing such products. Additional per-chip royalties may be required and are to be paid by the purchaser to Dolby Laboratories, Inc. Details of the OEM Dolby Digital license may be obtained by writing to:

Dolby Laboratories Inc.  
Dolby Laboratories Licensing Corporation  
Attn: Intellectual Property Manager  
100 Potrero Avenue  
San Francisco, CA 94103-4813

### Macrovision Licensing

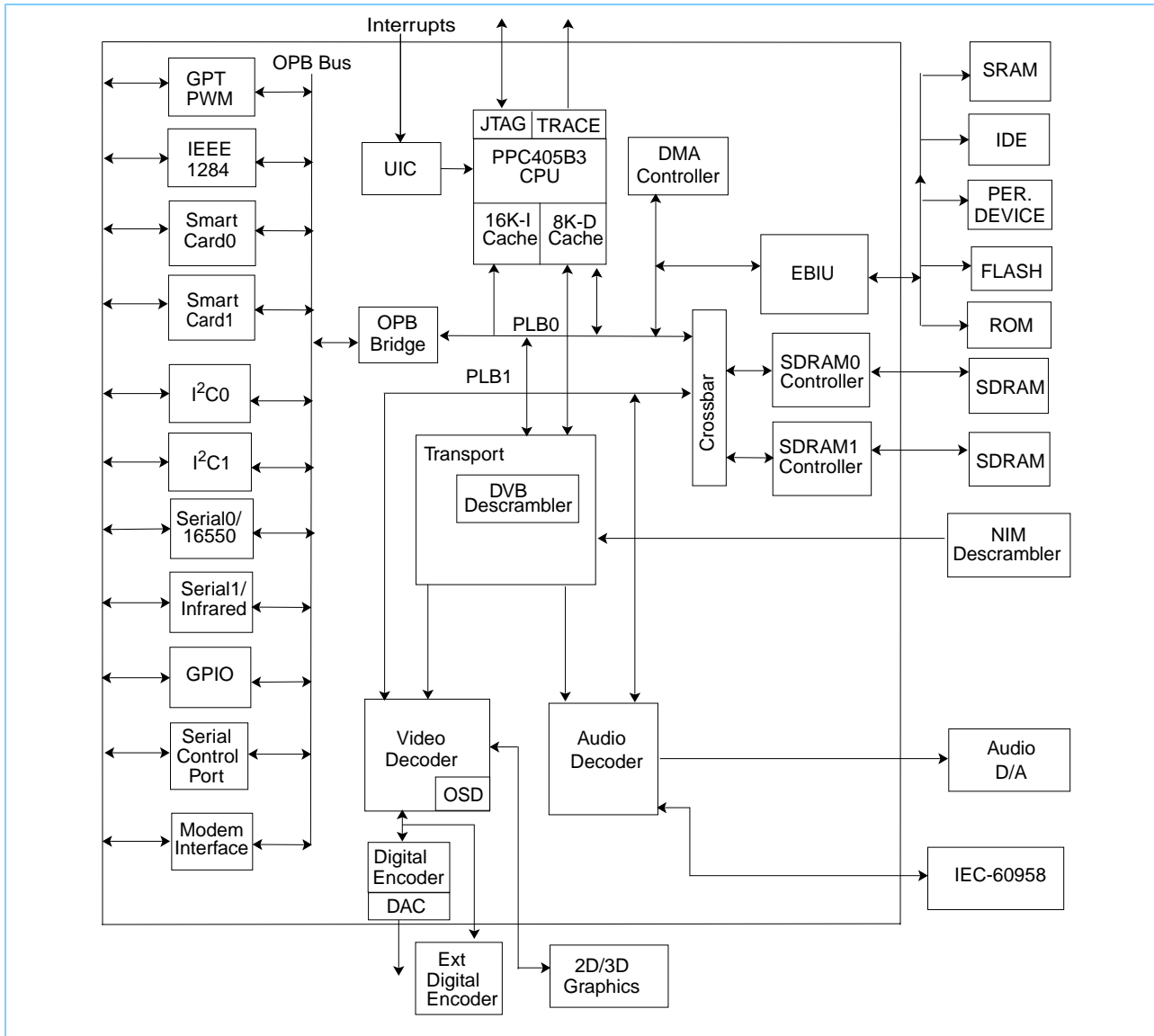
Macrovision Copy Protection is supported in the IBM39STB032x1 and IBM39STB034x1 products. These devices are protected by U.S. patent numbers 4,631,603, 4,577,216, and 4,819,098 and other intellectual property rights. The use of Macrovision's Copy Protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Macrovision.

Reverse engineering or disassembly is prohibited. A valid Macrovision license must be in effect between the STB03xx1 purchaser and Macrovision Corporation. Additional per-chip royalties may be required and are to be paid by the purchaser to Macrovision Corporation.

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## Architecture and Subsystem Information

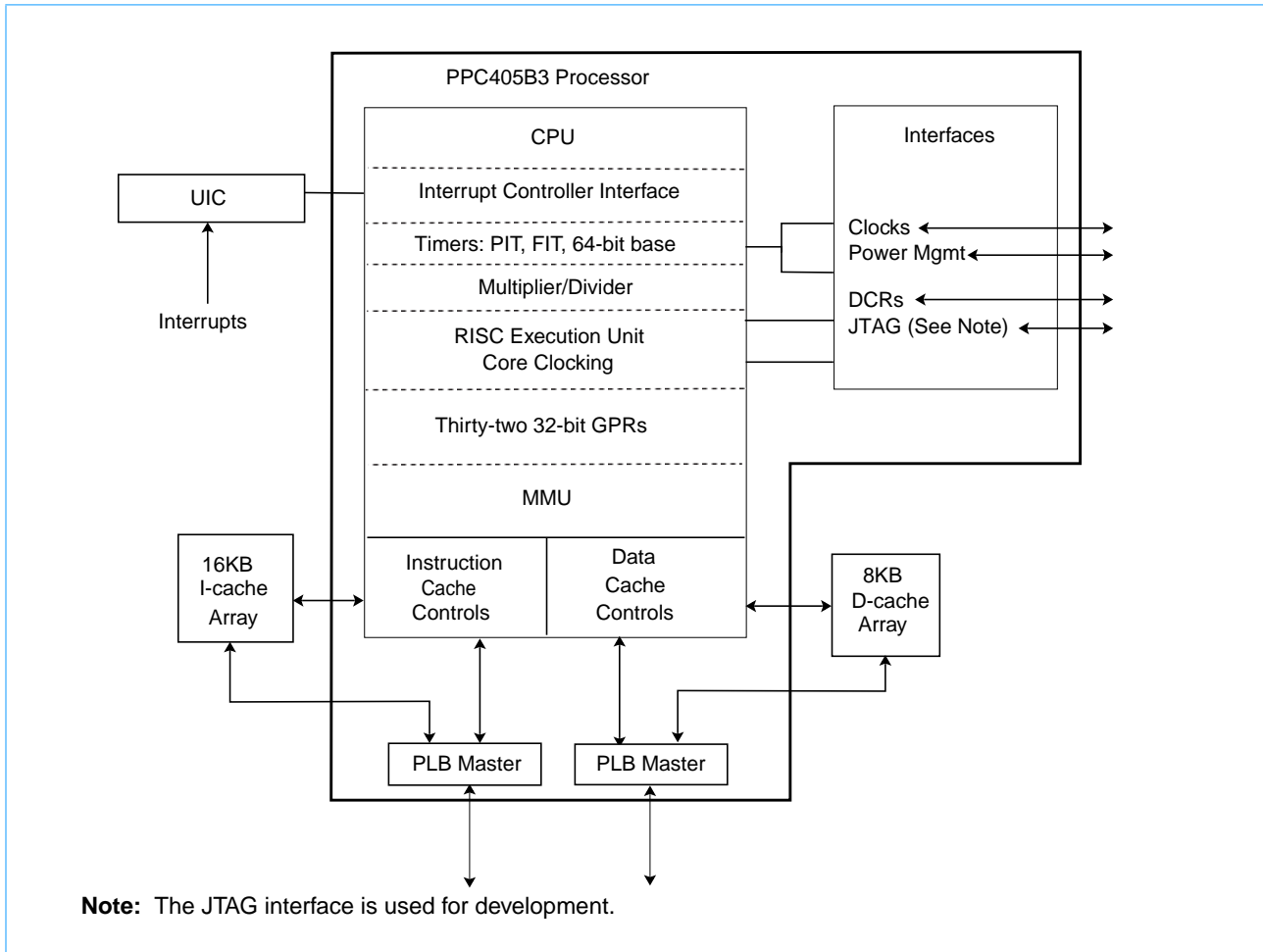
### Block Diagram



## PowerPC 405B3 Host Processor Subsystem

The PowerPC 405B3 (PPC405B3) subsystem handles all system initialization and control and also provides power and flexibility for product differentiation.

### PPC405B3 Subsystem



### PowerPC 405B3 CPU

The PPC405B3 provides high performance and low power consumption. The CPU executes at sustained speeds of greater than one cycle per instruction at 108 or 162 MHz. Interrupt latency is three cycles, the best time for critical interrupts.

On-chip instruction is compatible with PowerPC User Instruction Set Architecture, with branch prediction execution for most instructions. There are 32 x 32 bit general purpose registers. Instruction and data cache arrays improve system throughput. The CPU has a separate two-way set-associative 16KB instruction cache and an 8KB write-back/write-through data cache. Multiply and divide instructions are performed in hardware and are not emulated in software.

### Universal Interrupt Controller

The Universal Interrupt Controller (UIC) provides all necessary control, status, and communication functions between all sources of interrupts and the PPC405B3. The UIC combines STB03xxx interrupts and presents them to the PPC405B3's critical or non-critical inputs. All interrupts can be programmed to generate either critical or non-critical output. Interrupts can be level- or edge-sensitive and interrupt polarity is programmable.

An optional read-only vector is used to reduce critical interrupt servicing latency. This vector is generated by combining an offset (based on the bit position of the highest priority, enabled, and active critical interrupt) and a vector base address register. A configurable priority control bit determines whether the least significant or most significant bit in the status register has the highest priority.

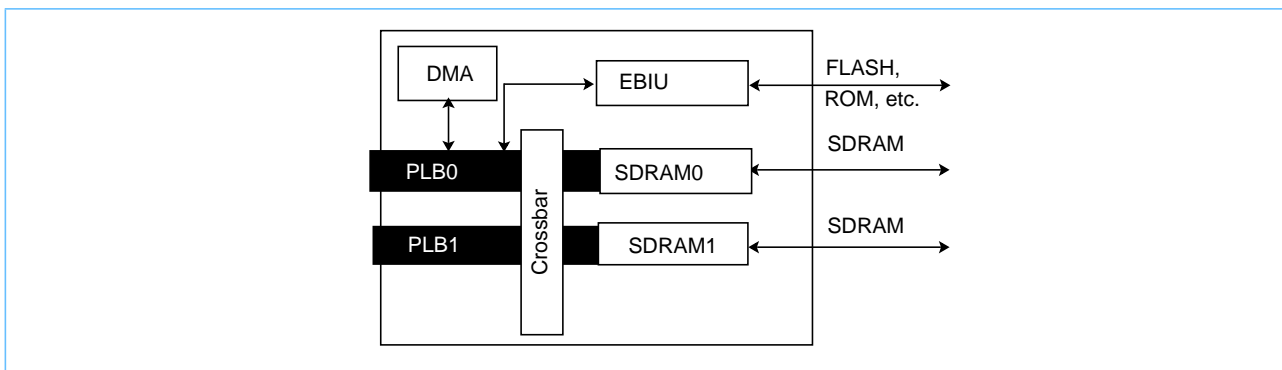
### Clock and Power Management

For power-saving purposes, a Clock and Power Management (CPM) input is used to shut down clocks and device functions. A reset is required to activate a unit.

### Memory Interface Subsystem

The memory interface subsystem provides the system memory controller interface for SRAM, FLASH Memory, ROM, and SDRAM. It also provides the Direct Memory Access (DMA) interfaces for these memories. A key advantage of the memory interface is its ability to gain concurrent access (one function to SDRAM0 and one function to SDRAM1) and mutual access (a given function can access either port).

### Memory Subsystem



### Direct Memory Access Controller

The four-channel DMA controller is a processor local bus master that allows faster data transfer between memory and peripherals than with program control. The controller supports memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. The DMA controller allows the PPC405B3 processor to execute instructions with no bus contention when the PPC405B3 is executing from cache. DMA is useful when

the overhead associated with the controller setup is minimal compared to the time it would take to move data using program control load and store instructions.

Each DMA channel has an independent set of registers for data transfer. The registers store data for control, source address, destination address, and transfer count. Each channel also supports chained DMA operations, therefore every channel also includes a chained count register in which case source address registers function as chained address registers. All DMA channels report their status to the DMA execution unit.

The DMA controller also supports:

- Internal DMA channels for 1284 parallel port, Smart Card interface, 16550 serial communications controller, infrared communications controller, etc.
- 16- and 32-bit peripherals (on-chip peripheral bus and external)
- 32-bit addressing
- Address increment or decrement
- Internal data buffering capability
- Memory-mapped peripherals

### Processor Local Bus

The Processor Local Bus (PLB) interfaces directly with the PPC405B3 and the other major subsystems (see "Block Diagram," on page 4). The STB03xxx uses three PLBs to provide high bandwidth between the function masters and the external memory interfaces for ROM, Flash, and SDRAM, etc. The STB03xxx PLB architecture includes a crossbar switch to present both memory interfaces as flat, shared memory spaces.

### External Bus Interface Unit

The External Bus Interface Unit (EBIU) expands the local bus to transfer data between the PLB and a wide range of memory and peripheral devices attached to the external bus (see the following list). The EBIU can control up to eight devices or banks or regions of FLASH memory (128 MB), and a low latency maximizes system performance.

The EBIU supports:

- A direct connect SRAM/ROM/PIA interface for
  - up to eight SRAM/ROM/PIA banks with programmable address select
  - programmable or device-paced wait states
  - burst mode (BME) and single-cycle transfers
- 16- and 32-bit byte addressable bus width
- Programmable target word first or sequential cache line fills
- IDE interface
  - supports ATA-3 Mode 4 register and PIO transfers
  - supports Mode 2 Multiword DMA transfers (see ANSI X3.298-1997, AT Attachment-3 Interface (ATA-3))
- DVB Common Interface Support
- External bus master with support for device master and master/slave
- Common bank-specific programmability
- Device-paced ready input

## SDRAM Controller

The SDRAM Controller transfers data between the PLB and up to two SDRAM memory banks attached to the external bus. The Controller implements address and data pipelining and supports 16Mb and 64Mb SDRAMs concurrently. It also provides the following:

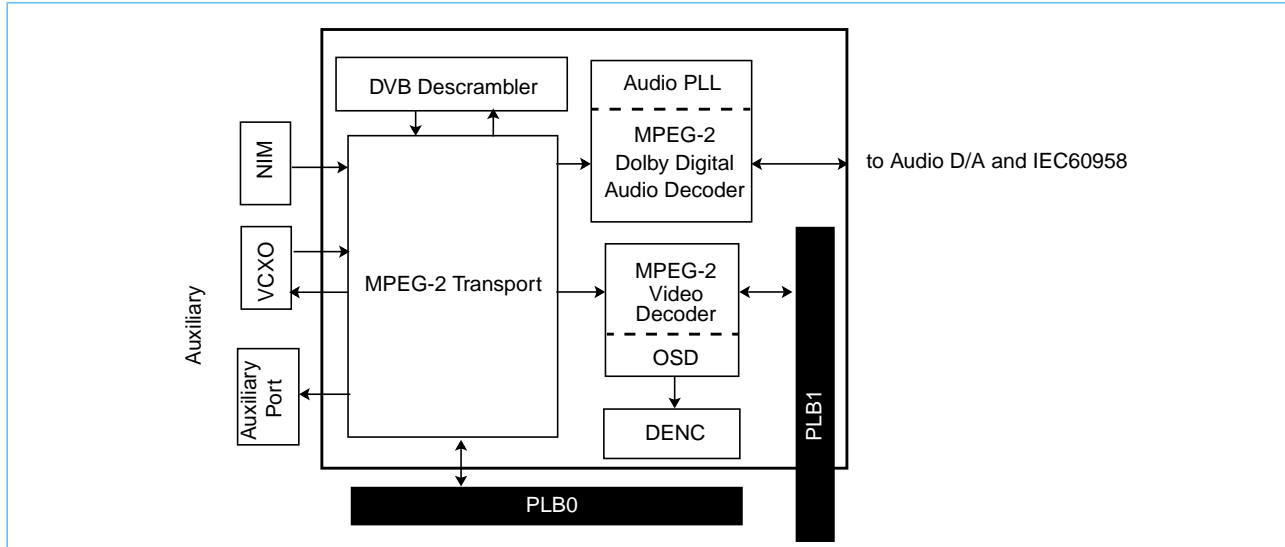
- Direct-connect SDRAM interface
- High bandwidth with a narrow 16-bit interface
- Page interleaving
- Programmable address select
- Programmable rates for automatic SDRAM refresh
- Software-initiated and self refresh modes for power savings

## Crossbar Switch

The PLB Crossbar Switch (CBS) creates a flat memory model and implements Unified Memory Architecture (UMA), which connects multiple PLB master buses to multiple PLB slave buses, thus allowing two sets of PLB buses to intercommunicate. Processor, transport, and the audio and video decoders can access memory through either memory controller.

## Digital Audio/Video Subsystem

The MPEG-2 Digital Audio/Video subsystem provides fully-synchronized playback of digital video and audio programs, with a minimum of interaction from the PPC405B3 processor.



## MPEG-2 Video Decoder with OSD

The MPEG-2 video decoder provides decompression, decoding, and synchronized playback of digital video streams with a minimum of host support. It produces interlaced video output and can support MPEG-2 compressed data streams up to an average rate of 15 Mbps. The video decoder is also backward compatible to support the ISO/IEC International Standard 11172-2 (11/93) (also called "MPEG-1 Standard"). It supports the ISO/IEC 13818-2 Main Profile at Main Level.



The decoder also supports MPEG-2 MP@ML compliance with 2MB memory. Only 2MB of memory are needed to decode full CCIR601 resolution NTSC and PAL encoded MPEG-2 bitstreams. It performs real-time decoding of all resolutions in 16-pixel multiples, up to and including 720x480x30 or 720x576x25. Horizontal and vertical filters deliver high-quality video. Chrominance filtering and up-sampling to provide CCIR601 4:2:2 video output. Pan and scan are supported in 1/16 pel accuracy for 16:9 source material. Video rates range from 1.5 Mbps to 15 Mbps (higher in bursts).

The MPEG-2 video decoder supports the European DVB standard and accepts Packetized Elementary or Elementary MPEG-2 streams. It uses Packetized Elementary Stream (PES) video decoding to extract the Presentation Time Stamp (PTS), and handles user data and other PES layer bit fields through memory access from the PPC405B3. Input can be from transport or directly from system memory. Outputs are provided for video-only and for video-with-OSD.

The decoder can insert data in the vertical blanking interval (VBI) with VBI Output Support. It supports decoding of still or fixed images and display of scaled video images. It also features:

- Letterbox format display
- Selectable anti-flicker filtering
- Output interface flexibility (programmable controls)
- Composite blanking and Field ID signals
- V-sync and H-sync signals
- CCIR656 master and slave modes
- Programmable signal polarity
- Sophisticated error concealment
- 3:2 pull-down support.
- Closed caption, teletext, or mixed (VPS)
- (1/4x, 1/2x, 2x) and three graphic planes
- Automated video channel change and time-base change features
- Blending of external graphics.

A multi-plane on-screen display (OSD) uses bitmap data in memory to be merged with or displayed in place of the motion video data. Three OSD planes (the cursor, graphics and image planes) are provided for increased display flexibility. The OSD includes:

- Programmable background color
- Multi-region link list graphic and image plane OSD with a color table for each region
- Programmable bitmap resolution on a region-by-region basis
- 64 x 64 pixel, 16-color cursor plane with blending controls
- Overlay and video blending of graphic plane
- Enhanced color mode for 24-bit color (YUV) in Direct Color and CLUT modes with 8-bit alpha blending
- Video shading in graphic plane OSD area
- OSD control output for external multiplexer (picture-in-picture support)
- Tiling capability in image and graphic planes
- Scrolling of image and graphic planes
- Horizontal scaling of image plane bitmaps
- Animation support
- 16 MB OSD addressing range to support more and larger bitmaps.

### MPEG-2 Transport and DVB Descrambler

The MPEG-2 transport demultiplexer provides ISO / IEC 13818-1 MPEG-2 transport system layer demultiplexing. Its integrated digital video broadcasting (DVB) descrambler complies with DVB system layer requirements and may be turned off for non-DVB applications. Peak input rates are 100-Mbps (parallel) or 60-Mbps

(serial), or 88-Mbps (parallel) or 60-Mbps (serial) with the optional descrambler. Packet Identifier (PID) filtering is based on 32 programmable entries with detection and notification of errors and lost packets. Hardware-based clock recovery on program clock references (PCRs) reduces processor load by:

- Calculating clock difference between PCR and System Time Clock (STC)
- Modulating output to drive an external VCXO
- Using an optional internal clock-recovery algorithm based on clock difference

Transport and descrambler features include:

- Internal DVB (1.0 or 1.1) descrambler, including filtering and storage of eight control word pairs
- Auxiliary output port for real-time data transfers:
  - 8-bit mode at 1X, 1/2X, 1/3X, 1/4X and 1/8X of the system clock speed
- Table section filtering:
  - 64 separate 4-byte filter blocks with bit-level masking with full match/not match capability
  - Multiple filters can be linked to extend filtering depth in 4-byte increments
  - Multiple filters per PID
  - Filters program-specific information (PSI), service information (SI), private tables
  - Handles multiple sections per packet and sections that span packets
  - Optional CRC checking of section data
- Selective routing of some or all packet data to system memory:
  - Based on 32 separate queues (one per PID)
  - Routing entire packets, payloads, adaptation fields, table sections (after filtering) and private data
- Direct transfer of audio / video (PES) data to decoders
- Simplified channel changes, time-base changes and error flagging / concealment through direct communication with decoders
- Interface for a Transport Assist Processor to provide additional processing:
  - Extended filtering / parsing of tables, private data, adaptation fields, and PES headers
  - Ability to selectively route alternative data fields to system memory

### MPEG-2/Dolby Digital Audio Decoder

The Audio Decoder receives and decodes either ES (Elementary Stream) or PES (Packetized Elementary Stream) audio data. The audio compute engine is a generic DSP processor that decodes MPEG, Dolby Digital<sup>1</sup>, or 16-, 18- or 20-bit unformatted Pulse Code Modulation (PCM) audio data via individual software programs.

The host processor downloads each program load to the Audio Decoder following initialization. The Audio Decoder generates up to two channels of decoded PCM for MPEG and PCM audio playback output. It provides 2-channel MPEG audio output and 6-channel Dolby Digital down-mixed to either two channels or six channels of Dolby Digital output. Unpacketized PCM (UPCM) plays back at sampling frequencies of 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz, along with quantization sample width selections of 16-, 18- or 20-bit input and 16 or 20-bit output.

The Audio Decoder:

- Decodes Dolby Digital, described in the ATSC Specification "Digital Audio Compression" (A/52).
- Decodes MPEG-1 and MPEG-2 audio (Layers I and II) and 2-channel output, including single channel, stereo, joint stereo, and dual channel modes.

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1. This feature available only on STB03x1x, Dolby Digital license required

- Performs MPEG-1 and MPEG-2 PES audio parsing, and also accepts audio elementary streams. Parses and stores ancillary data into external memory for later use by the host processor.
- Supports 16-kHz, 22.05-kHz, 24-kHz, 32-kHz, 44.1-kHz, and 48-kHz audio sampling frequencies.
- Supports audio/video synchronization through PTS/STC comparison with each audio frame.
- Supports Karaoke Mode for Dolby Digital and PCM playback.
- Supports an encoded audio bit rate up to 640 Kbps. This bit rate only pertains to encoded bitstream data.
- Includes Audio Clip Mode for PES, ES, and PCM formats with byte address granularity and 2MB maximum per clip buffer.
- Allows PCM Mixing with primary audio stream input including sample rate conversion. PCM audio data supplied via secondary clip mode feature.
- Supports expandable rate buffer size selectable from 4K to 64K (in 4K increments).
- Uses a re-locatable rate buffer region, with a programmable base register (128-byte location granularity).
- Has a re-locatable PTS Value and Ancillary data region, using a programmable base register with 128-byte location granularity.
- Uses a locatable Audio Temporary Data and Decoded Audio Data Bank region (programmable base register with 128-byte location granularity with additional offset register).
- Includes 256x and 512x DAC sampling clock frequency configurations.
- Has a programmable stream ID register with corresponding 8-bit enable field.
- Provides three PCM output formats in 16- or 20-bit precision:
  - I<sup>2</sup>S
  - Left-justified
  - Right-justified
- Performs audio bitstream error concealment, either by frame repeats or muting, due to loss of synchronization or detection of CRC errors.
- Performs MPEG error checking using frame size calculation for each frame.
- Provides de-emphasis pins that interface to external de-emphasis circuitry.
- Provides Dolby Surround Mode (dsurmod) pins that interface to external surround mode circuitry.
- Provides a programmable interface that supports the following:
  - Play, stop, and mute
  - Rate buffer purge to support channel and mode changes
  - Provides a compressed buffer full indicator
  - Synchronization enable/disable for PTS-STC comparison
- Includes SPDIF meeting IEC61937 and IEC60958 specs.
- Supports enhanced IEC61937 S/P DIF Channel Status bit by including 16 SPDIF Channel Status bits, with host control over most of the bits.
- Inserts host-controlled validity bit into SPDIF sub-frame via DCR register.

- Performs audio attenuation in 64 steps, with smooth transitions between steps.
- Provides tone generation with up to 128 generated tones at 31 different durations with seven levels of attenuation via processor command.
- Supports automated channel change.
- Supports automated time base change.

### **NTSC/PAL Digital Encoder Unit with Macrovision Copy Protection<sup>1</sup>**

The multi-standard Digital Encoder converts digital audio/video data into analog National Television System Committee (NTSC) or Phase Alternate Line (PAL) data output formats (see Macrovision Licensing on page 3). It provides up to six concurrent analog video outputs, including S-Video, composite video, YPbPr, and RGB. The encoder is compatible with SCART connectors, with support for Macrovision Copy Protection Revision 7. Analog outputs are driven by 10-bit D/A converters, operating at 27 MHz. The outputs drive standard video levels into 75- $\Omega$  loads. It supports closed caption, teletext insertion, and Line 23 WSS (Wide-screen Signaling) per ITU-R BT.1119. There is a switchable pedestal with gain compensation. Playback of synchronized video data can be locked to the incoming composite video stream.

## **Additional Interfaces**

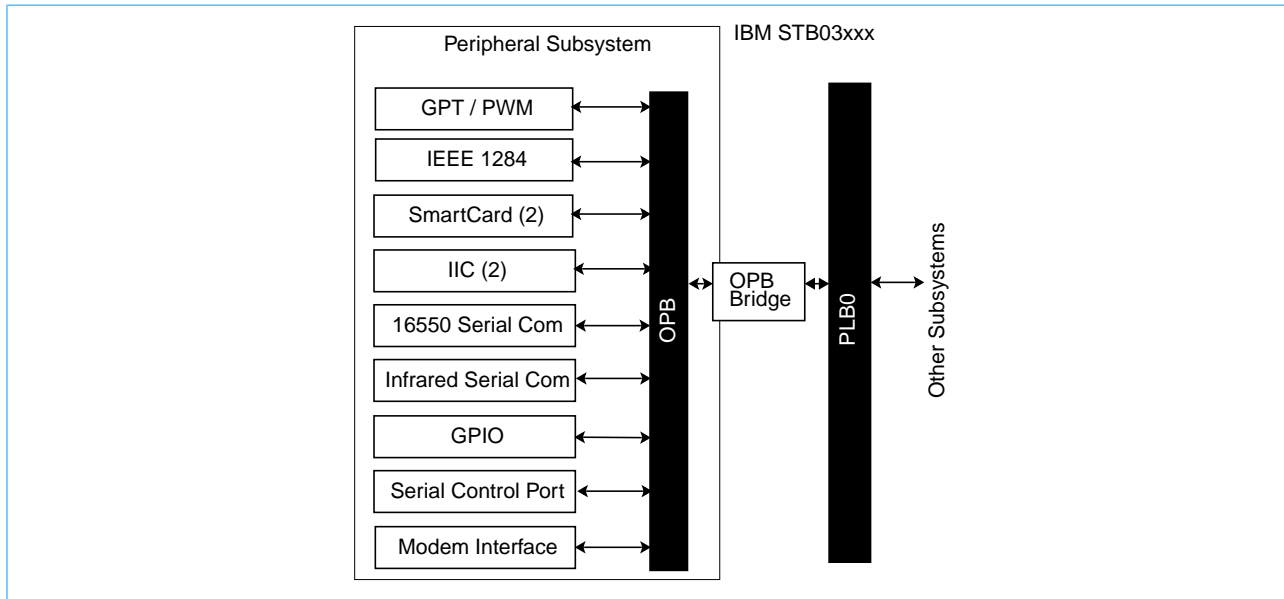
### **External Graphics and Video (EGV) Port**

External Graphics and Video (EGV) ports provide flexibility for interfacing external graphics and video components. When the EGV is used as an output, its signals may be routed to an external graphics device or DENC. When used as an input, either the internal OSD graphics can be replaced with data from an external graphics device, or external digital video data (from an analog signal converted to digital via DSMD, for example) could replace the internally decoded MPEG video. In the latter case, the external digital video can be merged/blended with the internal OSD graphics.

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1. This feature is available only on STB03xx1, Macrovision license required.

## Peripheral Subsystem



### General Purpose Timer

The General Purpose Timer (GPT) is an on-chip peripheral bus (OPB) function that provides a separate time base counter and additional system timers beyond those defined in the PPC405B3.

Three Inter-Character (IC) time-out timers are also implemented in this functional unit in the GPT. These timers receive the count signal inputs from other units they are timing. Each timer is a 10-bit down counter loaded with a programmable value (TOUT) upon the active edge of the count signal input. Once loaded, the IC timer counts down TOUT number of TCLK cycles until it reaches zero (that is, when the IC timer has expired). When a timer expires, it sets its corresponding bit in the IC interrupt status register.

There is a separate time base inside the GPT, distinct from the time base within the PPC405B3. Two event timers capture unique input events and there are two compare timers with unique outputs. Separately configurable and programmable synchronization controls edge detection and output levels. There are two reset inputs, one for the entire GPT unit, and one for the time base.

### Pulse Width Modulation

The pulse width modulation (PWM) function produces two square wave outputs with a variable duty cycle under program control. The duty cycle varies from 100 percent to zero percent in steps of 1/256. There is a control register with two bits for each PWM. This register controls the active status of the PWM, and determines what its inactive output level should be. When the PWM control register is set to disable a PWM, the 8-bit period counter will be inactive to minimize power.

The pulse width modulation portion of the GPT contains two identical blocks, each containing an 8-bit programmable and reloadable down counter and control logic. A time-base generator that is a free-running counter (TCLK based) generates the frequency of the pulse-width modulated output.

## IEEE 1284 Parallel Port

The IEEE 1284 Parallel Port is implemented as either the host side or peripheral side of the parallel port data bus. The parallel port bidirectional interface supports IEEE Std. 1284 extended capability port (ECP)<sup>1</sup>, byte<sup>2</sup>, nibble<sup>3</sup>, and compatibility<sup>4</sup> modes of operation. The parallel port also monitors IEEE Std. 1284 negotiation mode events, which allows the host to determine the capabilities of an attached peripheral and to set the interface into one of the four operational modes. The parallel port supports byte-wide FIFO but does not support Enhanced Parallel Port (EPP) mode. Two Direct Memory Access (DMA) channels for transmit and receive allow independent data transfers from other peripherals. The IEEE 1284 Parallel Port is compatible with existing parallel port hosts, and an Inter-Character Time-out Facility provides support with the GPT/PWM.

## Inter-Integrated Circuit (IIC) Units

Two unique IIC units are used to provide two independent IIC interfaces and provide a simple to use, highly programmable interface between the OPB and the industry standard IIC serial bus. They provide full management of all IIC bus protocols, compliant with Phillips Semiconductors I<sup>2</sup>C Specification, dated 1995, and support a fixed V<sub>DD</sub> IIC interface. These IICs can be programmed to operate as master, as slave, or as both master and slave on the IIC interface. In addition to sophisticated IIC bus protocol management, the IICs provide full data buffering between the OPB and the IIC bus.

The IIC units offer 5 V tolerant I/O for both 100- and 400-kHz operation with 8-bit data transfers and 7-bit and 10-bit address decode/generation. There is one programmable interrupt request signal, two independent 4 x 1-byte data buffers, and 12 memory-mapped, fully programmable configuration registers.

## Smart Card Interface Units

The Smart Card Interface Units handle communications between an Integrated Circuit Card and the host CPU. These 5 V tolerant I/O devices have a software-based control structure and are designed for use with asynchronous transmissions. They feature hardware activation/deactivation and reset with software overrides and byte-wide FIFO support. They are compatible with ISO/IEC 7816-3 and support T0 and T1 protocols. The Interface Units support 2-channel DMA with 8-bit memory-mapped registers and hardware error checking. An Inter-Character Time-out Facility provides timing support from the GPT/PWM.

## 16550 Serial Communication Controller

The 16550 Serial Communication Controller is a universal asynchronous receiver/transmitter (UART) with FIFOs, and is compatible with the 16550 part numbers manufactured by National Semiconductor (NS) Corporation. It is also compatible with National Semiconductor 16450 (non-FIFO version). Serial interface characteristics are fully programmable with complete modem control functions and status reporting capability. The controller supports:

- 5-, 6-, 7-, or 8-bit characters
- Even, odd, or no parity bit generation and detection
- 1-, 1.5-, or 2-stop-bit generation
- Variable baud rate and a programmable baud rate generator

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1. ECP refers to the extended capability port. An asynchronous, byte-wide, bidirectional channel.  
2. Byte refers to an asynchronous, reverse (peripheral-to-host) channel, under the control of the host.  
3. Nibble refers to an asynchronous, reverse (peripheral-to-host) channel, under the control of the host.  
4. Compatibility refers to an asynchronous, byte-wide forward (host-to-peripheral) channel.

There is also support for two DMA channels with a 16-byte FIFO for transmit/receive path. Internal loopback is provided for diagnostics and an Inter-Character Timeout Facility provides timing support from the GPT/PWM.

### **Infrared Serial Communications Controller**

In addition to standard UART functions, the Serial/Infrared Communications Controller can use an alternate mode (IrDA mode) to transfer and receive infrared characters. IrDA transmissions are specified by the Infrared Data Association (IrDA) Specification 1.1. IrDA mode supports RS-232 and infrared communications up to 1.152 Mbps with automatic insertion/removal of standard ASYNC communication bits. The controller includes:

- A programmable baud rate generator
- Individual enable for receiver and transmitter interrupts
- Internal loopback and auto-echo modes
- Full-duplex operation
- Programmable serial interface
- Status reporting capability
- Individual receiver and transmitter DMA support
- Auto-handshaking mode for receiver and transmitter
- Transmitter pattern generation capability
- Serial clock frequency up to 1/2 system clock frequency
- Inter-Character Timeout Facility support from the GPT/PWM

### **Modem Interface**

The Modem Interface provides a glueless communication from the device to and from many standard and economical telephony CODECs (Note: CODECs are the Audio ADC/DAC devices). The PPC405B3 CPU and applicable software can be used to implement an inexpensive interface for a modem. The external interface supports industry standard 4-wire parameters, consisting of transmit data, receive data, clock, and frame sync. Two channels of DMA allow off-loading data from the CPU. The Modem Interface supports digital audio MIC input, status reporting, and interrupt generation.

### **Serial Control Port**

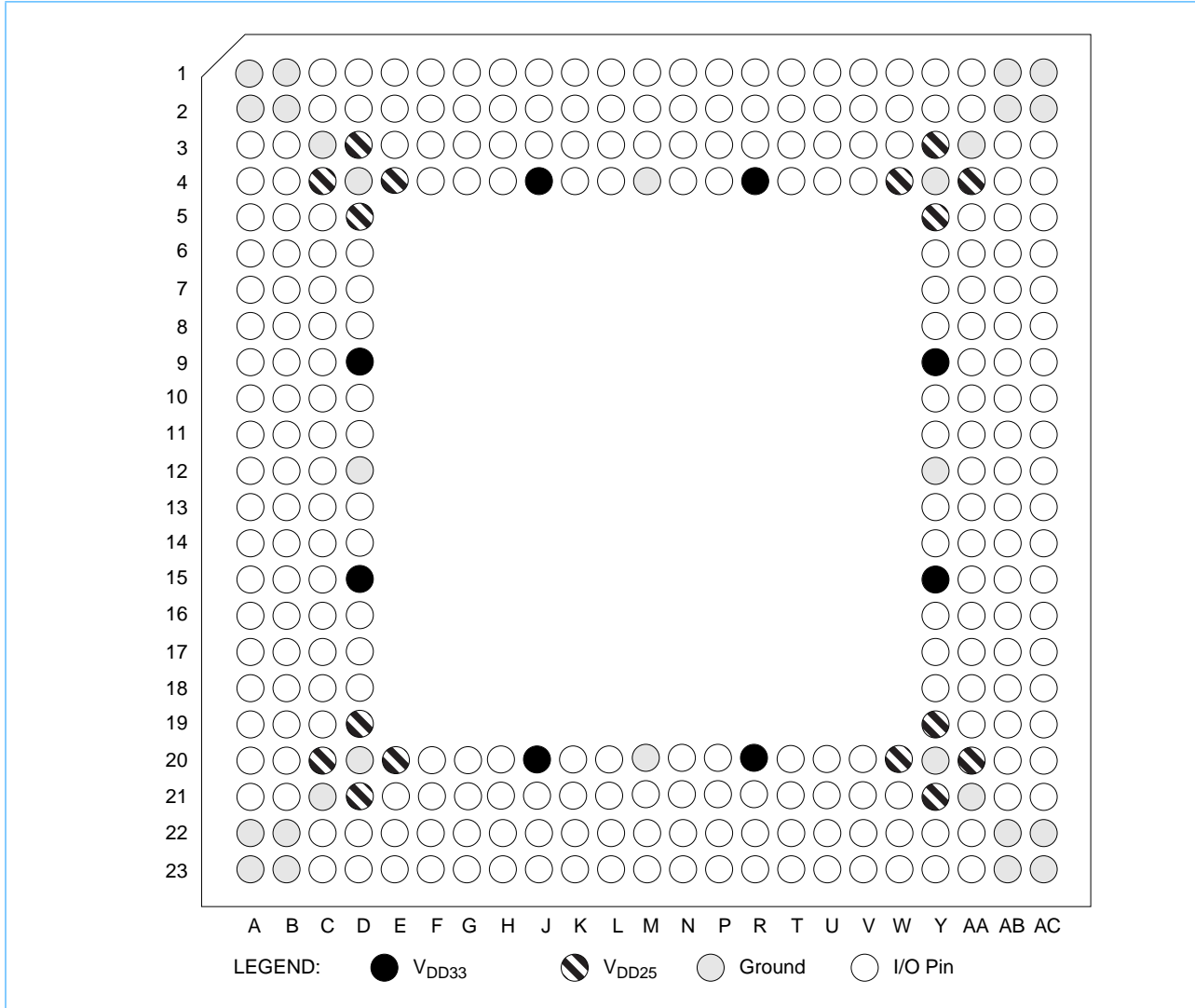
The Serial Control Port (SCP) is a full-duplex, synchronous, character-oriented (byte) port that allows the exchange of data with other SCP bus-compatible serial devices. The SCP is a slave device to the OPB bus, and supports a three-wire interface to the serial port (receive, transmit, and clock). It provides a glueless serial interface to many microcontrollers, with clock inversion and reverse data. The port includes a programmable clock rate divider (Sysclk/4 to Sysclk/1024), and bit rate is supported up to 1/4 the frequency of the system clock.

### **General Purpose I/O Controller**

The General Purpose I/O (GPIO) controller enables the multiplexing of module I/Os, with functions that include programmable open-drain output conversion, registered input and output functions, and simplified GPIO definition.

## Pin and I/O Information

### Pinout Diagram







**Signal Pins Sorted by Signal Name**

Signal	Grid (Pin) Position	Group	Signal	Grid (Pin) Position	Group
AUD_VDDA0	N22	PLL Analog PWR + GND	BI_DATA2	AB15	Bus Interface
AUD_VDDA1	K20	PLL Analog PWR + GND	BI_DATA3	AB16	Bus Interface
BI_ADDRESS8 (MSB)	AA2	Bus Interface	BI_DATA4	AB17	Bus Interface
BI_ADDRESS9	AC3	Bus Interface	BI_DATA5	AA16	Bus Interface
BI_ADDRESS10	AC4	Bus Interface	BI_DATA6	AA15	Bus Interface
BI_ADDRESS11	AB5	Bus Interface	BI_DATA7	AC14	Bus Interface
BI_ADDRESS12	AC5	Bus Interface	BI_DATA8	Y14	Bus Interface
BI_ADDRESS13	AA5	Bus Interface	BI_DATA9	AC15	Bus Interface
BI_ADDRESS14	AB9	Bus Interface	BI_DATA10	AC16	Bus Interface
BI_ADDRESS15	AA9	Bus Interface	BI_DATA11	AC17	Bus Interface
BI_ADDRESS16	AC8	Bus Interface	BI_DATA12	Y17	Bus Interface
BI_ADDRESS17	AB8	Bus Interface	BI_DATA13	Y16	Bus Interface
BI_ADDRESS18	AC7	Bus Interface	BI_DATA14	AB14	Bus Interface
BI_ADDRESS19	AB7	Bus Interface	BI_DATA15 (LSB)	AB13	Bus Interface
BI_ADDRESS20	AC6	Bus Interface	BI_OE	AC13	Bus Interface
BI_ADDRESS21	AB6	Bus Interface	BI_READY	AA10	Bus Interface
BI_ADDRESS22	AB4	Bus Interface	BI_RW	AB10	Bus Interface
BI_ADDRESS23	Y6	Bus Interface	BI_WBE0	Y11	Bus Interface
BI_ADDRESS24	AA6	Bus Interface	CI_CLOCK	U20	Channel Interface
BI_ADDRESS25	Y7	Bus Interface	CI_DATA0 (MSB)	Y23	Channel Interface
BI_ADDRESS26	AA7	Bus Interface	CI_DATA1	Y22	Channel Interface
BI_ADDRESS27	Y8	Bus Interface	CI_DATA2	W23	Channel Interface
BI_ADDRESS28	AA8	Bus Interface	CI_DATA3	W21	Channel Interface
BI_ADDRESS29	Y10	Bus Interface	CI_DATA4	W22	Channel Interface
BI_ADDRESS30	AC9	Bus Interface	CI_DATA5	V20	Channel Interface
BI_ADDRESS31 (LSB)/BI_WBE1	AC10	Bus Interface	CI_DATA6	V23	Channel Interface
BI_CS0	Y13	Bus Interface	CI_DATA7 (LSB)	V21	Channel Interface
BI_CS1	AB12	Bus Interface	CI_DATA_ENABLE	V22	Channel Interface
BI_CS2	AA12	Bus Interface	CLK_VDDA	C9	PLL Analog PWR + GND
BI_CS3	AC12	Bus Interface	DAC1_AGND0	L1	DAC Analog PWR + GND
BI_DATA0 (MSB)	AA13	Bus Interface	DAC1_AGND1	J1	DAC Analog PWR + GND
BI_DATA1	AA14	Bus Interface	DAC1_AGND2	G3	DAC Analog PWR + GND

**Signal Pins Sorted by Signal Name (Continued)**

Signal	Grid (Pin) Position	Group	Signal	Grid (Pin) Position	Group
DAC1_AVDD0	L3	DAC Analog PWR + GND	DA_SERIAL_DATA0	V4	Audio
DAC1_AVDD1	K2	DAC Analog PWR + GND	DV1_DATA0 (MSB)	E3	Video and Graphics
DAC1_AVDD2	J3	DAC Analog PWR + GND	DV1_DATA1	E2	Video and Graphics
DAC1_AVDD3	G2	DAC Analog PWR + GND	DV1_DATA2	E1	Video and Graphics
DAC1_BOUT	H4	Video and Graphics	DV1_DATA3	D2	Video and Graphics
DAC1_BREF_OUT	F1	Video and Graphics	DV1_DATA4	D1	Video and Graphics
DAC1_GOUT	K3	Video and Graphics	DV1_DATA5	C2	Video and Graphics
DAC1_GREF_OUT	L4	Video and Graphics	DV1_DATA6	C1	Video and Graphics
DAC1_ROUT	L2	Video and Graphics	DV1_DATA7 (LSB)	B3	Video and Graphics
DAC1_RREF_OUT	H3	Video and Graphics	DV1_HSYNC	F2	Video and Graphics
DAC1_VREF_IN	H2	Video and Graphics	DV1_PIXEL_CLOCK	F4	Video and Graphics
DAC2_AGND0	M2	DAC Analog PWR + GND	DV1_VSYNC	F3	Video and Graphics
DAC2_AGND1	P3	DAC Analog PWR + GND	EDMAC3_ACK/IDE_ACK	Y2	Direct Memory Access
DAC2_AGND2	U1	DAC Analog PWR + GND	EDMAC3_REQ/IDE_REQ	AA1	Direct Memory Access
DAC2_AVDD0	M1	DAC Analog PWR + GND	GND	B1	Ground
DAC2_AVDD1	N4	DAC Analog PWR + GND	GND	B2	Ground
DAC2_AVDD2	P4	DAC Analog PWR + GND	GND	B22	Ground
DAC2_AVDD3	T2	DAC Analog PWR + GND	GND	B23	Ground
DAC2_BOUT	T3	Video and Graphics	GND	C21	Ground
DAC2_BREF_OUT	U2	Video and Graphics	GND	D4	Ground
DAC2_GOUT	N3	Video and Graphics	GND	D20	Ground
DAC2_GREF_OUT	N1	Video and Graphics	GND	Y4	Ground
DAC2_ROUT	M3	Video and Graphics	GND	Y20	Ground
DAC2_RREF_OUT	T1	Video and Graphics	GND	AA3	Ground
DAC2_VREF_IN	R3	Video and Graphics	GND	AA21	Ground
DA_BIT_CLOCK	V1	Audio	GND	AB1	Ground
DA_IEC_958	W1	Audio	GND	AB2	Ground
DA_LR_CHANNEL_CLOCK	V3	Audio	GND	AB22	Ground
DA_OVERSAMPLING_CLOCK	V2	Audio	GND	AB23	Ground



## Signal Pins Sorted by Signal Name (Continued)

Signal	Grid (Pin) Position	Group	Signal	Grid (Pin) Position	Group
GND	AC1	Ground	GPIO_22	R2	General Purpose I/O
GND	AC2	Ground	GPIO_23	R1	General Purpose I/O
GND	AC22	Ground	GPIO_24	P2	General Purpose I/O
GND	AC23	Ground	GPIO_25	P1	General Purpose I/O
GND	A1	Ground	GPIO_26	N2	General Purpose I/O
GND	A2	Ground	GPIO_27	K4	General Purpose I/O
GND	A22	Ground	GPIO_28	K1	General Purpose I/O
GND	A23	Ground	GPIO_29	C6	General Purpose I/O
GND	C3	Ground	GPIO_30	G23	General Purpose I/O
GND	D12	Ground	GPIO_31	G21	General Purpose I/O
GND	M20	Ground	G_SYSTEM_CLOCK	C8	Global
GND	Y12	Ground	G_SYSTEM_RST	C7	Global
GND	M4	Ground	I2C0_SCL	U4	Inter-Integrated Circuit (IIC)
GPIO_0	N23	General Purpose I/O	I2C0_SDA	U3	Inter-Integrated Circuit (IIC)
GPIO_1	N21	General Purpose I/O	INT0	AA17	Interrupt
GPIO_2	G4	General Purpose I/O	INT1	AB3	Interrupt
GPIO_3	AC11	General Purpose I/O	INT2	J23	Interrupt
GPIO_4	A15	General Purpose I/O	INT3	K22	Interrupt
GPIO_5	H20	General Purpose I/O	MUX0_0	K23	Multiplexed I/O
GPIO_6	AA18	General Purpose I/O	MUX0_1	K21	Multiplexed I/O
GPIO_7	AC18	General Purpose I/O	MUX0_2	J21	Multiplexed I/O
GPIO_8	AB20	General Purpose I/O	MUX0_3	L23	Multiplexed I/O
GPIO_9	B7	General Purpose I/O	MUX0_4	L22	Multiplexed I/O
GPIO_10	A7	General Purpose I/O	MUX0_5	L21	Multiplexed I/O
GPIO_11	D7	General Purpose I/O	MUX0_6	L20	Multiplexed I/O
GPIO_12	B8	General Purpose I/O	MUX0_7	M21	Multiplexed I/O
GPIO_13	A8	General Purpose I/O	MUX0_8	N20	Multiplexed I/O
GPIO_14	D8	General Purpose I/O	MUX0_9	P21	Multiplexed I/O
GPIO_15	B9	General Purpose I/O	MUX0_10	P22	Multiplexed I/O
GPIO_16	AB11	General Purpose I/O	MUX0_11	P23	Multiplexed I/O
GPIO_17	AA11	General Purpose I/O	MUX0_12	M22	Multiplexed I/O
GPIO_18	G1	General Purpose I/O	MUX0_13	M23	Multiplexed I/O
GPIO_19	H1	General Purpose I/O	MUX0_14	J22	Multiplexed I/O
GPIO_20	J2	General Purpose I/O	MUX0_15	H21	Multiplexed I/O
GPIO_21	T4	General Purpose I/O	MUX0_16	H23	Multiplexed I/O

**Signal Pins Sorted by Signal Name (Continued)**

Signal	Grid (Pin) Position	Group	Signal	Grid (Pin) Position	Group
MUX0_17	G20	Multiplexed I/O	Reserved - Tie to 3.3 V	B6	Global
MUX0_18	B20	Multiplexed I/O	SC0_CLK	AB21	Smart Card Interface 0
MUX0_19	A21	Multiplexed I/O	SC0_DETECT	Y18	Smart Card Interface 0
MUX0_20	C23	Multiplexed I/O	SC0_IO	AC21	Smart Card Interface 0
MUX0_21	D23	Multiplexed I/O	SC0_RESET	AA23	Smart Card Interface 0
MUX0_22	E21	Multiplexed I/O	SC0_VCC_COMMAND	AA22	Smart Card Interface 0
MUX0_23	F21	Multiplexed I/O	SC1_CLK	AA19	Smart Card Interface 1
MUX0_24	F23	Multiplexed I/O	SC1_DETECT	AB18	Smart Card Interface 1
MUX0_25	G22	Multiplexed I/O	SC1_IO	AC19	Smart Card Interface 1
MUX0_26	F20	Multiplexed I/O	SC1_RESET	AB19	Smart Card Interface 1
MUX0_27	F22	Multiplexed I/O	SC1_VCC_COMMAND	AC20	Smart Card Interface 1
MUX0_28	E23	Multiplexed I/O	SD1_ADDRESS0 (MSB)	C16	SDRAM1 Controller
MUX0_29	E22	Multiplexed I/O	SD1_ADDRESS1	A17	SDRAM1 Controller
MUX0_30	D22	Multiplexed I/O	SD1_ADDRESS2	B16	SDRAM1 Controller
MUX0_31	C22	Multiplexed I/O	SD1_ADDRESS3	B17	SDRAM1 Controller
MUX0_32	B21	Multiplexed I/O	SD1_ADDRESS4	D16	SDRAM1 Controller
MUX0_33	A20	Multiplexed I/O	SD1_ADDRESS5	C17	SDRAM1 Controller
MUX0_34	H22	Multiplexed I/O	SD1_ADDRESS6	D17	SDRAM1 Controller
MUX1_0	Y1	Multiplexed I/O	SD1_ADDRESS7	C18	SDRAM1 Controller
MUX1_1	W2	Multiplexed I/O	SD1_ADDRESS8	D18	SDRAM1 Controller
MUX1_2	W3	Multiplexed I/O	SD1_ADDRESS9	C19	SDRAM1 Controller
MUX2_0	A3	Multiplexed I/O	SD1_ADDRESS10	B19	SDRAM1 Controller
MUX2_1	B4	Multiplexed I/O	SD1_ADDRESS11	A19	SDRAM1 Controller
MUX2_2	A4	Multiplexed I/O	SD1_ADDRESS12	B18	SDRAM1 Controller
MUX2_3	B5	Multiplexed I/O	SD1_ADDRESS13 (LSB)	A18	SDRAM1 Controller
MUX3_0	U23	Multiplexed I/O	SD1_CAS	B15	SDRAM1 Controller
MUX3_1	U21	Multiplexed I/O	SD1_CLK	D14	SDRAM1 Controller
MUX3_2	U22	Multiplexed I/O	SD1_CS0	A16	SDRAM1 Controller
MUX3_3	T20	Multiplexed I/O	SD1_DATA0 (MSB)	D10	SDRAM1 Controller
MUX3_4	T23	Multiplexed I/O	SD1_DATA1	B10	SDRAM1 Controller
MUX3_5	T21	Multiplexed I/O	SD1_DATA2	D11	SDRAM1 Controller
MUX3_6	T22	Multiplexed I/O	SD1_DATA3	B11	SDRAM1 Controller
MUX3_7	R23	Multiplexed I/O	SD1_DATA4	C12	SDRAM1 Controller
MUX3_8	R21	Multiplexed I/O	SD1_DATA5	A12	SDRAM1 Controller
MUX3_9	R22	Multiplexed I/O	SD1_DATA6	C13	SDRAM1 Controller
MUX3_10	P20	Multiplexed I/O	SD1_DATA7	D13	SDRAM1 Controller

**Signal Pins Sorted by Signal Name (Continued)**

Signal	Grid (Pin) Position	Group	Signal	Grid (Pin) Position	Group
SD1_DATA8	A13	SDRAM1 Controller	VDD25	D3	2.5 V Power
SD1_DATA9	B13	SDRAM1 Controller	VDD25	D5	2.5 V Power
SD1_DATA10	B12	SDRAM1 Controller	VDD25	D19	2.5 V Power
SD1_DATA11	A11	SDRAM1 Controller	VDD25	D21	2.5 V Power
SD1_DATA12	C11	SDRAM1 Controller	VDD25	E4	2.5 V Power
SD1_DATA13	A10	SDRAM1 Controller	VDD25	E20	2.5 V Power
SD1_DATA14	C10	SDRAM1 Controller	VDD25	W4	2.5 V Power
SD1_DATA15 (LSB)	A9	SDRAM1 Controller	VDD25	W20	2.5 V Power
SD1_DQMH	C14	SDRAM1 Controller	VDD25	Y3	2.5 V Power
SD1_DQML	B14	SDRAM1 Controller	VDD25	Y5	2.5 V Power
SD1_RAS	C15	SDRAM1 Controller	VDD25	Y19	2.5 V Power
SD1_WE	A14	SDRAM1 Controller	VDD25	Y21	2.5 V Power
SERIAL1/INFRARED_CTS	A6	Serial1 / Infrared	VDD33	D9	3.3 V Power
SERIAL1/INFRARED_RTS	D6	Serial1 / Infrared	VDD33	D15	3.3 V Power
SERIAL1/INFRARED_RXD	A5	Serial1 / Infrared	VDD33	J4	3.3 V Power
SERIAL1/INFRARED_TXD	C5	Serial1 / Infrared	VDD33	J20	3.3 V Power
VDD25	AA4	2.5 V Power	VDD33	R4	3.3 V Power
VDD25	AA20	2.5 V Power	VDD33	R20	3.3 V Power
VDD25	C4	2.5 V Power	VDD33	Y9	3.3 V Power
VDD25	C20	2.5 V Power	VDD33	Y15	3.3 V Power

### Signal Pins Sorted by Pin Number

Grid (Pin) Position	Signal	Group	Grid (Pin) Position	Signal	Group
A1	GND	Ground	AA13	BI_DATA0 (MSB)	Bus Interface
A2	GND	Ground	AA14	BI_DATA1	Bus Interface
A3	MUX2_0	Multiplexed I/O	AA15	BI_DATA6	Bus Interface
A4	MUX2_2	Multiplexed I/O	AA16	BI_DATA5	Bus Interface
A5	SERIAL1/INFRARED_RXD	Serial1 / Infrared	AA17	INT0	Interrupt
A6	SERIAL1/INFRARED_CTS	Serial1 / Infrared	AA18	GPIO_6	General Purpose I/O
A7	GPIO_10	General Purpose I/O	AA19	SC1_CLK	Smart Card Interface 1
A8	GPIO_13	General Purpose I/O	AA20	VDD25	2.5 V Power
A9	SD1_DATA15 (LSB)	SDRAM1 Controller	AA21	GND	Ground
A10	SD1_DATA13	SDRAM1 Controller	AA22	SC0_VCC_COMMAND	Smart Card Interface 0
A11	SD1_DATA11	SDRAM1 Controller	AA23	SC0_RESET	Smart Card Interface 0
A12	SD1_DATA5	SDRAM1 Controller	AB1	GND	Ground
A13	SD1_DATA8	SDRAM1 Controller	AB2	GND	Ground
A14	SD1_WE	SDRAM1 Controller	AB3	INT1	Interrupt
A15	GPIO_4	General Purpose I/O	AB4	BI_ADDRESS22	Bus Interface
A16	SD1_CS0	SDRAM1 Controller	AB5	BI_ADDRESS11	Bus Interface
A17	SD1_ADDRESS1	SDRAM1 Controller	AB6	BI_ADDRESS21	Bus Interface
A18	SD1_ADDRESS13 (LSB)	SDRAM1 Controller	AB7	BI_ADDRESS19	Bus Interface
A19	SD1_ADDRESS11	SDRAM1 Controller	AB8	BI_ADDRESS17	Bus Interface
A20	MUX0_33	Multiplexed I/O	AB9	BI_ADDRESS14	Bus Interface
A21	MUX0_19	Multiplexed I/O	AB10	BI_RW	Bus Interface
A22	GND	Ground	AB11	GPIO_16	General Purpose I/O
A23	GND	Ground	AB12	BI_CS1	Bus Interface
AA1	EDMAC3_REQ/IDE_REQ	Direct Memory Access	AB13	BI_DATA15 (LSB)	Bus Interface
AA2	BI_ADDRESS8 (MSB)	Bus Interface	AB14	BI_DATA14	Bus Interface
AA3	GND	Ground	AB15	BI_DATA2	Bus Interface
AA4	VDD25	2.5 V Power	AB16	BI_DATA3	Bus Interface
AA5	BI_ADDRESS13	Bus Interface	AB17	BI_DATA4	Bus Interface
AA6	BI_ADDRESS24	Bus Interface	AB18	SC1_DETECT	Smart Card Interface 1
AA7	BI_ADDRESS26	Bus Interface	AB19	SC1_RESET	Smart Card Interface 1
AA8	BI_ADDRESS28	Bus Interface	AB20	GPIO_8	General Purpose I/O
AA9	BI_ADDRESS15	Bus Interface	AB21	SC0_CLK	Smart Card Interface 0
AA10	BI_READY	Bus Interface	AB22	GND	Ground
AA11	GPIO_17	General Purpose I/O	AB23	GND	Ground
AA12	BI_CS2	Bus Interface	AC1	GND	Ground

**Signal Pins Sorted by Pin Number (Continued)**

Grid (Pin) Position	Signal	Group	Grid (Pin) Position	Signal	Group
AC2	GND	Ground	B15	SD1_CAS	SDRAM1 Controller
AC3	BI_ADDRESS9	Bus Interface	B16	SD1_ADDRESS2	SDRAM1 Controller
AC4	BI_ADDRESS10	Bus Interface	B17	SD1_ADDRESS3	SDRAM1 Controller
AC5	BI_ADDRESS12	Bus Interface	B18	SD1_ADDRESS12	SDRAM1 Controller
AC6	BI_ADDRESS20	Bus Interface	B19	SD1_ADDRESS10	SDRAM1 Controller
AC7	BI_ADDRESS18	Bus Interface	B20	MUX0_18	Multiplexed I/O
AC8	BI_ADDRESS16	Bus Interface	B21	MUX0_32	Multiplexed I/O
AC9	BI_ADDRESS30	Bus Interface	B22	GND	Ground
AC10	BI_ADDRESS31 (LSB)/BI_WEB1	Bus Interface	B23	GND	Ground
AC11	GPIO_3	General Purpose I/O	C1	DV1_DATA6	Video and Graphics
AC12	BI_CS3	Bus Interface	C2	DV1_DATA5	Video and Graphics
AC13	BI_OE	Bus Interface	C3	GND	Ground
AC14	BI_DATA7	Bus Interface	C4	VDD25	2.5 V Power
AC15	BI_DATA9	Bus Interface	C5	SERIAL1/INFRARED_TXD	Serial1 / Infrared
AC16	BI_DATA10	Bus Interface	C6	GPIO_29	General Purpose I/O
AC17	BI_DATA11	Bus Interface	C7	G_SYSTEM_RST	Global
AC18	GPIO_7	General Purpose I/O	C8	G_SYSTEM_CLOCK	Global
AC19	SC1_IO	Smart Card Interface 1	C9	CLK_VDDA	PLL Analog PWR + GND
AC20	SC1_VCC_COMMAND	Smart Card Interface 1	C10	SD1_DATA14	SDRAM1 Controller
AC21	SC0_IO	Smart Card Interface 0	C11	SD1_DATA12	SDRAM1 Controller
AC22	GND	Ground	C12	SD1_DATA4	SDRAM1 Controller
AC23	GND	Ground	C13	SD1_DATA6	SDRAM1 Controller
B1	GND	Ground	C14	SD1_DQMH	SDRAM1 Controller
B2	GND	Ground	C15	SD1_RAS	SDRAM1 Controller
B3	DV1_DATA7 (LSB)	Video and Graphics	C16	SD1_ADDRESS0 (MSB)	SDRAM1 Controller
B4	MUX2_1	Multiplexed I/O	C17	SD1_ADDRESS5	SDRAM1 Controller
B5	MUX2_3	Multiplexed I/O	C18	SD1_ADDRESS7	SDRAM1 Controller
B6	Reserved - Tie to 3.3 V	Global	C19	SD1_ADDRESS9	SDRAM1 Controller
B7	GPIO_9	General Purpose I/O	C20	VDD25	2.5 V Power
B8	GPIO_12	General Purpose I/O	C21	GND	Ground
B9	GPIO_15	General Purpose I/O	C22	MUX0_31	Multiplexed I/O
B10	SD1_DATA1	SDRAM1 Controller	C23	MUX0_20	Multiplexed I/O
B11	SD1_DATA3	SDRAM1 Controller	D1	DV1_DATA4	Video and Graphics
B12	SD1_DATA10	SDRAM1 Controller	D2	DV1_DATA3	Video and Graphics
B13	SD1_DATA9	SDRAM1 Controller	D3	VDD25	2.5 V Power
B14	SD1_DQML	SDRAM1 Controller	D4	GND	Ground

**Signal Pins Sorted by Pin Number (Continued)**

Grid (Pin) Position	Signal	Group	Grid (Pin) Position	Signal	Group
D5	VDD25	2.5 V Power	G2	DAC1_AVDD3	DAC Analog PWR + GND
D6	SERIAL1/INFRARED_RTS	Serial1 / Infrared	G3	DAC1_AGND2	DAC Analog PWR + GND
D7	GPIO_11	General Purpose I/O	G4	GPIO_2	General Purpose I/O
D8	GPIO_14	General Purpose I/O	G20	MUX0_17	Multiplexed I/O
D9	VDD33	3.3 V Power	G21	GPIO_31	General Purpose I/O
D10	SD1_DATA0 (MSB)	SDRAM1 Controller	G22	MUX0_25	Multiplexed I/O
D11	SD1_DATA2	SDRAM1 Controller	G23	GPIO_30	General Purpose I/O
D12	GND	Ground	H1	GPIO_19	General Purpose I/O
D13	SD1_DATA7	SDRAM1 Controller	H2	DAC1_VREF_IN	Video and Graphics
D14	SD1_CLK	SDRAM1 Controller	H3	DAC1_RREF_OUT	Video and Graphics
D15	VDD33	3.3 V Power	H4	DAC1_BOUT	Video and Graphics
D16	SD1_ADDRESS4	SDRAM1 Controller	H20	GPIO_5	General Purpose I/O
D17	SD1_ADDRESS6	SDRAM1 Controller	H21	MUX0_15	Multiplexed I/O
D18	SD1_ADDRESS8	SDRAM1 Controller	H22	MUX0_34	Multiplexed I/O
D19	VDD25	2.5 V Power	H23	MUX0_16	Multiplexed I/O
D20	GND	Ground	J1	DAC1_AGND1	DAC Analog PWR + GND
D21	VDD25	2.5 V Power	J2	GPIO_20	General Purpose I/O
D22	MUX0_30	Multiplexed I/O	J3	DAC1_AVDD2	DAC Analog PWR + GND
D23	MUX0_21	Multiplexed I/O	J4	VDD33	3.3 V Power
E1	DV1_DATA2	Video and Graphics	J20	VDD33	3.3 V Power
E2	DV1_DATA1	Video and Graphics	J21	MUX0_2	Multiplexed I/O
E3	DV1_DATA0 (MSB)	Video and Graphics	J22	MUX0_14	Multiplexed I/O
E4	VDD25	2.5 V Power	J23	INT2	Interrupt
E20	VDD25	2.5 V Power	K1	GPIO_28	General Purpose I/O
E21	MUX0_22	Multiplexed I/O	K2	DAC1_AVDD1	DAC Analog PWR + GND
E22	MUX0_29	Multiplexed I/O	K3	DAC1_GOUT	Video and Graphics
E23	MUX0_28	Multiplexed I/O	K4	GPIO_27	General Purpose I/O
F1	DAC1_BREF_OUT	Video and Graphics	K20	AUD_VDDA1	PLL Analog PWR + GND
F2	DV1_HSYNC	Video and Graphics	K21	MUX0_1	Multiplexed I/O
F3	DV1_VSYNC	Video and Graphics	K22	INT3	Interrupt
F4	DV1_PIXEL_CLOCK	Video and Graphics	K23	MUX0_0	Multiplexed I/O
F20	MUX0_26	Multiplexed I/O	L1	DAC1_AGND0	DAC Analog PWR + GND
F21	MUX0_23	Multiplexed I/O	L2	DAC1_ROUT	Video and Graphics
F22	MUX0_27	Multiplexed I/O	L3	DAC1_AVDD0	DAC Analog PWR + GND
F23	MUX0_24	Multiplexed I/O	L4	DAC1_GREF_OUT	Video and Graphics
G1	GPIO_18	General Purpose I/O	L20	MUX0_6	Multiplexed I/O





**Signal Pins Sorted by Pin Number (Continued)**

Grid (Pin) Position	Signal	Group	Grid (Pin) Position	Signal	Group
L21	MUX0_5	Multiplexed I/O	T1	DAC2_RREF_OUT	Video and Graphics
L22	MUX0_4	Multiplexed I/O	T2	DAC2_AVDD3	DAC Analog PWR + GND
L23	MUX0_3	Multiplexed I/O	T3	DAC2_BOUT	Video and Graphics
M1	DAC2_AVDD0	DAC Analog PWR + GND	T4	GPIO_21	General Purpose I/O
M2	DAC2_AGND0	DAC Analog PWR + GND	T20	MUX3_3	Multiplexed I/O
M3	DAC2_ROUT	Video and Graphics	T21	MUX3_5	Multiplexed I/O
M4	GND	Ground	T22	MUX3_6	Multiplexed I/O
M20	GND	Ground	T23	MUX3_4	Multiplexed I/O
M21	MUX0_7	Multiplexed I/O	U1	DAC2_AGND2	DAC Analog PWR + GND
M22	MUX0_12	Multiplexed I/O	U2	DAC2_BREF_OUT	Video and Graphics
M23	MUX0_13	Multiplexed I/O	U3	I2C0_SDA	Inter-Integrated Circuit (IIC)
N1	DAC2_GREF_OUT	Video and Graphics	U4	I2C0_SCL	Inter-Integrated Circuit (IIC)
N2	GPIO_26	General Purpose I/O	U20	CI_CLOCK	Channel Interface
N3	DAC2_GOUT	Video and Graphics	U21	MUX3_1	Multiplexed I/O
N4	DAC2_AVDD1	DAC Analog PWR + GND	U22	MUX3_2	Multiplexed I/O
N20	MUX0_8	Multiplexed I/O	U23	MUX3_0	Multiplexed I/O
N21	GPIO_1	General Purpose I/O	V1	DA_BIT_CLOCK	Audio
N22	AUD_VDDA0	PLL Analog PWR + GND	V2	DA_OVERSAMPLING_CLOCK	Audio
N23	GPIO_0	General Purpose I/O	V3	DA_LR_CHANNEL_CLOCK	Audio
P1	GPIO_25	General Purpose I/O	V4	DA_SERIAL_DATA0	Audio
P2	GPIO_24	General Purpose I/O	V20	CI_DATA5	Channel Interface
P3	DAC2_AGND1	DAC Analog PWR + GND	V21	CI_DATA7 (LSB)	Channel Interface
P4	DAC2_AVDD2	DAC Analog PWR + GND	V22	CI_DATA_ENABLE	Channel Interface
P20	MUX3_10	Multiplexed I/O	V23	CI_DATA6	Channel Interface
P21	MUX0_9	Multiplexed I/O	W1	DA_IEC_958	Audio
P22	MUX0_10	Multiplexed I/O	W2	MUX1_1	Multiplexed I/O
P23	MUX0_11	Multiplexed I/O	W3	MUX1_2	Multiplexed I/O
R1	GPIO_23	General Purpose I/O	W4	VDD25	2.5 V Power
R2	GPIO_22	General Purpose I/O	W20	VDD25	2.5 V Power
R3	DAC2_VREF_IN	Video and Graphics	W21	CI_DATA3	Channel Interface
R4	VDD33	3.3 V Power	W22	CI_DATA4	Channel Interface
R20	VDD33	3.3 V Power	W23	CI_DATA2	Channel Interface
R21	MUX3_8	Multiplexed I/O	Y1	MUX1_0	Multiplexed I/O
R22	MUX3_9	Multiplexed I/O	Y2	EDMAC3_ACK/IDE_ACK	Direct Memory Access
R23	MUX3_7	Multiplexed I/O	Y3	VDD25	2.5 V Power



**Signal Pins Sorted by Pin Number (Continued)**

Grid (Pin) Position	Signal	Group	Grid (Pin) Position	Signal	Group
Y4	GND	Ground	Y14	BI_DATA8	Bus Interface
Y5	VDD25	2.5 V Power	Y15	VDD33	3.3 V Power
Y6	BI_ADDRESS23	Bus Interface	Y16	BI_DATA13	Bus Interface
Y7	BI_ADDRESS25	Bus Interface	Y17	BI_DATA12	Bus Interface
Y8	BI_ADDRESS27	Bus Interface	Y18	SC0_DETECT	Smart Card Interface 0
Y9	VDD33	3.3 V Power	Y19	VDD25	2.5 V Power
Y10	BI_ADDRESS29	Bus Interface	Y20	GND	Ground
Y11	BI_WBE0	Bus Interface	Y21	VDD25	2.5 V Power
Y12	GND	Ground	Y22	CI_DATA1	Channel Interface
Y13	BI_CS0	Bus Interface	Y23	CI_DATA0 (MSB)	Channel Interface



## STB03xxx Multiplexed I/O Signal Table

STB03xxx has four sets of multiplexed I/O signals: Mux0, Mux1, Mux2, and Mux3. At reset, the multiplexed I/O signals are tristated, unless noted.

The multiplexed I/O can be selected by column in the following tables. For example, if Input/Output 1 is selected, Input/Output 2 and Input/Output 3 are not available.

Blank entries indicate reserved multiplexing.

### Multiplexed I/O Signal Table

Bit #	Input/Output 1	I/O	Input/Output 2	I/O
00	SD0_ADDRESS0 (MSB)	O	IEEE1284_PD0 (MSB)	I/O
01	SD0_ADDRESS1	O	IEEE1284_PD1	I/O
02	SD0_ADDRESS2	O	IEEE1284_PD2	I/O
03	SD0_ADDRESS3	O	IEEE1284_PD3	I/O
04	SD0_ADDRESS4	O	IEEE1284_PD4	I/O
05	SD0_ADDRESS5	O	IEEE1284_PD5	I/O
06	SD0_ADDRESS6	O	IEEE1284_PD6	I/O
07	SD0_ADDRESS7	O	IEEE1284_PD7	I/O
08	SD0_ADDRESS8	O	IEEE1284_AUTOFEED	I/O
09	SD0_ADDRESS9	O	IEEE1284_SELECT_IN	I/O
10	SD0_ADDRESS10	O	IEEE1284_BUSY	I/O
11	SD0_ADDRESS11	O	IEEE1284_SELECT	I/O
12	SD0_ADDRESS12	O	IEEE1284_PE	I/O
13	SD0_ADDRESS13	O	IEEE1284_ERROR	I/O
14	SD0_CS0	O	IEEE1284_ACK	I/O
15	SD0_RAS	O	IEEE1284_PDIR	O
16	SD0_CAS	O	IEEE1284_INIT	I/O
17	SD0_WE	O	IEEE1284_STROBE	I/O
18	SD0_DATA0	I/O	BI_DATA16	I/O
19	SD0_DATA1	I/O	BI_DATA17	I/O
20	SD0_DATA2	I/O	BI_DATA18	I/O
21	SD0_DATA3	I/O	BI_DATA19	I/O
22	SD0_DATA4	I/O	BI_DATA20	I/O
23	SD0_DATA5	I/O	BI_DATA21	I/O
24	SD0_DATA6	I/O	BI_DATA22	I/O
25	SD0_DATA7	I/O	BI_DATA23	I/O
26	SD0_DATA8	I/O	BI_DATA24	I/O
27	SD0_DATA9	I/O	BI_DATA25	I/O
28	SD0_DATA10	I/O	BI_DATA26	I/O

**Multiplexed I/O Signal Table (Continued)**

Bit #	Input/Output 1	I/O	Input/Output 2	I/O
29	SD0_DATA11	I/O	BI_DATA27	I/O
30	SD0_DATA12	I/O	BI_DATA28	I/O
31	SD0_DATA13	I/O	BI_DATA29	I/O
32	SD0_DATA14	I/O	BI_DATA30	I/O
33	SD0_DATA15	I/O	BI_DATA31 (LSB)	I/O
34	SD0_CLK	O	IEEE1284_HOST	O

**Multiplexed I/O Signal Table - Mux1**

Bit #	Input/Output 1	I/O	Input/Output 2	I/O
00	EDMAC2_ACK	O	EBM_HOLDACK	I/O
01	EDMAC2_REQ	I	EBM_HOLDREQ	I/O
02	EDMAC2_EOT	I/O	EBM_BUSREQ	I/O

**Multiplexed I/O Signal Table - Mux2**

Bit #	Input/Output 1	I/O	Input/Output 2	I/O
00	SERIAL0/16550_TXD	O	SSP_TXD	O
01	SERIAL0/16550_RXD	I	SSP_RXD	I
02	SERIAL0/16550_CTS	I	SSP_CLK	I
03	SERIAL0/16550_RTS	O	SSP_FS	I/O

**Multiplexed I/O Signal Table - Mux3**

Bit #	Input/Output 1	I/O	Input/Output 2	I/O	Input/Output 3	I/O	Input/Output 4	I/O
00	HSP_DATA0	O	IEEE1284_PD0 (MSB)	I/O	SERIAL1/INFRARED_D_DSR (through GPIO bit 31 alt rcv 2)	I	RT_TS1E	O
01	HSP_DATA1	O	IEEE1284_PD1	I/O	SERIAL1/INFRARED_D_DTR	O	RT_TS2E	O
02	HSP_DATA2	O	IEEE1284_PD2	I/O	RW_TMS (through GPIO bit 11 alt rcv 1)	I	RT_TS1O	O
03	HSP_DATA3	O	IEEE1284_PD3	I/O	RW_TDI (through GPIO bit 12 alt rcv 1)	I	RT_TS2O	O
04	HSP_DATA4	O	IEEE1284_PD4	I/O	RW_TCK (through GPIO bit 13 alt rcv 1)	I	RT_TS3	O

**Multiplexed I/O Signal Table - Mux3 (Continued)**

Bit #	Input/Output 1	I/O	Input/Output 2	I/O	Input/Output 3	I/O	Input/Output 4	I/O
05	HSP_DATA5	O	IEEE1284_PD5	I/O	RW_TDO	O	RT_TS4	O
06	HSP_DATA6	O	IEEE1284_PD6	I/O	RW_HALT (through GPIO bit 15 alt rcv 1)	I	RT_TS5	O
07	HSP_DATA7	O	IEEE1284_PD7	I/O	SERIAL0/16550_DS R (through GPIO bit 5 alt rcv 3)	I	RT_TS6	O
08	HSP_CLOCK	O	IEEE1284_ STROBE	I/O	SERIAL0/16550_DT R	O	RT_CLK	O
09	HSP_DATA_ ENABLE	O	IEEE1284_ACK	I/O	SERIAL0/16550_DC D (through GPIO bit 6 alt rcv 3)	I		
10	HSP_PACKET_ START	O	IEEE1284_INIT	I/O	SERIAL0/16550_RI (through GPIO bit 8 alt rcv 3)	I		

## General Purpose I/O (GPIO)

The following table describes the GPIO bits. For each GPIO bit only one signal can be selected at a time.

Each table row lists the signal associated with each logical GPIO bit number. The first column lists the GPIO bit number. The second column lists the signal connected as input or output to the first alternate GPIO multiplexer. The signal name is listed first, followed by the signal description. The third column gives the direction of the signal listed in column 2. The same format is used for columns 4 through 7.

Blank entries indicate reserved GPIO multiplexing.

GPIO bit number refers to the device GPIO signal name, not the physical device pin number.

After reset all GPIOs are programmed as inputs, with the exception of GPIO0 bit 29 (PWM output), which defaults to an open-drain output, and GPIO bit 14 (JTAG TDO output), which defaults to an output (if BI\_DATA[4] is set to '0' during reset).

### General Purpose I/O Bits

Bit #	Input/Output Mux 1	I/O	Input/Output Mux 2	I/O	Input/Output Mux 3	I/O
00	I2C1_SCL	I/O	DA_DEEMPHASIS0	O	DA_SURMOD0	O
01	I2C1_SDA	I/O	DA_DEEMPHASIS1	O	DA_SURMOD1	O
02	AV_CS SYNC BI_CS4	I O	GPT_FreqGenOut	O	DA_SURMOD0 INT4	O I
03	SYS_CLK	O	BI_CS5	O	DA_SURMOD1 INT5	O I
04	EDMAC0_REQ	I	SD1_CS1	O	SERIAL0/16550_DTR	O
05	EDMAC0_ACK	O	SD0_CS1	O	SERIAL0/16550_DSR	I
06	SCP_TXD	O	CI_PACKET_START	I	SERIAL0/16550_DCD	I
07	SCP_RXD	I	CI_DATA_ERROR	I	TS_BCLKEN	I
08	SCP_CLK	O	TS_REQ	O	SERIAL0/16550_RI	I
09	PWM0	O	GPT_COMP0	O	GPT_CAPT0	I O
10	PWM1	O	GPT_COMP1	O	GPT_CAPT1 BI_CS7	I O
11	RW_TMS	I	SSP_TXD	O	BI_CS6	O
12	RW_TDI	I	SSP_RXD	I	BI_CS7	O
13	RW_TCK	I	SSP_CLK	I	INT6	I
14	RW_TDO	O	SSP_FS	I/O	INT7	I
15	RW_HALT	I	SERIAL0/16550_CLK - External SERIAL0/16550 Clock Input	I	SYS_CLK	O
16	DA_SERIAL_DATA1	O	BI_CS4	O		
17	DA_SERIAL_DATA2	O	BI_CS5	O	HSP_ERROR	O
18	DV_TRANSPARENCY_ GATE	I/O	DV2_PIXEL_CLOCK	I	SERIAL1/INFRARED_CLK - External SERIAL1/INFRARED Clock Input	I

**General Purpose I/O Bits (Continued)**

Bit #	Input/Output Mux 1	I/O	Input/Output Mux 2	I/O	Input/Output Mux 3	I/O
19	TTX_REQ	I/O	DV2_VSYNC	I/O		
20	TTX_DATA	I/O	DV2_HSYNC	I/O		
21	DV2_DATA0 (MSB)	I/O	$\overline{\text{IEEE1284\_AUTOFEED}}$	I/O	INT8	I
22	DV2_DATA1	I/O	$\overline{\text{IEEE1284\_SELECT\_IN}}$	I/O	INT9	I
23	DV2_DATA2	I/O	IEEE1284_BUSY	I/O		
24	DV2_DATA3	I/O	IEEE1284_SELECT	I/O		
25	DV2_DATA4	I/O	$\overline{\text{IEEE1284\_PE}}$	I/O		
26	DV2_DATA5	I/O	$\overline{\text{IEEE1284\_ERROR}}$	I/O		
27	DV2_DATA6	I/O	IEEE1284_PDIR	O		
28	DV2_DATA7	I/O	IEEE1284_HOST	O		
29	DENC_PWM_OUTPUT	O	XPT_PWM_OUTPUT	O		
30	$\overline{\text{EDMAC1\_REQ}}$ BI_WBE2	I O	$\overline{\text{SERIAL1/INFRARED\_DTR}}$	O	SD0_DQMH	O
31	$\overline{\text{EDMAC1\_ACK}}$	O	$\overline{\text{SERIAL1/INFRARED\_DSR}}$ BI_WBE3	I O	SD0_DQML	O

## Electrical Information

The following tables give the absolute ratings for various electrical characteristics.

### Drivers/Receivers

Four types of I/O drivers and receivers are used on the STB03xxx device, as follows:

#### I/O Driver Types

Driver/Receiver Type	Characteristics	Used on I/O signals:
BP3365	5 V tolerant, no pull-up or pull-down (external pull-up is required)	G_SYSTEM_RESET, GPIO[2], GPIO[29], SC0_IO, SC0_CLK, SC0_DETECT, SC0_RESET, SC0_VCC_COMMAND, SC1_IO, SC1_CLK, SC1_DETECT, SC1_RESET, SC1_VCC_COMMAND, BI_READY
BP3335	5 V tolerant, no pull-up or pull-down (external pull-up is required)	I2C0_SDA, I2C0_SCL, GPIO[0], GPIO[1]
BT3350PU	3.3 V I/O with pull-up	BI_DATA[0:15], MUX0[18:33]
BT3365PU	3.3 V I/O with pull-up	all other digital I/O signals

### DC Electrical Characteristics

The table, "DC Electrical Characteristics," gives the absolute ratings for various electrical characteristics. The temperature is 70° C in all cases.

#### DC Electrical Characteristics

Driver / Receiver	Symbol	Parameter	Conditions	Min	Typ	Max	Units
BP3335	V <sub>IH</sub>	High Level Input Voltage		2.00		5.50 <sup>1</sup>	V
	V <sub>IL</sub>	Low Level Input Voltage		-0.60 <sup>2</sup>		0.80	V
	V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = 17.0 mA	2.40			V
	V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 11.0 mA			0.4	V
BP3365	V <sub>IH</sub>	High Level Input Voltage		2.00		5.50 <sup>1</sup>	V
	V <sub>IL</sub>	Low Level Input Voltage		-0.60 <sup>2</sup>		0.80	V
	V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = 9.0 mA	2.40			V
	V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 6.0 mA			0.4	V

1. Maximum V<sub>IH</sub> applies to overshoot only.
2. Minimum V<sub>IL</sub> applies to undershoot only.





**DC Electrical Characteristics (Continued)**

Driver / Receiver	Symbol	Parameter	Conditions	Min	Typ	Max	Units
BT3350PU	V <sub>IH</sub>	High Level Input Voltage		2.00		4.0 <sup>1</sup>	V
	V <sub>IL</sub>	Low Level Input Voltage		-0.60 <sup>2</sup>		0.80	V
	V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = 12.0 mA	2.40			V
	V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA			0.4	V
BT3365PU	V <sub>IH</sub>	High Level Input Voltage		2.00		4.0 <sup>1</sup>	V
	V <sub>IL</sub>	Low Level Input Voltage		-0.60 <sup>2</sup>		0.80	V
	V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = 9.0 mA	2.40			V
	V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 6.0 mA			0.4	V
BT3350PU, BT3365PU	I <sub>I</sub>	Maximum Input Current	V <sub>IN</sub> = 0 V			-250	μA
BP3335, BP3365	I <sub>I</sub>	Maximum Input Current				0	μA
N/A	I <sub>CC</sub>	Supply Current, 2.5 V	V <sub>CC</sub> = Max			TBD	mA
N/A	I <sub>CC330</sub>	Supply Current, 3.3 V	V <sub>CC330</sub> = Max			TBD	mA
All	C <sub>I</sub>	Input Capacitance	V <sub>CC</sub> = Nom, V <sub>I</sub> = Nom			2.6	pF
All	ESD	Electro Static Discharge		-3000		3000	V
N/A	PD	Power Dissipation			2.5		W

1. Maximum V<sub>IH</sub> applies to overshoot only.  
2. Minimum V<sub>IL</sub> applies to undershoot only.

The absolute maximum ratings in the following table are stress ratings only. Operation at or beyond these maximum ratings may cause permanent damage to the device.

### Absolute Maximum Ratings

Parameter	Maximum Rating
Supply voltage with respect to GND, 2.5 V supply	3.0 V
Supply voltage with respect to GND, 3.3 V supply	3.9 V
Case temperature under bias	TBD
Storage temperature	-65° C to 150° C

### Operating Conditions

The STB03xxx Digital Set-Top Box Integrated Controller can interface to either 3.3 V or 5 V technologies. 5 V interfaces are supported only for drivers/receivers supporting 5 V tolerance (see *Drivers/Receivers*). The range for supply voltages is specified for five-percent margins relative to a nominal 2.5 V and 3.3 V power supply.

**Note:** Device operation beyond the conditions specified in the table below is not recommended. Extended operation beyond the recommended conditions may affect device reliability.

### Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage, 2.5 V	2.38	2.62	V
V <sub>CC330</sub>	Supply Voltage, 3.3 V	3.14	3.47	V
T <sub>A</sub>	Operating Free Air Temperature	0°	70°	C

### Power Considerations

Power dissipation is determined by operating frequency, temperature, and supply voltage, as well as external source/sink current requirements.

### Power Sequencing

The 2.5 V power supply must maintain the following relationship whenever the 3.3 V power supply voltage is greater than 0.4 V:

2.5 V power supply voltage  $\geq$  0.4 V

Supply excursions outside this range must be limited to less than 25 ms duration during each power-up or power-down event.

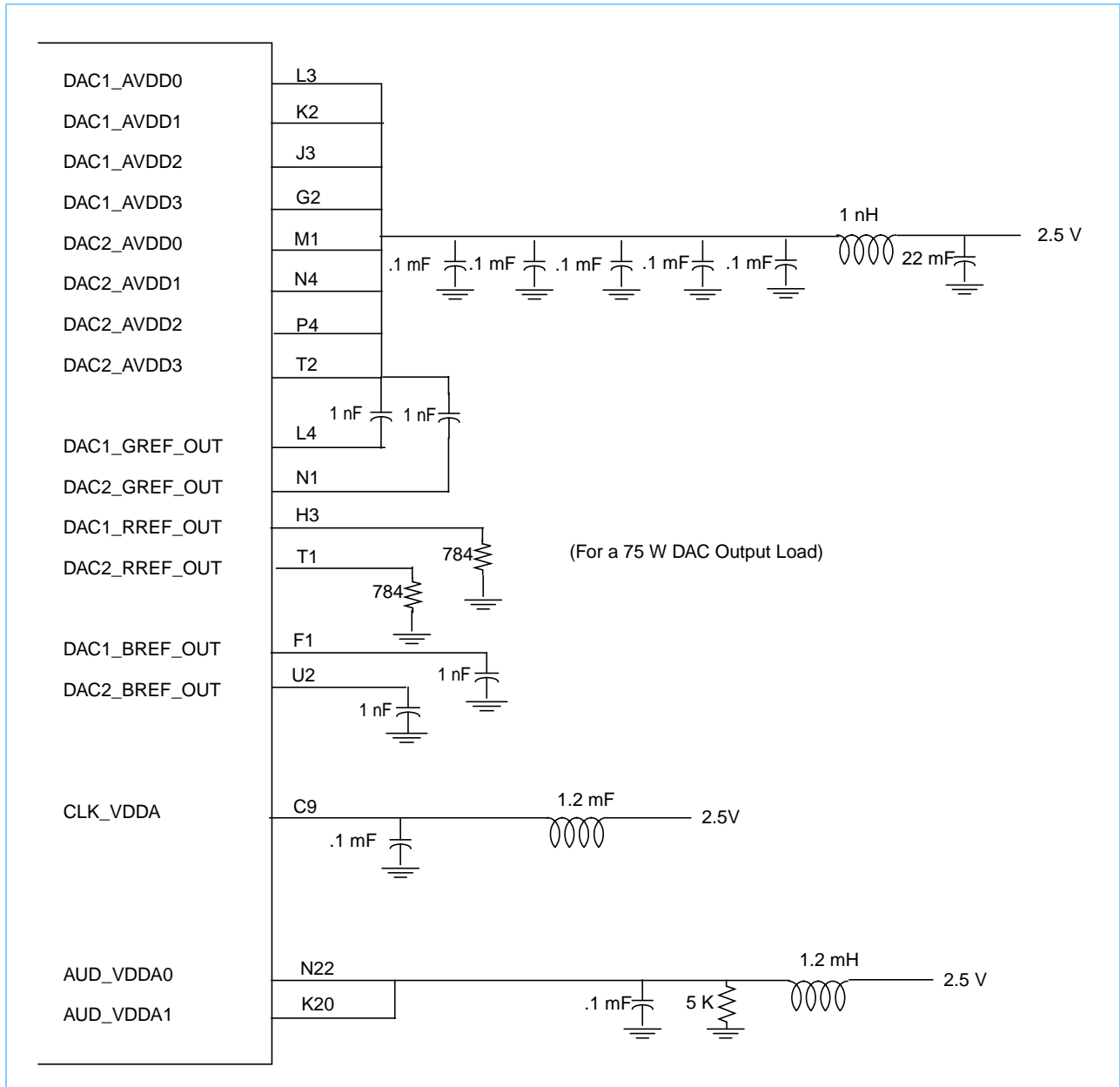
### General Recommendation

System designs that derive the 2.5 V supply from a regulator running from the 3.3 V supply are recommended to ensure a fixed relationship between the two voltage supplies. Such usage substantially reduces the potential for the 3.3 V supply to be present without the 2.5 V supply.

### Recommended Connections

Power and ground pins should all be connected to separate power and ground planes in the circuit board to which the STB03xxx is mounted. Unused input pins must be tied inactive, either high or low.

### Recommended Connections for Analog I/O Pins



## I/O Timing Diagrams

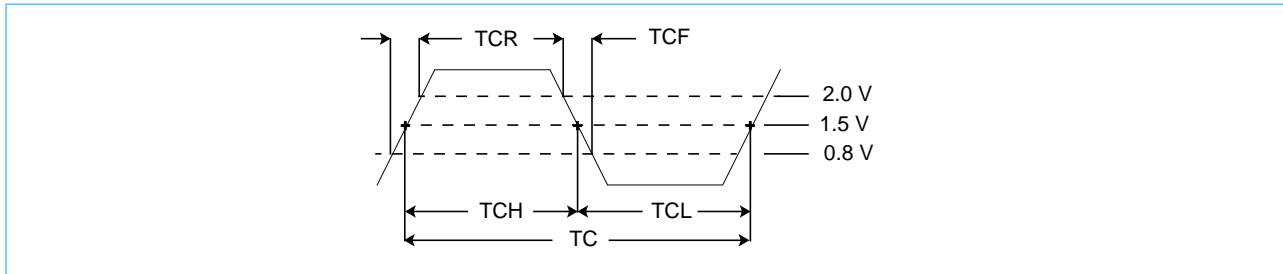
### AC Specification

**Note 1.** Clock timing and switching characters are specified in accordance with operating conditions in *Recommended Operating Conditions* on page 34. AC specifications assume a 30 pF output load. All input slow rates *must be* 5 ns or less, unless otherwise specified (rise and fall times measured between 0.8 V and 2.0 V). Also, all input clocks *must* have a 40–60% duty cycle, unless otherwise specified.

**Note 2.** The internal SysClk is shown in the diagrams to indicate the relationship of the number of cycles between various signal edges on the timing diagram.

**Note 3.** Where multiple interfaces share the same timing diagram, the signals names are listed using an 'n' to indicate that the timings apply to both interfaces. For example, the SD0 and SD1 interface signal names in the SDRAM interface timing diagram are listed as 'SDn'.

### G\_SysClk Timing



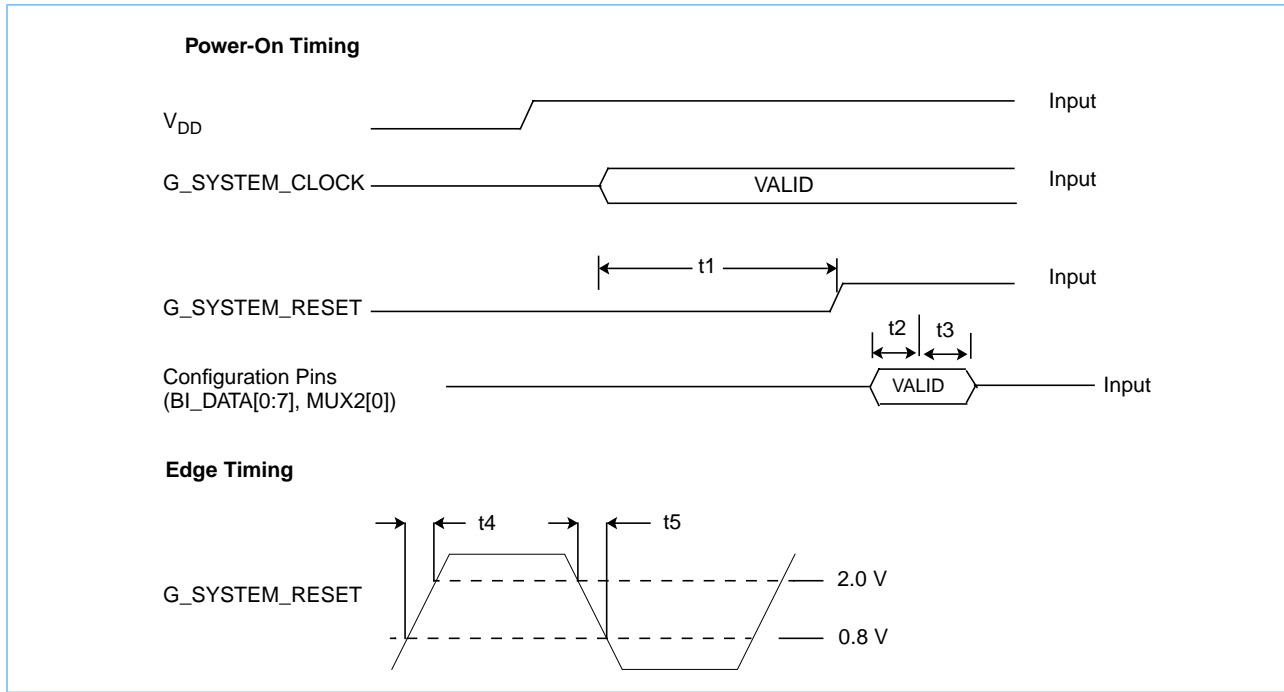
### SysClk Timing Values

Symbol	Parameter	Min	Max	Units
$F_C$	SysClk clock input frequency	(Nominal 27)		MHz
$T_{CS}$	Clock edge stability <sup>1</sup>		0.15	ns
$T_{CH}$	Clock input high time	15		ns
$T_{CL}$	Clock input low time	15		ns
$T_{CR}$	Clock input rise time <sup>2</sup>		0.6	ns
$T_{CF}$	Clock input fall time <sup>2</sup>		0.6	ns

**Note 1.** Cycle-to-cycle jitter allowed between any two edges.

**Note 2.** Rise and fall times measured between 0.8 V and 2.0 V.

### G\_System\_Reset Timing

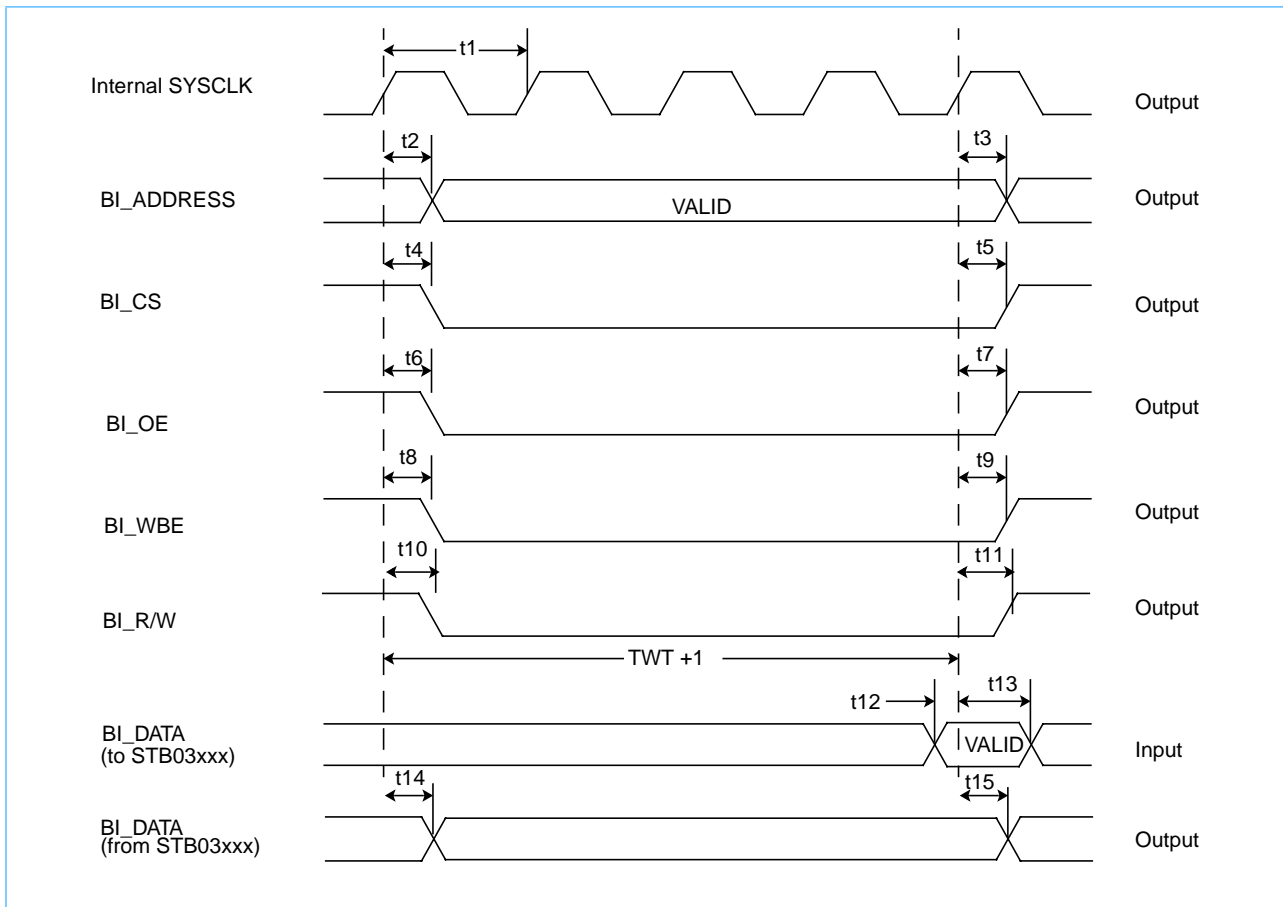


### G\_SYSTEM\_RESET Timing Values

Symbol	Parameter	Min	Max	Units
T <sub>1</sub>	Clock to Reset inactive	152		μs
T <sub>2</sub>	Input setup time	0		ns
T <sub>3</sub>	Input hold time	80		ns
T <sub>4</sub>	Input rise time		37	ns
T <sub>5</sub>	Input fall time		37	ns

**Note:** External logic must drive G\_SYSTEM\_RESET low during power-on, using an open-drain driver.

### SRAM Interface Timing

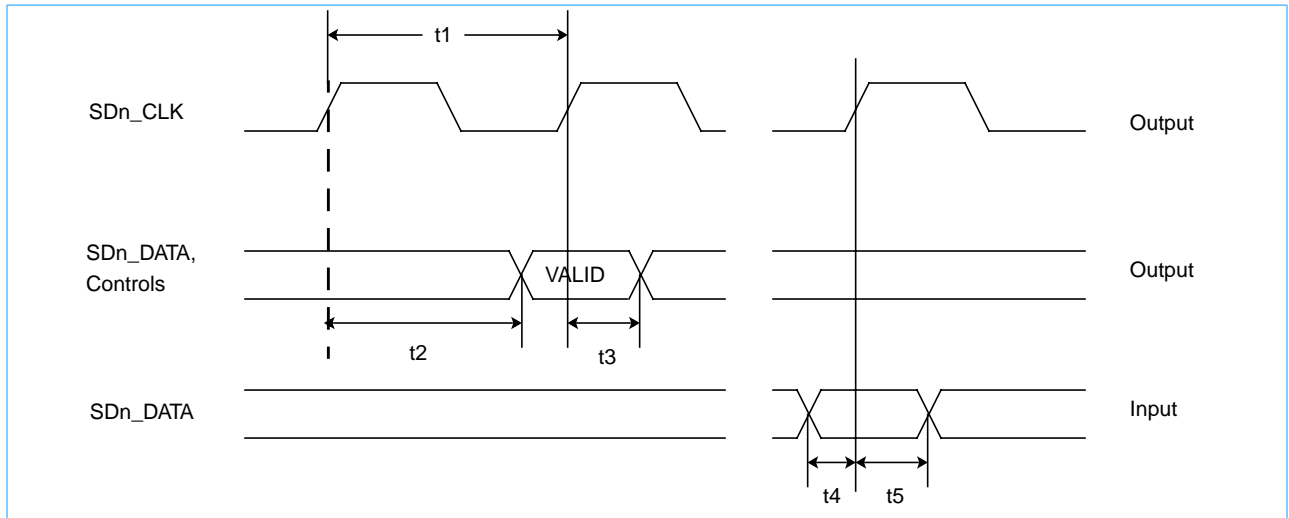


### SRAM Interface Timing Values

Symbol	Parameter	Min	Max	Units
$T_1$	At SYSCLK = 54 MHz		19.25	ns
$T_2$	Address output valid time		12	ns
$T_3$	Address output hold time	3		ns
$T_4$	Chip Select output valid time		12	ns
$T_5$	Chip Select output hold time	3		ns
$T_6$	Output Enable output valid time		12	ns
$T_7$	Output Enable output hold time	3		ns
$T_8$	Write Byte Enable output valid time		12	ns
$T_9$	Write Byte Enable output hold time	3		ns
$T_{10}$	Read/Write output valid time		12	ns
$T_{11}$	Read/Write output hold time	3		ns
$T_{12}$	Data input setup time	7		ns

**SRAM Interface Timing Values (Continued)**

Symbol	Parameter	Min	Max	Units
T <sub>13</sub>	Data input hold time	3		ns
T <sub>14</sub>	Data output valid time		15	ns
T <sub>16</sub>	Data output hold time	3		ns

**SDRAM Interface Timing Diagram**

**SDRAM Interface Timing Values**

Symbol	Parameter	Min	Max	Units
T <sub>1</sub>	SD_clk clock period (at SYSCLK = 54 MHz)	9.25		ns
T <sub>2</sub>	Output valid time		7.25	ns
T <sub>3</sub>	Output hold time	1		ns
T <sub>4</sub>	Input setup time	1		ns
T <sub>5</sub>	Input hold time	2.5		ns

**Notes:**

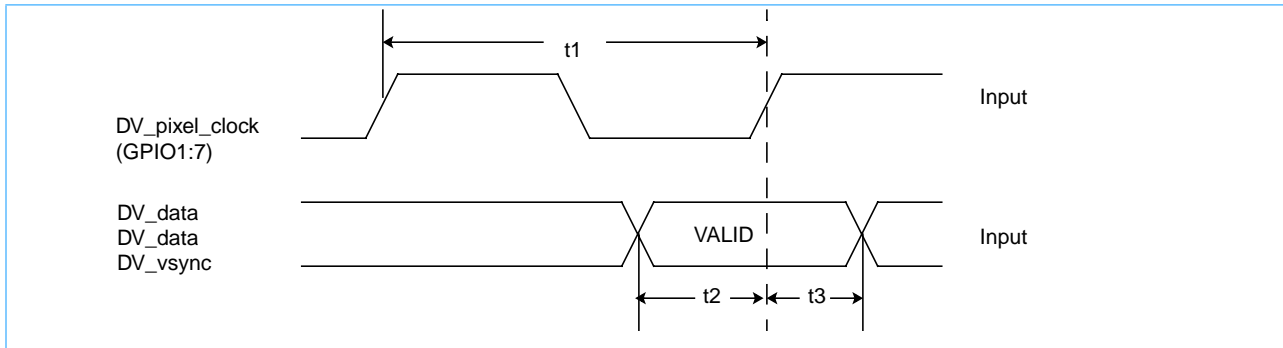
T<sub>RCD</sub> = (2, 3, or 4) x t<sub>1</sub> – controlled by SDRAMC Bank Register bits [21:22]

T<sub>RAS</sub> = (5 or 6) x t<sub>1</sub> – controlled by SDRAMC System Register bit 4

T<sub>RP</sub> = (2, 3, or 4) x t<sub>1</sub> – controlled by SDRAMC Bank Register bits [25:26]

T<sub>RC</sub> = (7, 8, 9, or 10) x t<sub>1</sub> – controlled by SDRAMC Bank Register bits [30:31]

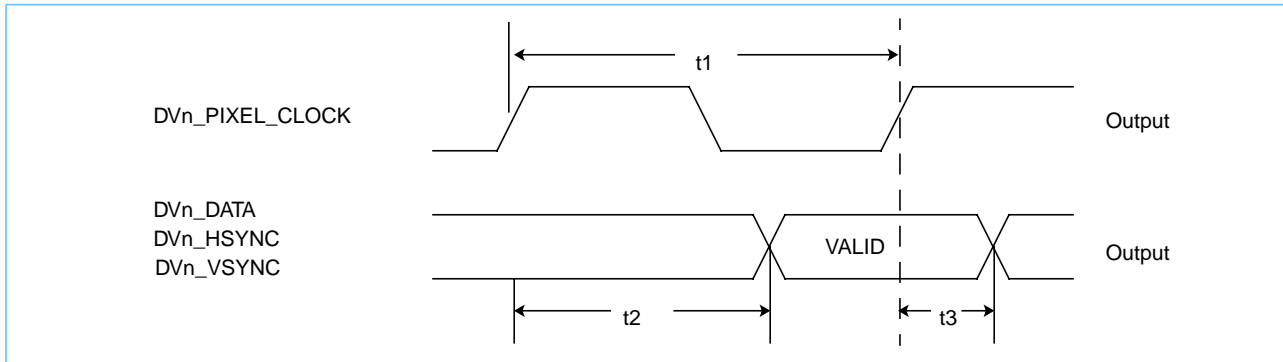
### Video Input Interface Timing



### Video Input Timing Values

Symbol	Parameter	Min	Max	Units
T <sub>1</sub>	Pixel clock period		37	ns
T <sub>2</sub>	Output valid time	16		ns
T <sub>3</sub>	Output valid time	4		ns
T <sub>4</sub>	Input setup time	11		

### Video Output Interface Timing

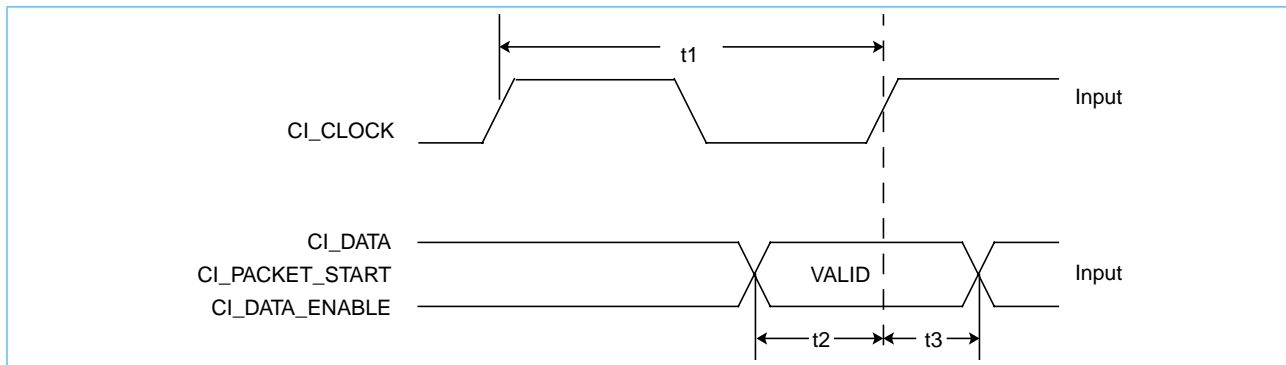


### Video Output Timing Values

Symbol	Parameter	Min	Max	Units
T <sub>1</sub>	Pixel Clock period		37	ns
T <sub>2</sub>	Output valid time		15	ns
T <sub>3</sub>	Output hold time	4		ns



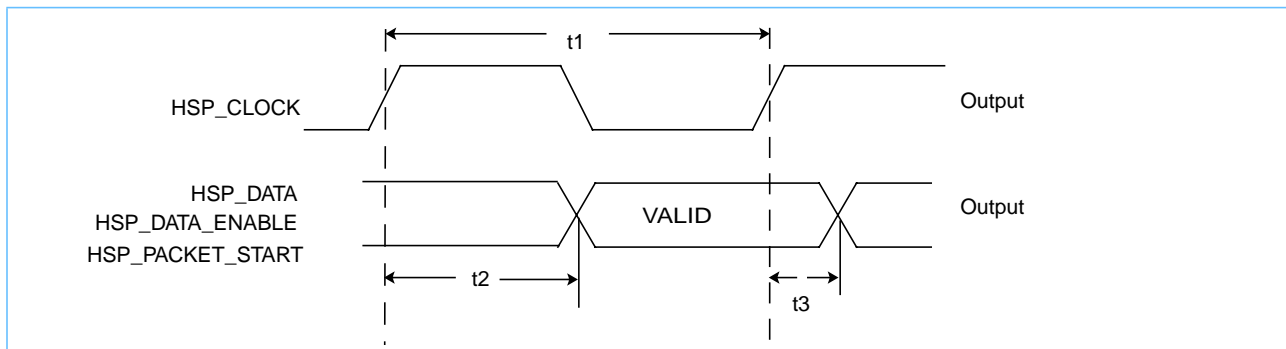
## Transport Input Interface Timing



## Transport Input Interface Timing Values

Symbol	Parameter	Min	Max	Units
T <sub>1</sub>	CI_CLOCK period	15		ns
T <sub>2</sub>	Input setup time	4		ns
T <sub>3</sub>	Input hold time	3		ns

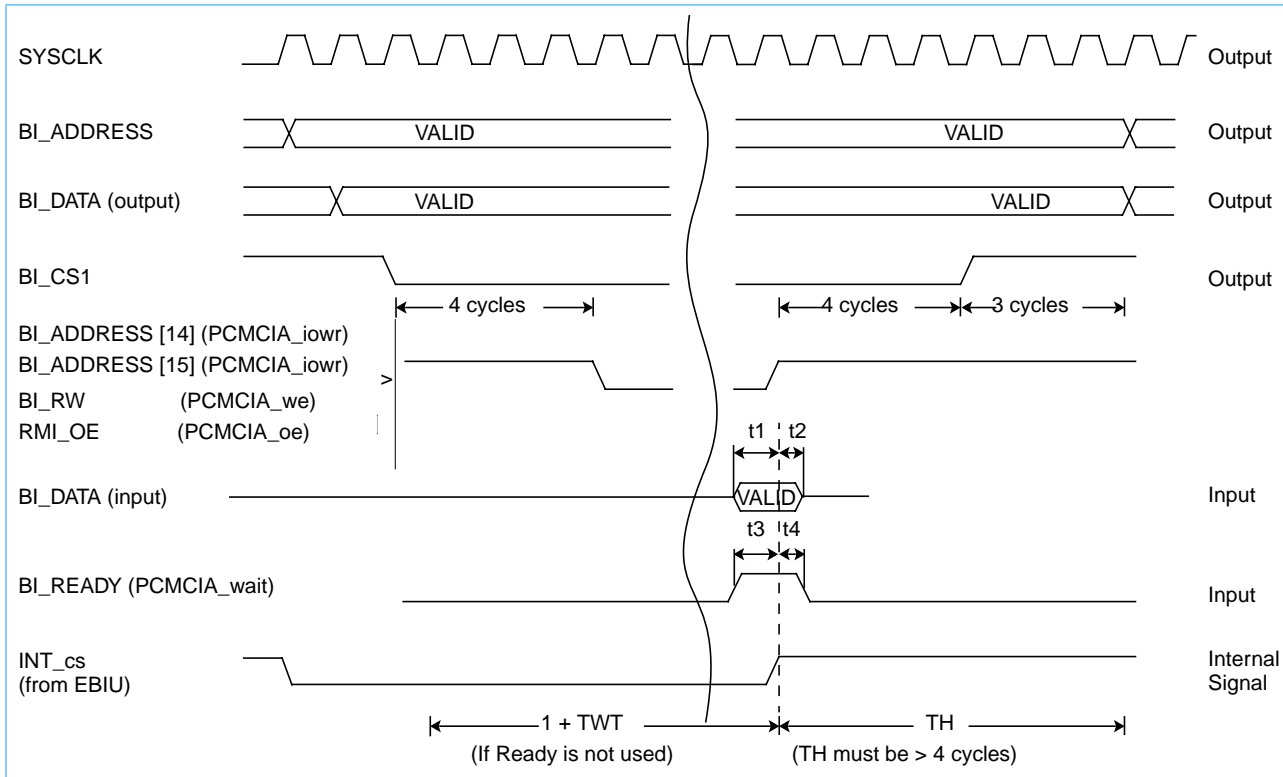
## Transport Auxiliary Output Interface Timing



## Transport Auxiliary Output Interface Timing Values

Symbol	Parameter	Min	Max	Units
T <sub>1</sub>	HSP_clock period (at SYSCLK = 54 MHz)	19.25		ns
T <sub>2</sub>	Output valid time		10	ns
T <sub>3</sub>	Output hold time	2		ns

### DVB-CI (PCMCIA) Interface Timing



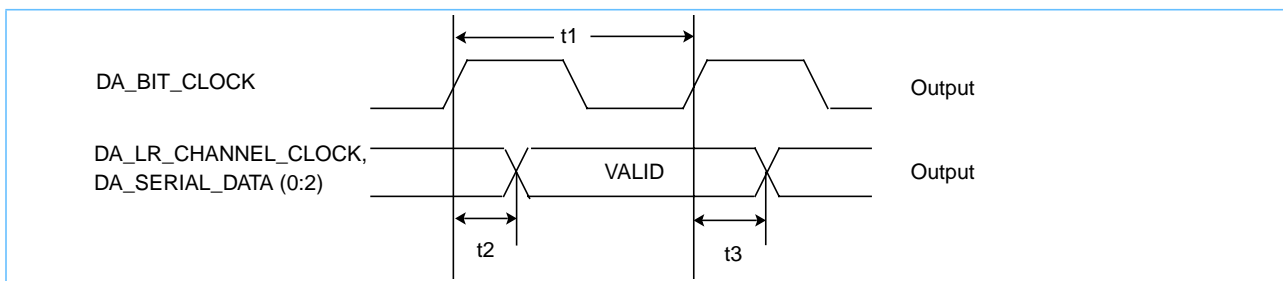
### DVB-CI (PCMCIA) Interface Timing Values

Symbol	Parameter	Min	Max	Units
$T_1$	Input set-up time	5		ns
$T_2$	Input hold time	3		ns
$T_3$	Input set-up time	15		ns
$T_4$	Input hold time	2		ns

**Note 1.** Refer to the SRAM timing diagram for DVB-CI output timing values on page (SRAM page).

**Note 2.** BI\_READY can also be configured as an asynchronous input.

### Audio Output Timing

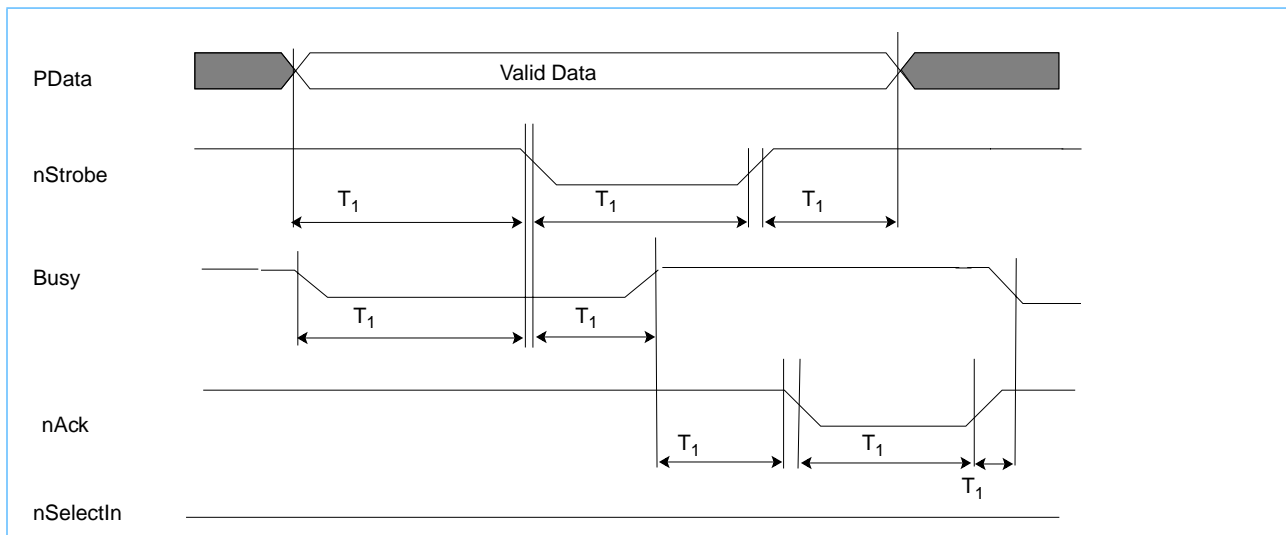


### Audio Output Timing Values

Symbol	Parameter	Min	Max	Units
T <sub>1</sub>	DA_bit_clock period (1/[64 x 48 kHz])	326		ns
T <sub>2</sub>	Output valid time		18	ns
T <sub>3</sub>	Output hold time	0		ns

### IEEE 1284 Timings

#### Compatibility Mode Handshake



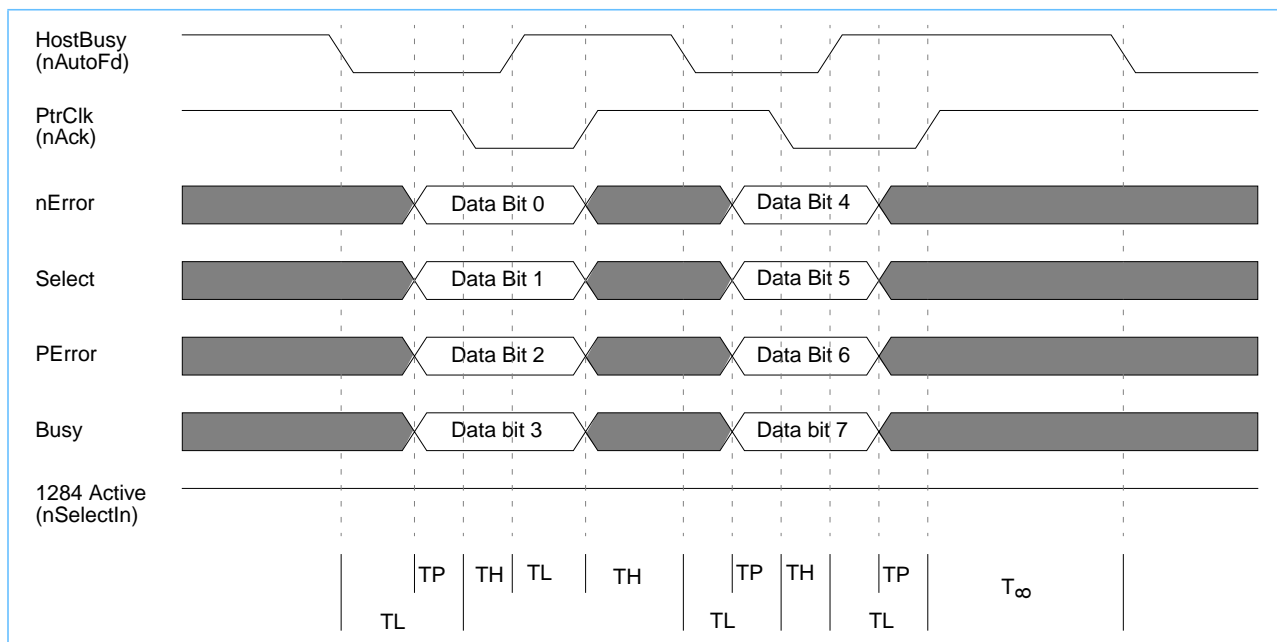
#### Compatibility Mode Handshake Timing Values

Symbol	Parameter	Min	Max	Units
T <sub>1</sub>	Host	750		ns
T <sub>2</sub>	Strobe	750 ns	500 μs	ns/μs
T <sub>3</sub>	Hold	750		ns
T <sub>4</sub>	Ready	0		ns
T <sub>5</sub>	Busy		500	ns
T <sub>6</sub>	Reply	0		ns
T <sub>7</sub>	Acknowledge (Ack)	500 ns	10 μs	ns/μs
T <sub>8</sub>	nBusy	0		ns

### IEEE 1284 Mode Handshake Timing Values

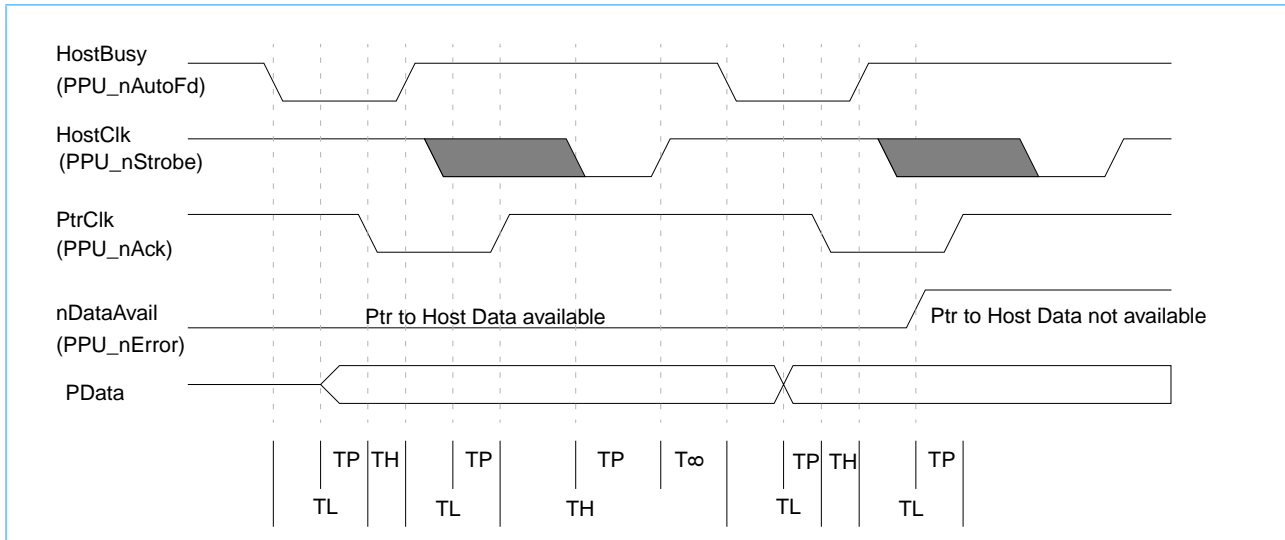
Symbol	Parameter	Min	Max	Units
$T_H$	Host response time	0	1	sec
$T_\infty$	Infinite response time	0	Infinite	
$T_L$	Peripheral response time	0	35	ms
$T_R$	Peripheral response time (ECP mode only)	0		
$T_P$	Minimum setup or pulse width	0.5 $\mu$ s		$\mu$ S
$T_D$	Minimum data setup time (ECP Modes only)	0		

### Nibble Mode Handshake



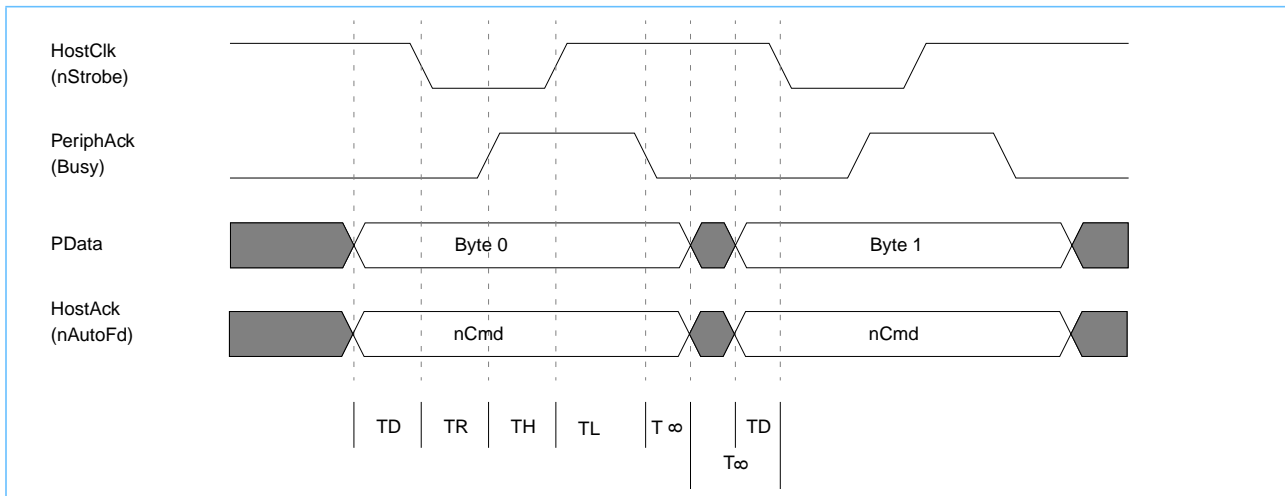
**Note:** See the table, "IEEE 1284 Mode Handshake Timing Values," for symbol values.

### Byte Mode Handshake



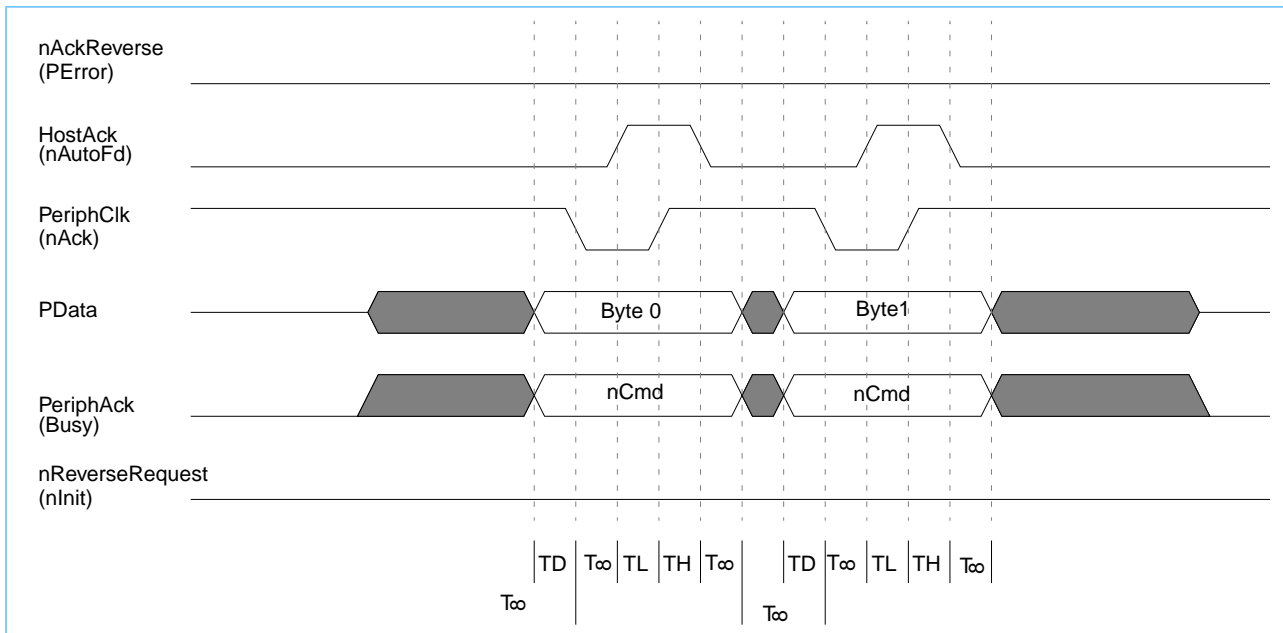
**Note:** See the table, "IEEE 1284 Mode Handshake Timing Values," on page 44 for symbol values.

### ECP Forward Mode Handshake



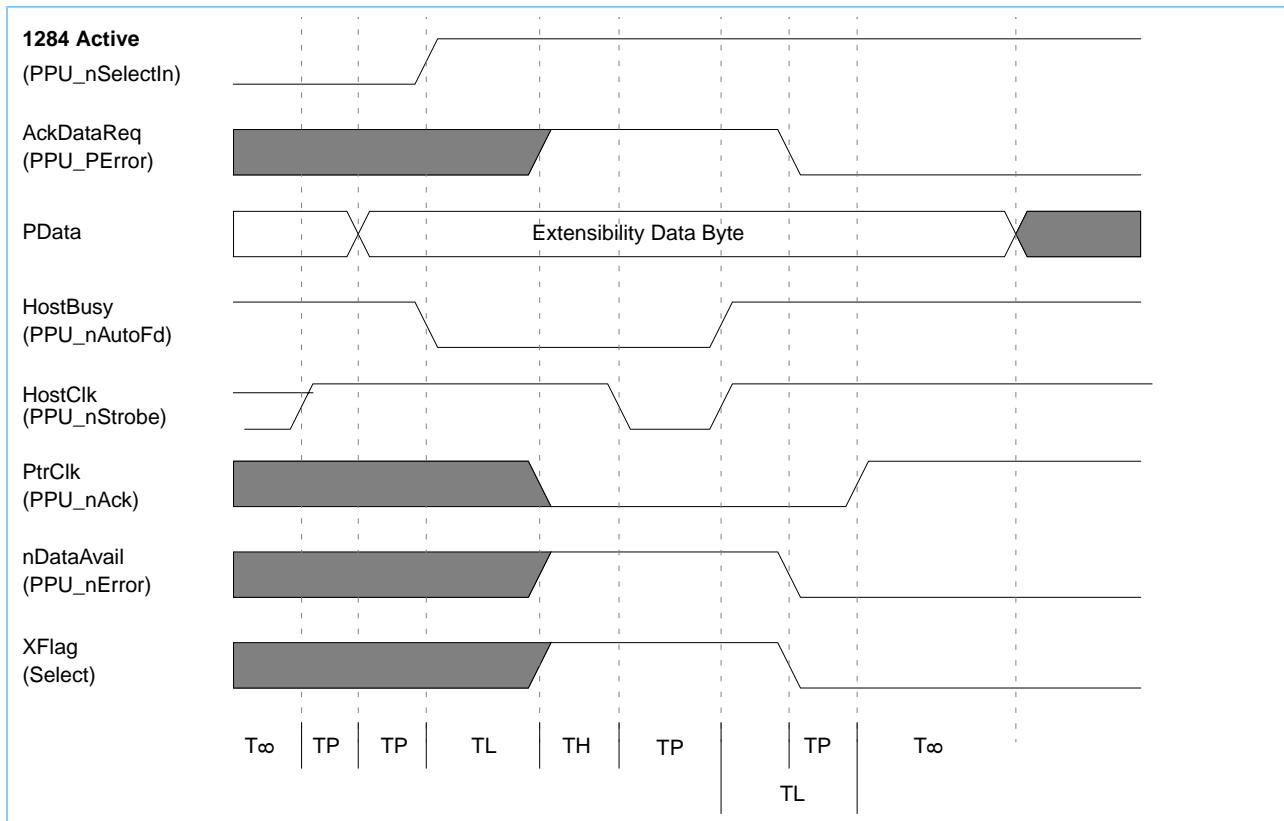
**Note:** See the table, "IEEE 1284 Mode Handshake Timing Values," on page 44 for symbol values.

### ECP Reverse Mode Handshake



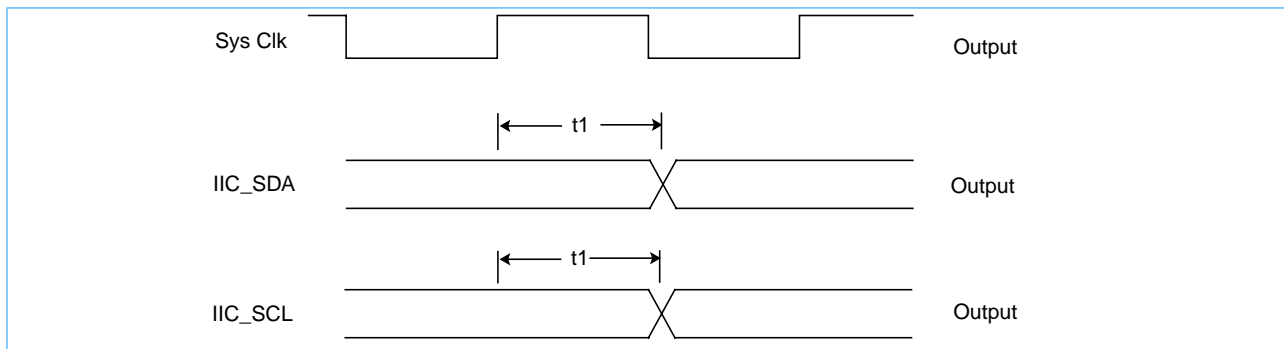
**Note:** See the table, "IEEE 1284 Mode Handshake Timing Values," on page 44 for symbol values.

### Negotiation Phase



**Note:** See the table, "IEEE 1284 Mode Handshake Timing Values," on page 44 for symbol values.

### IIC Timing

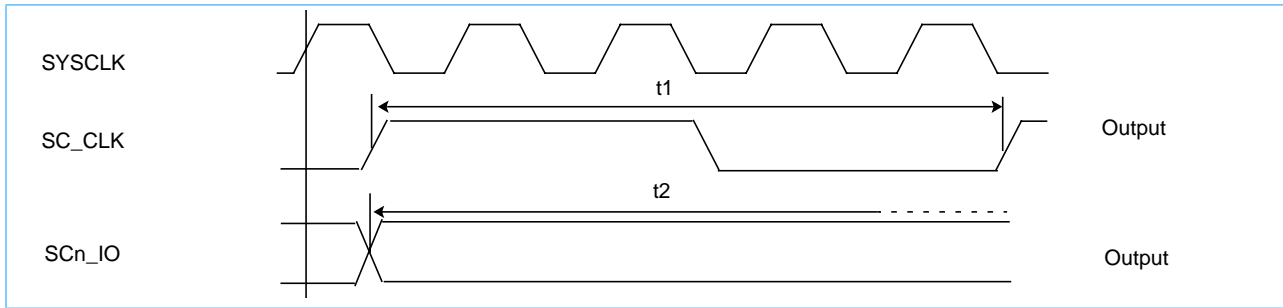


### IIC Timing Values

Symbol	Parameter	Min	Max	Units
$T_1$	Output valid time (falling edge)		15	ns

**Note:** SDA and SCL outputs are open-drain.

### Smart Card (SCI) Timing



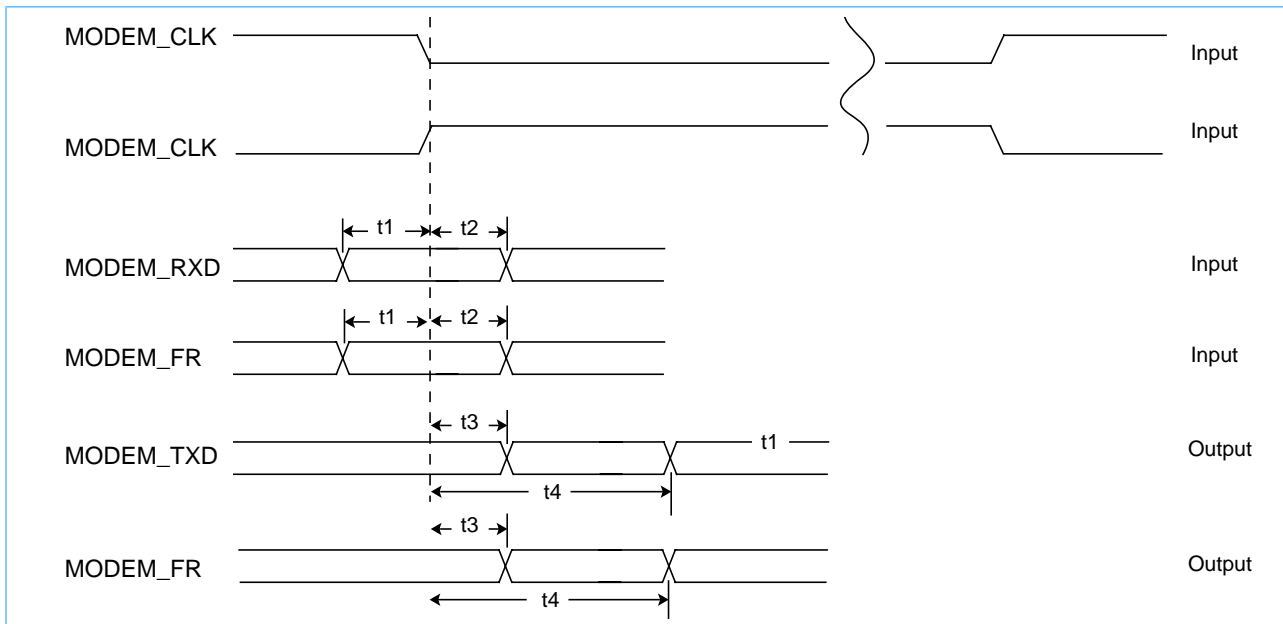
#### SCI Timing Values

$t1 = (2 \times SCCLK\_CNT0) \text{ SYSCLK periods}$

$t2 = \text{bit width} = \text{variable from 32 to 512 SC\_clk periods} = SCETU \times SC\_clk \text{ periods}$

**Note:** SC\_DETECT, SC\_RESET, SC\_SELECT, and SC\_VCC\_COMMAND are synchronous to the system clock and are not shown here.

### Modem Serial Interface Timing



#### Modem CODEC Timing Values

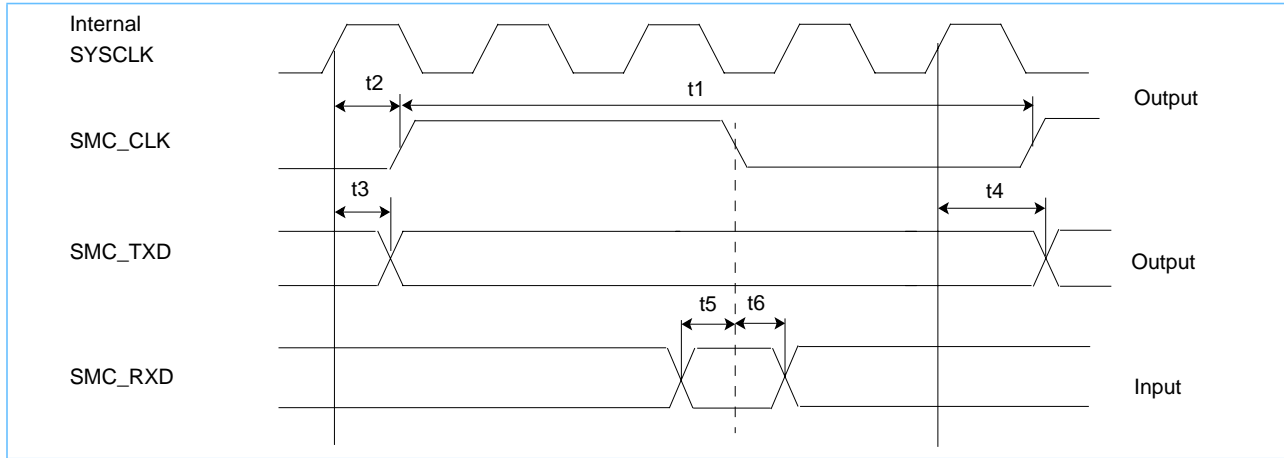
Symbol	Parameter	Min	Max	Units
$T_1$	Input setup time	15		ns
$T_2$	Input hold time	3		ns
$T_3$	Output hold time	3		ns
$T_4$	Output valid time		16	ns



**Note 1.** MODEM\_CLK can be configured to send and receive data on the rising or falling clock edge.

**Note 2.** MODEM\_FR can be an input or an output.

### Serial Control Port Timing



### SCP Timing Values

Symbol	Parameter	Min	Max	Units
$T_1$	SMC_clk period		80.8	ns
$T_2$	Output valid time		12	ns
$T_3$	Output valid time		13	ns
$T_4$	Output hold time	4		ns
$T_5$	Input setup time	10		ns
$T_6$	Input hold time	3		ns

**Note:** This timing diagram assumes the CI bit in the SCP SPMODE register is set to 0. If CI is set to 1, the LK signal is inverted.

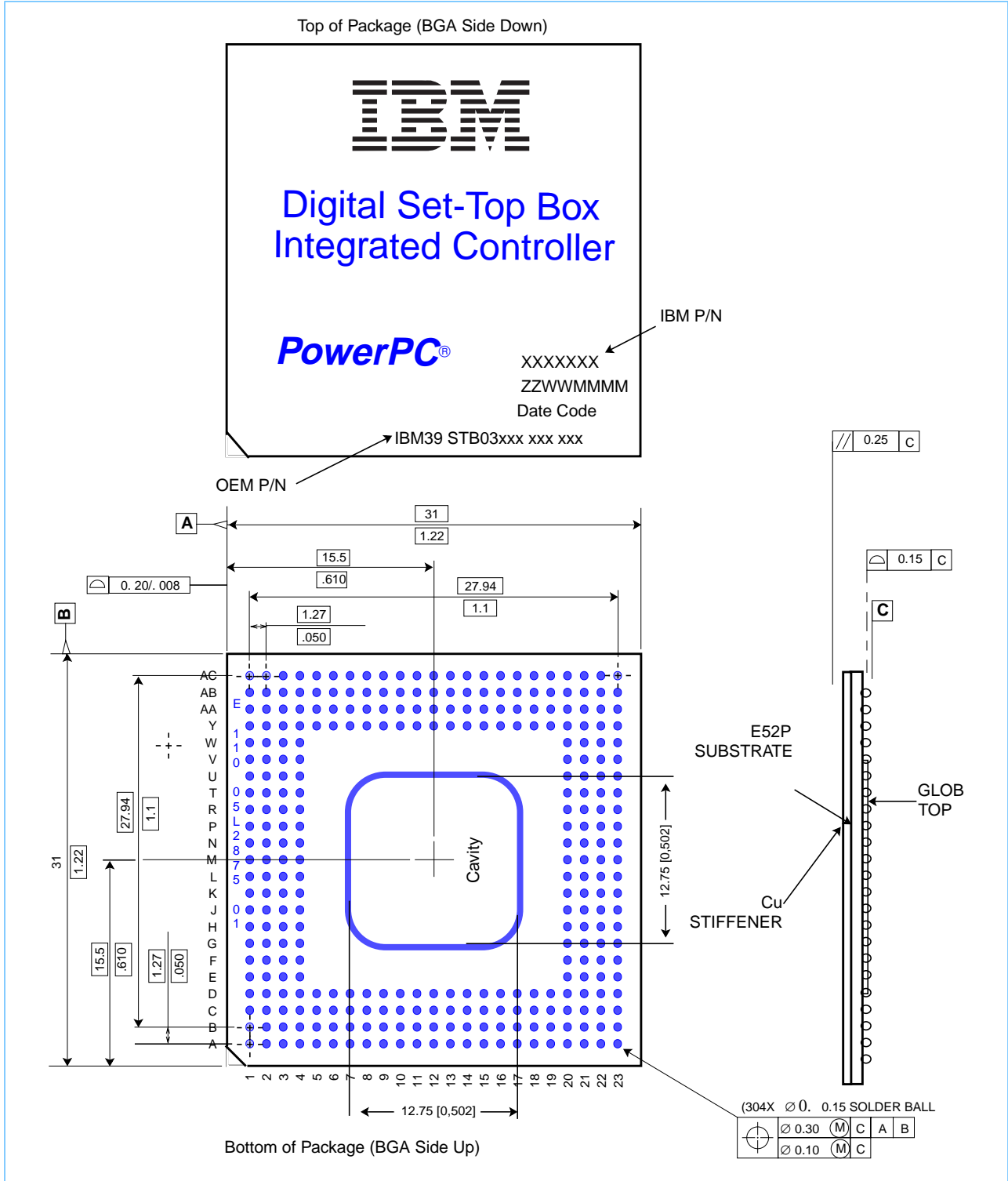
### Additional Timing Information

Interface	Timing Information
IIC	Compliant with Philips Semiconductors I <sup>2</sup> C Specification, dated 1995. Interface is asynchronous. Direct connect
Smart Card (SC)	Compatible with ISO/IEC 7816-3. Interface is asynchronous. Direct connect.
Serial0/16550	Functionally identical to National Semiconductor NS16450 in character mode (after reset). Interface is asynchronous. External transceiver logic is required.
Serial1/Infrared	Functionally identical to IBM PowerPC403™ Serial Port Unit (SPU) (after reset). Compatible with the IrDA Specification 1.1 IrDA 1.0 SIR with data rates up to 115.2 Kbps IrDA 1.1 FIR with data rates up to 1.152 Mbps Interface is asynchronous External transceiver logic is required
External Interrupts	Inputs are asynchronous
DMA	External DMA request inputs are asynchronous
GPT	Capture timer inputs are asynchronous
External Bus Master	Interface is asynchronous
RISCWatch	Compatible with IBM RISCWatch probe Direct connect to probe Contact your IBM Applications Engineer for more information
RISCTrace	Compatible with IBM RISCTrace probe Direct connect to probe Contact your IBM Applications Engineer for more information



# Mechanical Information

## Package Diagram



## Development Support

With IBM tools and the IBM PowerPC Embedded Tools Program, you receive the support you need to develop and debug your STB applications quickly.

### IBM Tools

IBM offers Windows<sup>®</sup> 95/98 – hosted development tools for STB applications that include:

- STB and processor reference design and evaluation kits, including board, compiler, debugger, ROM source, schematics, etc.
- RISCWatch debugger, with in-circuit, ROM monitor, RTOS-aware debugging and real-time non-invasive trace capability
- Metaware High C/C++ compiler, highly optimized for the PowerPC processors

### Debug

The STB03xxx facilitates development through its JTAG test access port.

With IBM RISCWatch or other third-party debugger on a workstation, you can single-step the processor and interrogate the internal processor state.

Additionally, the real-time debug port supports tracing the executed instruction stream out of the instruction cache. The trace status signals provide trace information in real-time instruction trace debug mode. This mode does not alter the performance of the processor.

### Third-Party Tool Support

Through the IBM PowerPC Embedded Tools Program, you have access to hundreds of tools offered by over 75 industry-leading vendors. Often, the tools you currently use support PowerPC embedded processor products, such as the IBM STB010XX Digital Set-Top Box Integrated Controllers. For a list of the tools that are offered, visit IBM's tool support Web page at:

<http://www.chips.ibm.com/products/powerpc/tools/>

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## Revision Log

Revision	Contents of Modification
March 23, 2000	Initial Release (revision 00).



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STB03\_sds\_0323.fm.00  
March 23, 2000