iC-DI
DUAL SENSOR INTERFACE

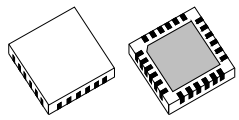
FEATURES

- Dual channel switches, configurable for high-side, low-side and push-pull operation
- Switches are current limited
- Push-pull operation with tristate function
- Output current of up to 100 mA per channel
- Parallel connection of both channels possible
- Channel 1 can be inverted (antivalent output)
- Wide supply voltage range of 9 to 30 V
- Sensor parameterisation via a feedback channel (up to 30 V)
- Switching converters and regulators for 3.3/5 V voltage generation
- Error detection with hysteresis with excessive temperature, overload and low voltage
- Driver shutdown in the event of error
- Error messaging via two open-collector outputs

APPLICATIONS

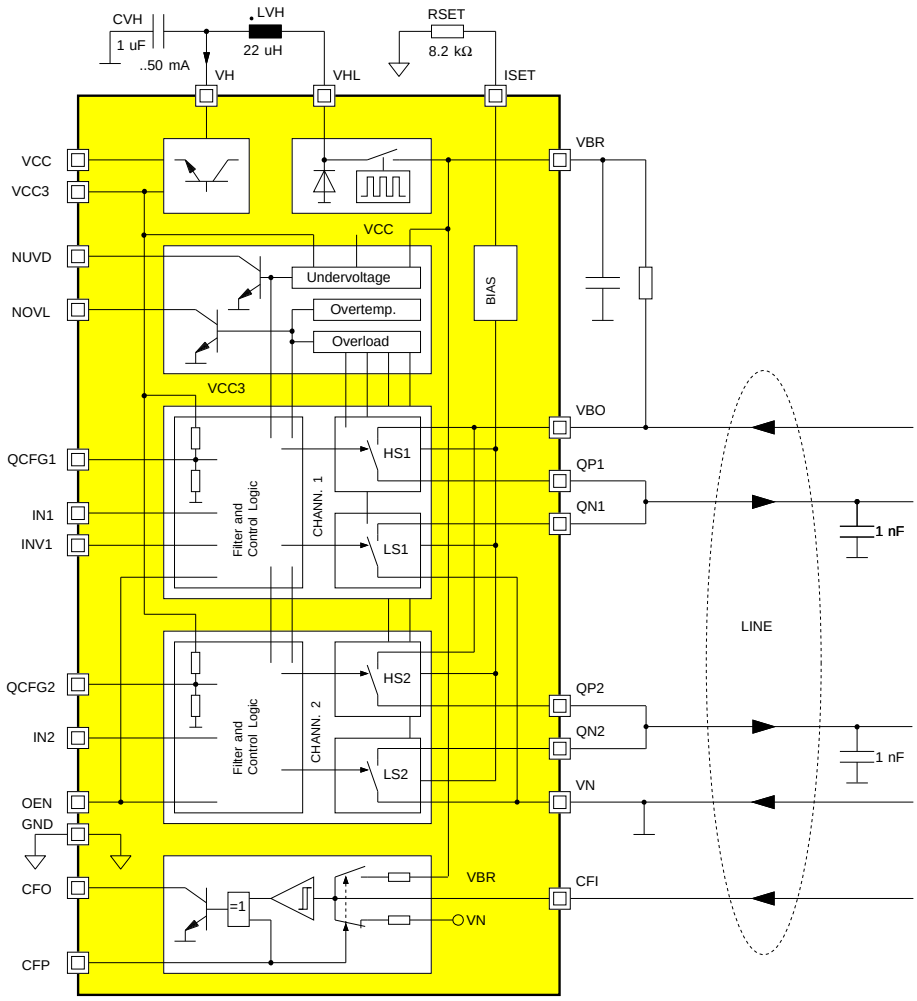
- Sensor interface for light barriers and proximity switches, for example

PACKAGES



QFN24 4 mm x 4 mm

BLOCK DIAGRAM



DESCRIPTION

iC-DI is a monolithic interface iC with two independent switching channels which enables digital sensors to drive peripheral elements, such as programmable logic controllers (PLC) and relays, for example.

The switches can be operated as push-pull, high-side or low-side switches using inputs QCFG1 and QCFG2 (open, high and low) and are enabled or disabled via input OEN. They are designed to cope with high driver currents of 100 mA (RSET = 8.2 kΩ), are current limited and also short-circuit-proof in that they shut down should excessive temperature or an overload occur. The output current limit can be set via an external resistor at ISET.

The protective overload feature is included here as an integrator so that capacitive loads with low repeat rates can be switched without the protective circuitry cutting in. In the event of excessive temperature an error message is generated immediately.

Errors are signalled by two open-collector outputs: NOVL (for excessive temperature and overloads) and NUVD (for low voltage at VBR or voltages VCC and VCC3, generated internally). The output switches are shut down with all types of error.

To avoid errors occurring when the device is switched on the outputs remain at high impedance for ca. 50 ms after the low voltage threshold has been exceeded.

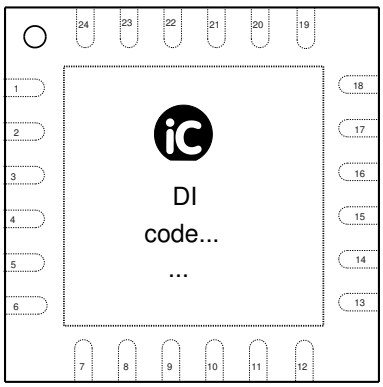
Sensor interface iC-DI has an integrated switching converter which generates voltages VCC (5 V) and VCC3 (3.3 V) with the aid of two back-end series-regulators. If only a low current is required inductor LVH may be omitted; the series regulators are then powered directly by VBR.

Input INV1 permits the input signal at channel 1 (IN1) to be inverted.

The connected sensor can be parameterised using the feedback channel with a high volt input (CFI → CFO).

PACKAGES QFN24 4 mm x 4 mm to JEDEC Standard

PIN CONFIGURATION QFN24 4 mm x 4 mm



PIN FUNCTIONS

No.	Name	Function
1	ISET	Reference Current for current limitation of driver outputs
2	INV1	Inverting Input Channel 1
3	IN1	Input Channel 1
4	QCFG1	Configuration Input Channel 1
5	QCFG2	Configuration Input Channel 2
6	IN2	Input Channel 2
7	OEN	Output Enable Input
8	NOVL	Overload Error Output
9	NUVD	Undervoltage Error Output
10	CFO	Output Feedback Channel
11	CFP	Configuration Input Feedback Channel
12	CFI	Input Feedback Channel
13	QP2	Output High Side Switch Channel 2
14	QN2	Output Low Side Switch Channel 2
15	VN	Reference Voltage Low Side Switch
16	QN1	Output Low Side Switch Channel 1
17	QP1	Output High Side Switch Channel 1
18	VBO	Reference Voltage High Side Switch
19	VBR	Power Supply switching converter and linear regulators
20	VHL	Inductor Switching Converter
21	VH	Input Linear Regulators
22	VCC	5 V Sensor Supply
23	VCC3	3.3 V Sensor Supply
24	GND	Ground

Pins GND and VN must not be externally connected, otherwise with reverse bias intolerably high current may flow!
The *Thermal Pad* is to be connected to a Ground Plane (VN) on the PCB.

Only pin 1 marking on top or bottom defines the package orientation (iC-DI label and coding is subject to change).

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed. Absolute Maximum Ratings are no Operating Conditions. Integrated circuits with system interfaces, e.g. via cable accessible pins (I/O pins, line drivers) are per principle endangered by injected interferences, which may compromise the function or durability. The robustness of the devices has to be verified by the user during system development with regards to applying standards and ensured where necessary by additional protective circuitry. By the manufacturer suggested protective circuitry is for information only and given without responsibility and has to be verified within the actual system with respect to actual interferences.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VBO	Power Supply at VBO	Referenced to lowest voltage of VN, VBR, QP1, QN1, QP2, QN2, CFI, VH, VHL Referenced to highest voltage of VN, VBR, QP1, QN1, QP2, QN2, CFI, VH, VHL	 -36	36	V V
G002	I(VBO)	Current in VBO		-10	600	mA
G003	VBR	Power Supply at VBR	Referenced to lowest voltage of VN, VBO, QP1, QN1, QP2, QN2, CFI, VH, VHL Referenced to highest voltage of VN, VBO, QP1, QN1, QP2, QN2, CFI, VH, VHL	 -36	36	V V
G004	I(VBR)	Current in VBR		-10	600	mA
G005	V(VH)	Voltage at VH	Referenced to lowest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, CFI, VHL Referenced to highest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, CFI, VHL	 -36	36	V V
G006	I(VH)	Current in VH		-5	70	mA
G007	V(VHL)	Voltage at VHL	Referenced to lowest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, CFI, VH Referenced to highest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, CFI, VH	 -36	36	V V
G008	I(VHL)	Current in VHL		-150	5	mA
G009	V(VN)	Voltage at GND vs. VN	VN < VBO VN > VBO (reverse bias)	-1 -27	3 3	V V
G010	I(VN)	Current in VN	VN < VBO VN > VBO (reverse bias)	-500 -10	500 10	mA mA
G011	I(GND)	Current in GND		-300	300	mA
G012	V()	Voltage at VCC, VCC3		-0.3	7	V
G013	I()	Current in VCC, VCC3		-50	10	mA
G014	V()	Voltage at QP1, QN1, QP2, QN2	Referenced to lowest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, CFI, VH, VHL Referenced to highest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, CFI, VH, VHL; VN < VBO, VBO < 29 V VN < VBO, VBO > 29 V VN > VBO (reverse bias)	 -7 -36 -36	36	V V V V
G015	I()	Current in QP1, QP2		-400		mA
G016	I()	Current in QN1, QN2			400	mA
G017	V(CFI)	Voltage at CFI	Referenced to lowest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, CFI, VH, VHL Referenced to highest voltage of VN, VBO, VBR, QP1, QN1, QP2, QN2, CFI, VH, VHL	 -36	36	V V
G018	I(CFI)	Current in CFI		-4	4	mA
G019	V()	Voltage at INV1, QCFG1, QCFG2, IN1, IN2, OEN, CFP		-0.3	7	V
G020	I()	Current in INV1, QCFG1, QCFG2, IN1, IN2, OEN, CFP		-4	4	mA
G021	V()	Voltage at NOVL, NUVD, CFO		-0.3	7	V
G022	I()	Current in NOVL, NUVD, CFO		-5	20	mA
G023	V(ISET)	Voltage at ISET		-0.3	7	V
G024	I(ISET)	Current in ISET		-4	4	mA
G025	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		0.6	kV
G026	Tj	Operating Junction Temperature		-40	150	°C

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

ABSOLUTE MAXIMUM RATINGS (cont'd)

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G027	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions:
VBO = 9...30 V, VBR = 9...30 V (both referenced to VN), Tj = -40...125 °C, RSET = 8.2 kΩ ±1%, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended range on request)		-40		85	°C
T02	Rthja	Thermal Resistance Chip/Ambient	Surface mounted, thermal pad soldered to ca. 2 cm² heat sink		30	40	K/W

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions:
VBO = 9...30 V, VBR = 9...30 V (both referenced to VN), Tj = -40...125 °C, RSET = 8.2 kΩ ±1%, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VBO	Permissible Supply Voltage	Referenced to VN	9	24	30	V
002	I(VBO)	Supply Current in VBO	No load, I(QP1) = I(QP2) = 0, HSx switched on			0.3	mA
003	VBR	Permissible Supply Voltage		9	24	30	V
004	I(VBR)	Supply Current in VBR	VH connected to VBR, no load, I(VCC) = I(VCC3) = 0, V(OEN) = hi			6	mA
005	Vc()hi	Clamp Voltage hi at VBO, VBR vs. VN	I() = 10 mA	36			V
006	Vc()lo	Clamp Voltage lo at VBO, VBR vs. VN	I() = -10 mA			-36	V
007	Vc()hi	Clamp Voltage hi at QN1, QN2 vs. VN	I() = 1 mA, VBO and VBR > VN	36		39	V
008	Vc()lo	Clamp Voltage lo at QP1, QP2 vs. VN	I() = -1 mA, VBO and VBR > VN	-9		-6	V
009	Vc(CFI)hi	Clamp Voltage hi at CFI vs. VN	I() = 1 mA	36			V
010	Vc(CFI)lo	Clamp Voltage lo at CFI vs. VN	I() = -1 mA			-36	V
011	Vc(VN)hi	Clamp Voltage hi at VN vs. lowest voltage of QP1, QN1, QP2, QN1, CFI	I() = 1 mA	36			V
012	Vc()hi	Clamp Voltage hi at VH, VHL	I() = 1 mA	36			V
013	Vc()lo	Clamp Voltage lo at VH, VHL	I() = -1 mA			-36	V
014	Vc()hi	Clamp Voltage hi at VCC, VCC3, ISET, INV1, IN1, IN2, QCFG1, QCFG2, OEN, CFO, CFP, NOVL, NUVD	I() = 1 mA	7			V
015	Vc()lo	Clamp Voltage lo at VCC, VCC3, ISET, INV1, IN1, IN2, QCFG1, QCFG2, OEN, CFO, CFP, NOVL, NUVD	I() = -1 mA			-0.5	V
016	tpio	Propagation Delay IN1 → QP1, QN1 IN2 → QP2, QN2		2.4		11	µs
017	R(GND)off	Resistance of GND switch	VBO < VN (reverse bias)	10			kΩ
018	R(GND)on	Resistance of GND switch	VBO > VN; V(GND) < VN + 0.6V			20	Ω
Low-Side Switch QN1, QN2; V(QCFG1) = V(QCFG2) = 0 V							
101	Vs()lo	Saturation Voltage lo at QN1, QN2 vs. VN	RSET = 5.1 kΩ; I() = 100 mA I() = 50 mA I() = 10 mA			 1.5 1 0.3	 V V V
102	Isc()lo	Short-Circuit Current lo in QN1, QN2	RSET = 8.2 kΩ, V() = 1.4 V...VBO	100	125	160	mA
103	Vol()on	Overload Detection Threshold on	QN1, QN2 lo → hi; referenced to GND	1.55		2.1	V
104	Vol()off	Overload Detection Threshold off	QN1, QN2 hi → lo; referenced to GND	1.5		1.8	V
105	Vol()hys	Overload Detection Threshold Hysteresis	Vol()hys = Vol()on − Vol()off	0.1			V
106	Ilk()	Leakage Current at QN1, QN2	OEN = lo; V(QN1, QN2) = VBO...VBO + 6 V V(QN1, QN2) = 0...VBO V(QN1, QN2) = -6...0 V	 0 0 -500		 50 50 0	 µA µA µA
107	SR()	Slew Rate (switch off → on)	VBO = 30 V, Cl = 2.2 nF			45	V/µs
108	Imax()	Maximum Current in QN1, QN2	V(ISET) = 0 V, QNx > 3 V	195	300	450	mA
109	Ir()	Reverse Current in QN1, QN2	QNx activated; V(QNx) = -6 V	-10			mA

ELECTRICAL CHARACTERISTICS

Operating Conditions:
VBO = 9...30 V, VBR = 9...30 V (both referenced to VN), Tj = -40...125 °C, RSET = 8.2 kΩ ±1%, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
High-Side Switch QP1, QP2; V(QCFG1) = V(QCFG2) = 5 V							
201	Vs()hi	Saturation Voltage hi vs. VBO	RSET = 5.1 kΩ; I() = -100 mA I() = -50 mA I() = -10 mA	 -1.2 -0.7 -0.3			 V V V
202	Isc()hi	Short-Circuit Current hi	RSET = 8.2 kΩ, V() = 0...VBO − 1.5 V	-160	-125	-100	mA
203	Vol()on	Overload Detection Threshold on	QP1, QP2 hi → lo; referenced to VBO	-2.1		-1.5	V
204	Vol()off	Overload Detection Threshold off	QP1, QP2 lo → hi; referenced to VBO	-1.8		-1.4	V
205	Vol()hys	Overload Detection Threshold Hysteresis	Vol()hys = Vol()off − Vol()on	0.1			V
206	Ilk()	Leakage Current at QP1, QP2	OEN = lo; V(QP1, QP2) = -6...0 V V(QP1, QP2) = 0 V...VBO V(QP1, QP2) > VBO...VBO + 6 V	 -500 -40 0		 0 0 500	 µA µA µA
207	SR()	Slew Rate (switch off → on)	VBO = 30 V, Cl = 2.2 nF			40	V/µs
208	Imax()	Maximum Current in QP1, QP2	V(ISET) = 0 V, VBO − QPx > 4 V	-630	-450	-350	mA
209	Ir()	Reverse Current in QP1, QP2	QPx activated; V(QPx) = VBO...VBO + 6 V			1	mA
Short-Circuit/Overload Monitor							
301	toldly	Time to Overload Message (NOVL 1 → 0, switch tri-state)	Permanent overload (see Fig. 1)	126	180	280	µs
302	tolcl	Time to Overload Message Reset (NOVL 0 → 1, switch active)	No overload (see Fig. 2)	35	50	80	ms
VBR Voltage Monitor							
401	VBRon	Turn-On Threshold VBR	Referenced to GND	8		9	V
402	VBRoff	Turn-Off Threshold VBR	Decreasing voltage VBR	7.3		8.5	V
403	VBRhys	Hysteresis	VBRhys = VBRon − VBRoff	200	500		mV
404	tuvdly	Time to Undervoltage Message (NUVD 1 → 0, switch tri-state)	Permanent undervoltage at VBR, VCC or VCC3	15		100	µs
405	tuvcl	Time to Undervoltage Message Reset (NUVD 0 → 1, switch active)	No undervoltage at VBR, VCC and VCC3 (see Fig. 1)	35	50	80	ms
Temperature Monitor							
501	Toff	Overtemperature Shutdown (NOVL 1 → 0, switch tri-state)	Increasing temperature Tj	130		155	°C
502	ton	Overtemperature Shutdown Reset Delay (NOVL 0 → 1, switch active)	Temperature Tj < Toff	35	50	80	ms
Inputs IN1, IN2, INV1, QCFG1, QCFG2, OEN							
601	Vt()hi	Input Threshold Voltage hi at IN1, IN2, INV1, OEN				2	V
602	Vt()lo	Input Threshold Voltage lo at IN1, IN2, INV1, OEN		0.8			V
603	Vt()hys	Hysteresis at IN1, IN2, INV1, OEN	Vt()hys = Vt()hi − Vt()lo	300	500		mV
604	Ipd()	Pull-Down Current at IN1, IN2, INV1	V() = 0.4 V...Vt()lo V() > Vt()hi	30 10		168 40	µA µA
605	Ipd(OEN)	Pull-Down Current at OEN	V(OEN) > 0.4 V	1		6	µA
606	Vahi()	Input Threshold hi at QCFG1, QCFG2 (V() > Va()hi ⇒ QN1, QN2 tri-state)	Referenced to VCC3 (see Fig. 3)	52	64	69	%
607	Vahi()hys	Hysteresis hi at QCFG1, QCFG2 (V() < Vahi() − Vahi()hys ⇒ QN1, QN2 active)	Referenced to VCC3 (see Fig. 3)	3		7	%

ELECTRICAL CHARACTERISTICS

Operating Conditions:
VBO = 9...30 V, VBR = 9...30 V (both referenced to VN), Tj = -40...125 °C, RSET = 8.2 kΩ ±1%, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
608	Valo()	Input Threshold lo at QCFG1, QCFG2 (V() < Va()lo ⇒ QP1, QP2 tri-state)	Referenced to VCC3 (see Fig. 3)	24	29	34	%
609	Valo()hys	Hysteresis lo at QCFG1, QCFG2 (V() > Valo() + Valo()hys ⇒ QN1, QN2 active)	Referenced to VCC3 (see Fig. 3)	3		7	%
610	Vpp()	Open Circuit Voltage at QCFG1, QCFG2	Referenced to VCC3	42	46.5	51	%
611	Ri()	Internal Resistance at QCFG1, QCFG2		40	85	190	kΩ
612	tsup	Permissible Spurious Pulse Width at IN1, IN2, INV1, OEN	No activity triggered			2.2	µs
613	ttrig	Required Pulse Width at IN1, IN2, INV1, OEN	Activity triggered	7			µs
614	tsup	Permissible Spurious Pulse Width at QCFG1, QCFG2	No activity triggered			4.5	µs
615	ttrig	Required Pulse Width at QCFG1, QCFG2	Activity triggered	14			µs
Error Output NOVL, NUVD							
701	Vs()lo	Saturation Voltage lo	I() = 1.0 mA			0.4	V
702	Isc()lo	Short Circuit Current lo	V() = 0.4 V...VCC	1.2		25	mA
703	Ilk()	Leakage Current	V() = 0 V...VCC, no error	-10		10	µA
Feedback Channel CFI to CFO							
801	Vt1(CFI)hi	Input Threshold 1 hi at CFI	VBR < 18 V	59	66	74	%VBR
802	Vt1(CFI)lo	Input Threshold 1 lo at CFI	VBR < 18 V	44	50	56	%VBR
803	Vt2(CFI)hi	Input Threshold 2 hi at CFI	VBR > 18 V	10.5	11.3	12	V
804	Vt2(CFI)lo	Input Threshold 2 lo at CFI	VBR > 18 V	8	9	10.5	V
805	Vt()hys	Hysteresis at CFI	Vt(CFI)hys = Vt(CFI)hi − Vt(CFI)lo	1			V
806	Ipu(CFI)	Pull-Up Current at CFI	CFP = hi, V(CFI) = 0...VBR − 3 V, V(CFI) > Vt(CFI)lo	-300		-40	µA
807	Ipd(CFI)	Pull-Down Current at CFI	CFP = lo, V(CFI) = 3 V...VBR, V(CFI) < Vt(CFI)lo	40		300	µA
808	tpcf	Propagation Delay CFI → CFO	V(CFO) = 10 ↔ 90%VCC	2.4		11	µs
809	Vs()lo	Saturation Voltage lo at CFO	I(CFO) = 1.2 mA			0.4	V
810	Isc()lo	Short Circuit Current lo in CFO	V(CFO) = 0.4 V...VCC	1.2		25	mA
811	Ilk()	Leakage Current at CFO	V(CFO) = 0 V...VCC, CFO inaktive	-10		10	µA
812	Vt()hi	Input Threshold Voltage hi at CFP				2	V
813	Vt()lo	Input Threshold Voltage lo at CFP		0.8			V
814	Vt()hys	Hysteresis at CFP	Vt(CFP)hys = Vt(CFP)hi − Vt(CFP)lo	300	500		mV
815	Ipd(CFP)	Pull-Down Current at CFP	V(CFP) = 0.4 V...Vt(CFP)lo V(CFP) > Vt(CFP)hi	30 10		168 40	µA µA
816	tsup	Permissible Spurious Pulse Width at CFI	No activity triggered			2.2	µs
817	ttrig	Required Pulse Width at CFI	Activity triggered	7			µs
818	tsup	Permissible Spurious Pulse Width at CFP	No activity triggered			4.5	µs
819	ttrig	Required Pulse Width at CFP	Activity triggered	14			µs
820	Ipd(CFI)+ Ilk(QPx)	Pull-Down Current at CFI plus leakage current at QPx	CFP = lo, V(CFI) = 3 V...VBR, OEN = lo	20			µA
Switching Regulator VHL, VH							
901	VHn	Nominal Voltage at VH	LVH = 22 µH, Ri(LVH) < 1.1 Ω, CVH = 1 µF; I(VH) = 0...50 mA	6.4		7.7	V

ELECTRICAL CHARACTERISTICS

Operating Conditions:
VBO = 9...30 V, VBR = 9...30 V (both referenced to VN), Tj = -40...125 °C, RSET = 8.2 kΩ ±1%, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
902	Ia(VHL)	max. DC Cut-Off Current from VHL		-200			mA
903	Va(VH)	Cut-Off Voltage at VH	Va(VH) > VHn	6.5	7.3	7.7	V
904	Va()hys	Hysteresis at VH		10	25	150	mV
905	Vs(VHL)	Saturation Voltage at VHL vs. VBR	I(VHL) = -50 mA I(VHL) = -150 mA			1.1 3.0	V V
906	Vf(VHL)	Forward Voltage of Fly-Back Diode	Vf() = V(GND) − V(VHL); I(VHL) = -50 mA I(VHL) = -150 mA			 1.5 2.9	 V V
907	Ilk(VHL)	Leakage Current at VHL	VHL = lo, V(VHL) = V(VH)	-20		20	µA
908	ηVH	Efficiency of VH-switching regulator	I(VH) = 50 mA, Ri(LVH) < 1.1 Ω, V(VBR) = 12...30 V	70			%
Series Regulator VCC							
A01	VCCn	Nominal Voltage at VCC	I(VCC) = -50...0 mA, VH = VHn	4.75	5	5.25	V
A02	CVCC	Required Capacitor at VCC vs. GND		150			nF
A03	RiCVCC	Maximum Permissible Internal Resisitance of capacitor at VCC				1	Ω
A04	VCCon	VCC Monitor Threshold hi		90		99	%VCCn
A05	VCCoff	VCC Monitor Threshold lo	Decreasing Voltage at VCC	83		95	%VCCn
A06	VCChys	Hysteresis	VCChys = VCCon − VCCoff	50	150		mV
Series Regulator VCC3							
B01	VCC3n	Nominal Voltage at VCC3	I(VCC3) = -50...0 mA, VH = VHn	3.1	3.3	3.5	V
B02	CVCC3	Required Capacitor at VCC3 vs. GND		150			nF
B03	RiCVCC3	Maximum Permissible Internal Resisitance of capacitor at VCC3				1	Ω
B04	VCC3on	VCC3 Monitor Threshold hi		90		98	% VCC3n
B05	VCC3off	VCC3 Monitor Threshold lo	Decreasing Voltage at VCC3	83		95	% VCC3n
B06	VCC3hys	Hysteresis	VCC3hys = VCC3on − VCC3off	50	150		mV
Oscillator							
C01	fos	Oscillator Frequency	 Tj = 27 °C	1.2 1.5	2	2.75 2.3	MHz MHz
Reference and Bias							
D01	V(ISET)	Voltage at ISET	Tj = 27 °C	1.16	1.22	1.28	V
D02	I(ISET)	Current in ISET	V(ISET) = 0 V, Tj = 27 °C	-1.1	-0.65	-0.25	mA
D03	rIbeg	Transmission Ratio for driver output current limitation	Imax(QP1) = Imax(QP2) = Imax(QN1) = Imax(QN2) = I(ISET) ∗ rIbeg, RSET = 5.1...20 kΩ		800		

DESCRIPTION OF FUNCTIONS

Overload detection

To protect the device against excessive power dissipation due to high currents the switches are clocked if an overload occurs. If a short circuit is detected, i.e. if the voltage at the switch output overshoots or undershoots *Overload Detection Threshold off* (cf. Electrical Characteristics Nos. 104 and 204), the switches are shut down for a typical 50 ms (cf. Electrical Characteristics No. 302) and the current flow thus interrupted.

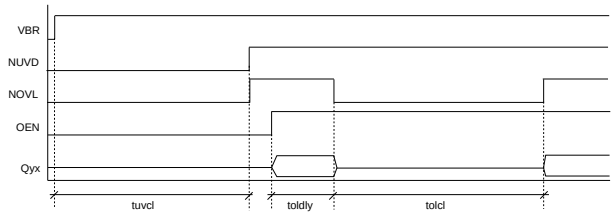


Figure 1: Permanent short circuit

The level of power dissipation is dependent on the current and the time during which this current flows. A current which fails to trigger the overload detection is not critical; high current can also be tolerated for a short period and with low repeat rates. This is particularly important when switching capacitive loads (charge/discharge currents).

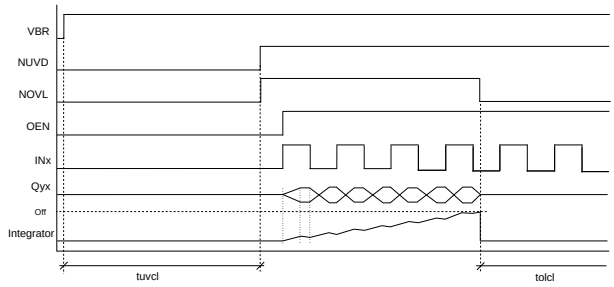


Figure 2: Overload

So that this is possible a shared back-end integrator follows the switches for the purpose of overload detection. This integrator is an 8-bit counter which is updated together with the oscillator clock. If an overload is detected on one channel the counter is raised by 1; an overload on both channels increases the counter value by 2. If no overload is apparent the counter is reduced by 1 every 10 clock pulses. Provided that the time during which excessive current flows does not exceed the value stipulated by Electrical Characteristics No. 301, a maximum duty cycle – without deactivation of the switches – of 1:10 results if one channel is overloaded; if both channels signal an overload this changes to 1:5. Only when these ratios are exceeded can the counter achieve its maximum value, this then generating an error message at NOVL and deactivating the switches.

Configuring the switches

The various functions of the switches are determined by pins QCFG1 and QCFG2. A voltage at the QCFG pins which is lower than Va()lo deactivates the relevant high-side switches; with a voltage higher than Va()hi the relevant low-side switches are deactivated. Both high-side and low-side switches are activated in the open-circuit voltage range (pin open).

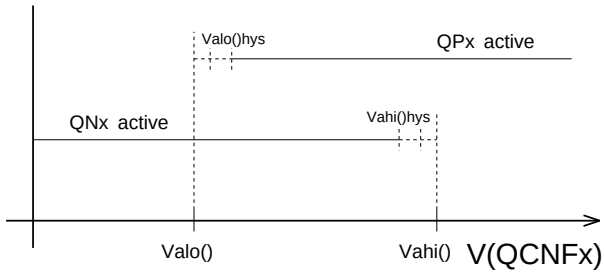


Figure 3: Levels at QCFG1/QCFG2 and switch activation

Pull-up and pull-down currents

The pull-down currents at pins IN1, IN2, INV1 and CFP are two-stage with switching thresholds Vt()hi and Vt()lo (cf. Electrical Characteristics Nos. 604 and 815).

Function tables

CHANNEL 1					
IN1	QCFG1	INV	OEN	QN1	QP1
X	X	X	L	off	off
L	Z	L	H	on	off
H	Z	L	H	off	on
L	Z	H	H	off	on
H	Z	H	H	on	off
L	H	L	H	off	off
H	H	L	H	off	on
L	H	H	H	off	on
H	H	H	H	off	off
L	L	L	H	off	off
H	L	L	H	on	off
L	L	H	H	on	off
H	L	H	H	off	off

Table 1: Function table Channel 1

CHANNEL 2				
IN2	QCFG2	OEN	QN2	QP2
X	X	L	off	off
L	Z	H	on	off
H	Z	H	off	on
L	H	H	off	off
H	H	H	off	on
L	L	H	off	off
H	L	H	on	off

Table 2: Function table Channel 2

FEEDBACK CHANNEL		
CFI	CFP	CFO
H	H	Z
H	L	L
L	H	L
L	L	Z

Table 3: Function table Feedback Channel

APPLICATION NOTES

Figure 4 shows recommended protective circuitry against reverse bias and transients on the transmission line; suggested values as follows:

CQx:	22 nF
CVB:	1 µF
CVBO:	100 nF

DQx, DVBO: *High speed* diodes (eg. BAS16)

DVN:	*General purpose* diode, high reverse voltage
RCFI:	50 Ω
RQxx:	5 Ω
RVB:	> 20 Ω

Pins GND and VN must not be externally connected, otherwise with reverse bias intolerably high current may flow!

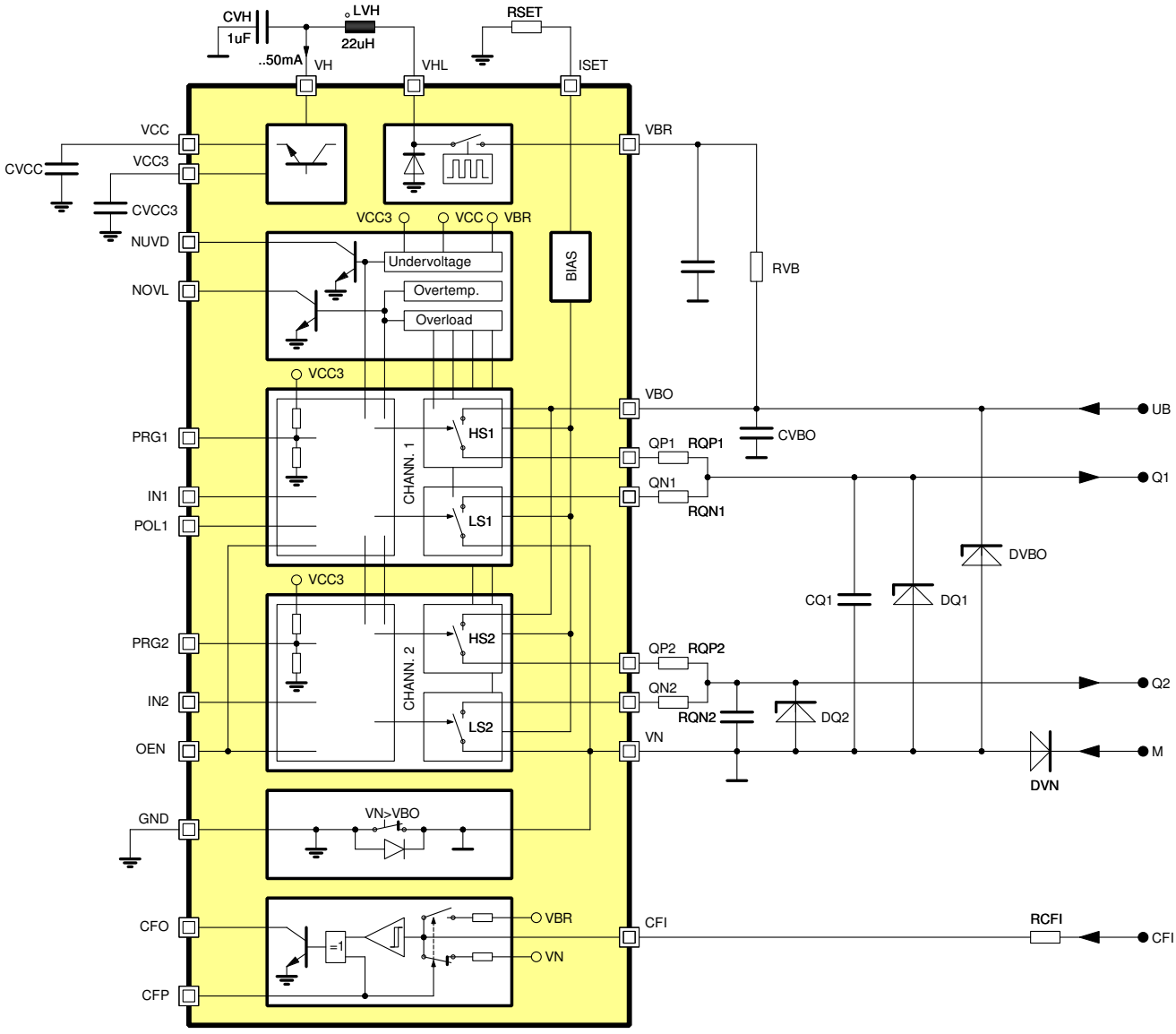


Figure 4: Recommended external protective circuitry for differential push-pull operation

DEMO BOARD

iC-DL comes with a demo board for test purposes. Figures 5 and 6 show both the schematic and the component side of the demo board.

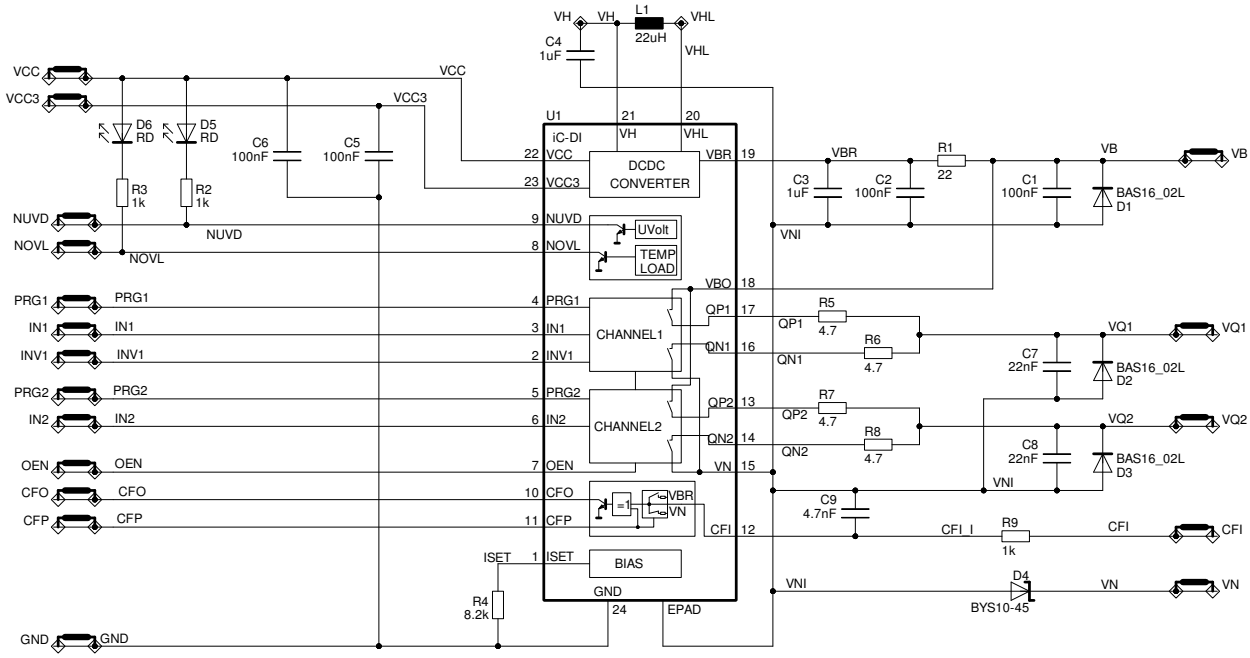


Figure 5: Schematic of the demo board

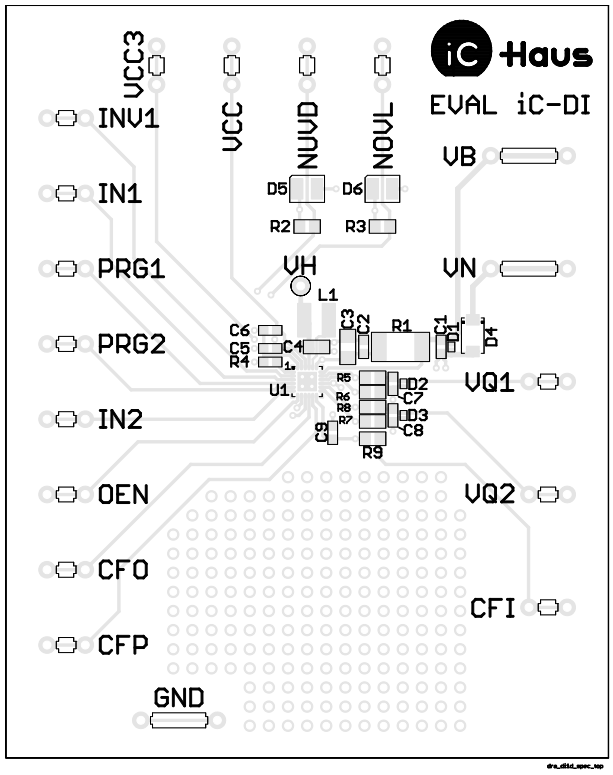


Figure 6: Demo board (component side)

ORDERING INFORMATION

Type	Package	Order Designation
iC-DI	QFN24 4 x 4 mm² Evaluation Board	iC-DI QFN24 iC-DI EVAL DI1D

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (61 35) 92 92-0
Fax: +49 (61 35) 92 92-192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

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