iC149

PROGRAMMABLE ns-PULSE GENERATOR

preliminary

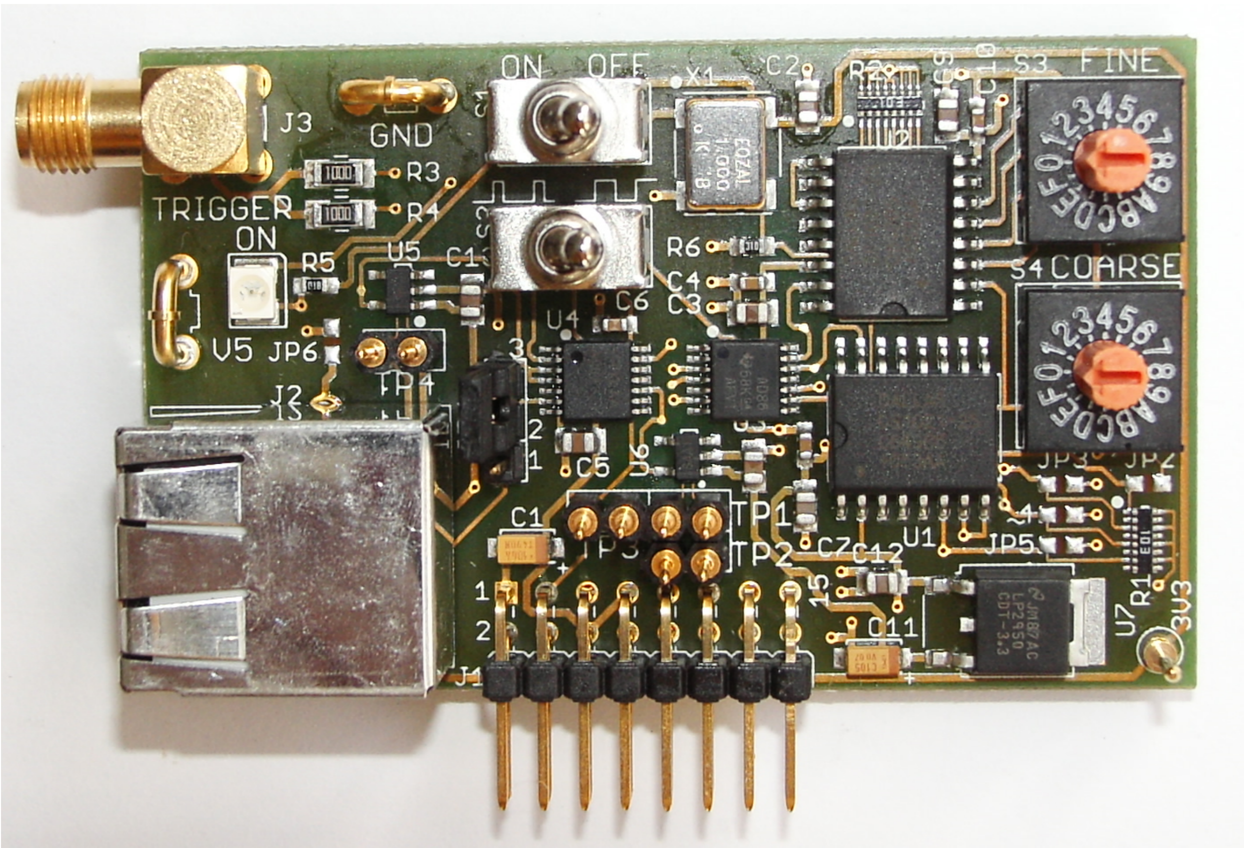
FEATURES

Pulse width 1 bis 64 ns in steps of 0.25 ns
Fixed frequency of 1 MHz
LVDS und TTL outputs
Compatible with HG1D, NZN1D, NZP1D

APPLICATIONS

Pulse generator for fast laser diode drivers

BLOCK DIAGRAM



DESCRIPTION

Pulse generator iC149 produces pulses with a small duty cycle in the range of ca. 1 ns up to 64 ns max. in steps of 0.25 ns at a pulse frequency of 1 MHz. The pulse width is set by means of two hexadecimal coding switches in coarse and fine steps.

The pulses are output both as LVDS and TTL signals.

This module can easily be used with the evaluation boards HG1D, NZN1D ans NZP1D.

ELECTRICAL CHARACTERISTICS

Test Conditions: Vs = ±15 V, Ta = 25 °C, System Impedace 50 Ω

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supply							
101	V5	Power Supply		4.75	5	5.25	V
102	I(V5)	Supply Current	V5 = 5 V, S1 = OFF V5 = 5 V, S1 = ON, TRIGGER open V5 = 5 V, S1 = ON, TRIGGER 50 Ω vs. Ground		45 50 75		mA mA mA
Pulse Width							
201	Tp_{max}	Maximum Pulsweite	V5 = 5 V, Ta = 27 °C, *coarse* = "F", *fine* = "F"		63.75		ns
202	Tp_{min}	Minimum Pulsweite	V5 = 5 V, Ta = 27 °C, *coarse* = "0", *fine* = "C"		1		ns

SETTING THE PULSE WIDTH

Typical pulse widths as follows (measured values in parentheses):

m = 15	ΔT = 15 * 4 ns = 60 ns	(60.2 ns)
m = 14	ΔT = 14 * 4 ns = 56 ns	(56.4 ns)
m = 13	ΔT = 13 * 4 ns = 52 ns	(52.3 ns)
m = 12	ΔT = 12 * 4 ns = 48 ns	(48.7 ns)
m = 11	ΔT = 11 * 4 ns = 44 ns	(44.7 ns)
m = 10	ΔT = 10 * 4 ns = 40 ns	(40.9 ns)
m = 9	ΔT = 9 * 4 ns = 36 ns	(36.7 ns)
m = 8	ΔT = 8 * 4 ns = 32 ns	(32.6 ns)
m = 7	ΔT = 7 * 4 ns = 28 ns	(28.7 ns)
m = 6	ΔT = 6 * 4 ns = 24 ns	(24.7 ns)
m = 5	ΔT = 5 * 4 ns = 20 ns	(20.2 ns)
m = 4	ΔT = 4 * 4 ns = 16 ns	(15.7 ns)
m = 3	ΔT = 3 * 4 ns = 12 ns	(12.4 ns)
m = 2	ΔT = 2 * 4 ns = 8 ns	(7.5 ns)
m = 1	ΔT = 1 * 4 ns = 4 ns	(3.0 ns)

Table 2: m = 1...15 (*coarse*), n = 0 (*fine*)

n = 15	ΔT = 4 ns + 15 * 0.25 ns = 7.75 ns	(7.2 ns)
n = 14	ΔT = 4 ns + 14 * 0.25 ns = 7.50 ns	(6.8 ns)
n = 13	ΔT = 4 ns + 13 * 0.25 ns = 7.25 ns	(6.5 ns)
n = 12	ΔT = 4 ns + 12 * 0.25 ns = 7.00 ns	(6.2 ns)
n = 11	ΔT = 4 ns + 11 * 0.25 ns = 6.75 ns	(6.0 ns)
n = 10	ΔT = 4 ns + 10 * 0.25 ns = 6.50 ns	(5.8 ns)
n = 9	ΔT = 4 ns + 9 * 0.25 ns = 6.25 ns	(5.5 ns)
n = 8	ΔT = 4 ns + 8 * 0.25 ns = 6.00 ns	(4.9 ns)
n = 7	ΔT = 4 ns + 7 * 0.25 ns = 5.75 ns	(4.5 ns)
n = 6	ΔT = 4 ns + 6 * 0.25 ns = 5.50 ns	(4.4 ns)
n = 5	ΔT = 4 ns + 5 * 0.25 ns = 5.25 ns	(4.3 ns)
n = 4	ΔT = 4 ns + 4 * 0.25 ns = 5.00 ns	(4.1 ns)
n = 3	ΔT = 4 ns + 3 * 0.25 ns = 4.75 ns	(3.9 ns)
n = 2	ΔT = 4 ns + 2 * 0.25 ns = 4.50 ns	(3.5 ns)
n = 1	ΔT = 4 ns + 1 * 0.25 ns = 4.25 ns	(3.2 ns)
n = 0	ΔT = 4 ns + 0 * 0.25 ns = 4.00 ns	(3.0 ns)

Table 3: m = 1 (*coarse*), n = 1...15 (*fine*)

n = 15	ΔT = 2.8 ns ±0.4ns	(2.8 ns)
n = 14	ΔT = 2.5 ns ±0.4ns	(2.6 ns)
n = 13	ΔT = 2.2 ns ±0.4ns	(2.1 ns)
n = 12	ΔT = 1.0 ns ±0.4ns	(1.1 ns)
n < 12	ΔT = 0.0 ns	

Table 4: m = 0 (*coarse*) und n $\geq$ 12 (*fine*)

Formula to calculate the pulse width:

$$\Delta T = (m * 4\,ns + n * 0.25\,ns) \pm 2\,ns$$

$1 \leq$ m (coarse) $\leq$ 15,
$0 \leq$ n (fine)) $\leq$ 15,
m = 0 s. Tab. 4

PIN CONFIGURATION

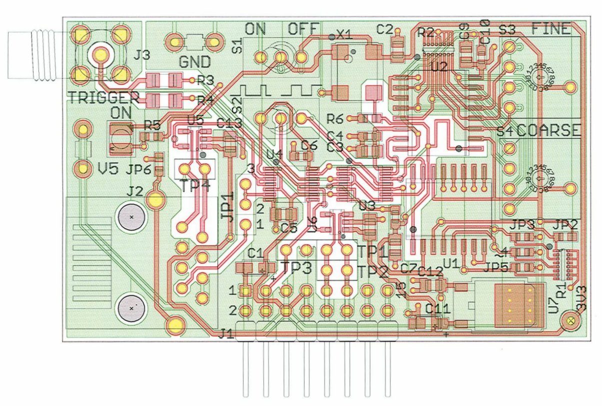


Figure 1: The populated PCB

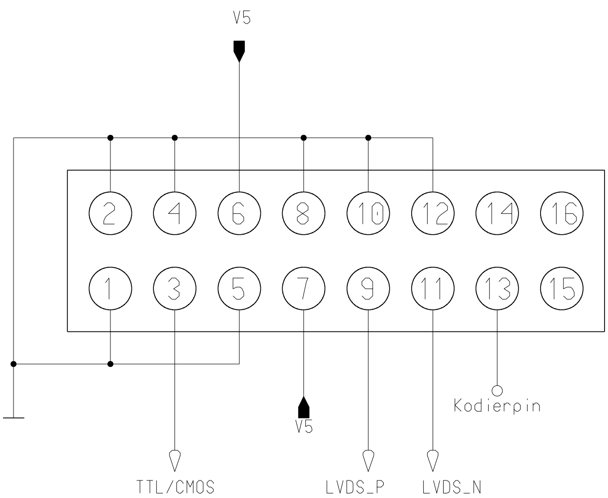


Figure 2: Pin configuration J1

J1	16 pole pin header for power supply and signal outputs
J2	RJ45 connector for output signals with LVDS or TTL/CMOS levels
J3	TRIGGER: SMA connector for trigger output, Rout = 50 Ω
JP1	Jumper at position 1-2 selects TTL/CMOS signals for J2
S1	Oscillator ON/OFF
S2	Selector switch: programmable pulse or symmetrical 1 MHz signal
S3	Coding switch *fine*
S4	Coding switch *coarse*
TP1	LVDS signal at J1 (must be terminated with 100 Ω for measurement purpose)
TP2	LVDS signal at J1
TP3	TTL/CMOS signal at J1
TP4	LVDS signal at J2
GND	GND
V5	V5
3V3	3.3 V

Table 5: Connectors on the PCB

SAMPLE PULSES

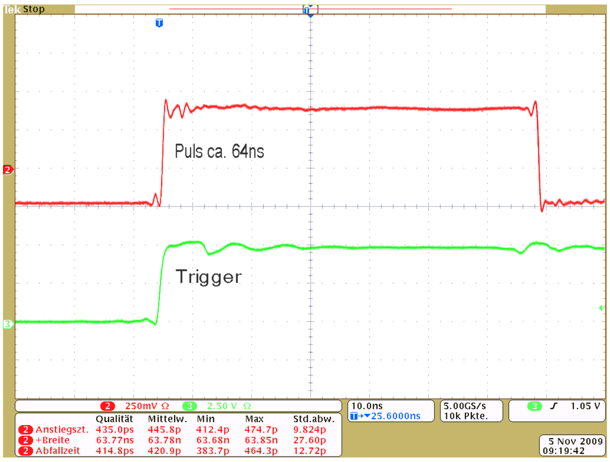


Figure 3: Maximum pulse width

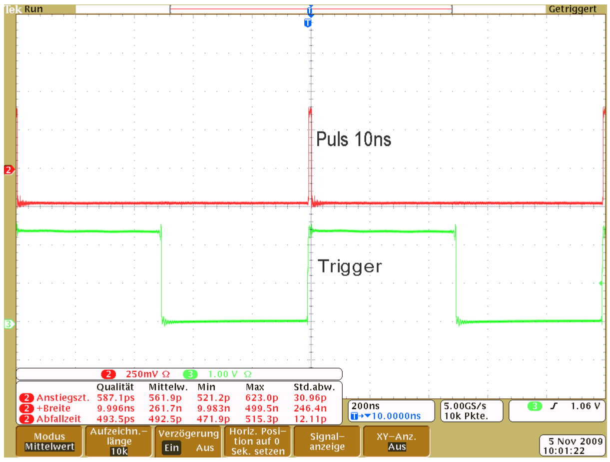


Figure 5: Trigger and LVDS pulse

Figure 4: Minimum pulse width

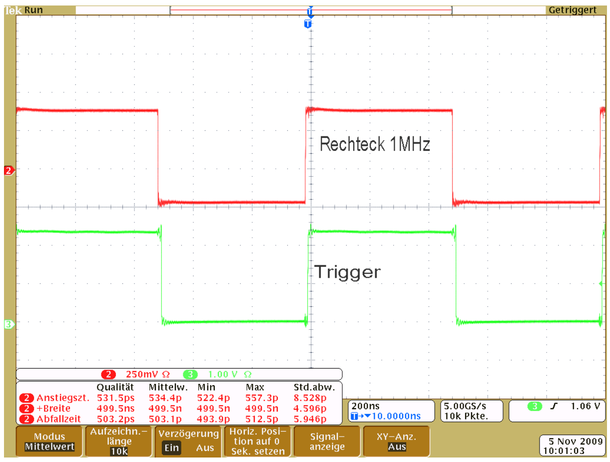


Figure 6: Trigger and 1 MHz LVDS signal

BLOCK DIAGRAM

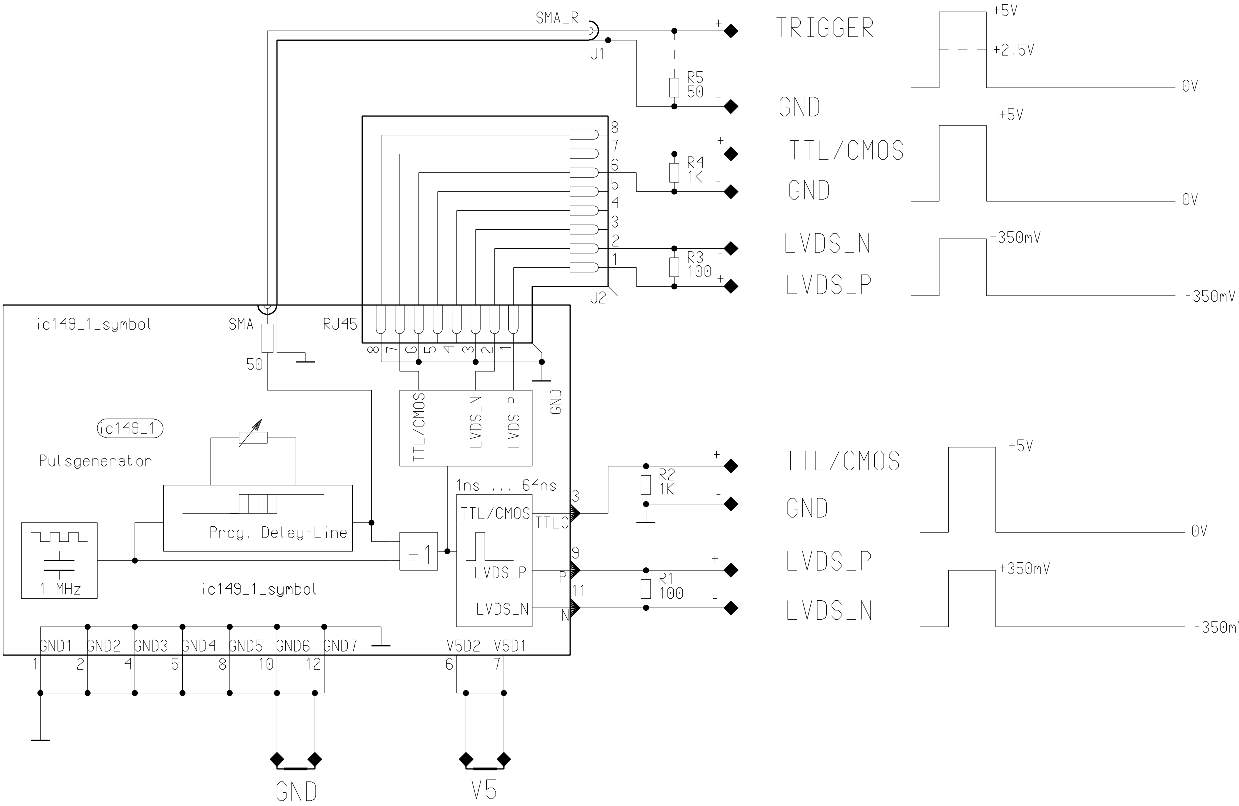


Figure 7: Block diagram of the iC149