ICD2061A

Dual Programmable Graphics Clock Generator

Single-Chip Dual Programmable Oscillator Handles All Frequency Requirements of Popular Graphics Chip Sets

- 2nd Generation Dual Oscillator Graphics Clock Generator
- 2 Independent Clock Outputs from 390 KHz – 120 MHz
- Individually Programmable Oscillators Using a Highly Reliable Manchester-Encoded 21-Bit Serial Data Word
- 2-Pin Serial Programming Interface Allows Direct Connection to most Graphics Chip Sets with no External Hardware Required
- 2 Advanced Power-Down Capabilities
- 3-State Oscillator Control Disables Outputs for Test Purposes
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- Sophisticated Internal Loop-Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- 5V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 16-Pin SOIC Package Configuration

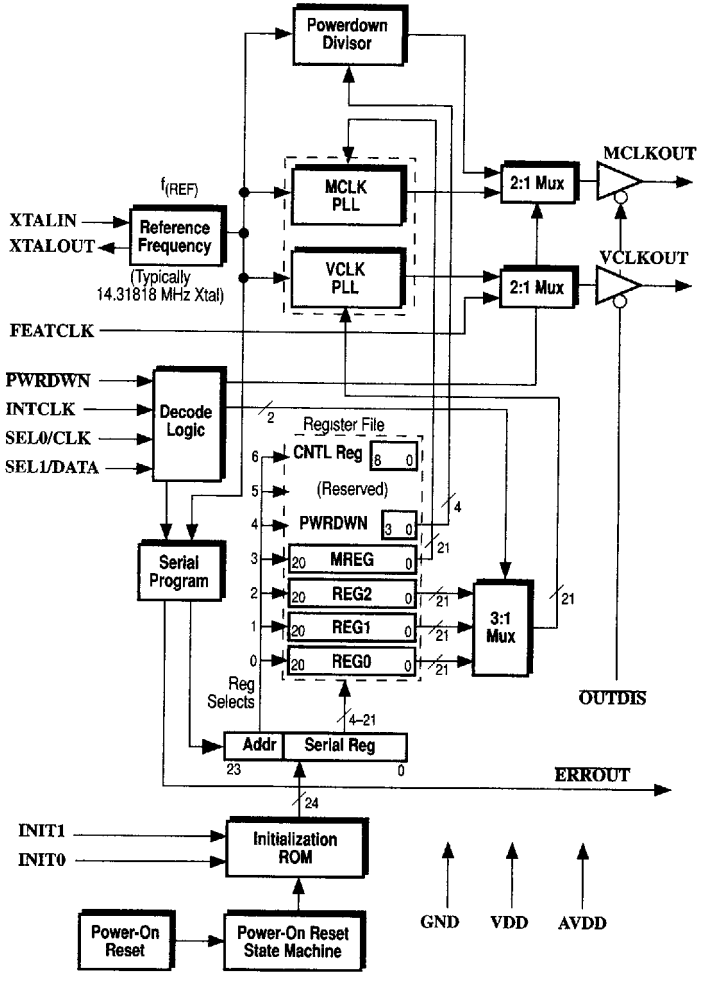

Fig. 1: ICD2061A Block Diagram

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Introduction

The ICD2061A Dual Programmable Graphics Clock Generator features a fully programmable set of clock oscillators which can handle all frequency requirements of most graphics systems. The ICD2061A offers the selection ease of ROM-based clock chips, while also offering the versatility of serial programmed frequency synthesizers. It features advanced power-down capabilities, making it ideally suited for the portable computer market. The ICD2061A has extended frequency range and improved voltage/temperature stability when compared to first-generation frequency synthesizers.

The ICD2061A Dual Programmable Graphics Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value between 390 KHz and 120 MHz. The ICD2061A is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators.

Being able to change the output frequency dynamically adds a whole new degree of freedom for the electrical engineer heretofore unavailable with existing crystal oscillator devices. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption or speeding it up can mean faster operation; graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example: ±10%) allows worst case evaluations.

While primarily designed for the graphics subsystem market, the programming versatility of the ICD2061A makes it ideal wherever two variable, yet highly accurate, clock sources are required.

ICD2061A Changes from the ICD2061

The ICD2061A revision of the ICD2061 is a complete mask redesign which includes feature enhancements as well as minor bug fixes. The following major modifications have been implemented:

- **Increased Frequency Resolution** — 3 additional bits have been added to the CNTL Register to allow an optional pre-divide by 2 on the P Counter. Full upward compatibility with existing software is maintained.
- **Reduced Power Consumption** — By dynamically switching in a weak pull-up when the user pulls the PWRDWN pin low, the power consumption of the ICD2061A in Power-down Mode 2 has been reduced to $^1/_4$ that of the ICD2061 (less than 50 µA).
- **Glitch-Free Transitions** — Reprogramming the MCLK and the active VCLK registers is now glitch-free; the Reference Frequency is automatically multiplexed to the appropriate output pin during the transition period.
- **Extended Low-Frequency Range** — The lower frequency limit has been extended to 390 KHz as a result of the addition of a ÷128 value to the Post-VCO Divide Register.
- **Enhanced VCO** — The redesigned VCOs generate 30% less jitter than those of previous versions.
- **New Index Table** — The new VCOs require a change in the Index Table values.

Pin & Signal Descriptions

Fig. 2: Pin Descriptions

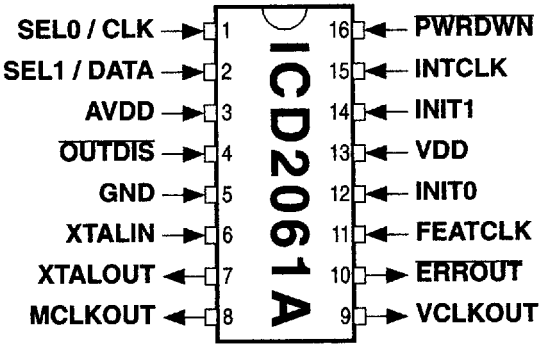


Table 1: Signal Descriptions

Pin #	Signal	Function
1	SEL0 / CLK	Bit 0 (LSB) of frequency select logic, used to select oscillator frequencies. Clock Input in serial programming mode. (Internal pull-down allows no-connect.)
2	SEL1 / DATA	Bit 1 (MSB) of frequency select logic, used to select oscillator frequencies. Data Input in serial programming mode. (Internal pull-down allows no-connect.)
3	AVDD	+5V to Analog Core
4	$\overline{\text{OUTDIS}}$	Output Disable (3-State Output Enable) when signal is pulled low. (Internal pull-up allows no-connect.)
5	GND	Ground
6	XTALIN	Input Reference Oscillator for all Phase-Locked Loops (nominally 14.31818 MHz). An optional PC System Bus Clock signal may be used as input if available.
7	XTALOUT	Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
8	MCLKOUT	Memory Clock out
9	VCLKOUT	Video Clock out
10	$\overline{\text{ERROUT}}$	Error Output: a low signals an error during serial programming.
11	FEATCLK	External clock input (Feature Clock) (Internal pull-up allows no-connect.)
12	INIT0	Select power-up initial conditions (LSB) (Internal pull-down allows no-connect.)
13	VDD	+5V to I/O Ring
14	INIT1	Select power-up initial conditions (MSB) (Internal pull-down allows no-connect.)
15	INTCLK	Selects the Feature Clock external clock input as VCLKOUT output (Internal pull-up allows no-connect.)
16	$\overline{\text{PWRDWN}}$	Power-down pin (active low) (Internal pull-up allows no-connect if power-down operation not required. See *Power Management Issues* on page 145 for specific details concerning the use of this pin.)

Register Definitions

Register File

The Register File consists of the following registers and their selection addresses:

Table 2: Register Addressing

Address	Register	Usage
000	REG0	Video Clock Register 1
001	REG1	Video Clock Register 2
010	REG2	Video Clock Register 3
011	MREG	Memory or I/O Timing Clock
100	PWRDWN	Divisor for Power-Down mode
101	(Reserved)	
110	CNTL Reg	Control Register

All register values are preserved in power-down mode.

Power-On Reset and Register Initialization

The ICD2061A Clock Synthesizer has several of its registers in a known state upon power-up. This is implemented by the Power-On initialization circuitry. Three VGA registers are initialized based on the state of the INIT1 and INIT0 pins at power-up. Also, the Memory Clock is initialized based on the INIT pins.

The Power-On Reset Function operates transparently to the video subsystem. It performs its initialization function and is cleared before the system Power-On Reset permits the system to begin its boot process. The INIT pins must ramp up with VDD if a 1 on either of these pins is desired. They are internally pulled down, and so will default to 0 if left unconnected.

The various registers are initialized as follows (all frequencies in MHz):

Table 3: Register Initialization — ROM Option 1

INIT1	INIT0	MREG	REG0	REG1	REG2
		(Frequencies in MHz)			
0	0	32.500	25.175	28.322	28.322
0	1	40.000	25.175	28.322	28.322
1	0	50.350	40.000	28.322	28.322
1	1	56.644	40.000	50.350	50.350

Register Selection

The Video Clock output is controlled not only by the SEL0 & SEL1 bits, but also by the $\overline{\text{PWRDWN}}$ and $\overline{\text{OUTDIS}}$ signals. Additionally, the Clock Synthesizer is multiplexed with an external frequency input (FEATCLK) which corresponds to the IBM VGA Feature Clock standard. The following table shows the VCLKOUT selection criteria:

Table 4: VCLKOUT Selection

$\overline{\text{OUTDIS}}$	$\overline{\text{PWRDWN}}$	INTCLK	SEL1	SEL0	VCLKOUT
0	X	X	X	X	High-Z
1	0	X	X	X	Forced High
1	1	X	0	0	REG0
1	1	X	0	1	REG1
1	1	0	1	0	FEATCLK
1	1	1	1	X	REG2
1	1	X	1	1	REG2

The Memory Clock output is controlled by the PWRDWN and OUTDIS signals as indicated below:
MCLKOUT Selection

Table 5: MCLKOUT Selection

OUTDIS	PWRDWN	MCLKOUT
0	X	High-Z
1	1	MREG
1	0	PWRDWN[a]

a. Power-Down Mode (1 or 2) is determined by the setting of bit C5 in the CNTL Reg. See *Control Register Definition* on page 135.

The Clock Select pins SEL0 & SEL1 have a dual purpose. When these pins are performing serial download, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins SEL0 & SEL1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming. At the end of the timeout interval, new register selection occurs. At this point, the VCLKOUT signal will be multiplexed to the reference signal $f_{(REF)}$ for an additional timeout interval to give the VCO time to settle to its new value. [The timeout interval in both cases is approximately 5 msec — see the timeout interval spec in *AC Characteristics* on page 153.]

When a new frequency is being set for MCLK, or if the active VCLK register is reprogrammed, then a glitch-free multiplexing to the Reference Frequency is performed. Once the STOP bit is sent after the MCLK or active VCLK Programming Word, the appropriate output signal will be multiplexed to the reference signal $f_{(REF)}$ for an extra timeout interval (See *AC Characteristics* on page 153 for further details).

Control Register Definition

The Control Register (CNTL Reg) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined as follows:

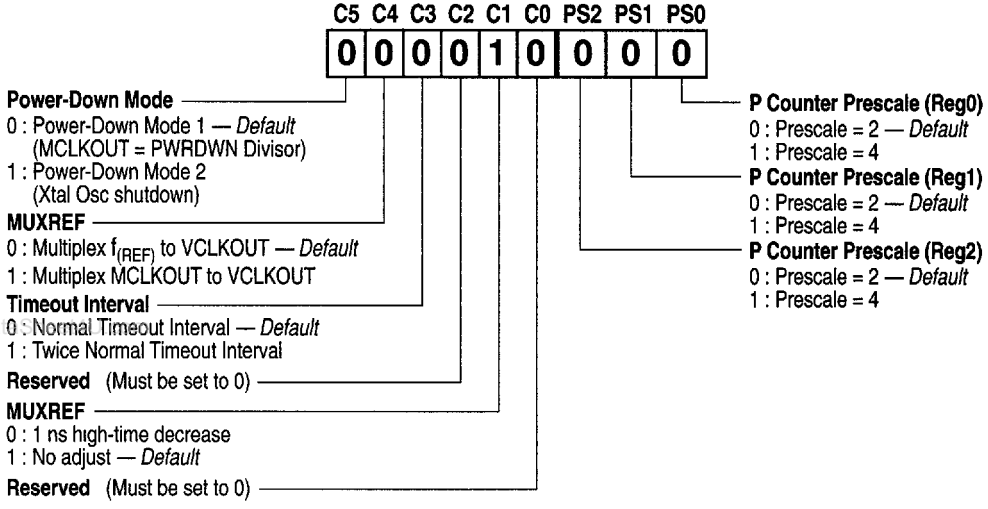


Fig. 3: Control Register

Duty Cycle Adjust — This control bit causes a 1 ns decrease in the output waveform high time. The default is no adjustment. In situations in which the capacitive load is beyond device specifications, or where the Threshold Voltage V_{TH} is to be changed from CMOS to TTL levels, this adjustment can sometimes bring the output closer to 50% duty cycle.

Timeout Interval — The Timeout Interval is normally defined as in the *AC Characteristics* on page 153. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, then the timeout may be too short. If this control bit is set, then the Timeout Interval is doubled.

MUXREF — This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the $f_{(REF)}$ reference frequency, but some graphic controllers cannot run as slow as $f_{(REF)}$. This bit, when set, allows the MCLK to be used as an alternative frequency.

Power-Down Mode — This control bit determines which Power-Down Mode the $\overline{\text{PWRDWN}}$ pin will implement. The default (Power-Down Mode 1) forces the MCLKOUT signal to be a function of the PWRDWN register. Power-Down Mode 2 turns off the crystal oscillator and disables all outputs. There is a more detailed description in the section entitled *Power Management Issues* on page 145.

P Counter Prescale (REG0, REG1, REG2) — These control bits determine whether or not to prescale the P Counter value, which allows "fine tuning" the output frequency of the respective register. Prescaling is explained in more detail in various sections of this Datasheet.

Serial Programming Architecture

The ICD2061A programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual functions of clock selection and serial programming. The Serial Program Block (See *Fig. 1: ICD2061A Block Diagram* on page 125.) contains several components: a Serial Unlock Decoder (containing the Unlocking Mechanism and Manchester Decoder), a Watchdog Timer, the Serial Data Register (Serial Reg) and a Demultiplexer to the Register File.

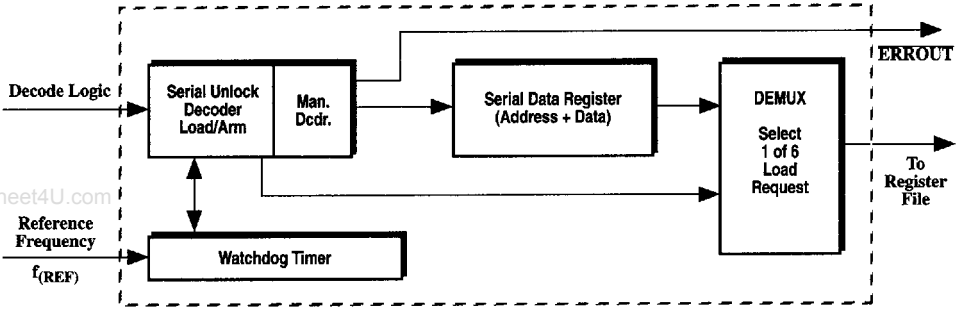


Fig. 4: Serial Program Block Diagram — Detail

Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence, detailed in the following timing diagram:

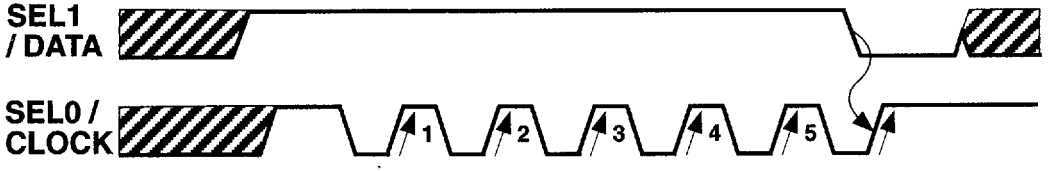


Fig. 5: Unlock Sequence

The initial unlock sequence consists of at least five low-to-high transitions of CLK with DATA high, followed immediately by a single low-to-high transition of CLK with DATA low. Following this unlock sequence, the encoded serial data is clocked into the Serial Data Register (Serial Reg).

NOTE: The ICD2061A may not be serially programmed when in Power-Down Mode.

Watchdog Timer

Following any transition of CLK or DATA, the Watchdog Timer is reset and begins counting. Throughout the entire programming process, the Watchdog Timer ensures that successive edges of CLK or DATA do not violate the timeout specification (of 2 msec — see *AC Characteristics* on page 153.). If a timeout does occur, the Lock Mechanism is rearmed and the current data in the Serial Data Register (Serial Reg) is ignored.

Since the VCLK registers are selected by the SEL0 or SEL1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted to pass through to the Decode Logic after the Watchdog Timer has timed out. This delay of SEL0 or SEL1 data permits a serial program cycle to take place without affecting the current register selection. The process of serial programming has no effect on the performance of the graphics subsystem. [Note that there is a latency amounting to the duration of the Watchdog Timer before any new VCLK register selections take effect.]

Serial Data Register

The serial data is clocked into the Serial Data Register (Serial Reg) in the following order:

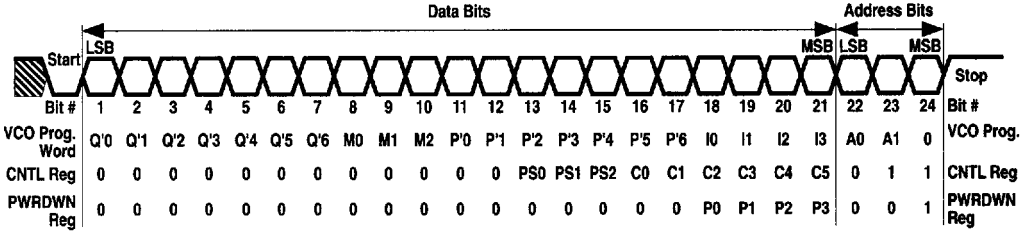


Fig. 6: Serial Data Timing

The serial data is sent using a modified Manchester encoded data format. This is defined as follows:

1 — An individual data bit is sampled on the rising edge of CLK.

2 — The complement of the data bit must be sampled on the previous falling edge of CLK.

3 — The Setup and Hold Time requirements must be met on both CLK edges.

4 — The unlock sequence, start, and stop bits are not Manchester encoded.

For specifics on timing, see *Fig. 14: Serial Programming Timing* on page 157.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (REG0, REG1, REG2, MREG), the data is made up of 4

fields: D[20:17] = Index; D[16:10] = P'; D[9:7] = Mux; D[6:0] = Q'. [See *Programming the ICD2061A* on page 140 for more details on the VCO data word.] For the other registers with fewer than 21 bits (PWRDWN, CNTL Reg), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data Register (or an error is issued). Undefined bits should always be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last data bit, a stop bit or Load command is issued by bringing DATA high and toggling CLK high-to-low and low-to-high. The Unlocking Mechanism then automatically rearms itself following the load. Only when the Watchdog Timer has timed out are the SEL0 & SEL1 Selection Pins permitted to return to their normal register select function.

Note that the Serial Data Register (Serial Reg) which receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command which passes the Serial Reg contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data Register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the Unlocking Mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the Serial Buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the Unlocking Mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the Unlocking Mechanism is rearmed, the Serial Counter reset, all received data ignored, and $\overline{\text{ERROUT}}$ is asserted.

ERROUT Operation

The ERROUT signal is used to report when a program error has been detected internally by the ICD2061A. The signal stays active until the next unlock sequence.

The following circuit shows the basic mechanism used to detect valid and erroneous serial data:

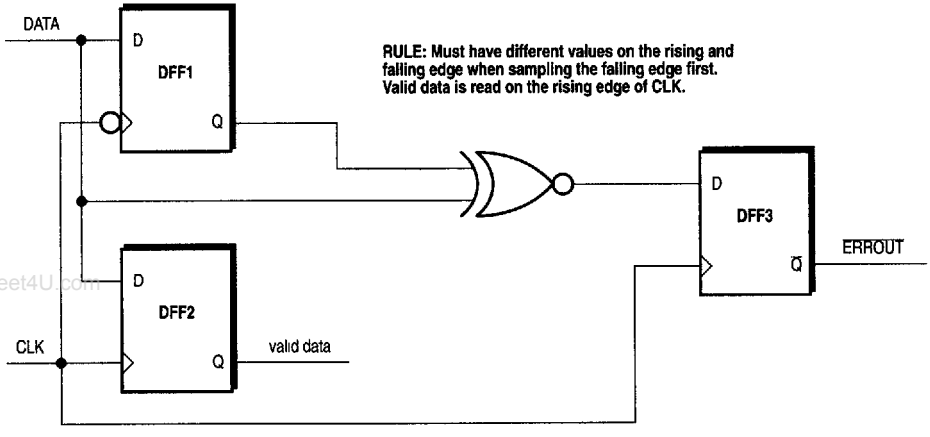


Fig. 7: Modified Manchester Decoder Circuit

The ERROUT signal is invoked for any of the following error conditions: incorrect start bit; incorrect Manchester encoding; incorrect length of data word; incorrect stop bit; timeout.

NOTE: If there is no input pin available on the target VGA controller chip to monitor ERROUT, a software routine which counts VSYNC pulses in order to measure output frequency may be used as a determination of programming accuracy.

Programming the ICD2061A

The desired output frequency is defined via a serial interface, with a 21–bit number shifted in. The ICD2061A has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields:

Table 6: Programming Word Bit Fields

Field	# of Bits	Notes
Index (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Mux (M)	3	
Q Counter Value (Q')	7	LSB (Least Significant Bits)

The frequency of the Programmable Oscillator f(VCO) is determined by these fields as follows:

$$P' = P - 3 \qquad Q' = Q - 2$$

$$f_{(VCO)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

where $f_{(REF)}$ = Reference frequency (between 1 MHz – 60 MHz; typically 14.31818 MHz)

NOTE: If a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

The value of $f_{(VCO)}$ must remain between 50 MHz and 120 MHz inclusive. Therefore, for output frequencies below 50 MHz, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux Field (M) as follows:

Table 7: Post-VCO Divisor

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Index Field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (This table is referenced to the VCO frequency, $f_{(VCO)}$, rather than to the desired output frequency.) Note that VCLK may be shut off, but that MCLK must be left running.

When the Index Field is set to **1111**, VCLK is turned off and both channels run from the same MCLK VCO. To reduce jitter, one doesn't want the two VCOs to run at integral multiples of each other; therefore, if one does want the clocks to run at 2^n (n = 0, 1, 2 .. 7) multiples of each other, this is done by turning off the VCLK VCO and multiplexing the MCLK VCO over to VCLKOUT, dividing down to the desired frequency. This will significantly reduce heterodyne jitter.

Table 8: Index Field (I)

I	VCLK f_{VCO} (MHz)	MCLK f_{VCO} (MHz)
0000	50.0 – 51.0	50.0 – 51.0
0001	51.0 – 53.2	51.0 – 53.2
0010	53.2 – 58.5	53.2 – 58.5
0011	58.5 – 60.7	58.5 – 60.7
0100	60.7 – 64.4	60.7 – 64.4
0101	64.4 – 66.8	64.4 – 66.8
0110	66.8 – 73.5	66.8 – 73.5
0111	73.5 – 75.6	73.5 – 75.6
1000	75.6 – 80.9	75.6 – 80.9
1001	80.9 – 83.2	80.9 – 83.2
1010	83.2 – 91.5	83.2 – 91.5
1011	91.5 – 100.0	91.5 – 100.0
1100	100.0 – 120.0	100.0 – 120.0
1101	100.0 – 120.0	100.0 – 120.0
1110	Turn off VCLK	100.0 – 120.0
1111	Mux MCLK to VCLK	100.0 – 120.0

If the desired VCO frequency lies on a boundary in the table — in other words, if it is exactly the upper limit of one entry and the lower limit of the next — then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, IC DESIGNS provides ***BitCalc*** (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. For Macintosh or DOS environments, please ask about availability. Please specify disk size (5" or 3") when ordering ***BitCalc***.

Programming Constraints

There are five primary programming constraints the user must be aware of:

$$1\ \text{MHz} \le f_{(REF)} \le 60\ \text{MHz}$$

$$200\ \text{KHz} \le \frac{f_{(REF)}}{Q} \le 1\ \text{MHz}$$

$$50\ \text{MHz} \le f_{(VCO)} \le 120\ \text{MHz}$$

$$3 \le Q \le 129$$

$$4 \le P \le 130$$

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the ***BitCalc*** program, these constraints become transparent.

Programming Example — Prescaling = 2 (default)

The following is an example of the calculations ***BitCalc*** performs:

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 50 MHz, double it to 79.0 MHz. Set M to 001. Set I to 1000. The result:

$$f_{(VCO)} = 79.0 = (2 \times 14.31818 \times \frac{P}{Q})$$

$$\frac{P}{Q} = 2.7857$$

Several choices of P and Q are available:

Table 9: P & Q Value Pairs

P	Q	$f_{(VCO)}$ (MHz)	Error (ppm)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q) = (80,29) for best accuracy (40 PPM).

Therefore:

$$P' = P - 3 = 80 - 3 = 77 = 1001101 \text{ (4dH)}$$

$$Q' = Q - 2 = 29 - 2 = 27 = 0011011 \text{ (1bH)}$$

and the full programming word, W, is:

$$W = I, P', M, Q' = 1000, 1001101, 001, 0011011 = 1000100110100100011011 \text{ (11349bH)}$$

The programming word W is then sent as a serial bit stream, LSB first. Appropriate address bits and start & stop bits must also be included as defined in the Serial Programming Scheme section.

Programming Example — Prescaling = 4

Assume the desired VCLKOUT frequency is 100 MHz. The table below compares the results of using the default prescaling value of 2 and the optional prescaling value of 4:

Table 10: Prescale Values

Prescale	Actual Frequency (MHz)	P	Q	PPM Err
2	99.84028	129	37	1600
4	99.99998	110	63	0

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0–2 (corresponding to REG0–2) — which involves loading a Control Word (taking care to preserve the current values of the other Control Bits) — before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before, unless and until it is desired to program a new frequency without prescaling, at which point a new Control Word must first be loaded with the proper bits set, and observing the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale bits (load a Control Word)

2. Program the VCO (load a Program Word)

NOTE: Care must be taken not to change the Prescale Bit of the currently active register: the results will be unpredictable at best, and it could cause the VCO to go out of lock.

Power Management Issues

Power-Down Mode 1

The ICD2061A contains a mechanism to reduce the quiescent power when stand-by operation is desired. In Power-Down Mode 1 (invoked by pulling the $\overline{\text{PWRDWN}}$ signal low and having the proper CNTL Reg bit set to zero), both VCOs are shut down, the VCLKOUT output is forced high, and the MCLKOUT output is set to a user-defined low-frequency value to refresh dynamic RAM.

The Power-down MCLKOUT value is determined by the following equation:

$$\text{MCLKOUT}_{\text{Power-Down}} = f_{(REF)} \div (\text{PWRDWN Reg Divisor Value})$$

The Power-Down Register divisor is determined according to the following 4-bit word programmed into the PWRDWN Register:

Table 11: PWRDWN Register Programming

PWRDWN bits P3 P2 P1 P0	PWRDWN Register Value	Power-Down Divisor	$\text{MCLKOUT}_{\text{Power-Down}}$ ($f_{(REF)}$ = 14.31818 MHz)
0 0 0 0	0	N/A	N/A
0 0 0 1	1	32	447.4 KHz
0 0 1 0	2	30	477.3 KHz
0 0 1 1	3	28	511.4 KHz
0 1 0 0	4	26	550.7 KHz
0 1 0 1	5	24	596.6 KHz
0 1 1 0	6	22	650.8 KHz
0 1 1 0	7	20	715.9 KHz
1 0 0 0	**8 (default)**	**18**	**795.5 KHz**
1 0 0 1	9	16	894.9 KHz
1 0 1 0	A	14	1.023 MHz
1 0 1 1	B	12	1.193 MHz
1 1 0 0	C	10	1.432 MHz
1 1 0 1	D	8	1.790 MHz
1 1 1 0	E	6	2.386 MHz
1 1 1 1	F	4	3.580 MHz

On Power-Up, the value of the PWRDWN Register is loaded with a default value of 8 (1000 binary), which yields an MCLKOUT frequency of 795 KHz (14.31818 / 18). The default mode is Power-Down Mode 1.

NOTE: The ICD2061A may not be serially programmed when in Power-Down Mode.

Power-Down Mode 2

If there is no need for any output during power-down operation, then an alternate power-down mode is available, which will completely shut down all outputs and the reference oscillator, yet still preserve all register contents. This results in the absolute least power consumption.

Power-Down Mode 2 is invoked by first programming the Power-Down bit in the CNTL Reg, and then pulling the $\overline{\text{PWRDWN}}$ pin low.

The $\overline{\text{PWRDWN}}$ Pin

This pin has a standard internal pull-up during normal operation. When the user pulls it down to invoke power-down Mode 1 or 2, the normal pull-up resistor is dynamically switched to a weak pull-up, which significantly reduces power consumption. If, after pulling this pin low, the pin is allowed to float, the weak pull-up will gradually cause the signal to rise, enabling the normal pull-up, and will eventually turn the device back on.

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: $I = C \cdot V \cdot f$, where

I = current (in mA),

C = load capacitance (max. 25pF),

V = output voltage (usually 5V), and

f = output frequency (in MHz).

To calculate total operating current, sum the following terms:

VCLKOUT $\Rightarrow$ $C \cdot V \cdot f_{(VCLK)}$

MCLKOUT $\Rightarrow$ $C \cdot V \cdot f_{(MCLK)}$

Internal $\Rightarrow$ 12 mA

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5–10pF loading, depending on package type.

Table 12: Typical Values

Frequency	Capacitive Load	Current (mA)
low	low	15
high	low	40
high	high	65

When in Power-Down Mode 1, and using a 14.31818 MHz reference crystal, the power consumption should not exceed 7.5 mA. In Power-Down Mode 2, the power consumption should not exceed 50 µA.

Circuit Operation

Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown below. The external input frequency $f_{(REF)}$ goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO either to go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will quickly lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

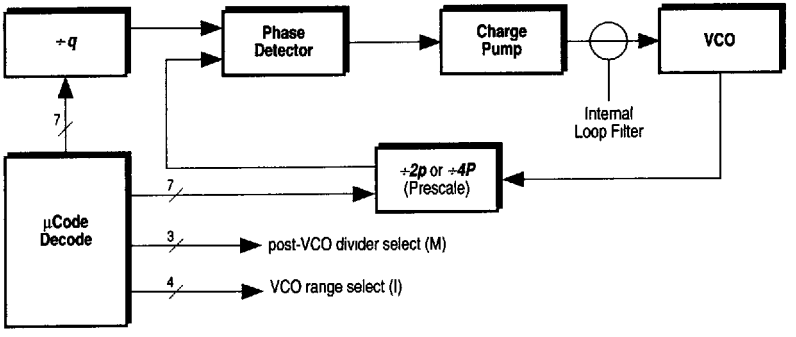


Fig. 8: Phase-Locked Loop Oscillator

Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCO's and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for graphics designs.

Frequency Range

The output frequency range of both Phase-Locked Loop sections is 390 KHz – 120 MHz.

Output Disable

When the $\overline{\text{OUTDIS}}$ pin is asserted (active low), all the output pins except XTAL OUT and $\overline{\text{ERROUT}}$ enter a high impedance mode, to support automated board testing.

External Clock Input (Feature Connector Compatibility)

To maintain backward compatibility to the VGA feature connector standard, the Video Clock output VCLKOUT can multiplex between the clock synthesizer output and the external clock input FEATCLK. This multiplexing is controlled by the INTCLK input signal and appropriate decode of selection signals (SEL0, SEL1). See the section on Register Definitions for more information.

PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. The analog power pin (AVDD) should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply lines. Refer to IC DESIGNS Application Note *Power Feed and Board Layout Issues* on page 281 for more details and for illustrative schematics.

The designer should also avoid routing any of the output traces of the ICD2061A in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies. When designing with this device, it is best to locate the ICD2061A closest to the device requiring the highest frequency.

FCC & Noise issues

A conscious design effort was made to achieve the optimum rise & fall times at the output pads in order to produce acceptable signals at the clock destinations when operating at high frequencies. Unfortunately, the production of the squarest possible square waves can lead to the generation of high-energy odd harmonics, which can result in extraneous emissions.

For techniques on how to design with this device while taking FCC emission issues into consideration, please refer to the IC DESIGNS Application Note *Minimizing Radio Frequency Emissions* on page 285.

Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on opposite sides of the die. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate power and ground buses for the analog and digital circuitry are used.

Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2061A is inherently stable over temperature, voltage and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2061A, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

Ordering Information

Table 13: Order Codes

Part Number	Package Type	Temperature Range	Chip Options
ICD2061A	S = 16-Pin SOIC DIP	C = Commercial[a]	–1 (Other ROM options by special order.)

a. 0°C to +70°C

Example: order ICD2061ASC–1 for the ICD2061A, 16-pin plastic SOIC, commercial temperature range device with the initial frequencies shown in *Table 3: Register Initialization — ROM Option 1* on page 133.

Device Specifications

Electrical Data

Table 14: Absolute Maximum Ratings

Name	Description	Min	Max	Units
V_{DD} & AV_{DD}	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input voltage with respect to GND	–0.5	V_{DD} + 0.5	Volts
T_{STOR}	Storage temperature	–65	+150	°C
T_{SOL}	Max soldering temperature (10 sec)		+260	°C
T_J	Junction temperature		+125	°C
P_{DISS}	Power dissipation		350	mWatts

NOTE: Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

OPERATING RANGE: V_{DD} & AV_{DD} = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

Table 15: DC Characteristics

Name	Description	Min	Typ	Max	Units	Conditions
V_{IH}	High-level input voltage	2.0			Volts	
V_{IL}	Low-level input voltage			0.8	Volts	
V_{OH}	High-level CMOS output voltage	2.4			Volts	I_{OH} = –4.0 mA
V_{OL}	Low-level output voltage			0.4	Volts	I_{OL} = 4.0 mA
I_{IH}	Input high current			150	µA	$V_{IH} = V_{DD}$
I_{IL}	Input low current			–250	µA	V_{IH} = 0.5V
I_{OZ}	Output leakage current			10	µA	(3-state)
I_{DD}	Power supply current	15		65	mA	
I_{DD-TYP}	Power supply current (typical)		35		mA	@ 60 MHz
I_{ADD}	Analog power supply current			10	mA	
I_{PD1}	Power-down current (Mode 1)		6	7.5	mA	
I_{PD2}	Power-down current (Mode 2)		25	50	µA	

Table 16: AC Characteristics

Symbol	Name	Description	Min	Typ	Max	Units
$f_{(REF)}$	reference frequency	Reference Oscillator nominal value (Note: for references of other than 14.31818 MHz, the pre-loaded ROM frequencies will not be accurate.)	1	14.318	60	MHz
$t_{(REF)}$	reference period	$1 \div f_{(REF)}$	16.6		1000	ns
t_1	input duty cycle	Duty cycle for the input oscillator defined as $t_1 \div t_{(REF)}$	25%	50%	75%	
t_2	output clock periods	Output oscillator values	8.33 120 MHz		2564 390 KHz	ns
t_3	output duty cycle	Duty cycle for the output oscillators (NOTE: duty cycle is measured at CMOS threshold levels. At 5V, $V_{TH} = 2.5V$.)	40%		60%	
t_4	rise times	Rise time for the output oscillators into a 25pF load			3	ns
t_5	fall times	Fall time for the output oscillators into a 25pF load			3	ns
t_{freq1}	freq1 output	Old frequency output				
t_{freq2}	freq2 output	New frequency output				
t_A	$f_{(REF)}$ mux time	Time clock output remains high while output muxes to reference frequency	$\frac{t_{(REF)}}{2}$		$3\frac{t_{(REF)}}{2}$	ns
$t_{timeout}$	timeout interval	Internal interval for serial programming and for VCO changes to settle. [If the interval is too short, see the *Timeout Interval* paragraph on page 135.]	2	5	10	msec
t_B	t_{freq2} mux time	Time clock output remains high while output muxes to new frequency value	$\frac{t_{freq2}}{2}$		$3\frac{t_{freq2}}{2}$	ns
t_6	3-state	Time for the output oscillators to go into 3-state mode after $\overline{OUTDIS}$ signal assertion	0		12	ns
t_7	clk valid	Time for the output oscillators to recover from 3-state mode after $\overline{OUTDIS}$ signal goes high	0		12	ns
t_8	Power-Down	Time for Power-Down Mode of operation to take effect			12	ns
t_9	Power-Up	Time for recovery from Power-Down Mode of operation			12	ns

Table 16: AC Characteristics (Continued)

Symbol	Name	Description	Min	Typ	Max	Units
t_{10}	MCLKOUT high	Time for MCLKOUT to go high after $\overline{PWRDWN}$ is asserted high	0		$t_{PWR-DWN}$	ns
t_{11}	MCLKOUT delay	Delay of MCLKOUT prior to f_{MCLK} signal at output	$\frac{t_{MCLK}}{2}$		$3\frac{t_{MCLK}}{2}$	ns
t_{serclk}		Clock period of serial clock	$2 \cdot t_{(REF)}$		2	msec
t_{HI}		Minimum high time	$t_{(REF)}$			ns
t_{LO}		Minimum low time	$t_{(REF)}$			ns
t_{SU}		Setup time	20			ns
t_{HD}		Hold time	10			ns
t_{ldcmd}		Load command	0		$t_1 + 30$	ns

NOTE: Input capacitance is typically 10pF, except for the crystal pads.

Timing Diagrams

Fig. 9: Rise and Fall Times

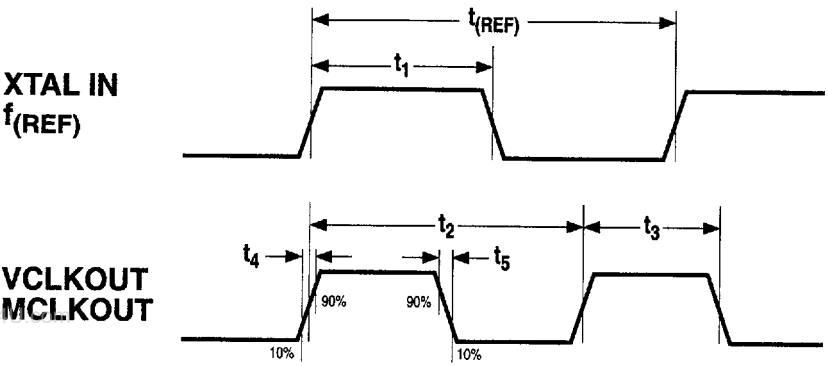


Fig. 10: 3-State Timing

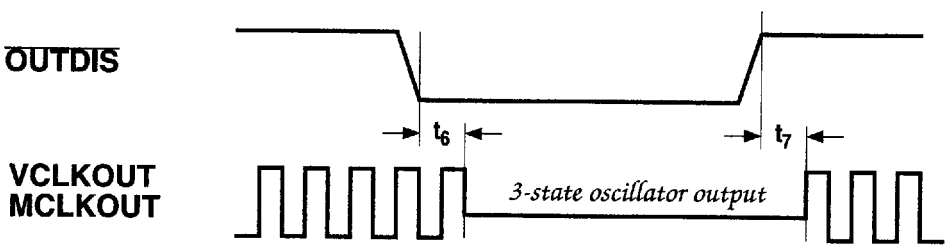


Fig. 11: Selection Timing

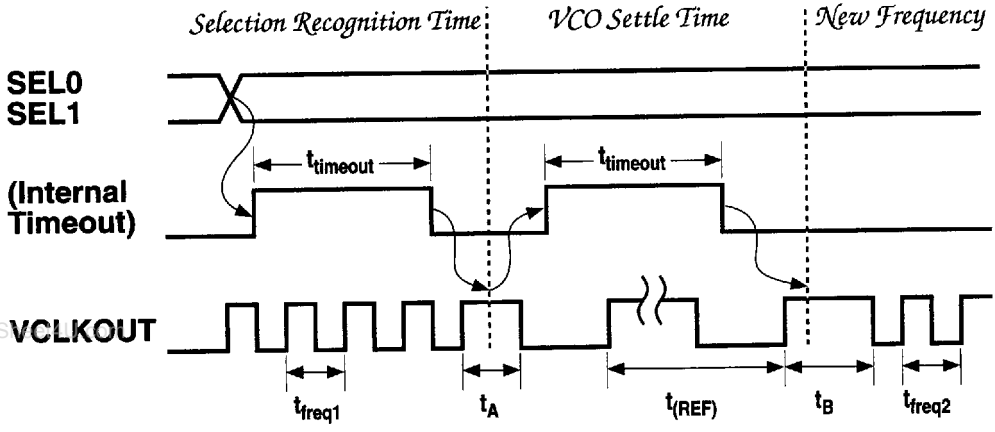


Fig. 12: MCLK & Active VCLK Register Programming Timing

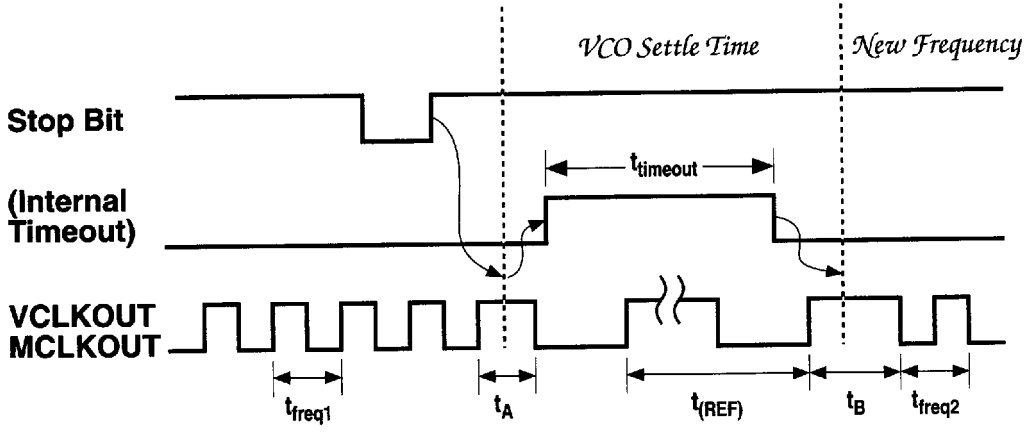
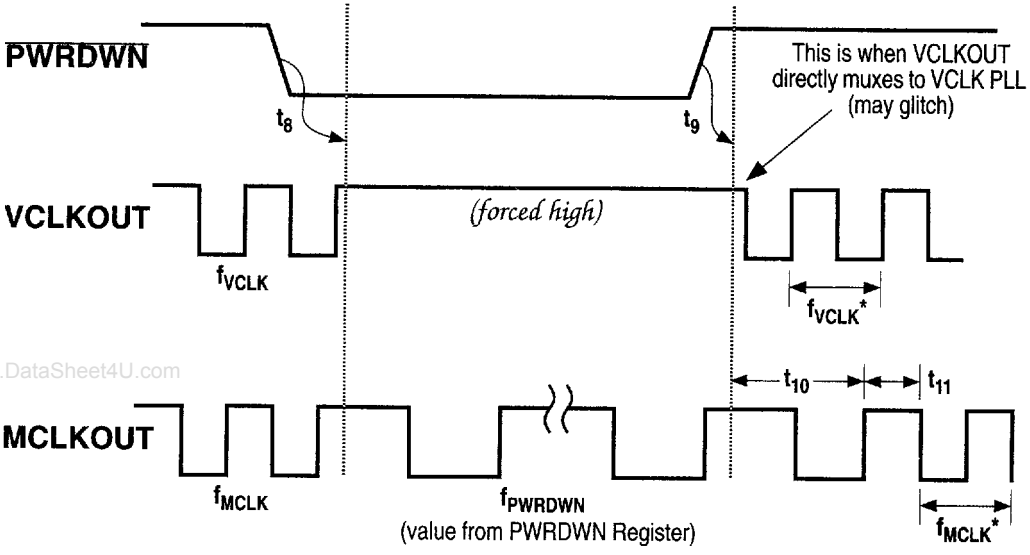
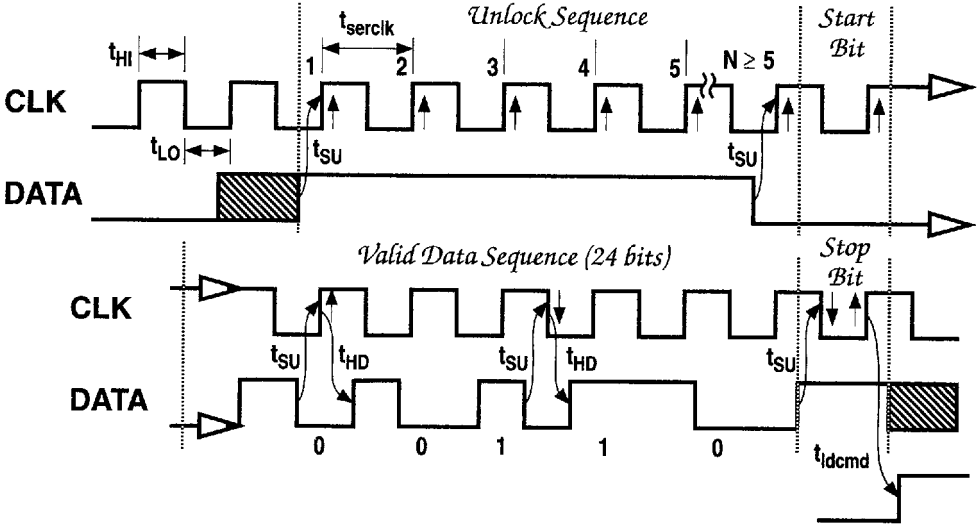


Fig. 13: Soft Power-Down Timing (Mode 2)



* It takes 2–10 msec after Soft Power-Down to guarantee lock of VCLKOUT & MCLKOUT PLLs

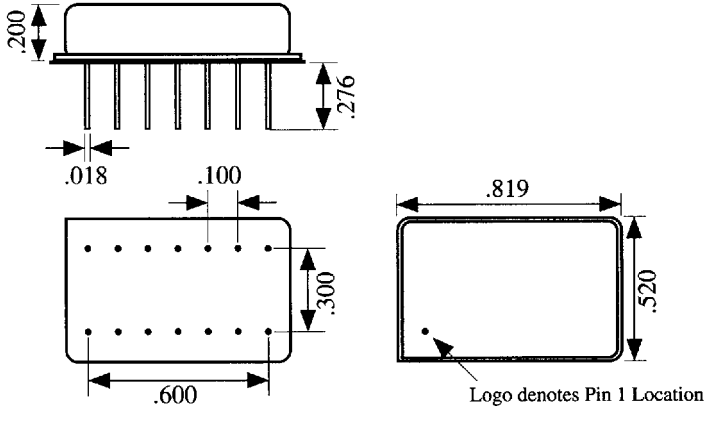
Fig. 14: Serial Programming Timing



14-Pin Packages

Table 1: 14-Pin Metal Can Outline

Package (Lead Count = 14)



(Dimensions in inches)

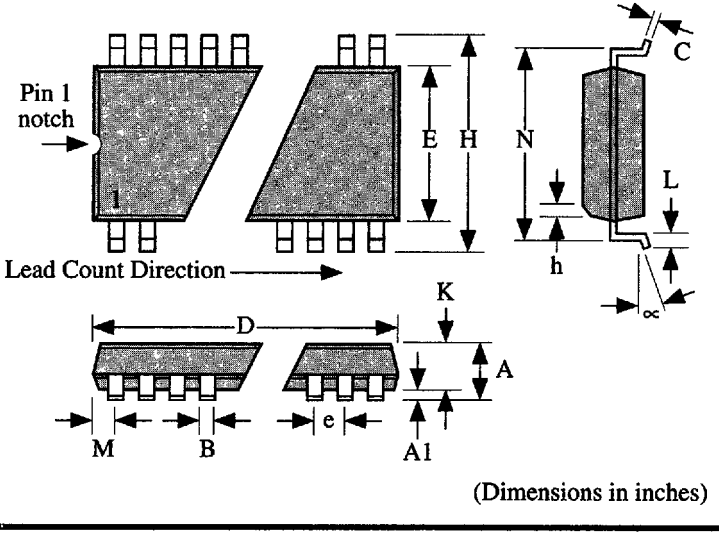
8

16-Pin Packages

Table 2: 16-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.405	.410
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x	45°
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 16)

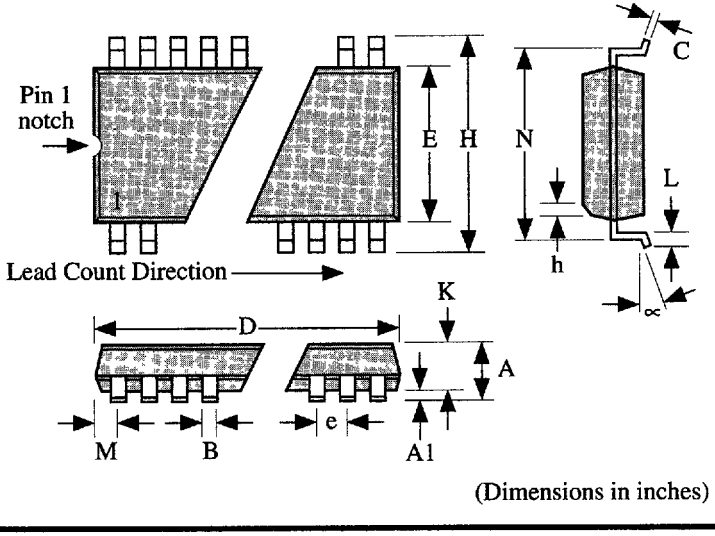


20-Pin Packages

Table 3: 20-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.505	.512
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x	45°
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 20)



(Dimensions in inches)

8