IC Ensemble, Inc.

ICE 1230

AC‘97 Audio Codec

Preliminary

Features

- AC’97 compliant codec
- Exceeds Microsoft® PC’98 requirements
- 16-bit stereo full duplex ∑Δ codec
- 48kHz fixed sampling rate
- Stereo LINE IN, CD, VIDEO, and AUX analog line-level inputs
- Mono speaker-phone and PC beeper analog line-level inputs
- Mono line-level microphone inputs switchable from two external sources
- Multiple codec mode
- Power management support
- 48-pin TQFP or LQFP package
- 3.3V or 5V operating supply

Description

IC Ensemble’s ICE 1230 ∑Δ audio codec is an AC’97 fully compliant codec designed to bring CD-quality audio in personal computers and multimedia systems. The ICE 1230 integrates an analog mixer, full duplex 16-bit stereo ADC and 16-bit stereo DAC, and a digital audio stream interface (for interface with PCI audio controllers) into a single IC, making it ideal for motherboard host-based applications or in add-in card designs (when coupled with a PCI digital audio controller) where outstanding audio quality is required.

Additional Features

- Multiple codec support
- 3.3V analog supply operation

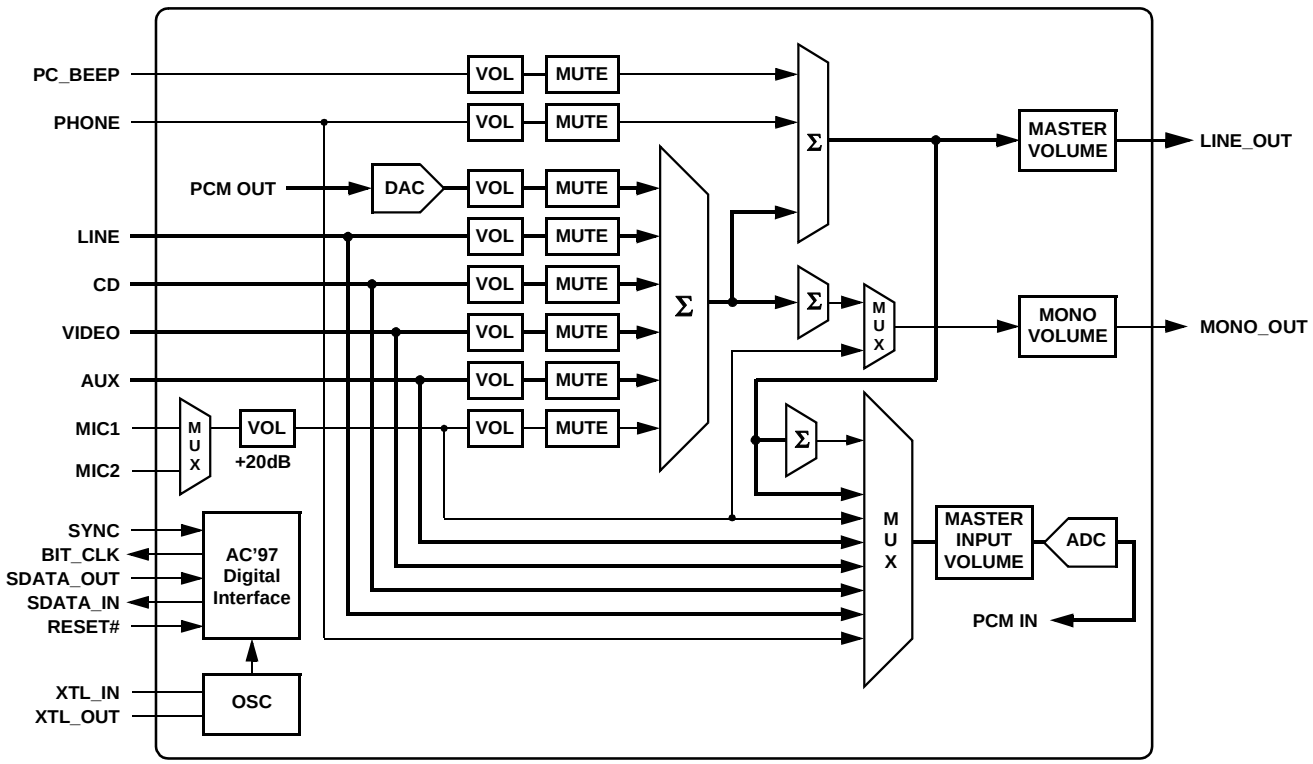


Figure 1. Functional Block Diagram

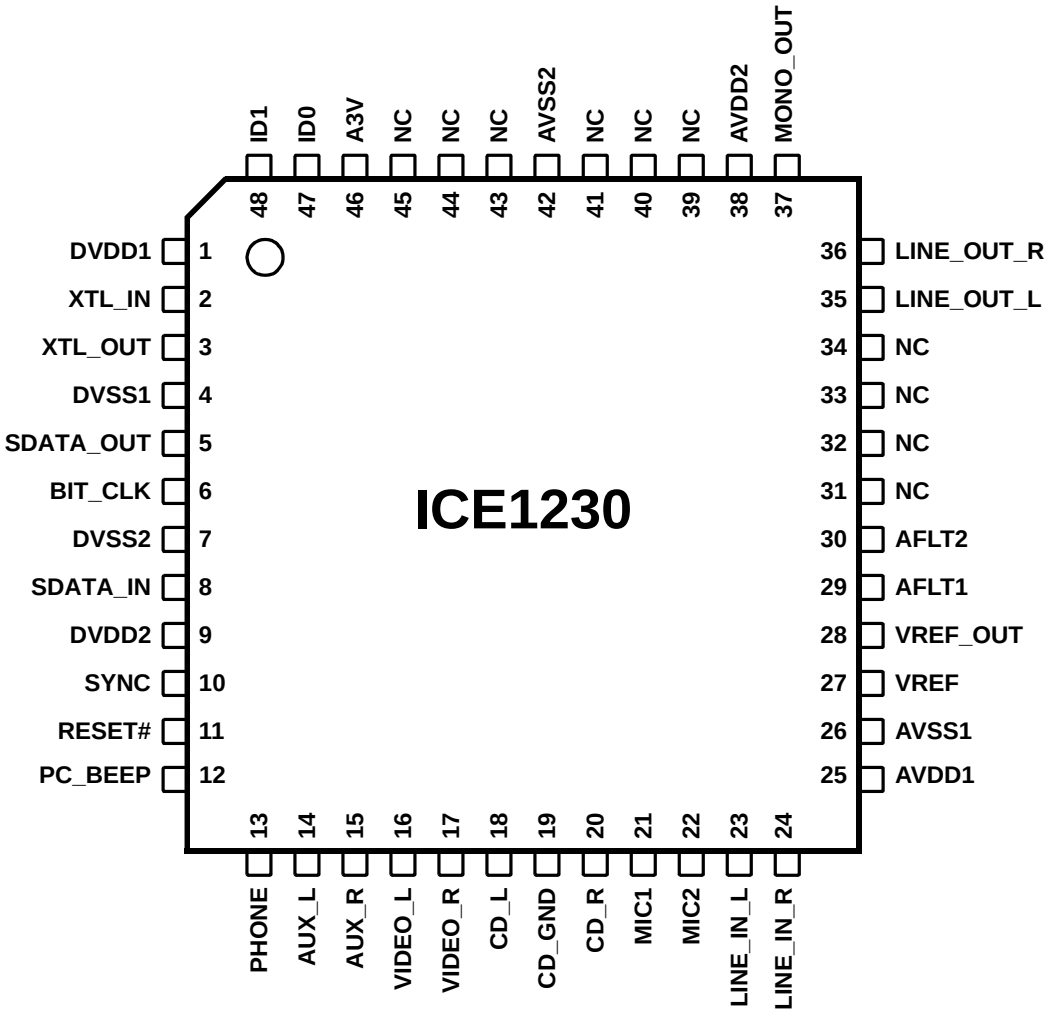


Figure 2. 48-pin TQFP/LQFP

Table 1. Pin Description

Pin #	Symbol	Type	Description
1	DVDD1	I	Digital Supply Voltage, 5V or 3.3V
2	XTL_IN	I	24.576MHz Crystal
3	XTL_OUT	O	24.576MHz Crystal
4	DVSS1	I	Digital Ground
5	SDATA_OUT	I	AC'97 Serial Data Input Stream
6	BIT_CLK	I/O	12.288MHz Serial Data Clock
7	DVSS2	I	Digital Ground
8	SDATA_IN	O	AC'97 Serial Data Output Stream
9	DVDD2	I	Digital Supply Voltage, 5V or 3.3V
10	SYNC	I	48kHz Fixed Rate Sync Pulse
11	RESET#	I	AC'97 Master Reset
12	PC_BEEP	I	PC Speaker Beep Pass Through
13	PHONE	I	Telephony Subsystem Speakerphone
14	AUX_L	I	Auxiliary Audio Left Channel
15	AUX_R	I	Auxiliary Audio Right Channel
16	VIDEO_L	I	Video Audio Left Channel
17	VIDEO_R	I	Video Audio Right Channel
18	CD_L	I	CD Audio Left Channel
19	CD_GND	I	CD Audio Analog Ground
20	CD_R	I	CD Audio Right Channel
21	MIC1	I	Desktop Microphone
22	MIC2	I	Second Microphone
23	LINE_IN_L	I	Line In Left Channel
24	LINE_IN_R	I	Line In Right Channel
25	AVDD1	I	Analog Supply Voltage, 5V or 3.3V
26	AVSS1	I	Analog Ground
27	VREF	I	Reference Voltage
28	VREFOUT	O	Reference Voltage Output
29	AFLT1	O	Left Channel Anti-Aliasing Filter Capacitor
30	AFLT2	O	Right Channel Anti-Aliasing Filter Capacitor
31	NC	–	No Connect
32	NC	–	No Connect
33	NC	–	No Connect
34	NC	–	No Connect
35	LINE_OUT_L	O	Line Out Left Channel
36	LINE_OUT_R	O	Line Out Right Channel
37	MONO_OUT	O	Mono Output

Table 1. Pin Description (*continued...)*

Pin #	Symbol	Type	Description
38	AVDD2	I	Analog Supply Voltage, 5V or 3.3V
39	NC	–	No Connect
40	NC	–	No Connect
41	NC	–	No Connect
42	AVSS2	I	Analog Ground
43	NC	–	No Connect
44	NC	–	No Connect
45	NC	–	No Connect
46	A3V	I	3.3V Analog Operation Select (A3V = high, AVDD = 3.3V enabled)
47	ID0	I	Multiple Codec Select (Internal pull-down). *Please see **Table 16**.*
48	ID1	I	Multiple Codec Select (Internal pull-down). *Please see **Table 16**.*

Note: ICE 1230 supports mixed +5V and +3.3V power supply combinations except when DVDD=+5V and AVDD=+3.3V.

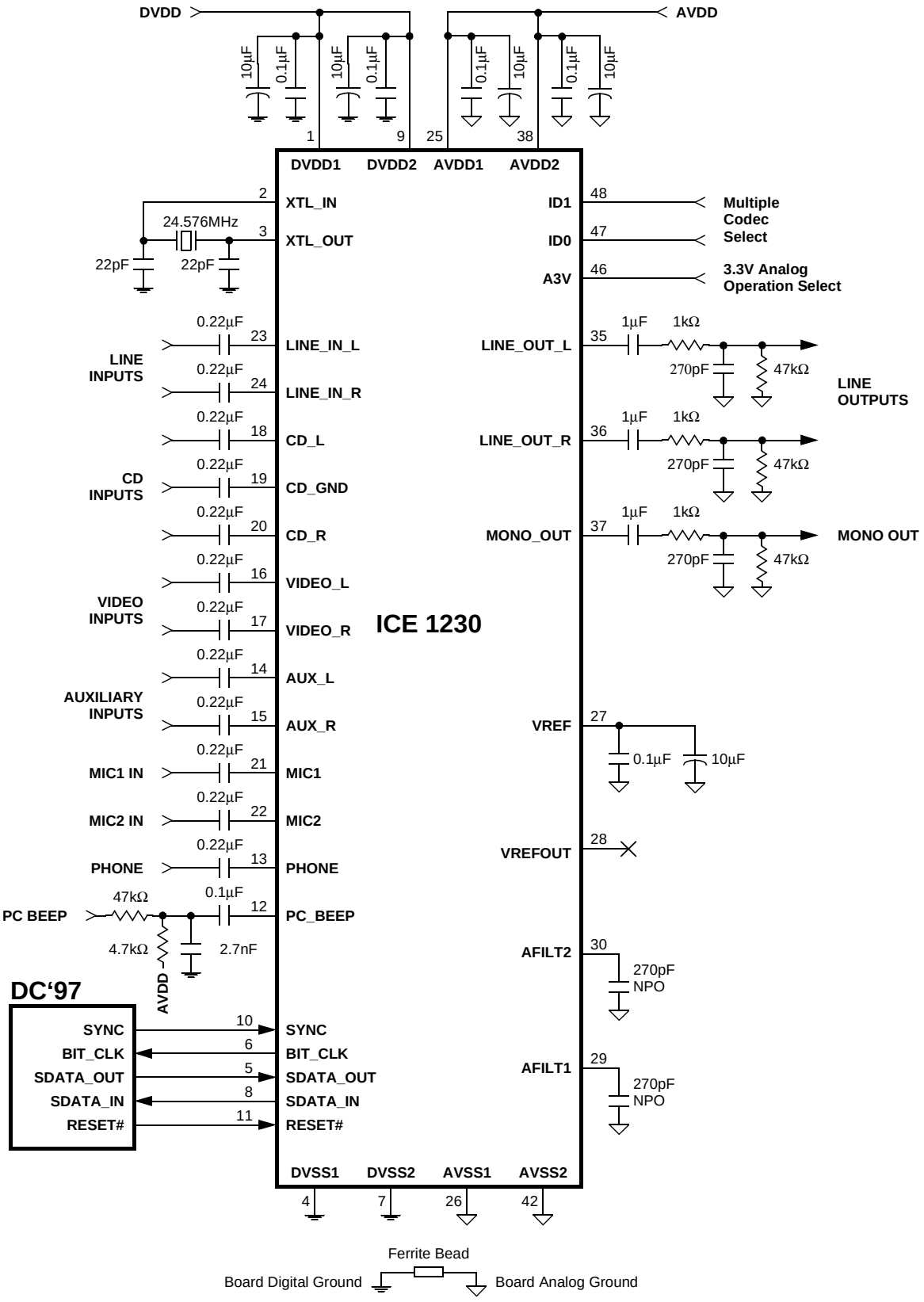


Figure 3. Typical Connection Diagram

Performance Specifications

Analog Performance Characteristics (+5V Power)

(T_A=25°C, AVDD = DVDD = 5.0V ± 5%; AVSS = DVSS =0V; 10kΩ / 50pF Load); F_S = 48kHz, 0dB = 1V_{RMS}; BW: 20Hz ~ 20kHz, 0dB Attentuation)

Symbol	Parameter		Min	Typ	Max	Unit
	Full Scale Input Voltage:	Line Inputs		1.0		V_{RMS}
		Mic Inputs (20dB = 0)		1.0		V_{RMS}
		Mic Inputs (20dB = 1)		0.1		V_{RMS}
	Full Scale Output Voltage:	Line Outputs		1.0		V_{RMS}
		Mono Output		1.0		V_{RMS}
	Analog S/N:	CD to LINE_OUT		91		dB
		Other to LINE_OUT		91		dB
	Analog Frequency Response		20		20,000	Hz
	Digital S/N:	DAC	85	89		dB
		ADC	75	92		dB
	Total Harmonic Distortion:	Line Outputs		0.007	0.02	%
	D/A and A/D Frequency Response:	DAC	20		19,200	Hz
		ADC	20		19,200	Hz
	Transition Band:	DAC	19,200		28,800	Hz
		ADC	19,200		28,800	Hz
	Stop Band:	DAC	28,800		infinity	Hz
		ADC	28,800		infinity	Hz
	Stop Band Rejection:	DAC	TBD			dB
		ADC	TBD			dB
	Out-of-Band Rejection			-40		dB
	Group Delay				1	ms
	Power Supply Rejection Ratio (1kHz)			-40		dB
	Input Channel Crosstalk				-70	dB
	Spurious Tone Reduction			-100		dB
	Attenuation, Gain Step Size			1.5		dB
	Input Impedance		10	50		kΩ
	Input Capacitance			15		pF
	V_{REFOUT}			2.4		V

Note: V_{IL} = 0.8V, V_{IH} = 2.4V
Analog Frequency Response has ±1dB limits
SNR of rms output level with 1kHz full-scale input to rms output level with all zeros into digital input
Measured "A wtd" over a 20Hz ~ 20kHz bandwidth (AES17-1991 Idle Channel Noise or EIAJ CP-307 SNR)
THD: 0dB gain, 20kHz BW, Fs = 48kHz
A/D and D/A Frequency Response has ±0.25dB limits
Stop Band Rejection determines filter requirements
Out-of-Band rejection determines audible noise
Integrated Out-of-band noise generated by DAC during normal PCM audio playback over: BW = 28.8kHz~100kHz, with respect to 1 V_{RMS} DAC output

Performance Specifications (*continued...*)

Table 2. Analog Performance Characteristics (+3.3V Power)

(T_A=25°C, AVDD = DVDD = 3.3V ± 5%; AVSS = DVSS =0V; 10kΩ / 50pF Load); F_S = 48kHz, 0dB = 0.70V_{RMS}; BW: 20Hz ~ 20kHz, 0dB Attenuation)

Symbol	Parameter		Min	Typ	Max	Unit
	Full Scale Input Voltage:	Line Inputs		0.70		V_{RMS}
		Mic Inputs (20dB = 0)		0.70		V_{RMS}
		Mic Inputs (20dB = 1)		0.07		V_{RMS}
	Full Scale Output Voltage:	Line Outputs		0.70		V_{RMS}
		Mono Output		0.07		V_{RMS}
	Analog S/N:	CD to LINE_OUT		86		dB
		Other to LINE_OUT		86		dB
	Analog Frequency Response		20		20,000	Hz
	Digital S/N:	DAC		85		dB
		ADC		90		dB
	Total Harmonic Distortion:	Line Outputs		.007	0.02	%
	D/A and A/D Frequency Response:	DAC	20		19,200	Hz
		ADC	20		19,200	Hz
	Transition Band:	DAC	19,200		28,800	Hz
		ADC	19,200		28,800	Hz
	Stop Band:	DAC	28,800		infinity	Hz
		ADC	28,800		infinity	Hz
	Stop Band Rejection:	DAC	TBD			dB
		ADC	TBD			dB
	Out-of-Band Rejection			-40		dB
	Group Delay				1	ms
	Power Supply Rejection Ration (1kHz)			-40		dB
	Input Channel Crosstalk				-70	dB
	Spurious Tone Reduction			-100		dB
	Attenuation, Gain Step Size			1.5		dB
	Input Impedance		10	50		kΩ
	Input Capacitance			15		pF
	V_{REFOUT}			1.5		V

Note: V_{IL} = 0.8V, V_{IH} = 2.4V
Analog Frequency Response has ±1dB limits
SNR of rms output level with 1kHz full-scale input to rms output level with all zeros into digital input
Measured "A wtd" over a 20Hz ~ 20kHz bandwidth (AES17-1991 Idle Channel Noise or EIAJ CP-307 SNR)
THD: 0dB gain, 20kHz BW, Fs = 48kHz
A/D and D/A Frequency Response has ±0.25dB limits
Stop Band Rejection determines filter requirements
Out-of-Band rejection determines audible noise
Integrated Out-of-band noise generated by DAC during normal PCM audio playback over: BW = 28.8kHz~100kHz, with respect to 0.70 V_{RMS} DAC output

Performance Specifications (*continued...*)

Table 3. Miscellaneous Analog Performance Characteristics

(T_A=25°C, AVDD = DVDD = 5.0V ± 5%; AVSS = DVSS =0V; 10kΩ / 50pF Load); F_S = 48kHz, 0dB = 1V_{RMS}; BW: 20Hz ~ 20kHz, 0dB Attentuation)

Symbol	Parameter	Min	Typ	Max	Unit
	Mixer Gain Range Span:				
	LINE_IN, AUX, VIDEO, MIC1, MIC2, PHONE, PC_BEEP		45		dB
	LINE_OUT, MONO_OUT		95		dB
	Mixer Step Size:				
	All Volume Controls except PC_BEEP		1.5		dB
	PC_BEEP		3.0		dB
	Mixer Mute Level		110		dB
	Mixer Gain: Interchannel Gain Mismatch	-0.5		0.5	dB
	Gain Drift		100		ppm/°C
	ADC and Analog Inputs (Rs=50Ω): Resolution			16	bits
	Gain Error		± 2	± 5	%
	Offset Error		10		mV
	Input Impedance		50		kΩ
	DAC and Analog Outputs: Resolution			16	bits
	Interchannel Isolation		85		dB
	Interchannel Gain Mismatch		0.1	0.2	dB
	Gain Error			± 5	%
	Gain Drift		60		ppm/°C

Electrical Specifications

Table 4. DC Characteristics

(T_A=25°C, AVDD = DVDD = 5.0V or 3.3V ± 5%; AVSS = DVSS =0V; 50pF Load)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	-0.3		V_{DD}+0.3	V
V_{IL}	Input Low Voltage			0.3 x V_{DD}	V
V_{IH}	Input High Voltage	0.4 x V_{DD}			V
V_{OL}	Output Low Voltage			0.2 x V_{DD}	V
V_{OH}	Output High Voltage	0.5 x V_{DD}			V
–	Input Leakage Current (AC-Link)	-10		10	µA
–	Output Leakage Current (AC-Link and Hi-Z)	-10		10	µA
–	Output Buffer Drive Current		TBD		mA

Electrical Specifications (*continued...*)

Table 5. Power Consumption (+5V Power)

(T_A=25°C, AVDD = DVDD = 5.0V ± 5%; AVSS = DVSS =0V; 50pF Load)

Symbol	Parameter	Min	Typ	Max	Unit
I_{VDD}	Digital Supply Current: Power Up		70		mA
I_{VDD}	Digital Supply Current: Power Down		TBD		mA
I_{AVDD}	Analog Supply Current: Power Up		28		mA
I_{AVDD}	Analog Supply Current: Power Down		TBD		mA

Table 6. Power Consumption (+3.3V Power)

(T_A=25°C, AVDD = DVDD = 3.3V ± 5%; AVSS = DVSS =0V; 50pF Load)

Symbol	Parameter	Min	Typ	Max	Unit
I_{VDD}	Digital Supply Current: Power Up		33		mA
I_{VDD}	Digital Supply Current: Power Down		TBD		mA
I_{AVDD}	Analog Supply Current: Power Up		18		mA
I_{AVDD}	Analog Supply Current: Power Down		TBD		mA

AC Timing Characteristics

(Test Conditions: T_A=25°C, AVDD = DVDD = 5.0V or 3.3V ± 5%; AVSS = DVSS =0V; 50pF Load)

Table 7. Cold Reset

Symbol	Parameter	Min	Typ	Max	Unit
T_{RST_LOW}	RESET# Active Low Pulse Width	1			µs
$T_{RST2CLK}$	RESET# Inactive to BIT_CLK Startup Delay	162.8			ns

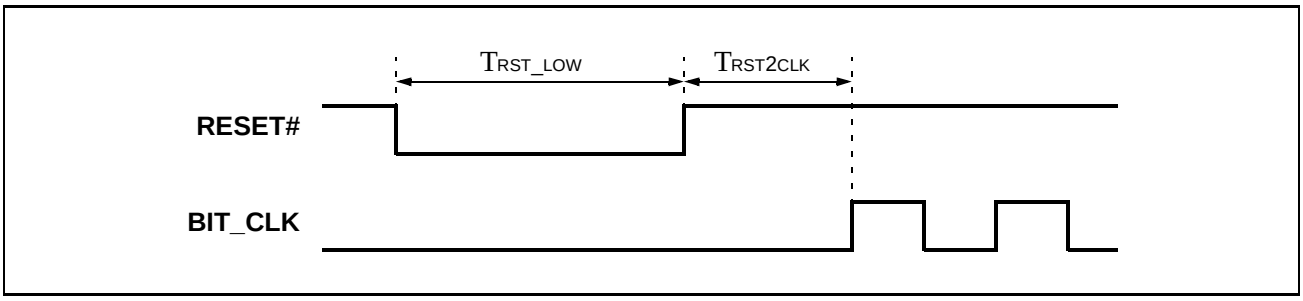


Figure 4. Cold Reset Timing

AC Timing Characteristics (*continued...*)

Table 8. Warm Reset

Symbol	Parameter	Min	Typ	Max	Unit
TSYNC_HIGH	Sync Active High Pulse Width		1.3		µs
TSYNC2CLK	SYNC Inactive to BIT_CLK Startup Delay	162.8			ns

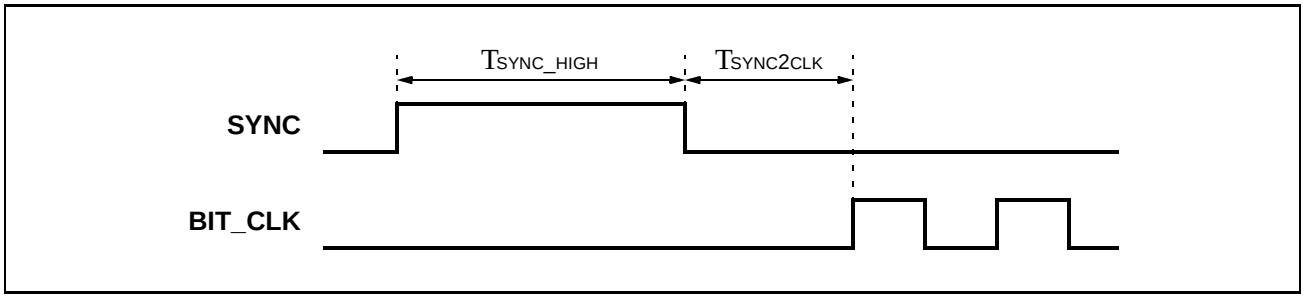


Figure 5. Warm Reset Timing

Table 9. BIT_CLK / SYNC Timing

Symbol	Parameter	Min	Typ	Max	Unit
	BIT_CLK Frequency		12.288		MHz
TCLK_PERIOD	BIT_CLK Period		81.4		ns
	BIT_CLK Output Jitter			750	ps
TCLK_HIGH	BIT_CLK Pulse Width (high)	32.56	40.7	48.84	ns
TCLK_LOW	BIT_CLK Pulse Width (low)	32.56	40.7	48.84	ns
TCLK_DC	BIT_CLK Duty Cycle	40		60	%
	SYNC Frequency		48		kHz
TSYNC_PERIOD	SYNC Period		20.8		µs
TSYNC_HIGH	SYNC Pulse Width (high)		1.3		µs
TSYNC_LOW	SYNC Pulse Width (low)		19.5		µs

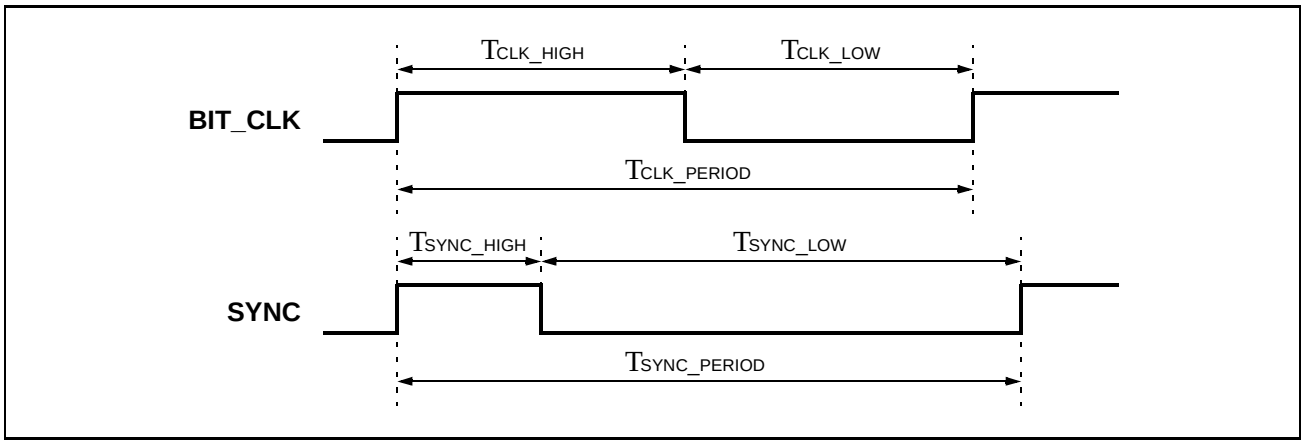


Figure 6. BIT_CLK to SYNC Timing

AC Timing Characteristics (*continued...*)

Table 10. Setup and Hold

Symbol	Parameter	Min	Typ	Max	Unit
TSETUP1	SDATA_OUT Setup to falling edge of BIT_CLK	15			ns
THOLD1	SDATA_OUT Hold from falling edge of BIT_CLK	5			ns
TSETUP2	SYNC Setup to rising edge of BIT_CLK	15			ns
THOLD2	SYNC Hold to rising edge of BIT_CLK	5			ns

Note: SDATA_IN seup and hold calculations determined by AC'97 controller propagation delay.

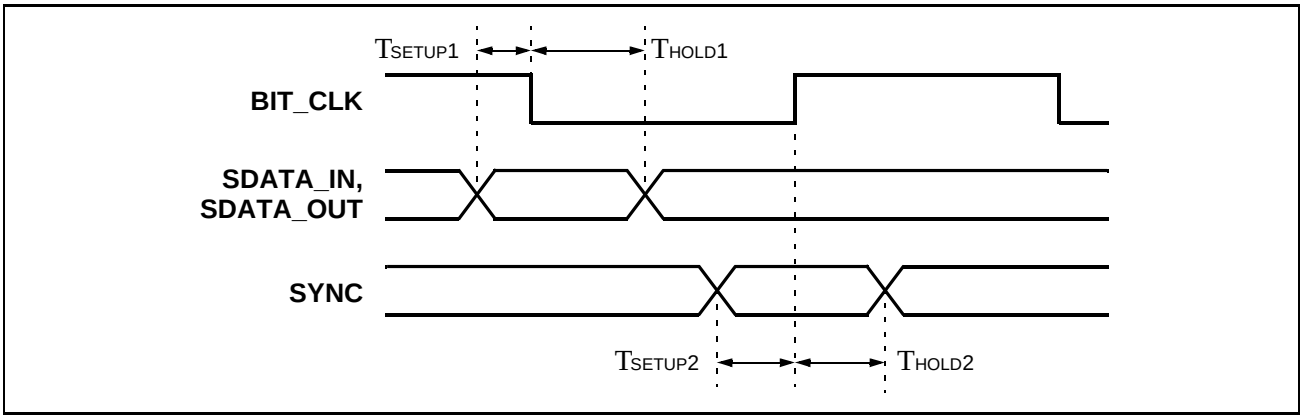


Figure 7. Setup and Hold Time

Table 11. Rise and Fall Time

Symbol	Parameter	Min	Typ	Max	Unit
TRISE	BIT_CLK rise time	2		6	ns
TFALL	BIT_CLK fall time	2		6	ns
TRISE	SYNC rise time	2		6	ns
TFALL	SYNC fall time	2		6	ns
TRISE	SDATA_IN rise time	2		6	ns
TFALL	SDATA_OUT fall time	2		6	ns
TRISE	SDATA_OUT rise time	2		6	ns
TFALL	SDATA_OUT fall time	2		6	ns

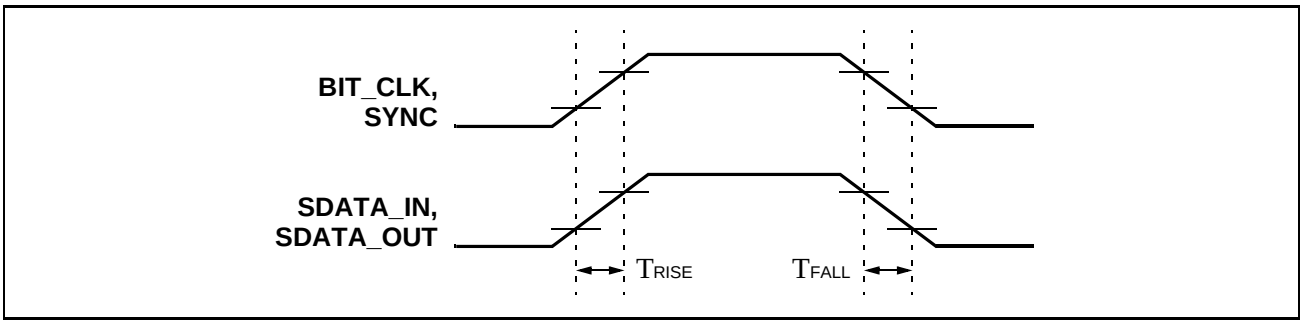


Figure 8. Rise Time and Fall Time

AC Timing Characteristics (*continued...*)

Table 12. AC Link Low Power Mode

Symbol	Parameter	Min	Typ	Max	Unit
T_{S2_PDOWN}	End of Slot 2 to BIT_CLK / SDATA_IN low			1	µs

Note: BIT_CLK not to scale.

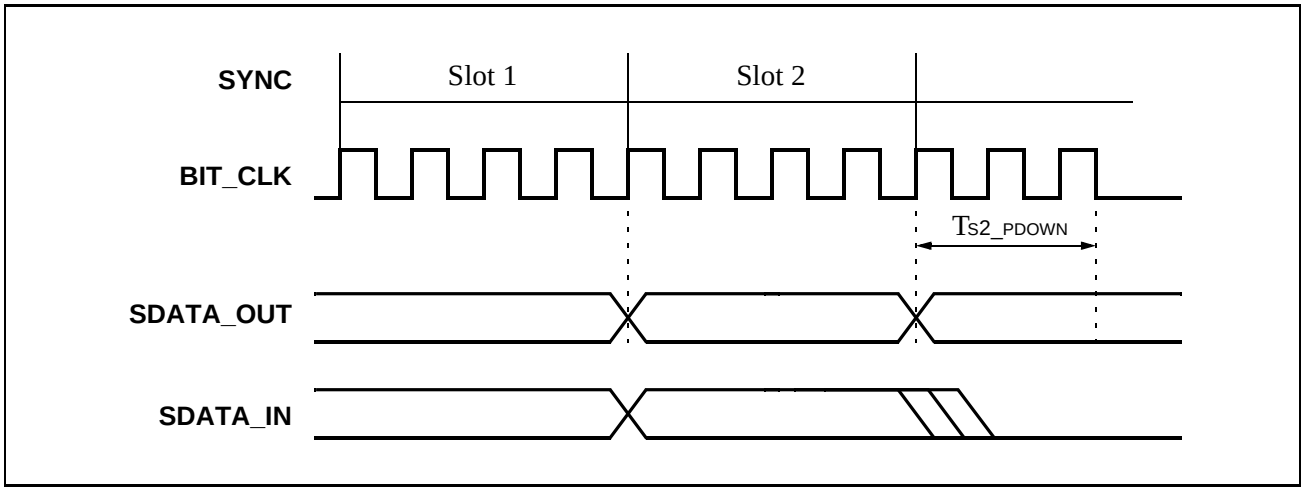


Figure 9. AC Link Power Mode Timing

Table 13. ATE/Vendor Test Mode

Symbol	Parameter	Min	Typ	Max	Unit
$T_{SETUP2RST}$	SDATA_OUT/SYNC setup to RESET# rising edge	15			ns
T_{OFF}	RESET# rising edge to Hi-Z state			25	ns

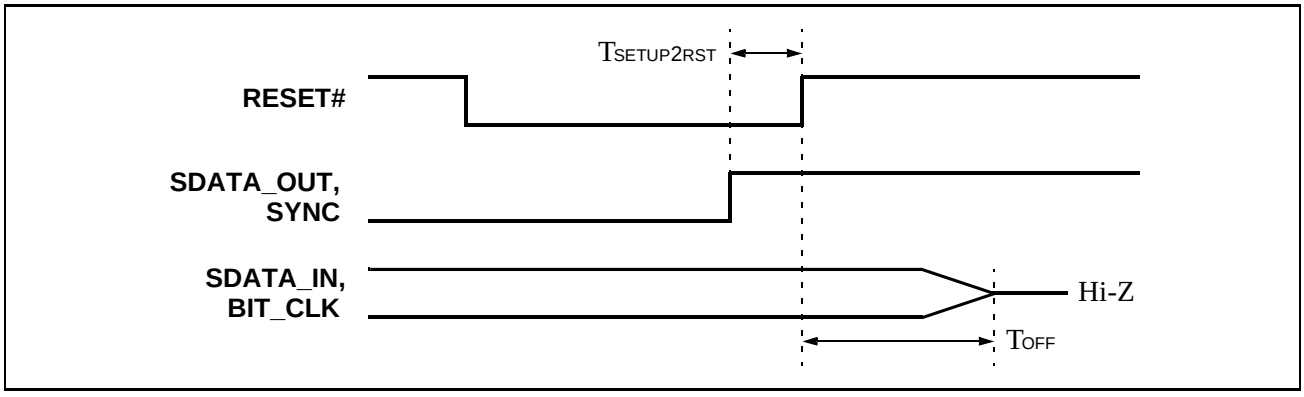


Figure 10. ATE/Vendor Test Mode Timing

Register Map

Index	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	Reset	–	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
02h	Stereo Output Volume	Mute	–	ML5	ML4	ML3	ML2	ML1	ML0	–	–	MR5	MR4	MR3	MR2	MR1	MR0
06h	Mono Output Volume	Mute	–	–	–	–	–	–	–	–	–	MM5	MM4	MM3	MM2	MM1	MM0
0Ah	PC Beep Volume	Mute	–	–	–	–	–	–	–	–	–	–	PV3	PV2	PV1	PV0	–
0Ch	Phone Volume	Mute	–	–	–	–	–	–	–	–	–	–	GN4	GN3	GN2	GN1	GN0
0Eh	Mic In Volume	Mute	–	–	–	–	–	–	–	–	20dB	–	GN4	GN3	GN2	GN1	GN0
10h	Line In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
12h	CD In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
14h	Video In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
16h	Aux In Volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
18h	PCM Out volume	Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0
1Ah	Record Select	–	–	–	–	–	SL2	SL1	SL0	–	–	–	–	–	SR2	SR1	SR0
1Ch	Record Gain	–	–	–	–	GL3	GL2	GL1	GL0	–	–	–	–	GR3	GR2	GR1	GR0
20h	General Purpose	–	–	–	–	–	–	MIX	MS	LPBK	–	–	–	–	–	–	–
26h	Power Down & Status	–	–	PR5	PR4	PR3	PR2	PR1	PR0	–	–	–	–	REF	ANL	DAC	ADC
28h	Reserved	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
5Ah	Test Control Register	–	–	–	–	–	–	–	–	ADC1	ENL	ADC2	DAC	–	–	–	–
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
7Ah	Vendor Reserved	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

Register Description

Reset Register (Index 00h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0000h

The Reset register is used to configure the hardware to a known state or is used to read the status of the current hardware configuration. Writing data to this register will set all the mixer registers to their default values. Reading data from this register will return the ID code for the device.

Register Description (*continued...*)

Stereo Output Control Register (Index 02h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	ML5	ML4	ML3	ML2	ML1	ML0	–	–	MR5	MR4	MR3	MR2	MR1	MR0	8000h

Mute **Stereo Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

ML[5:0] **Master Output (Left Channel) Volume Control**

These six bits select the level of attenuation applied to the Left channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -94.5dB in 1.5dB increments, providing a total of 64 programmable levels. Please refer to **Table 14** on page 14 for details.

MR[5:0] **Master Output (Right Channel) Volume Control**

These six bits select the level of attenuation applied to the Right channel of the Stereo Output signal. The level of attenuation is programmable from 0dB to -94.5dB in 1.5dB increments, providing a total of 64 programmable levels. Please refer to **Table 14** on page 14 for details.

Mono Output Control Register (Index 06h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	–	MM5	MM4	MM3	MM2	MM1	MM0	8000h

Mute **Mono Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

MM[5:0] **Mono Output Volume Control**

These six bits select the level of attenuation applied to the Mono Output signal. The level of attenuation is programmable from 0dB to -94.5dB in 1.5dB increments, providing a total of 64 programmable levels. Please refer to **Table 14** on page 14 for details.

Table 14. Stereo and Mono Output Attenuation

	M5	M4	M3	M2	M1	M0	Level (dB)
0	0	0	0	0	0	0	0.0
1	0	0	0	0	0	1	-1.5
2	0	0	0	0	1	0	-3.0
3	0	0	0	0	1	1	-4.5
4	0	0	0	1	0	0	-6.0
5	0	0	0	1	0	1	-7.5
..	..	..	..	..	..	..	..
..	..	..	..	..	..	..	..
60	1	1	1	1	0	0	-90.0
61	1	1	1	1	0	1	-91.5
62	1	1	1	1	1	0	-93.0
63	1	1	1	1	1	1	-94.5

Register Description (*continued...*)

PC Beep Input Volume Control Register (Index 0Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	–	–	PV3	PV2	PV1	PV0	–	0000h

Mute **PC Beep Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

PV[3:0] **PC Beep Input Volume Control**

These four bits select the level of attenuation applied to the PC beep input signal. The level of attenuation is programmable from 0dB to -45dB in 3dB increments, providing a total of 16 programmable levels. The beep gain is set at 0dB when PV[3:0] = 0h.

Phone Input Volume Control Register (Index 0Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	–	–	GN4	GN3	GN2	GN1	GN0	8008h

Mute **Phone Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GN[4:0] **Phone Input Volume Control**

These five bits select the gain applied to the Phone Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

Mic Input Volume Control Register (Index 0Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	–	–	–	–	–	20dB	–	GN4	GN3	GN2	GN1	GN0	8008h

Mute **Mic Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

20dB **Mic Boost Control**

"1" : Fixed 20dB gain enabled

"0" : Fixed 20dB gain disabled

GN[4:0] **Mic Input Volume Control**

These five bits select the gain applied to the Mic Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

Register Description (*continued...*)

Line Input Control Register (Index 10h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **Line Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the Line Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

CD Input Control Register (Index 12h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **CD Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the CD Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the CD Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

Register Description (*continued...*)

Video Input Control Register (Index 14h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **Video Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the Video Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the Video Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

Auxiliary Input Control Register (Index 16h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **Auxiliary Input Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the Auxiliary Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the Auxiliary Input signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

Register Description (*continued...*)

PCM Output Control Register (Index 18h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	GL4	GL3	GL2	GL1	GL0	–	–	–	GR4	GR3	GR2	GR1	GR0	8808h

Mute **PCM Output Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GL[4:0] **Left Channel Gain Control**

These five bits select the gain applied to the LEFT channel of the PCM Output signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

GR[4:0] **Right Channel Gain Control**

These five bits select the gain applied to the RIGHT channel of the PCM Output signal. The gain is programmable from -34.5dB to 12dB in 1.5dB increments, providing a total of 32 programmable levels. Please refer to **Table 15** on page 19 for details.

Record Select Register (Index 1Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	–	–	–	SL2	SL1	SL0	–	–	–	–	–	SR2	SR1	SR0	0000h

SL[2:0] **Record Source Select (Left Channel)**

These bits determine the record source for the left channel.

SL2	SL1	SL0	Left Record Source
0	0	0	Mic
0	0	1	CD (L)
0	1	0	Video In (L)
0	1	1	Aux In (L)
1	0	0	Line In (L)
1	0	1	Stereo Mix (L)
1	1	0	Mono Mix
1	1	1	Phone

SR[2:0] **Record Source Select (Right Channel)**

These bits determine the record source for the right channel.

SR2	SR1	SR0	Right Record Source
0	0	0	Mic
0	0	1	CD (R)
0	1	0	Video In (R)
0	1	1	Aux In (R)
1	0	0	Line In (R)
1	0	1	Stereo Mix (R)
1	1	0	Mono Mix
1	1	1	Phone

Register Description (*continued...*)

Table 15. Programmable Input and Output Gain Levels

	G4	G3	G2	G1	G0	Level (dB)
0	0	0	0	0	0	12.0
1	0	0	0	0	1	10.5
2	0	0	0	1	0	9.0
3	0	0	0	1	1	7.5
4	0	0	1	0	0	6.0
5	0	0	1	0	1	4.5
6	0	0	1	1	0	3.0
7	0	0	1	1	1	1.5
8	0	1	0	0	0	0.0
9	0	1	0	0	1	-1.5
10	0	1	0	1	0	-3.0
11	0	1	0	1	1	-4.5
12	0	1	1	0	0	-6.0
13	0	1	1	0	1	-7.5
14	0	1	1	1	0	-9.0
15	0	1	1	1	1	-10.5
16	1	0	0	0	0	-12.0
17	1	0	0	0	1	-13.5
18	1	0	0	1	0	-15.0
19	1	0	0	1	1	-16.5
20	1	0	1	0	0	-18.0
21	1	0	1	0	1	-19.5
22	1	0	1	1	0	-21.0
23	1	0	1	1	1	-22.5
24	1	1	0	0	0	-24.0
25	1	1	0	0	1	-25.5
26	1	1	0	1	0	-27.0
27	1	1	0	1	1	-28.5
28	1	1	1	0	0	-30.0
29	1	1	1	0	1	-31.5
30	1	1	1	1	0	-33.0
31	1	1	1	1	1	-34.5

Register Description (*continued...*)

Record Gain Control Register (Index 1Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
Mute	–	–	–	GL3	GL2	GL1	GL0	–	–	–	–	GR3	GR2	GR1	GR0	8000h

Mute **Record Mute Control**

"1" : Mute enabled

"0" : Mute disabled

GL[3:0] **Record Gain Control (Left Channel)**

These four bits select the gain applied to the LEFT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16 programmable levels. The gain is set at 0dB when GL[3:0] = 0h.

GR[3:0] **Record Gain Control (Right Channel)**

These four bits select the gain applied to the RIGHT channel recording source. The gain is programmable from 0dB to 22.5dB in 1.5dB increments, providing a total of 16 programmable levels. The gain is set at 0dB when GR[3:0] = 0h.

General Purpose Register (Index 20h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	–	–	–	–	MIX	MS	LPBK	–	–	–	–	–	–	–	0000h

MIX **Mono Output Mode**

"1" : Mic Output

"0" : Mono mix output

MS **Microphone Select**

"1" : Microphone 2

"0" : Microphone 1

LPBK **Loopback Mode**

"1" : DAC/ADC Loopback enabled

"0" : DAC/ADC Loopback disabled

Register Description (*continued...*)

Power Down and Status Register (Index 26h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	PR5	PR4	PR3	PR2	PR1	PR0	–	–	–	–	REF	ANL	DAC	ADC	0000h

PR[5:0] **Power Down Mode Bits**

These read/write bits are used to control the power down states of the ICE 1230. Each power down function bit is enabled by setting the respective bit high. The power down modes controlled by each bit is described in the table below:

Bit	Function
PR0	ADC and Mux Powerdown
PR1	DAC Powerdown
PR2	Mixer Powerdown (V_{REF} on)
PR3	Mixer Powerdown (V_{REF} off)
PR4	AC Link Powerdown (BIT_CLK off)
PR5	Internal Clock Disabled

Status (READ Only) bits

These bits are used to monitor the readiness of some sections of the ICE 1230. Reading a "1" from any of these bits would be an indication of a "ready" state.

Bit	Status Bit
REF	V_{REF} at nominal level
ANL	Mixer, Mux and Volume Controls ready
DAC	DAC ready to accept data
ADC	ADC ready to transmit data

Test Control Register (Index 5Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
–	–	–	–	–	–	–	–	ADC1	ENL	ADC2	DAC	–	–	–	–	0000h

Test Mode Bits

These four read/write bits are used for testing the digital modes of the audio codec.

Register Description (*continued...*)

Vendor Identification Register (Index 7Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	4943h

The upper and lower byte of this register (index 7Ch), in conjunction with the upper byte of index register 7Eh, make up the vendor identification code for the ICE 1230. The Vendor ID Code (in ASCII format) is equal to ICE, where:

F[7:0] **Upper Byte (Index 7Ch) D[15:8] = I**

S[7:0] **Lower Byte (Index 7Ch) D[7:0] = C**

T[15:8] **Upper Byte (Index 7Eh) D[15:8] = E**

Revision Identification Register (Index 7Eh)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	4501h

The upper byte of this register is used in conjuction with index register 7Ch to make up the Vendor ID code for the ICE 1230. The lower byte identifies the revision code of the ICE 1230.

T[15:8] **See description in Vendor Identification Register.**

REV[7:0] **Revision ID**

"01": Revision Number

Multiple Codec Extension

One primary and a maximum of three secondary codecs may be supported as an option.

Table 16. Multiple Codec Mode Select

ID1	ID0	Codec Mode
0	0	Primary Codec
0	1	Secondary Codec 1
1	0	Secondary Codec 2
1	1	Secondary Codec 3

Note: Digital Controller supports four DATA_IN pins to support one primary and three secondary codecs. BIT_CLK is an output for the primary codec and an input pin for the controller and secondary codecs. ID[1:0] pins with internal pull-down resistors select codec modes, default case = primary codec.

Multiple Codec Example

One primary codec and three secondary codecs, with tag bits ID[1:0] defining which codec is primary and the order of the secondary codecs. Note that the ID[1:0] pins are internally pulled down; therefore, an external 4.7kΩ pull-up resistor is necessary to pull the ID[1:0] pins high.

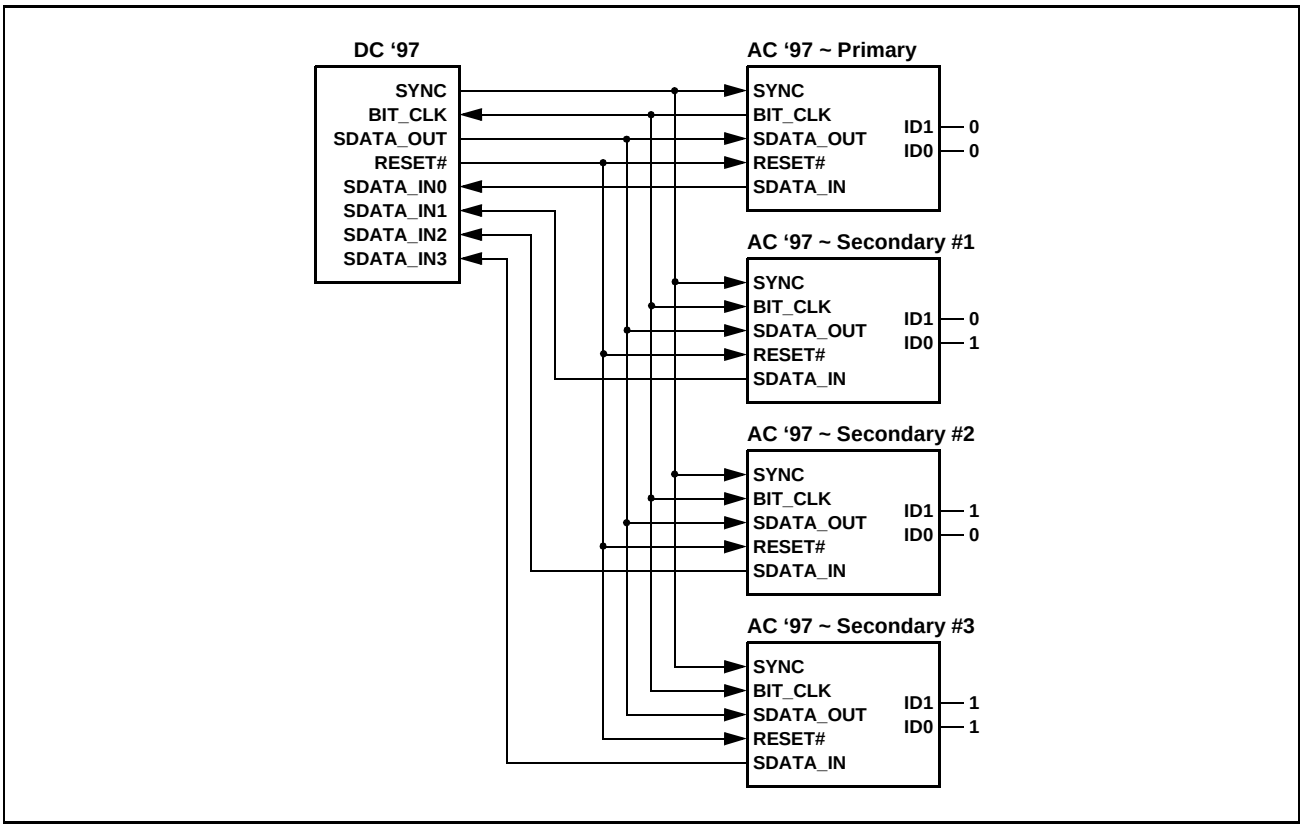


Figure 11. Multiple Codec Example

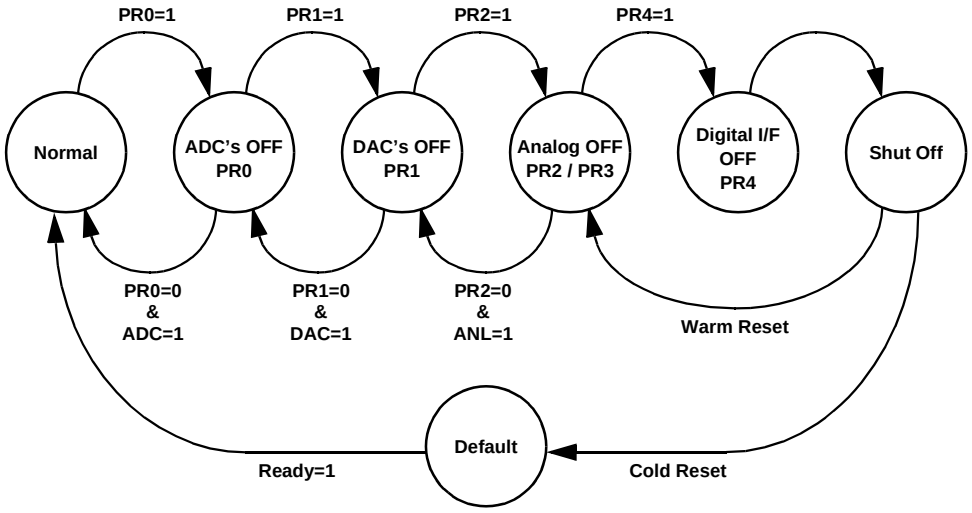
Power Management

The ICE1230 may be placed in several power down states using the power down control bits located in index register 26h. **Table 17** lists the power down states accessible through this register.

Table 17. Power Down Mode Bits

Bit	Function
PR0	ADC and Mux Powerdown
PR1	DAC Powerdown
PR2	Mixer Powerdown (VREF on)
PR3	Mixer Powerdown (VREF off)
PR4	AC Link Powerdown (BIT_CLK off)
PR5	Internal Clock Disabled

Note: Registers maintain values in sleep mode (PR4 write) and wake up with a warm reset (register values) or a cold reset (default values). Power Down and Status register (index 26h) read action verifies stability before power down write action occurs.



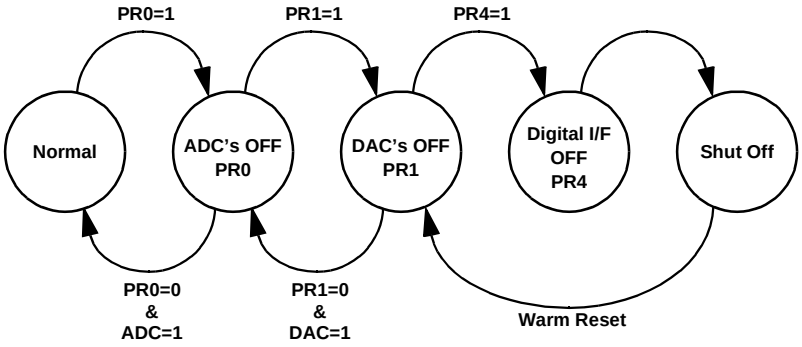
Note: In this example, the Analog Mixer has been disabled, but VREF is still on.

Figure 12. AC'97 Power Down / Power Up Procedure

Complete power down of the AC'97 device is achieved by sequential writes to the Power Down and Status Control Register (Index 26h) as follows:

Normal Operations:	PR[5:0] = 00h
ADC's and Input Mux:	PR0 = 1 (write)
DAC's:	PR1 = 1 (write)
Analog Mixer:	PR2 = 1 (write)
VREFOUT:	PR3 = 1 (write)
AC-Link:	PR4 = 1 (write)
Internal Clocks:	PR5 = 1 (write)

Power Management (*continued...*)



Note: To power up the codec, a warm reset is required; PR4 is reset to zero upon either reset.

Figure 13. AC'97 Power Down Procedure with Analog Section Still Active

Test Mode Operation

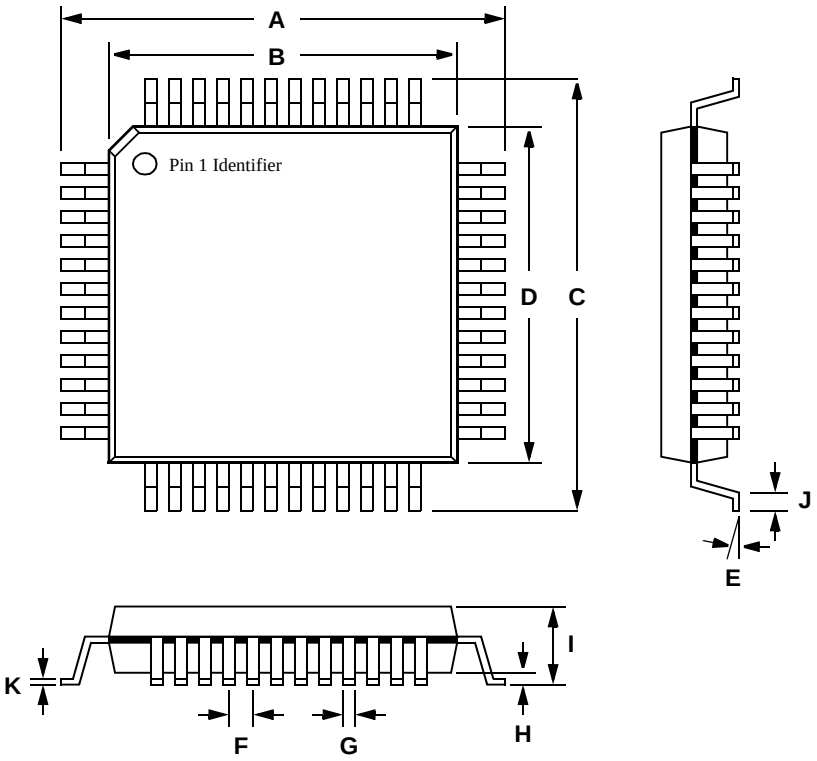
ATE Test Mode: (PCB in-circuit Testing of the ICE1230)

ATE Test mode is entered when the SDATA_OUT signal is sampled at the rising edge of the RESET# signal. In this mode, the SDATA_IN and BIT_CLK pins are placed in a high impedance (Hi-Z) state. This mode of operation doesn't occur under normal operating conditions.

Vendor Test Mode:

Vendor Test mode is entered when the SYNC signal is sampled during the rising edge of the RESET# signal. This mode of operation doesn't occur under normal operating conditions.

Package Dimensions



Mechanical Dimensions (millimeters, unless otherwise stated)

Symbol	A	B	C	D	E	F	G	H	I	J	K
48-pin (7x7) TQFP											
minimum	8.6	6.9	8.6	6.9	0°	0.5	0.17	0.05	1.0	0.45	0.100
maximum	9.4	7.1	9.4	7.1	10°		0.27	0.15		0.75	0.175
48-pin (7x7) LQFP											
minimum	8.6	6.9	8.6	6.9	0°	0.5	0.13	0.05	–	0.3	0.100
maximum	9.4	7.1	9.4	7.1	10°		0.28	0.15	1.7	0.7	0.175