

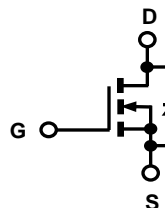
### ICE20N170B N-Channel Enhancement Mode MOSFET

Product Summary			
$I_D$	$T_A=25^\circ\text{C}$	20A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	600V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.17 $\Omega$	Typ
$Q_g$	$V_{DS}=480\text{V}$	62nC	Typ

#### Features

- Low  $r_{DS(on)}$
- Ultra Low Gate Charge
- High  $dv/dt$  capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 TO 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.



T0263

Standard Metal Heatsink

1=Gate, 2=Drain, 3=Source.

**Maximum ratings**<sup>b</sup>, at  $T_j=25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_c=25^\circ\text{C}$	20	A
Pulsed drain current	$I_{D, pulse}$	$T_c=25^\circ\text{C}$	62	A
Avalanche energy, single pulse	$E_{AS}$	$I_D=10\text{A}$	520	mJ
Avalanche current, repetitive	$I_{AR}$	limited by $T_j\text{max}$	20	A
MOSFET $dv/dt$ ruggedness	$dv/dt$	$V_{DS}=480\text{V}$ , $I_D=20\text{A}$ , $T_j=125^\circ\text{C}$	50	V/ns
Gate source voltage	$V_{GS}$	Static	$\pm 20$	V
		AC ( $f > 1\text{Hz}$ )	$\pm 30$	
Power dissipation	$P_{tot}$	$T_c=25^\circ\text{C}$	208	W
Operating and storage temperature	$T_j, T_{stg}$		-55 to +150	$^\circ\text{C}$

a When mounted on 1inch square 2oz copper clad FR-4

b Preliminary Data Sheet – Specifications subject to change

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

### Thermal characteristics

Thermal resistance, junction-case <sup>a</sup>	$R_{thJC}$		-	-	0.7	°C/W
Thermal resistance, junction-ambient <sup>a</sup>	$R_{thJA}$	leaded	-	-	62	
Soldering temperature, wave soldering only allowed at leads	$T_{sold}$	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

### Electrical characteristics <sup>b</sup>, at $T_j=25^{\circ}\text{C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\mu\text{A}$	600	640	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3	3.9	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=25^{\circ}\text{C}$	-	0.1	1	$\mu\text{A}$
		$V_{DS}=600\text{V}, V_{GS}=0\text{V}, T_j=150^{\circ}\text{C}$	-	-	100	
Gate source leakage current	$I_{GSS}$	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=10\text{A}, T_j=25^{\circ}\text{C}$	-	0.17	0.199	$\Omega$
		$V_{GS}=10\text{V}, I_D=10\text{A}, T_j=150^{\circ}\text{C}$	-	0.52	-	
Gate resistance	$R_G$	$f=1\text{ MHz}, \text{open drain}$	-	4.3	-	$\Omega$

#### Dynamic characteristics

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	-	2020	-	$\mu\text{F}$
Output capacitance	$C_{oss}$		-	980	-	
Reverse transfer capacitance	$C_{rss}$		-	9	-	
Transconductance	$g_{fs}$	$V_{DS}>2 * I_D * R_{DS}, I_D=10\text{A}$	-	19	-	S
Turn-on delay time	$t_{d(on)}$	$V_{DS}=380\text{V}, V_{GS}=10\text{V}, I_D=20\text{A}, R_G=4\Omega \text{ (External)}$	-	39	-	ns
Rise time	$t_r$		-	3.5	-	
Turn-off delay time	$t_{d(off)}$		-	55	-	
Fall time	$t_f$		-	7	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

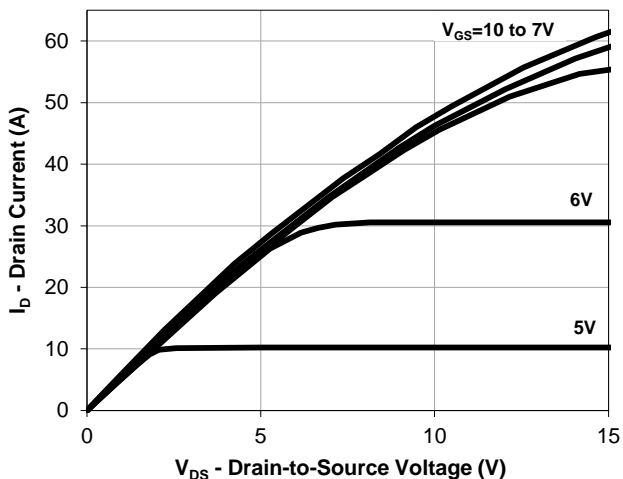
**Gate charge characteristics**

Gate to source charge	$Q_{gs}$	$V_{DS}=480\text{ V}, I_D=20\text{ A},$ $V_{GS}=10\text{ V}$	-	13	-	nC
Gate to drain charge	$Q_{gd}$		-	23	-	
Gate charge total	$Q_g$		-	62	-	
Gate plateau voltage	$V_{\text{plateau}}$		-	5.8	-	V

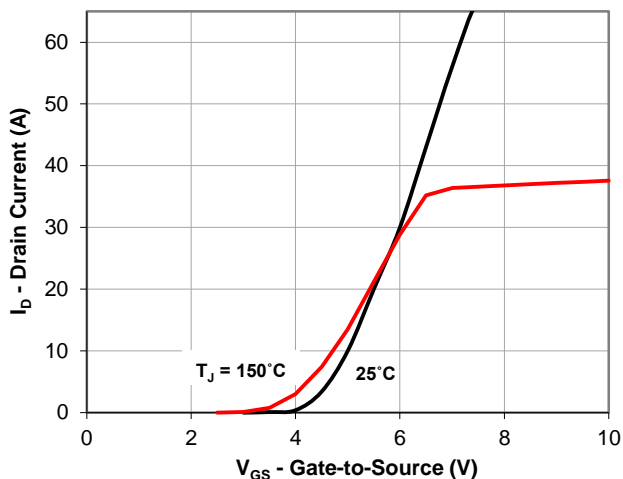
**Reverse Diode**

Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_S=I_F$	-	0.9	1.2	V
Reverse recovery time	$t_{rr}$	$V_{RR}=480\text{ V}, I_S=I_F,$ $d_{iF}/d_t=100\text{ A}/\mu\text{S}$	-	407	-	ns
Reverse recovery charge	$Q_{rr}$		-	6.7	-	$\mu\text{C}$
Peak reverse recovery current	$I_{rm}$		-	32	-	A

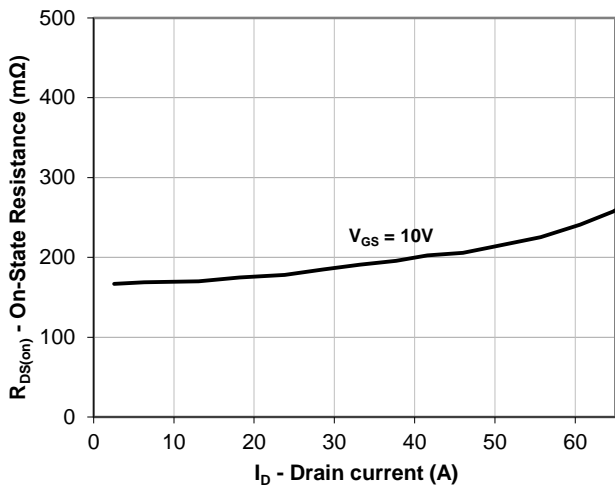
### Output Characteristics



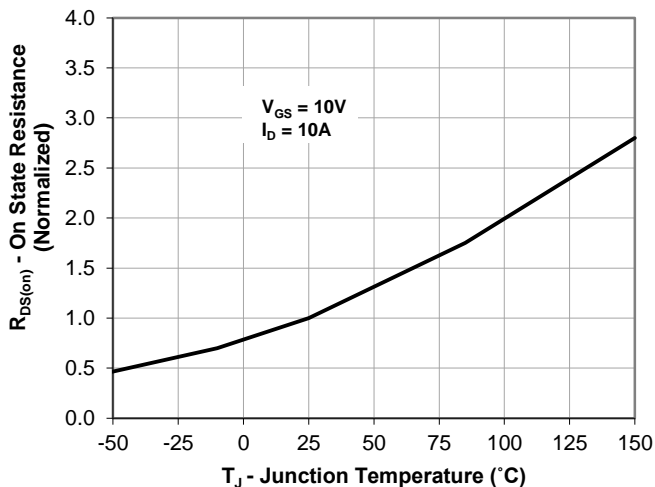
### Transfer Characteristics



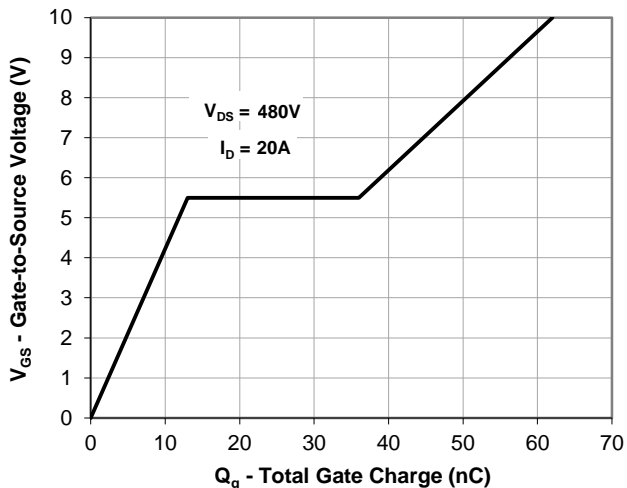
### On Resistance vs Drain Current



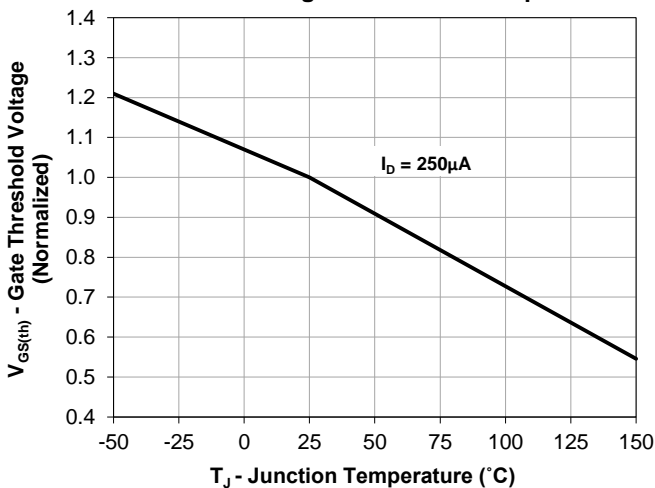
### On Resistance vs Junction Temperature

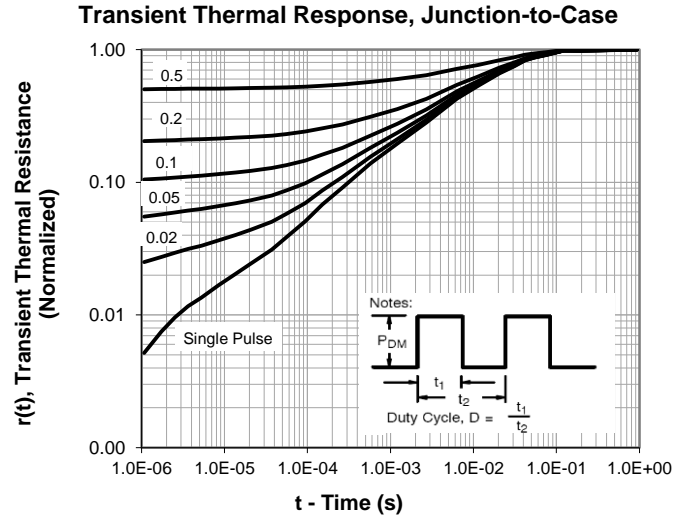
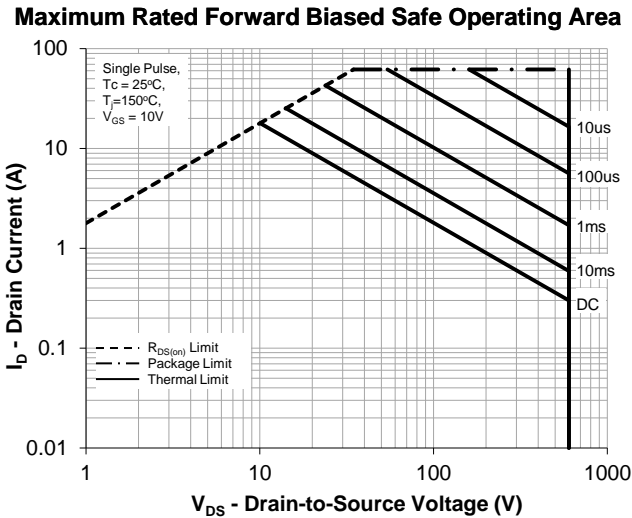
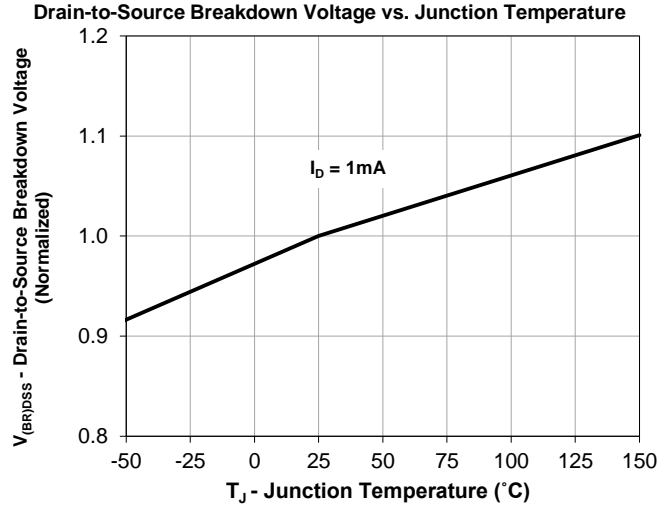
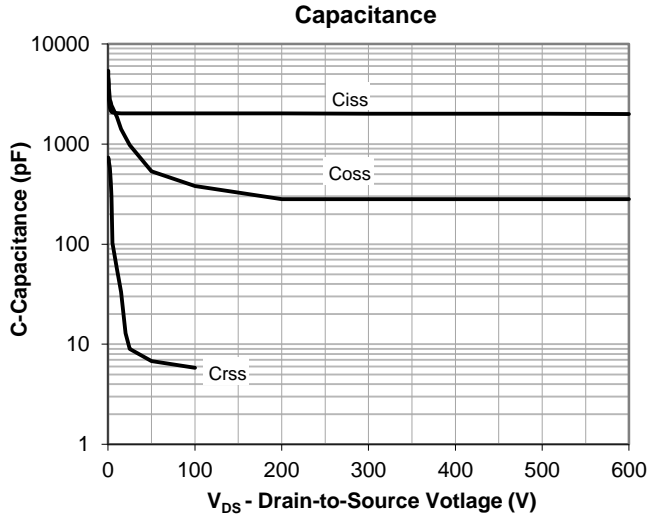


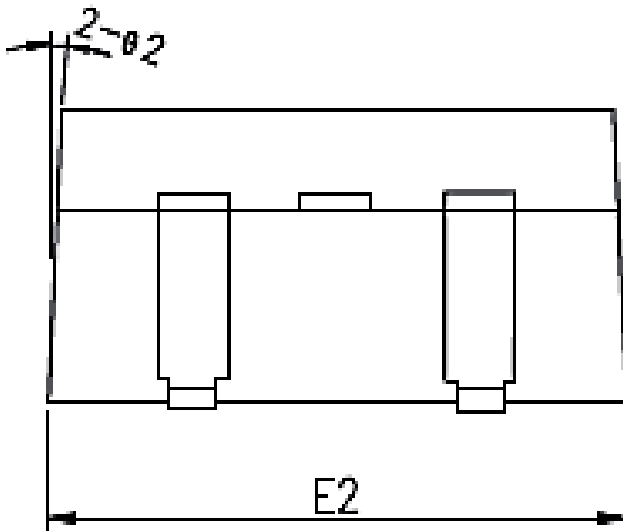
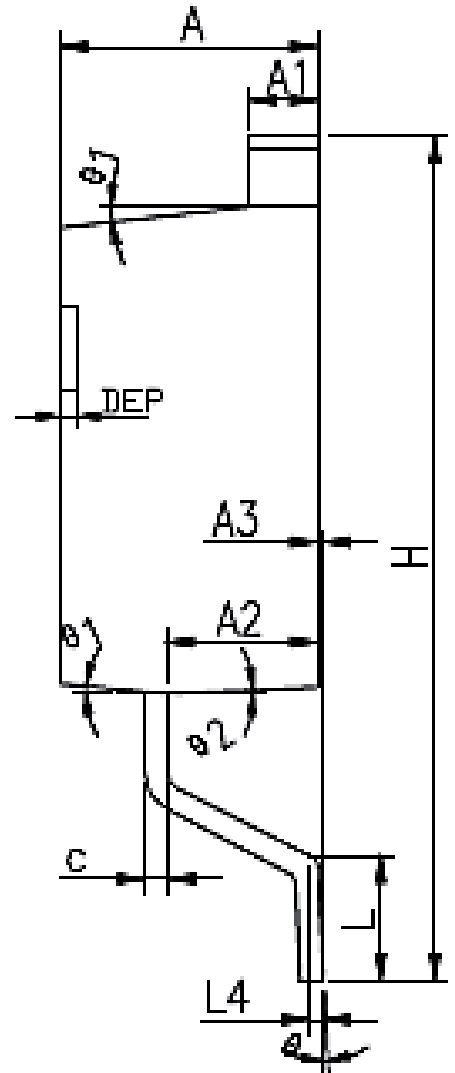
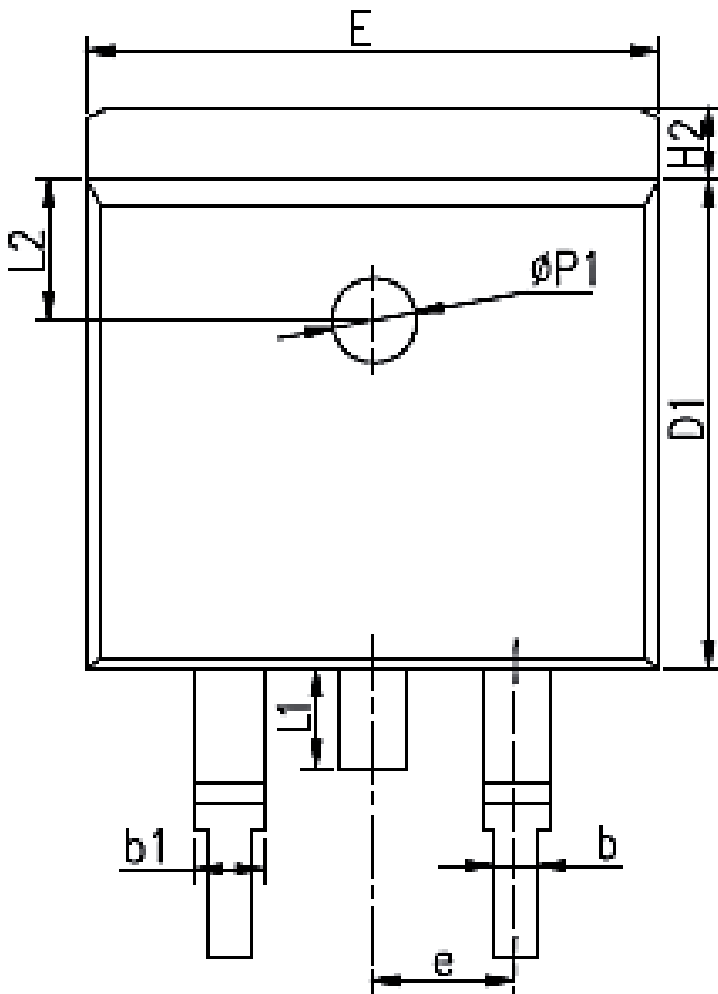
### Gate Charge



### Gate Threshold Voltage vs Junction Temperature







## COMMON DIMENSIONS

SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.22	1.27	1.32	0.048	0.050	0.052
A2	2.59	2.69	2.79	0.102	0.106	0.110
A3	0.00	0.10	0.20	0.000	0.004	0.008
b	0.77	0.813	0.90	0.030	0.032	0.035
b1	1.20	1.270	1.36	0.047	0.050	0.054
c	0.34	0.381	0.47	0.013	0.015	0.019
D1	8.60	8.70	8.80	0.339	0.343	0.346
E	10.00	10.16	10.26	0.394	0.400	0.404
E2	10.00	10.10	10.20	0.394	0.398	0.402
e	2.54 BSC			0.100 BSC		
H	14.70	15.10	15.50	0.579	0.594	0.610
H2	1.17	1.27	1.40	0.046	0.050	0.055
L	2.00	2.30	2.60	0.079	0.091	0.102
L1	1.45	1.55	1.70	0.057	0.061	0.067
L2	2.50 REF			0.098 REF		
L4	0.25 BSC			0.010 BSC		
θ	0°	5°	8°	0°	5°	8°
θ1	5°	7°	9°	5°	7°	9°
θ2	1°	3°	5°	1°	3°	5°
φP1	1.40	1.50	1.60	0.055	0.059	0.063
DEP	0.05	0.10	0.20	0.002	0.004	0.008

## **ICEMOS SUPERJUNCTION PATENT PORTFOLIO**

### **ICEMOS GRANTED PATENTS**

**US7,429,772**  
**US7,439,178**  
**US7,446,018**  
**US7,579,607**  
**US7,723,172**  
**US7,795,045**  
**US7,846,821**  
**US7,944,018**  
**US8,012,806**  
**US8,030,133**

### **3D SEMI PATENTS LICENSED TO ICEMOS**

**US7,041,560B2**  
**US7,023,069B2**  
**US7,364,994**  
**US7,227,197B2**  
**US7,304,944B2**  
**US7,052,982B2**  
**US7,339,252**  
**US7,410,891**  
**US7,439,583**  
**US7,227,197B2**  
**US6,635,906**  
**US6,936,867**  
**US7,015,104**  
**US9,109,110**  
**US7,271,067**  
**US7,354,818**  
**US7,052,982,**  
**US7,199,006B2**

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.



## Marking Information

**YY** = Last two digits of the year

**WW** = Work week calendar on Icemos subcon assembly & test house

**\*** = Initial for Icemos subcon assembly and test house

**XXXX** = Wafer Lot ID

**00** = may be used for wafer ID in a special case.  
= "00" is used unless specified.

**ICE20N170** = ICE is Icemos logo and 20N170 is a designated device part number

