

### ICE22N65W N-Channel Enhancement Mode MOSFET

RoHS compliant  
2011/65/EU



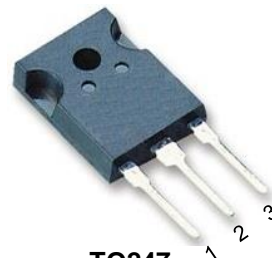
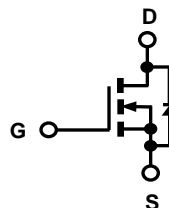
HALOGEN FREE

Product Summary			
$I_D$	$T_A=25^\circ\text{C}$	22A	Max
$V_{(BR)DSS}$	$I_D=250\mu\text{A}$	650V	Min
$r_{DS(on)}$	$V_{GS}=10\text{V}$	0.165 $\Omega$	Typ
$Q_g$	$V_{DS}=480\text{V}$	82nC	Typ

#### Features

- TO247 package
- Low  $r_{DS(on)}$
- Ultra Low Gate Charge
- High  $dv/dt$  capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 TO 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.



TO247  
1:G, 2:D,  
3:S, 4:D,  
(TO-247)

**Maximum ratings**<sup>b</sup>, at  $T_j=25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_c=25^\circ\text{C}$	22	A
Pulsed drain current	$I_{D, pulse}$	$T_c=25^\circ\text{C}$	66	A
Avalanche energy, single pulse	$E_{AS}$	$I_D=11.5\text{A}$	690	mJ
Avalanche current, repetitive	$I_{AR}$	limited by $T_{jmax}$	10	A
MOSFET $dv/dt$ ruggedness	$dv/dt$	$V_{DS}=480\text{V}$ , $I_D=22\text{A}$ , $T_j=125^\circ\text{C}$	50	V/ns
Gate source voltage	$V_{GS}$	Static	$\pm 20$	V
		AC ( $f > 1\text{Hz}$ )	$\pm 30$	
Power dissipation	$P_{tot}$	$T_c=25^\circ\text{C}$	208	W
Operating and storage temperature	$T_j, T_{stg}$		-55 to +150	$^\circ\text{C}$
Mounting torque		M 3 & 3.5 screws	60	Ncm

a When mounted on 1inch square 2oz copper clad FR-4

b Preliminary Data Sheet – Specifications subject to change

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

### Thermal characteristics

Thermal resistance, junction-case <sup>a</sup>	$R_{thJC}$		-	-	0.6	°C/W
Thermal resistance, junction-ambient <sup>a</sup>	$R_{thJA}$	leaded	-	-	50	
Soldering temperature, wave soldering only allowed at leads	$T_{sold}$	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

### Electrical characteristics <sup>b</sup>, at $T_j=25^{\circ}\text{C}$ , unless otherwise specified

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.1	3	3.9	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=650\text{ V}, V_{GS}=0\text{ V}, T_j=25^{\circ}\text{C}$	-	0.1	1	$\mu\text{A}$
		$V_{DS}=650\text{ V}, V_{GS}=0\text{ V}, T_j=150^{\circ}\text{C}$	-	-	100	
Gate source leakage current	$I_{GSS}$	$V_{GS}=\pm 20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=11\text{ A}, T_j=25^{\circ}\text{C}$	-	0.145	0.165	$\Omega$
		$V_{GS}=10\text{ V}, I_D=11\text{ A}, T_j=150^{\circ}\text{C}$	-	0.42	-	
Gate resistance	$R_G$	$f=1\text{ MHz}$ , open drain	-	4	-	$\Omega$

#### Dynamic characteristics

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	-	2650	-	$\mu\text{F}$
Output capacitance	$C_{oss}$		-	943	-	
Reverse transfer capacitance	$C_{rss}$		-	8	-	
Transconductance	$g_{fs}$	$V_{DS}>2 \cdot I_D \cdot R_{DS}, I_D=11\text{ A}$	-	22	-	S
Turn-on delay time	$t_{d(on)}$	$V_{DS}=380\text{ V}, V_{GS}=10\text{ V}, I_D=22\text{ A}, R_G=4\Omega$ (External)	-	10	-	ns
Rise time	$t_r$		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	67	-	
Fall time	$t_f$		-	4.5	-	

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

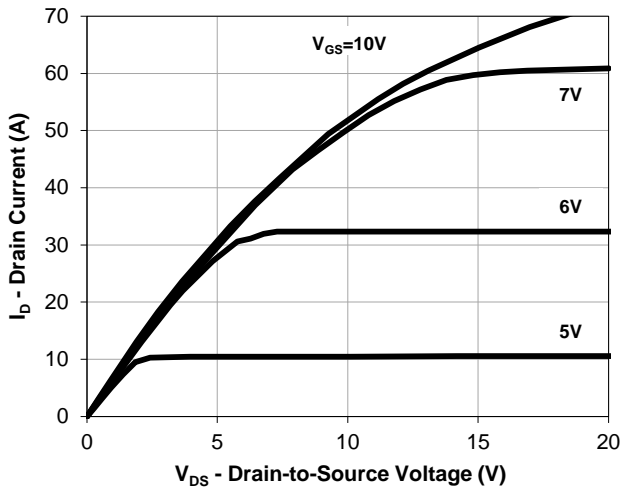
**Gate charge characteristics**

Gate to source charge	$Q_{gs}$	$V_{DS}=480\text{ V}, I_D=22\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	16	-	nC
Gate to drain charge	$Q_{gd}$		-	30	-	
Gate charge total	$Q_g$		-	82	-	
Gate plateau voltage	$V_{\text{plateau}}$		-	5	-	V

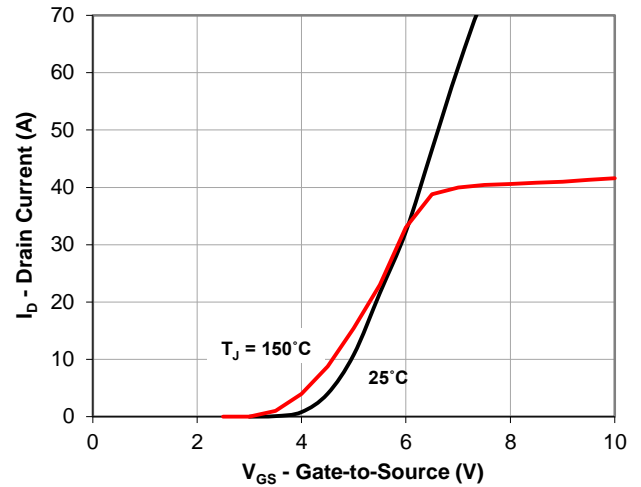
**Reverse Diode**

Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_S=I_F$	-	1.0	1.2	V
Reverse recovery time	$t_{rr}$	$V_{RR}=480\text{ V}, I_S=I_F,$ $d_{iF}/d_t=100\text{ A}/\mu\text{S}$	-	423	-	ns
Reverse recovery charge	$Q_{rr}$		-	8	-	$\mu\text{C}$
Peak reverse recovery current	$I_{rm}$		-	34	-	A

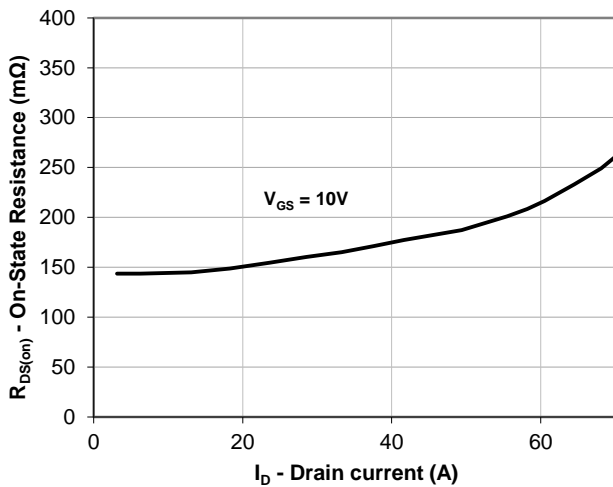
### Output Characteristics



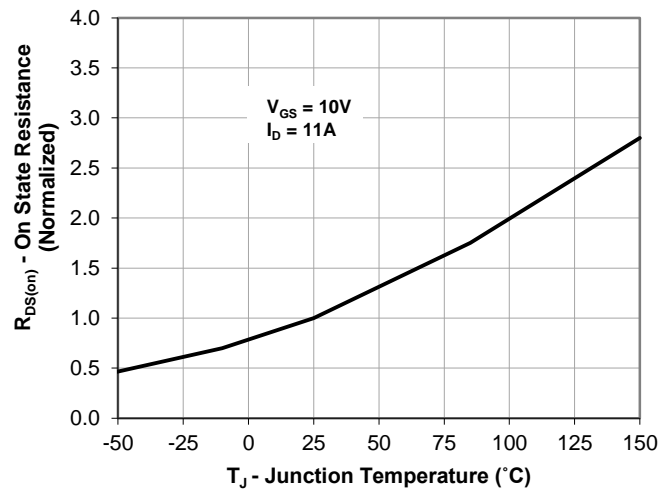
### Transfer Characteristics



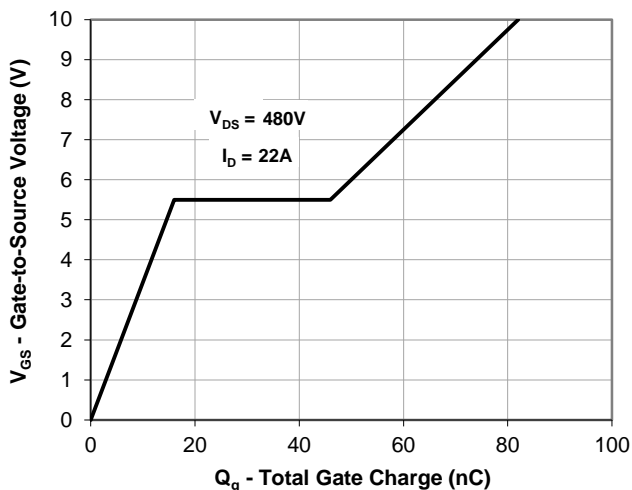
### On Resistance vs Drain Current



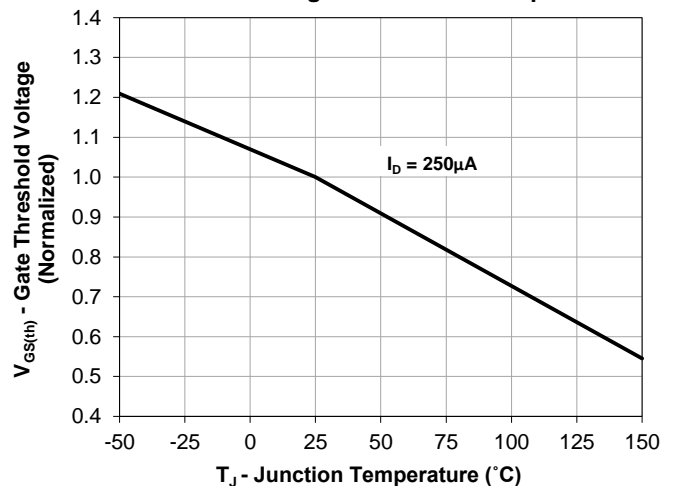
### On Resistance vs Junction Temperature



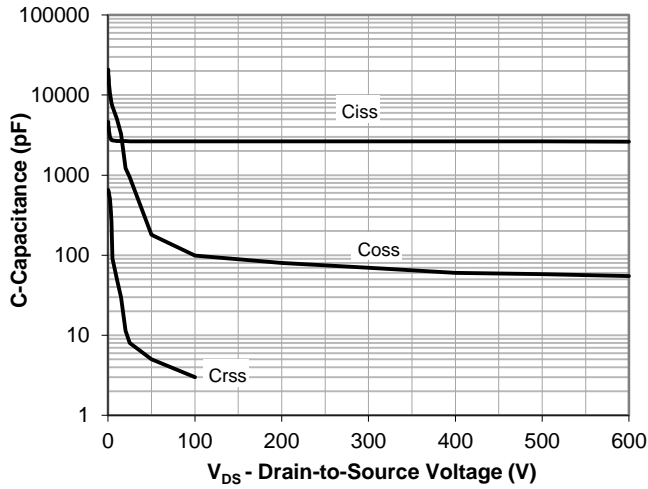
### Gate Charge



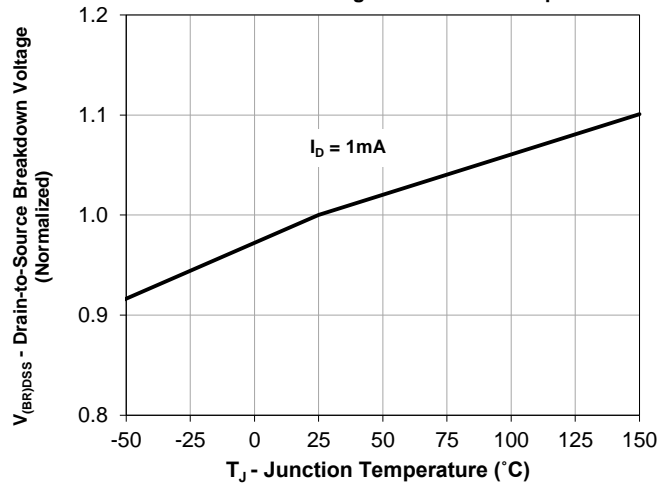
### Gate Threshold Voltage vs Junction Temperature



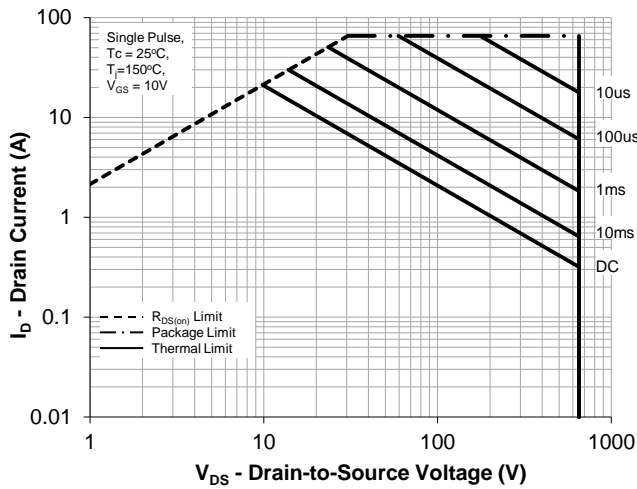
### Capacitance



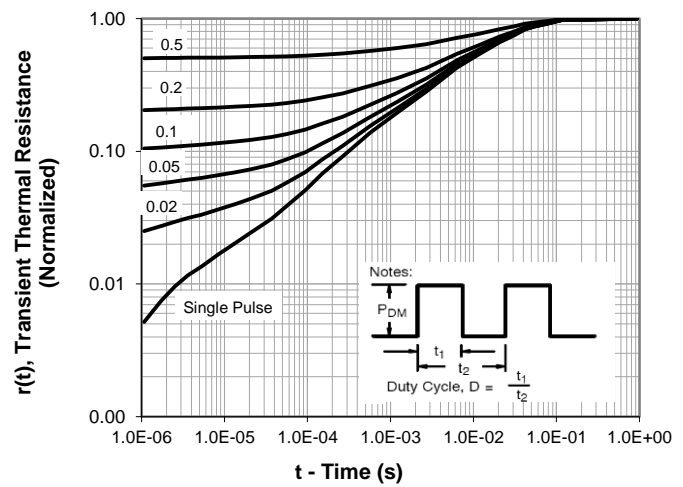
### Drain-to-Source Breakdown Voltage vs. Junction Temperature

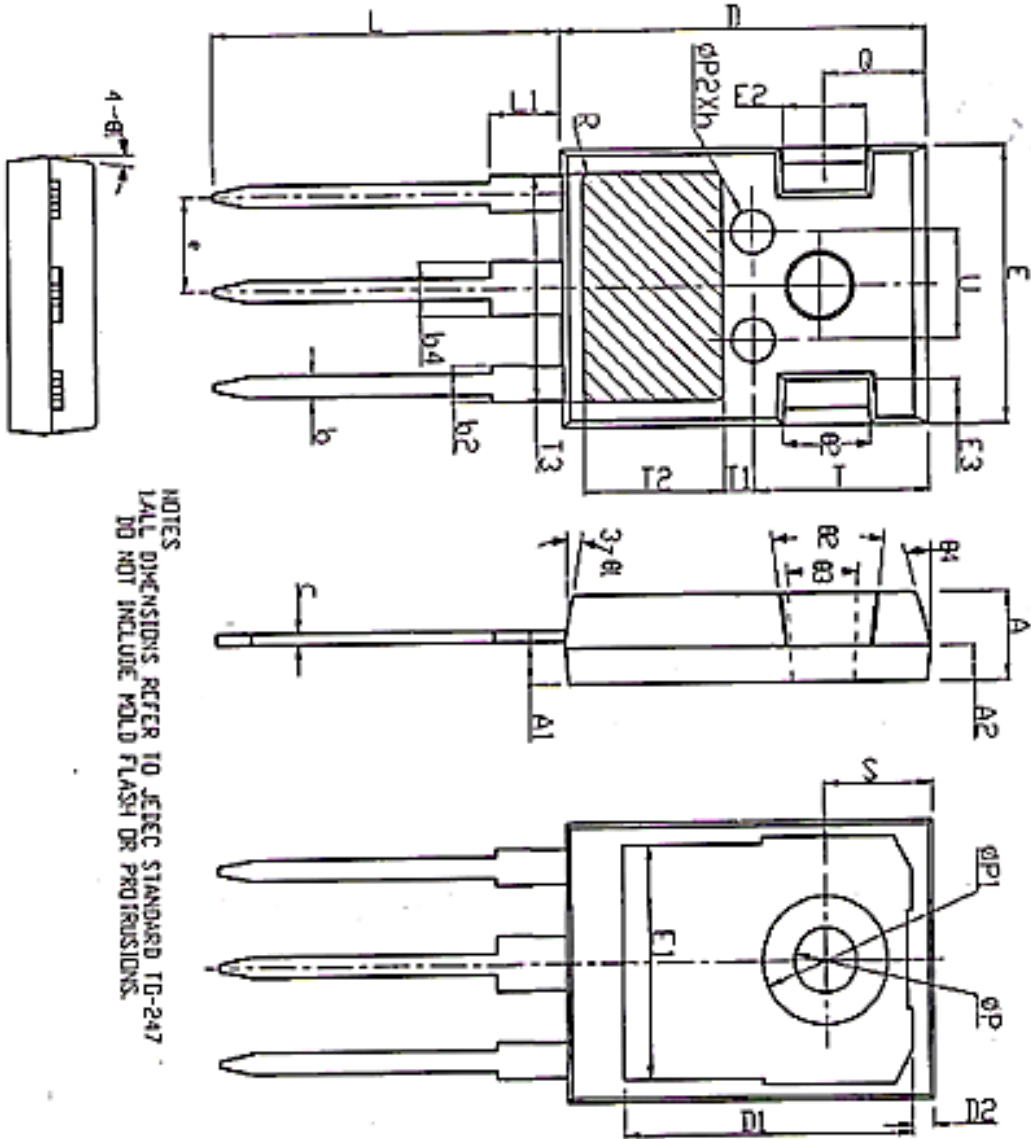


### Maximum Rated Forward Biased Safe Operating Area



### Transient Thermal Response, Junction-to-Case





NOTES  
 ALL DIMENSIONS REFER TO JEDEC STANDARD TD-247  
 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16	1.21	1.26
b2	1.96	2.01	2.06
b4	2.96	3.01	3.06
c	0.59	0.61	0.66
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.44 BSC		
h	0.05	0.10	0.15
L	19.80	19.92	20.10
L1	—	—	4.30
$\phi P$	3.50	3.60	3.70
$\phi P1$	—	—	7.30
$\phi P2$	2.40	2.50	2.60
Q	5.60	5.80	6.00
S	6.15 BSC		
R	0.50 BSC		
T	9.80	—	10.20
T1	1.65 REF		
T2	8.00 REF		
T3	12.80 REF		
U	6.00	—	6.40
$\theta 1$	6°	7°	8°
$\theta 2$	4°	5°	6°
$\theta 3$	1°	—	1.5°
$\theta 4$	14°	15°	16°

## **ICEMOS SUPERJUNCTION PATENT PORTFOLIO**

### **ICEMOS GRANTED PATENTS**

US7,429,772  
US7,439,178  
US7,446,018  
US7,579,607  
US7,723,172  
US7,795,045  
US7,846,821  
US7,944,018  
US8,012,806  
US8,030,133

### **3D SEMI PATENTS LICENSED TO ICEMOS**

US7,041,560B2  
US7,023,069B2  
US7,364,994  
US7,227,197B2  
US7,304,944B2  
US7,052,982B2  
US7,339,252  
US7,410,891  
US7,439,583  
US7,227,197B2  
US6,635,906  
US6,936,867  
US7,015,104  
US9,109,110  
US7,271,067  
US7,354,818  
US7,052,982,  
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.

## Marking Information

**YY** = Last two digits of the year

**WW** = Work week calendar on Icemos subcon assembly & test house

**\*** = Initial for Icemos subcon assembly and test house

**XXXX** = Wafer Lot ID

**00** = may be used for wafer ID in a special case.  
= "00" is used unless specified.

**ICE22N65** = ICE is Icemos logo and 22N65 is a designated device part number

