# Quasi-Resonant 700 V/800 V CoolSET™ - in DIP-7 and DSO-12 Package

## Product Highlights

- Integrated 700 V/800 V avalanche rugged CoolMOS™
- Novel Quasi-Resonant operation and proprietary implementation for low EMI
- Enhanced Active Burst Mode with selectable entry and exit standby power
- Active Burst Mode to reach the lowest standby power <100 mW
- Fast startup achieved with cascode configuration
- Digital frequency reduction for better overall system efficiency
- Robust line protection with input OVP and brownout
- Comprehensive protection
- Pb-free lead plating, halogen free mold compound, RoHS compliant

PG-DIP-7      PG-DSO-12

RoHS
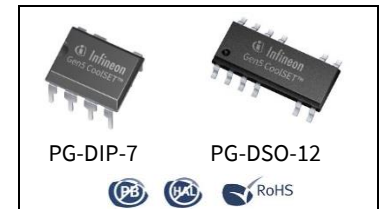
## Features

- Integrated 700 V/800 V avalanche rugged CoolMOS™
- Minimum switching frequency difference between low & high line for higher efficiency & better EMI
- Enhanced Active Burst Mode with selectable entry and exit standby power
- Active Burst Mode to reach the lowest standby power <100 mW
- Fast startup achieved with cascode configuration
- Digital frequency reduction up to 10 zero crossings
- Built-in digital soft start
- Cycle-by-cycle peak current limitation
- Maximum on/off time limitation to avoid audible noise during start up and power down
- Robust line protection with input OVP and brownout
- Auto restart mode protection for VCC Over Voltage, VCC Under Voltage, Over load/Open Loop, Output Over Voltage, Over Temperature and CS (Current Sense) short to GND
- Limited charging current for VCC short to GND
- Pb-free lead plating, halogen free mold compound, RoHS compliant

## Applications

- Auxiliary power supply for Home Appliances/white Goods, TV, PC & Server
- Blu-ray player, Set-top box & LCD/LED Monitor

## Description

The Quasi-Resonant CoolSET™- (ICE5QRxxxxAx) is the 5th generation of Quasi-Resonant integrated power IC optimized for off-line switch power supply in cascode configuration. It is housed in single package with 2 separate chips; one is controller chip and other is HV MOSFET chips. The IC can achieve lower EMI and higher efficiency with improved digital frequency reduction through the proprietary novel Quasi-Resonant operation. The enhanced Active Burst Mode enables flexibility in standby power range selection. The product has a wide operation range (10 ~ 25.5 V) of IC power supply and lower power consumption. The numerous protection functions including the robust line protection (both input OVP and brownout) to support the protections of the power supply system in failure situations. All of these make the CoolSET™ (ICE5QRxxxxAx) series an outstanding integrated power device in Quasi-Resonant flyback converter in the market.
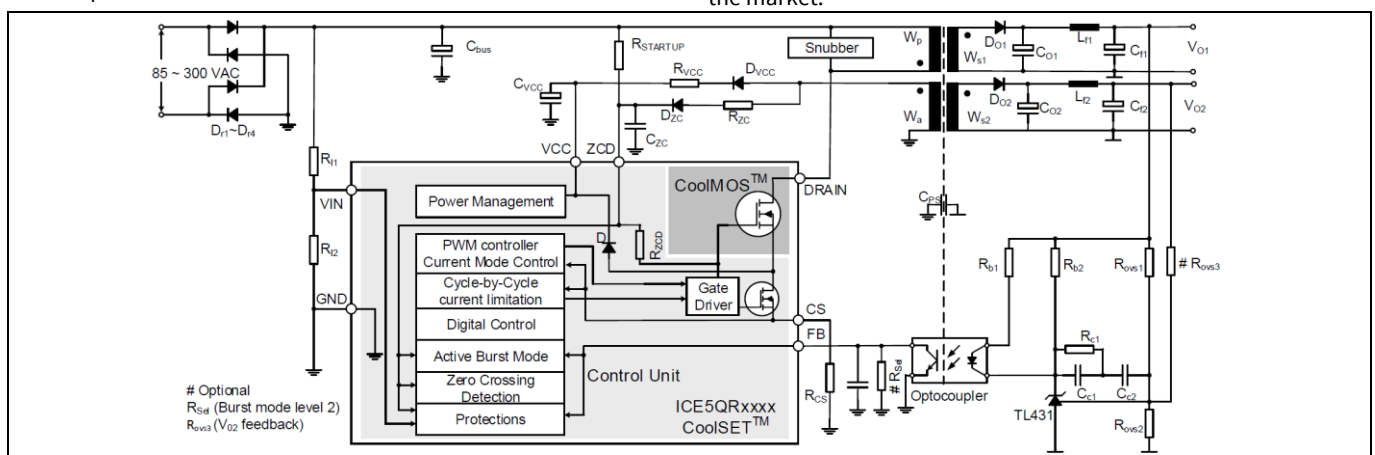


**Figure 1      Typical application**

Datasheet

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V 2.1

2017-08-11

# Quasi-Resonant 700 V/800 V CoolSET™ - in DIP-7 and DSO-12 Package

**Output Power of 5th generation Quasi-Resonant CoolSET™**

## Output Power of 5th generation Quasi-Resonant CoolSET™

**Table 1** **Output Power of 5th generation Quasi-Resonant CoolSET™**

| Type | Package | Marking | $V_{DS}$ | $R_{DSon}$[1] | 220$V_{AC}$ ±20%[2] | 85-300 $V_{AC}$[2] |
|------|---------|---------|----------|---------------|---------------------|--------------------|
| ICE5QR4770AZ | PG-DIP-7 | 5QR4770AZ | 700 V | 4.73 Ω | 27 W | 15 W |
| ICE5QR4780AZ | PG-DIP-7 | 5QR4780AZ | 800 V | 4.13 Ω | 28 W | 15 W |
| ICE5QR2270AZ | PG-DIP-7 | 5QR2270AZ | 700 V | 2.13 Ω | 41 W | 22 W |
| ICE5QR2280AZ | PG-DIP-7 | 5QR2280AZ | 800 V | 2.13 Ω | 41 W | 22 W |
| ICE5QR1070AZ | PG-DIP-7 | 5QR1070AZ | 700 V | 1.15 Ω | 58 W | 32 W |
| ICE5QR0680AZ | PG-DIP-7 | 5QR0680AZ | 800 V | 0.71 Ω | 74 W | 41 W |
| ICE5QR4770AG | PG-DSO-12 | 5QR4770AG | 700 V | 4.73 Ω | 27 W | 15 W |
| ICE5QR1680AG | PG-DSO-12 | 5QR1680AG | 800 V | 1.53 Ω | 50 W | 27 W |
| ICE5QR0680AG | PG-DSO-12 | 5QR0680AG | 800 V | 0.71 Ω | 77 W | 42 W |

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[1] Typ. at $T_J$ =25°C (inclusive of low side MOSFET)

[2] Calculated maximum output power rating in an open frame design at $T_a$=50°C, $T_J$=125°C (integrated high voltage MOSFET) and using minimum drain pin copper area in a 2 oz copper single sided PCB. The output power figure is for selection purpose only. The actual power can vary depending on particular designs. Please contact to a technical expert from Infineon for more information.

# Table of Contents

## Table of Contents

# 1 Pin Configuration and Functionality

The pin configuration is shown in Figure 2 and the functions are described in Table 2.



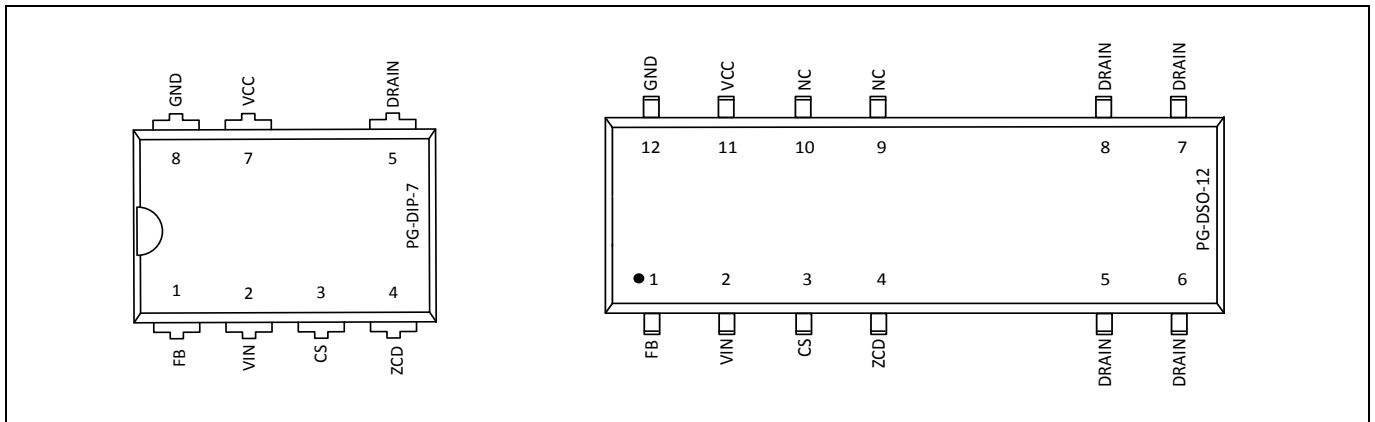**Figure 2**      Pin Configuration

**Table 2**      Pin Definitions and Functions

| Pin | | Symbol | Function |
|---|---|---|---|
| **DIP-7** | **DSO-12** | | |
| 1 | 1 | FB | **Feedback & Burst entry/exit control** <br> **FB** pin combines the functions of feedback control, selectable burst entry/exit control and overload/open loop protection. |
| 2 | 2 | VIN | **Input Line OVP & Brownout** <br> **VIN** pin is connected to the bus via resistor divider (see Figure 1) to sense the line voltage. This pin combines the functions of input Line OVP, Brownout and minimum ZC count setting for low and high line. |
| 3 | 3 | CS | **Current Sense** <br> The **CS** pin is connected to the shunt resistor for the primary current sensing externally and to the PWM signal generator block for switch-off determination (together with the feedback voltage) internally.  Moreover, CS pin short to ground protection is sensed by this pin. |
| 4 | 4 | ZCD | **Zero Crossing Detection** <br> **ZCD** pin combines the functions of start up, zero crossing detection and output over voltage protection. During the start up, it is used to provide a voltage level to the gate of power switch CoolMOS™ to charge $V_{CC}$ capacitor. |
| 5 | 5, 6, 7, 8 | DRAIN | **Drain** <br> The **DRAIN** pin is connected to the drain of the integrated CoolMOS™. |
| 7 | 11 | VCC | **VCC(Positive Voltage Supply)** <br> The **VCC** pin is the positive voltage supply to the IC. The operating range is between $V_{VCC\_OFF}$ and $V_{VCC\_OVP}$. |
| 8 | 12 | GND | **Ground** <br> The **GND** pin is the common ground of the CoolSET™. |
| - | 9, 10 | NC | Not connected. |

# 2 Representative Block Diagram
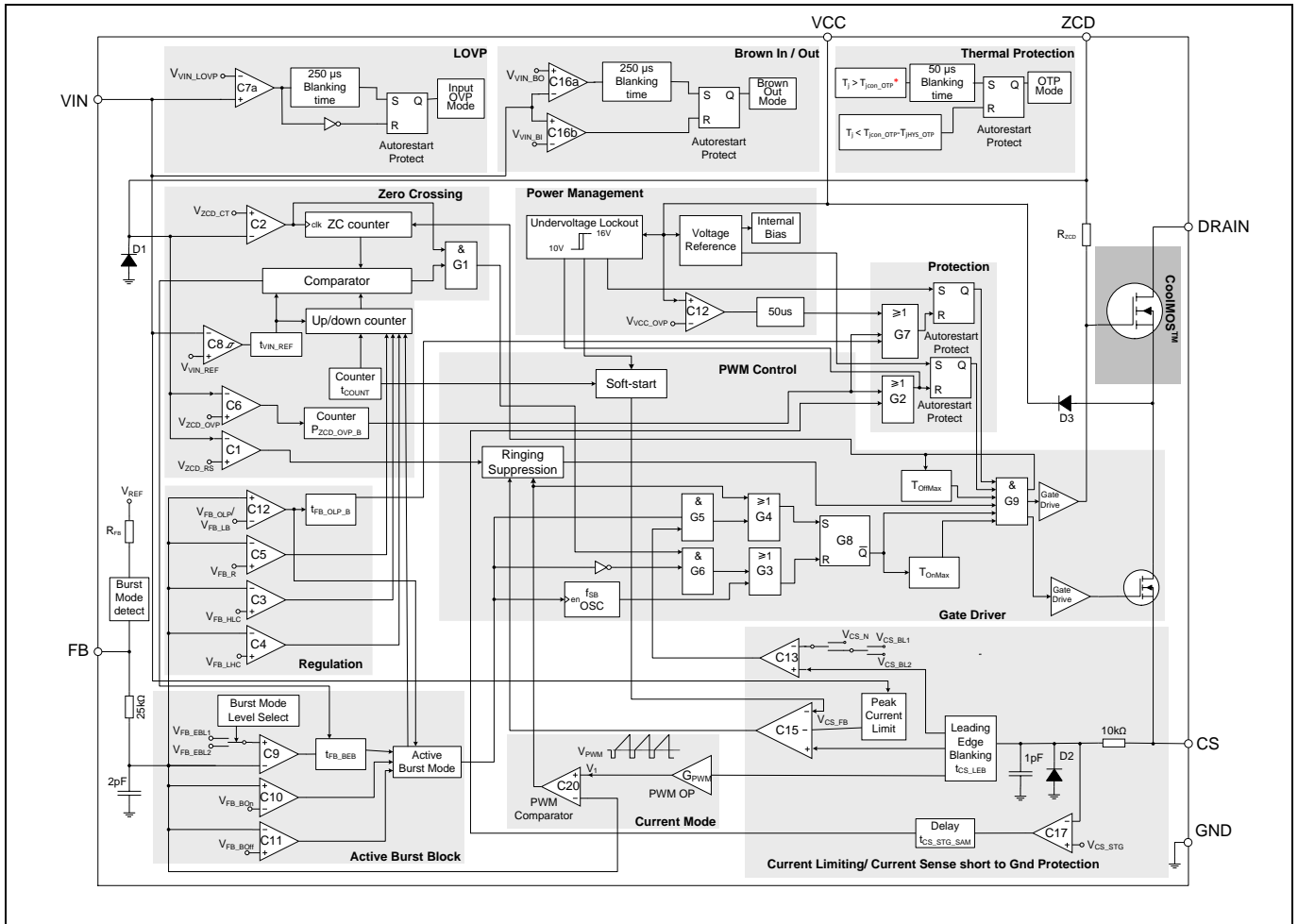


**Figure 3**     **Representative Block Diagram**

*Note: ∗ Junction temperature of the controller chip is sensed for over temperature protection. The CoolMOS™ is a separated chip from the controller chip in the same package. Please refer to the design guide and/or consult a technical expert from Infineon for the proper thermal design.*

# 3 Functional Description

## 3.1 V<sub>CC</sub> Pre-Charging and Typical V<sub>CC</sub> Voltage during Start-up

As shown in Figure 1, once the line input voltage is applied, a rectified voltage appears across the capacitor $C_{BUS}$. The pull up resistor $R_{STARTUP}$ provides a current to charge the $C_{iss}$ (input capacitance) of CoolMOS™ and gradually generate one voltage level. If the voltage over $C_{iss}$ is high enough, CoolMOS™ on and $V_{CC}$ capacitor will be charged through primary inductance of transformer $L_P$, CoolMOS™ and internal diode $D_3$ with two steps constant current source $I_{VCC\_Charge1}$[1] and $I_{VCC\_Charge3}$[1].

A very small constant current source ($I_{VCC\_Charge1}$) is charged to the $V_{CC}$ capacitor till $V_{CC}$ reach $V_{CC\_SCP}$ to protect the controller from $V_{CC}$ pin short to ground during the start up. After this, the second step constant current source ($I_{VCC\_Charge3}$) is provided to charge the $V_{CC}$ capacitor further, until the $V_{CC}$ voltage exceeds the turned-on threshold $V_{VCC\_ON}$. As shown in the time phase I in Figure 4, the $V_{CC}$ voltage increase almost linearly with two steps.
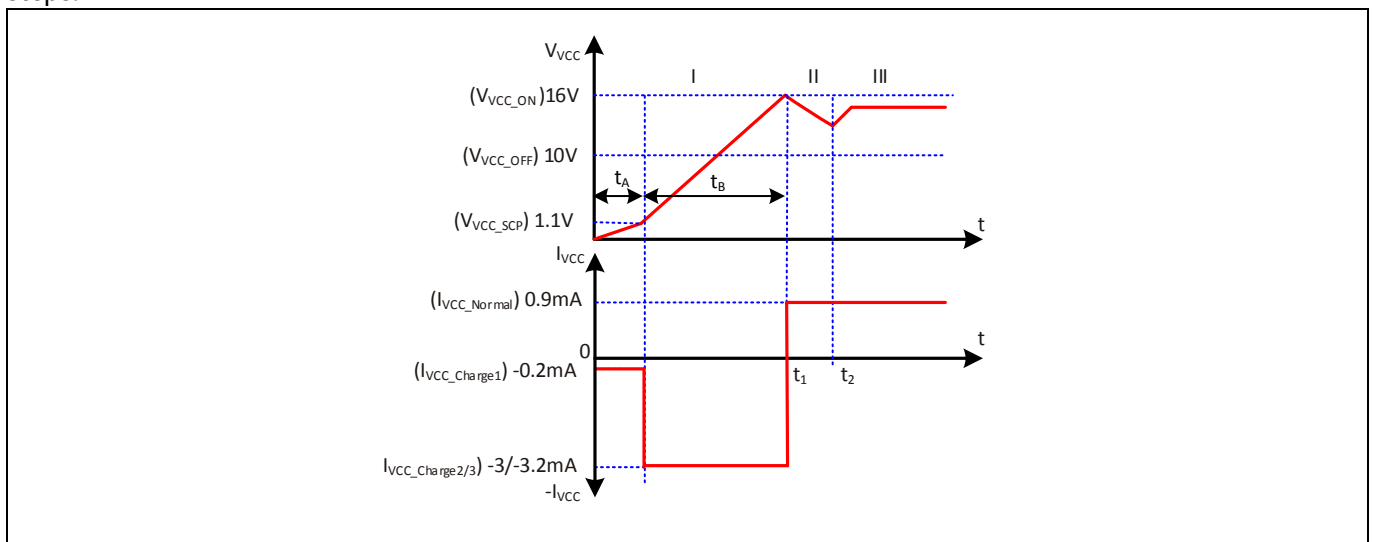


**Figure 4** VCC voltage and current at start up

The time taking for the $V_{CC}$ pre-charging can then be approximately calculated as:

$$t_1 = t_A + t_B = \frac{V_{VCC\_SCP} \cdot C_{VCC}}{I_{VCC\_Charge1}} + \frac{(V_{VCC\_ON} - V_{VCC\_SCP}) \cdot C_{VCC}}{I_{VCC\_Charge3}} \tag{1}$$

When the $V_{CC}$ voltage exceeds the $V_{CC}$ turned on threshold $V_{VCC\_ON}$ at time $t_1$, the IC begins to operate with soft start. Due to power consumption of the IC and the fact that there is still no energy from the auxiliary winding to charge the $V_{CC}$ capacitor before the output voltage is built up, the $V_{CC}$ voltage drops (Phase II). Once the output voltage is high enough, the $V_{CC}$ capacitor receives the energy from the auxiliary winding from the time $t_2$ onward and delivering the $I_{VCC\_Normal}$[2] to the CoolSET™. The $V_{CC}$ then will reach a constant value depending on output load.

## 3.2 Soft-start

As shown in Figure 5, at the time $t_{on}$, the IC begins to operate with a soft-start. By this soft-start the switching stresses for the MOSFET, diode and transformer are minimized. The soft-start implemented in ICE5QRxxxxAx is a digital time-based function. The preset soft-start time is $t_{SS}$ (12 ms) with 4 steps. If not limited by other functions, the peak voltage on CS pin will increase step by step from 0.3 V to 1 V finally. During the first 3 ms of

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[1] $I_{VCC\_Charge1/2/3}$ is charging current from the controller to VCC capacitor during start up

[2] $I_{VCC\_Normal}$ is supply current from VCC capacitor or auxiliary winding to the CoolSET™ during normal operation

**Functional Description**

soft start, the ringing suppression time is set to *25 µs* to avoid irregular switching due to switch off oscillation noise.
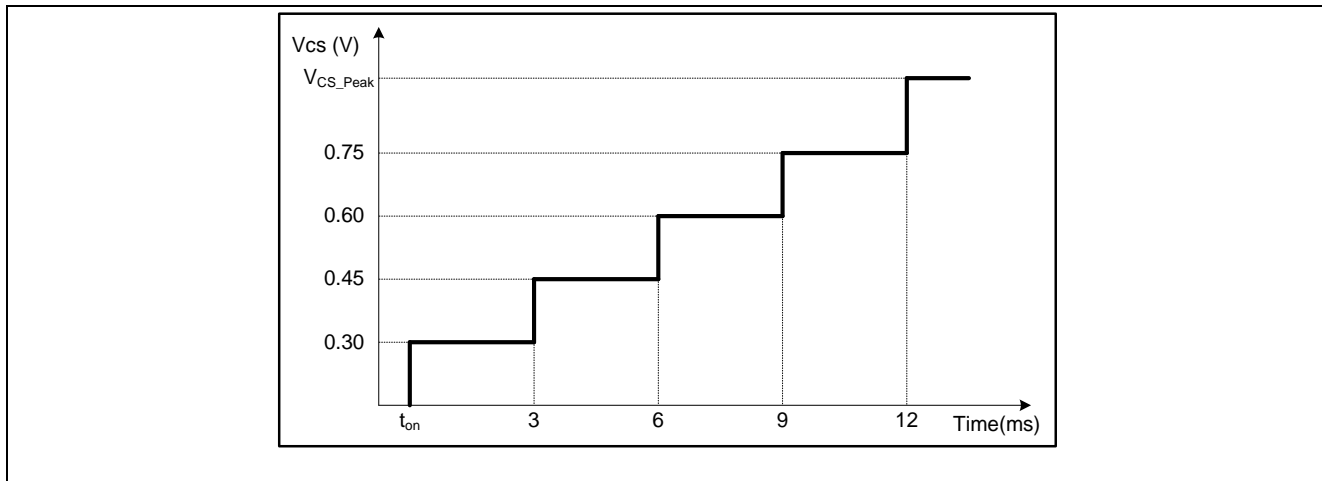


**Figure 5**        **Maximum current sense voltage during soft start**

## 3.3        Normal Operation

During normal operation, the ICE5QRxxxxAx works with a digital signal processing circuit composing an up/down counter, a zero-crossing counter (ZC counter) and a comparator, and an analog circuit composing a current measurement unit and a comparator. The switch-on and -off time points are each determined by the digital circuit and the analog circuit, respectively. The input information of the zero-crossing signal and the value of the up/down counter are needed to determine the switch-on while the feedback signal $V_{FB}$ and the current sensing signal $V_{CS}$ are necessary for the switch-off determination. Details about the full operation of the CoolSET™ in normal operation are illustrated in the following paragraphs.

## 3.3.1        Digital Frequency Reduction

As mentioned above, the digital signal processing circuit consists of an up/down counter, a ZC counter and a comparator. These three parts are key to implement digital frequency reduction with decreasing load. In addition, a ringing suppression time controller is implemented to avoid mis-triggering by the high frequency oscillation when the output voltage is very low under conditions such as soft start period or output short circuit. Functionality of these parts is described as in the following.

### 3.3.1.1        Minimum ZC Count Determination

To reduce the switching frequency difference between low and high line, minimum ZC count determination is implemented. Minimum ZC count is set to 1 if VIN less than $V_{VIN\_REF}$ which represents for low line. For high line, minimum ZC count is set to 3 after VIN higher than $V_{VIN\_REF}$. There is also a hysteresis $V_{VIN\_REF}$ with certain blanking time $t_{VIN\_REF}$ for stable AC line selection between low and high line.

### 3.3.1.2        Up/down counter

The up/down counter stores the number of the zero crossing which determines valley numbers to switch-on the main MOSFET after demagnetization of the transformer. This value is fixed according to the feedback voltage, $V_{FB}$, which contains information about the output power. Indeed, in a typical peak current mode control, a high output power results in a high feedback voltage, and a low output power leads to a low feedback voltage. Hence, according to $V_{FB}$, the value in the up/down counter is changed to vary the power

**Functional Description**

MOSFET off-time according to the output power. In the following, the variation of the up/down counter value according to the feedback voltage is explained.

The feedback voltage $V_{FB}$ is internally compared with three threshold voltages $V_{FB\_LHC}$, $V_{FB\_HLC}$ and $V_{FB\_R}$ at each clock period of 48 ms. The up/down counter counts then upward, keep unchanged or count downward, as shown in Table 3.

**Table 3        Operation of up/down counter**

| $V_{FB}$ | up/down counter action |
|---|---|
| Always lower than $V_{FB\_LHC}$ | Count upwards till n=8/10[1] |
| Once higher than $V_{F\_LHC}$, but always lower than $V_{FB\_HLC}$ | Stop counting, no value changing |
| Once higher than $V_{FB\_HLC}$, but always lower than $V_{FB\_R}$ | Count downwards till n=1/3[2] |
| Once higher than $V_{FB\_R}$ | Set up/down counter to n=1/3[2] |

The number of zero crossing is limited and therefore, the counter varies among 1 to 8 (for low line) or 3 to 10 (for high line) and any attempt beyond this range is ignored. When $V_{FB}$ exceeds $V_{FB\_R}$ voltage, the up/down counter is reset to 1 (low line) and 3 (high line) in order to allow the system to react rapidly to a sudden load increase. The up/down counter value is also reset to 1 (low line) and 3 (high line) at the start-up time, to ensure an efficient maximum load start up. Figure 6 shows some examples on how up/down counter is changed according to the feedback voltage over time.

The use of two different thresholds $V_{FB\_LHC}$ and $V_{FB\_HLC}$ to count upward or downward is to prevent frequency jittering when the feedback voltage is close to the threshold point.
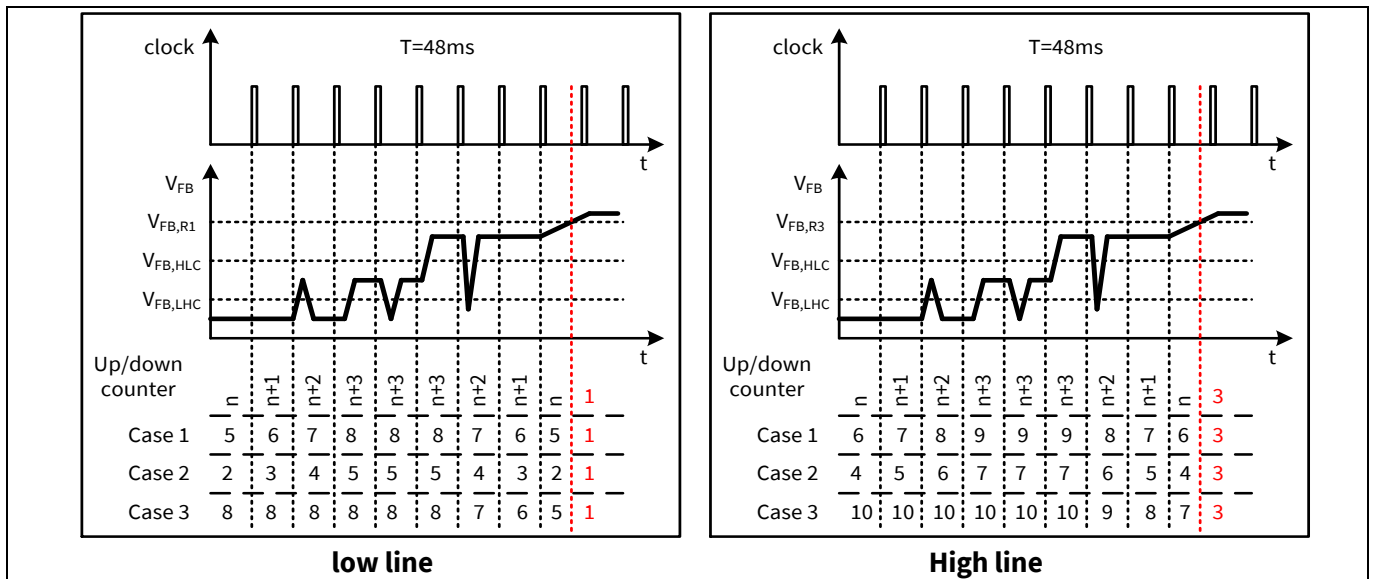


**Figure 6        Up/down counter operation**

## 3.3.1.3        Zero crossing (ZC counter)

In the system, the voltage from the auxiliary winding is applied to the ZCD pin through a RC network, which provides a time delay to the voltage from the auxiliary winding. Internally this pin is connected to a negative clamping network, a zero-crossing detector, an output overvoltage detector and a ringing suppression time controller.

During on-state of the power switch, a positive gate drive voltage is applied to the ZCD pin due to $R_{ZCD}$ resistor, hence external diode $D_{ZC}$ (see Figure 1) is added to block the negative voltage from the auxiliary winding.

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[1] *n=8 (for low line) and n=10 (for high line)*

[2] *n=1 (for low line) and n=3 (for high line)*

**Functional Description**

The ZC counter has a minimum value of 1 (for low line) or 3 (for high line) and maximum value of 8 (for low line) or 10 (for high line). After the internal high voltage CoolMOS™ is turned off, every time when the falling voltage ramp of on ZCD pin crosses the $V_{ZCD\_CT}$ threshold, a zero crossing is detected and ZC counter will increase by 1. It is reset every time after the DRIVER output is changed to high.

To achieve the switch on at voltage valley, the voltage from the auxiliary winding is fed to a time delay network (the RC network consists of $R_{ZC}$ and $C_{ZC}$ as shown in Figure 1) before it is applied to the zero-crossing detector through the ZCD pin. The needed time delay to the main oscillation signal $\Delta t$ should be approximately one fourth of the oscillation period, $T_{OSC}$ (by transformer primary inductor and drain-source capacitor) minus the propagation delay from the detected zero-crossing to the switch-on of the main switch $t_{delay}$, theoretically:

$$\Delta t = \frac{T_{OSC}}{4} - t_{delay} \tag{2}$$

This time delay should be matched by adjusting the time constant of the RC network which is calculated as:

$$\tau_{td} = C_{ZC} \cdot \frac{R_{ZC}.R_{ZCD}}{R_{ZC}+R_{ZCD}} \tag{3}$$

## 3.3.2 Ringing suppression time

After CoolMOS™ is turned off, there will be some oscillation on $V_{DS}$, which will also appear on $V_{ZCD}$. To avoid mis-triggering by such oscillations to turn on the CoolMOS™, a ringing suppression timer is implemented. This suppression time is depended on the voltage $V_{ZCD}$. If the voltage $V_{ZCD}$ is lower than the threshold $V_{ZCD\_RS}$, a longer preset time $t_{ZCD\_RS2}$ is applied. However, if the voltage $V_{ZCD}$ is higher than the threshold, a shorter time $t_{ZCD\_RS1}$ is set.

### 3.3.2.1 Switch on determination

After the gate drive goes to low, it cannot be changed to high during ring suppression time.

After ring suppression time, the gate drive can be turned on when the ZC counter value is equal to up/down counter value.

However, it is also possible that the oscillation between primary inductor and drain-source capacitor damps very fast and IC cannot detect zero crossings event. In this case, a maximum off time is implemented. After gate drive has been remained off for the period of $T_{OffMax}$, the gate drive will be turned on again regardless of the ZC counter values and $V_{ZCD}$. This function can effectively prevent the switching frequency from going lower than 20 kHz. Otherwise it will cause audible noise.

## 3.3.3 Switch off determination

In the converter system, the primary current is sensed by an external shunt resistor, which is connected between the internal low side MOSFET and the common ground. The sensed voltage across the shunt resistor $V_{CS}$ is applied to an internal current measurement unit, and its output voltage $V_1$ is compared with the feedback voltage $V_{FB}$. Once the voltage $V_1$ exceeds the voltage $V_{FB}$, the output flip-flop is reset. As a result, the main power switch is switched off. The relationship between the $V_1$ and the $V_{CS}$ is described by (see Figure 3):

$$V_1 = G_{PWM} \cdot V_{CS} + V_{PWM} \tag{4}$$

To avoid mis-triggering caused by the voltage spike across the shunt resistor at the turn on of the main power switch, a leading edge blanking time, $t_{LEB}$, is applied to the output of the comparator. In other words, once the gate drive is turned on, the minimum on time of the gate drive is the leading edge blanking time.

In addition, there is a maximum on time, $t_{OnMax}$, limitation implemented in the IC. Once the gate drive has been in high state longer than the maximum on time, it will be turned off to prevent the switching frequency from going too low because of long on time.

### 3.3.4 Modulated gate drive

The drive-stage is optimized for EMI consideration. The switch on speed is slowed down before it reaches the CoolMOS™ turn on threshold. That is a slope control of the rising edge at the output of driver (see Figure 7). Thus the leading switch spike during turn on is minimized.
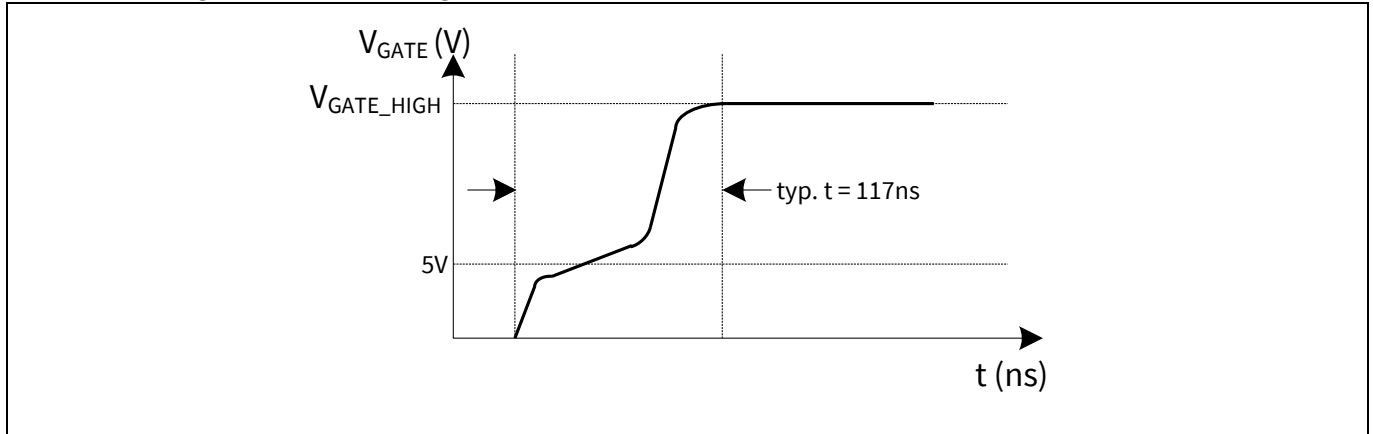


**Figure 7    Gate rising waveform**

## 3.4 Current limitation

There is a cycle by cycle current limitation realized by the current limit comparator to provide over-current detection. The source current of the CoolMOS™ is sensed via a sense resistor $R_{CS}$. By means of $R_{CS}$ the source current is transformed to a sense voltage $V_{CS}$ which is fed into the pin CS. If the voltage $V_{CS}$ exceeds an internal voltage limit, adjusted according to the Line voltage, the comparator immediately turns off the gate drive.

When the main bus voltage increases, the switch on time becomes shorter and therefore the operating frequency is also increased. As a result, for a constant primary current limit, the maximum possible output power is increased which is beyond the converter design limit.

To compensate such effect, both the internal peak current limit circuit ($V_{CS}$) and the ZC count varies with the bus voltage according to Figure.
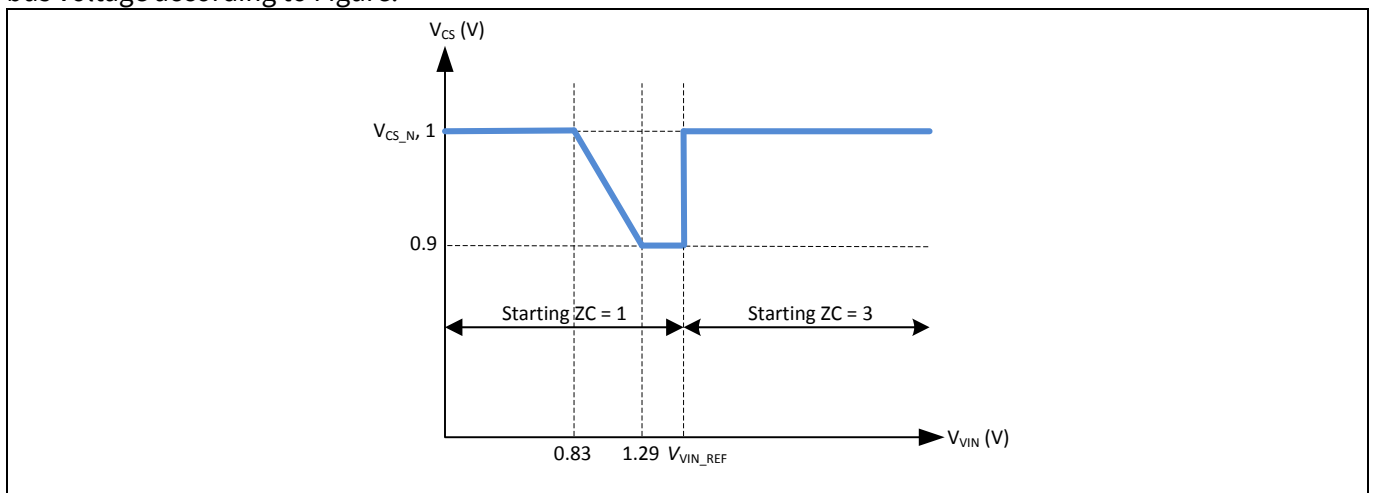


**Figure 8    Variation of the $V_{CS}$ limit voltage according to the $V_{IN}$ voltage**

## 3.5 Active Burst Mode with selectable power level

At light load condition, the IC enters Active Burst Mode operation to minimize the power consumption. Details about Active Burst Mode operation are explained in the following paragraphs.

**Functional Description**

The burst mode entry level can be selected by changing the different resistor $R_{Sel}$ at FB pin. There are 2 levels to be selected with different resistor which are targeted for low range of active burst mode power (Level 1) and high range of active burst mode power (Level 2). The following table shows the control logic for the entry and exit level with the FB voltage.

**Table 4    Two levels entry and exit active burst mode power**

| Level | $V_{FB}$ | $V_{CS}$ | Entry level | Exit level |
|---|---|---|---|---|
| | | | $V_{FB\_EBLX}$ | $V_{FB\_LB}$ |
| 1 | $V_{FB} > V_{REF\_B}$ | $V_{CS\_BL1} = 0.31$ V | 0.90 V | 2.75 V |
| 2 | $V_{FB} < V_{REF\_B}$ | $V_{CS\_BL2} = 0.35$ V | 1.05 V | 2.75 V |

During IC first startup, the internal $Ref_{GOOD}$ signal is logic low when $V_{CC} < 4$ V. It will reset the Burst Mode level Detection latch. When the Burst Mode Level Detection latch is low and IC is in OFF state, the IC internal $R_{FB}$ resistor is disconnected from the FB pin and a current source $I_{sel}$ is turned on instead.

From Vcc=4 V to Vcc on threshold, the FB pin will start to charge to a voltage level associated with $R_{Sel}$ resistor. When Vcc reaches Vcc on threshold, the FB voltage is sensed. The burst mode thresholds are then chosen according to the FB voltage level. The Burst Mode Level Detection latch is then set to high. Once the detection latch is set high, any change of the FB level will not change the threshold selection. The current source $I_{sel}$ is turned off in 2 μs after $V_{CC}$ reaches $V_{CC}$ on threshold and the $R_{FB}$ resistor is re-connected to FB pin (see Figure 9).
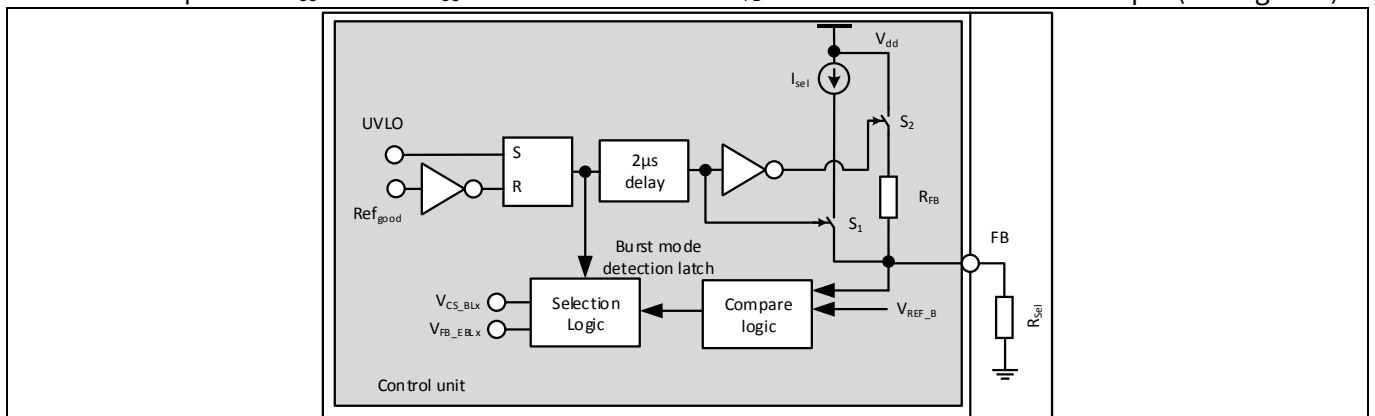


**Figure 9    Burst mode detect and adjust**

## 3.5.1    Entering Active Burst Mode Operation

For determination of entering Active Burst Mode operation, three conditions apply:
- the feedback voltage is lower than the threshold of $V_{FB\_EBLX}$
- the up/down counter is 8 for low line or 10 for high line and
- the above two conditions remain after a certain blanking time $t_{FB\_BEB}$ (20 ms).

Once all of these conditions are fulfilled, the Active Burst Mode flip-flop is set and the controller enters Active Burst Mode operation. This multi-condition determination for entering Active Burst Mode operation prevents mis-triggering of entering Active Burst Mode operation, so that the controller enters Active Burst Mode operation only when the output power is really low during the preset blanking time.

## 3.5.2    During Active Burst Mode Operation

After entering the Active Burst Mode the feedback voltage rises as $V_O$ starts to decrease due to the inactive PWM section. One comparator observes the feedback signal if the voltage level $V_{FB\_BOn}$ is exceeded. In that case the internal circuit is power up to restrart with switching.

**Functional Description**

Turn-on of the power MOSFET is triggered by ZC counter with a fixed value of 8 ZC for low line and 10 ZC for high line. Turn-off is resulted if the voltage across the shunt resistor at CS pin hits the threshold $V_{CS\_BLX}$.

If the output load is still low, the feedback signal decreases as the PWM section is operating. When feedback signal reaches the low threshold $V_{FB\_BOff}$, the internal circuit is reset again and the PWM section is disabled until next time $V_{FB}$ signal increases beyond the $V_{FB\_BOn}$ threshold. In Active Burst Mode, the feedback signal is changing like a saw tooth between $V_{FB\_BOff}$ and $V_{FB\_BOn}$ (see Figure 10).

### 3.5.3 Leaving Active Burst Mode Operation

The feedback voltage immediately increases if there is a high load jump. This is observed by a comparator with threshold of $V_{FB\_LB}$. As the current limit is $V_{CS\_BLX}$ (31% or 35%) during Active Burst Mode, a certain load is needed so that feedback voltage can exceed $V_{FB\_LB}$. After leaving active burst mode, normal peak current control through $V_{FB}$ is re-activated. In addition, the up/down counter will be set to 1 (low line) or 3 (high line) immediately after leaving Active Burst Mode. This is helpful to minimize the output voltage undershoot.
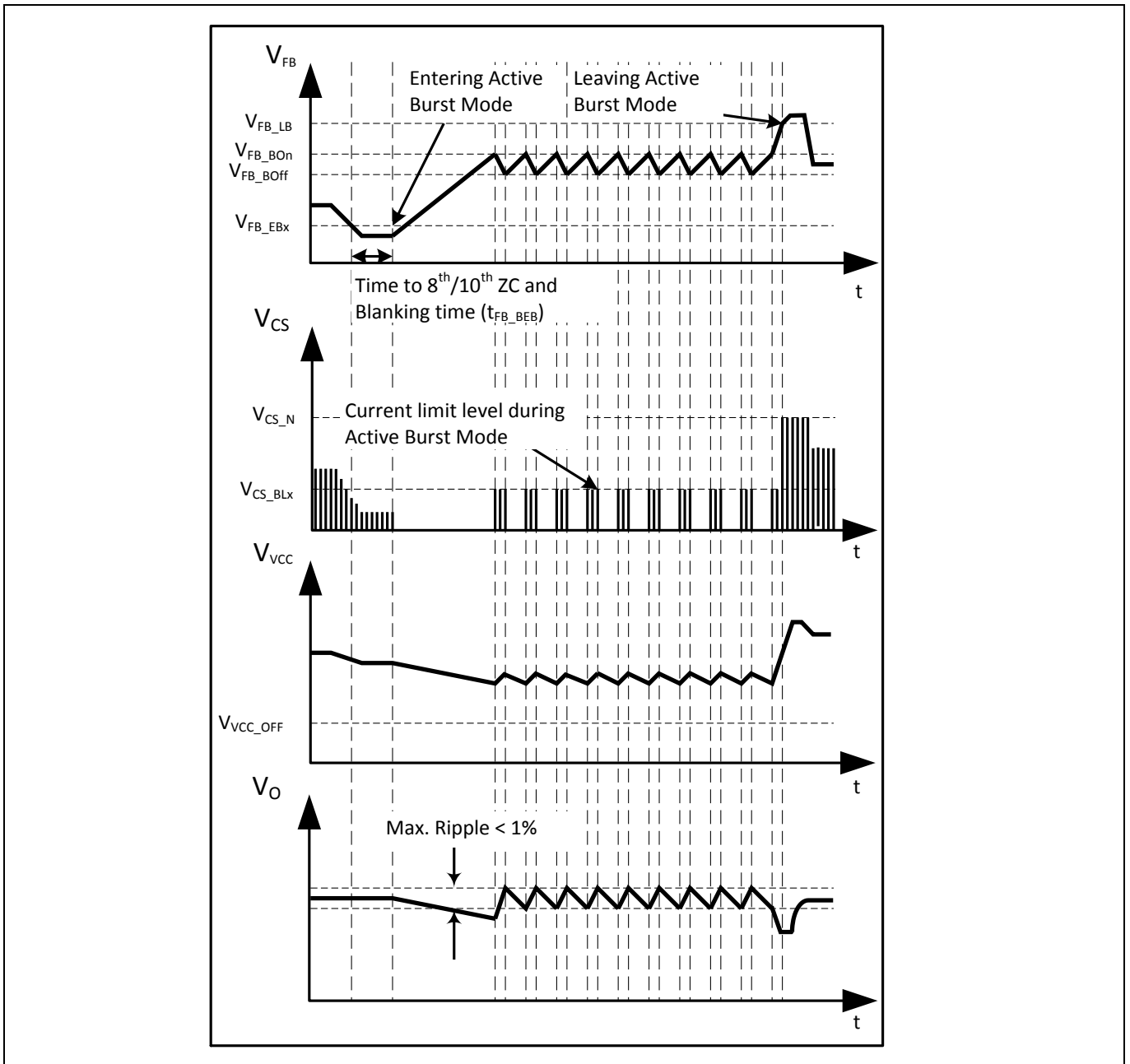


**Figure 10    Signals in Active Burst Mode**

**Functional Description**

## 3.6 Protection Functions

The ICE5QRxxxxAx provides numerous protection functions which considerably improve the power supply system robustness, safety and reliability. The following table summarizes these protection functions. There are 3 different kinds of protection mode; non switch auto restart, auto restart and odd skip auto restart. The details can refer to the Figure 11, Figure 12 and Figure 13.

**Table 5        Protection functions**

| Protection Functions | Normal Mode | Burst Mode | | Protection Mode |
| --- | --- | --- | --- | --- |
| | | Burst ON | Burst OFF | |
| Line Over Voltage | √ | √ | √ | Non switch Auto Restart |
| Brownout | √ | √ | √ | Non switch Auto Restart |
| $V_{CC}$ Over Voltage | √ | √ | NA[1] | Odd skip Auto Restart |
| $V_{CC}$ Under Voltage | √ | √ | √ | Auto Restart |
| Over Load | √ | NA[1] | NA[1] | Odd skip Auto Restart |
| Output Over Voltage | √ | √ | NA[1] | Odd skip Auto Restart |
| Over Temperature | √ | √ | √ | Non switch Auto Restart |
| CS Short to GND | √ | √ | NA[1] | Odd skip Auto Restart |

## 3.6.1 Line Over Voltage

The AC **Line Over Voltage** Protection is detected by sensing bus capacitor voltage through VIN pin via 2 potential divider resistors, $R_{l1}$ and $R_{l2}$ (see Figure 1). Once $V_{VIN}$ voltage is higher than the line over voltage threshold $V_{VIN\_LOVP}$, the controller enters Line Over Voltage Protection and it releases the protection mode after $V_{VIN}$ is lower than $V_{VIN\_LOVP}$.

## 3.6.2 Brownout

The **Brownout** protection is observed by VIN pin similar to line over voltage Protection method with a different voltage threshold level.  When $V_{VIN}$ voltage is lower than the brownout threshold ($V_{VIN\_BO}$), the controller enters Brownout  Protection and it releases the protection mode after $V_{VIN}$ higher  than  brownin threshold ($V_{VIN\_BI}$).

## 3.6.3 $V_{CC}$ Ovder Voltage or Under Voltage

During operation, the $V_{CC}$ voltage is continuously monitored. In case of a **$V_{CC}$ Over Voltage** or **Under Voltage**, the IC is reset and the main power switch is then kept off. After the $V_{CC}$ voltage falls below the threshold $V_{VCC\_OFF}$, the new start up sequence is activated. The $V_{CC}$ capacitor is then charged up. Once the voltage exceeds the threshold $V_{VCC\_ON}$, the IC begins to operate with a new soft-start.

## 3.6.4 Over Load

In case of open control loop or output **Over Load**, the feedback voltage will be pulled up and exceed $V_{FB\_OLP}$. After a blanking time of $t_{FB\_OLP\_B}$, the IC enters auto restart mode. The blanking time here enables the converter to operate for a certain time during a sudden load jump.

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[1] Not Applicable

**Functional Description**

## 3.6.5    Output Over Voltage

During off-time of the power MOSFET, the voltage at the ZCD pin is monitored for **Output Over Voltage** detection. If the voltage is higher than the preset threshold $V_{ZCD\_OVP}$ for 10 consecutive pulses, the IC enters Output Over Voltage Protection.

## 3.6.6    Over Temperature

If the junction temperature of controller chip exceeds $T_{jcon\_OTP}$, the IC enters into **Over Temperature** protection (OTP) auto restart mode. The controller implements with a 40 °C hysteresis. In another word, the controller/IC can only resume from OTP if its junction temperature drops 40 °C from OTP trigger point. Please be noted that the separated CoolMOS™ chip may have different temperature (mostly higher) from the controller chip.

## 3.6.7    CS Short to GND

If the voltage at the current sense pin is shorted and lower than the preset threshold $V_{CS\_STG}$ with certain blanking time $t_{CS\_STG\_B}$ for 3 consecutive pulses during on-time of the power MOSFET, the IC enters **CS Short to GND** Protection.
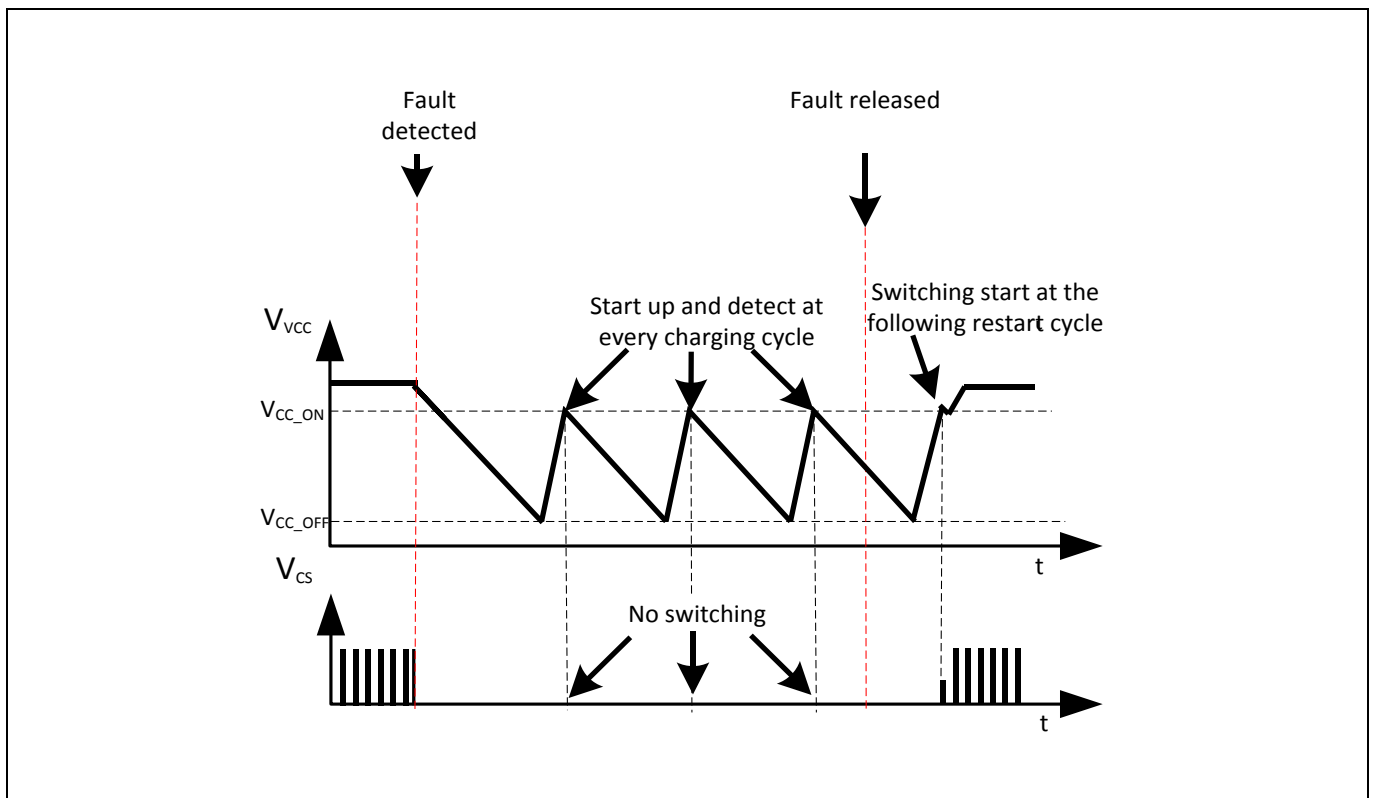


**Figure 11    Non switch Auto Restart Mode**

**Functional Description**
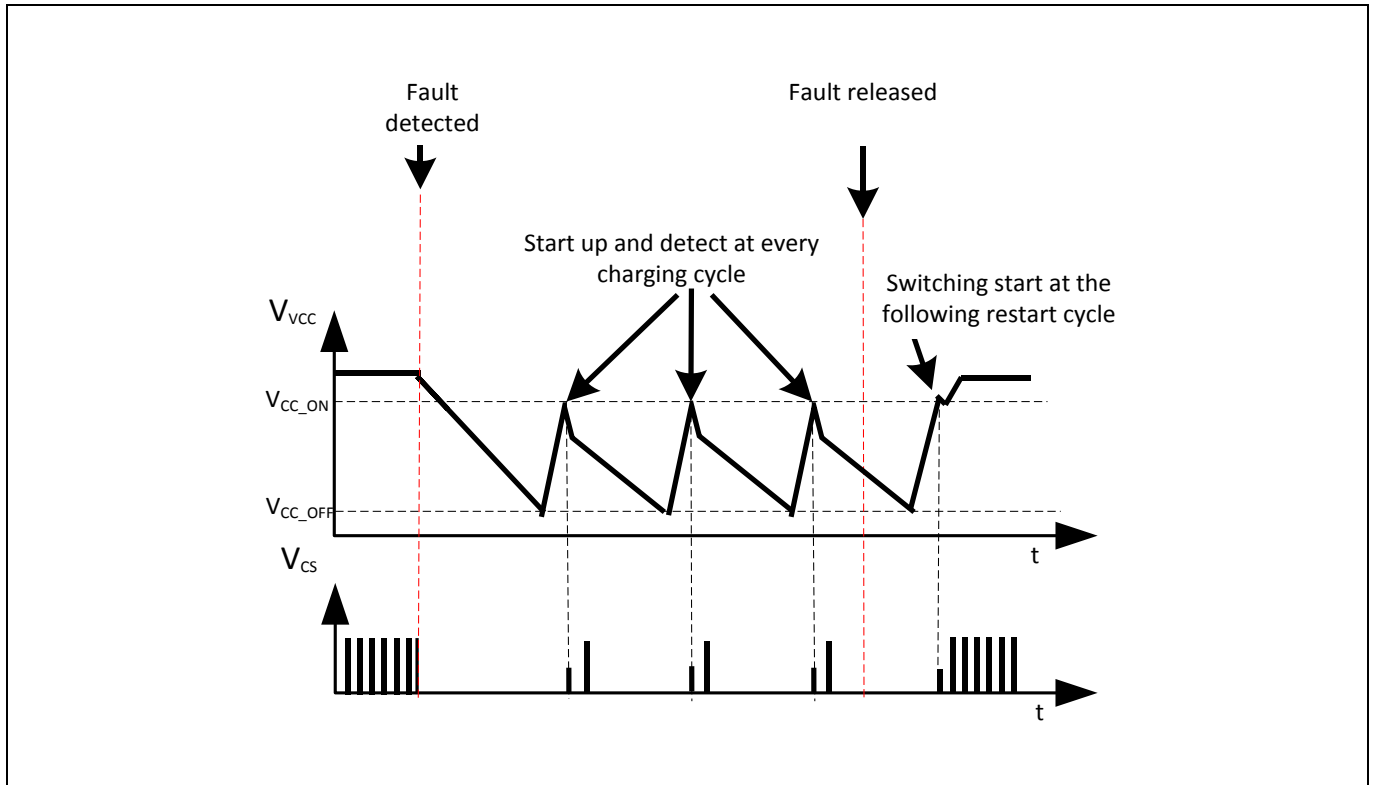


**Figure 12    Auto Restart Mode**
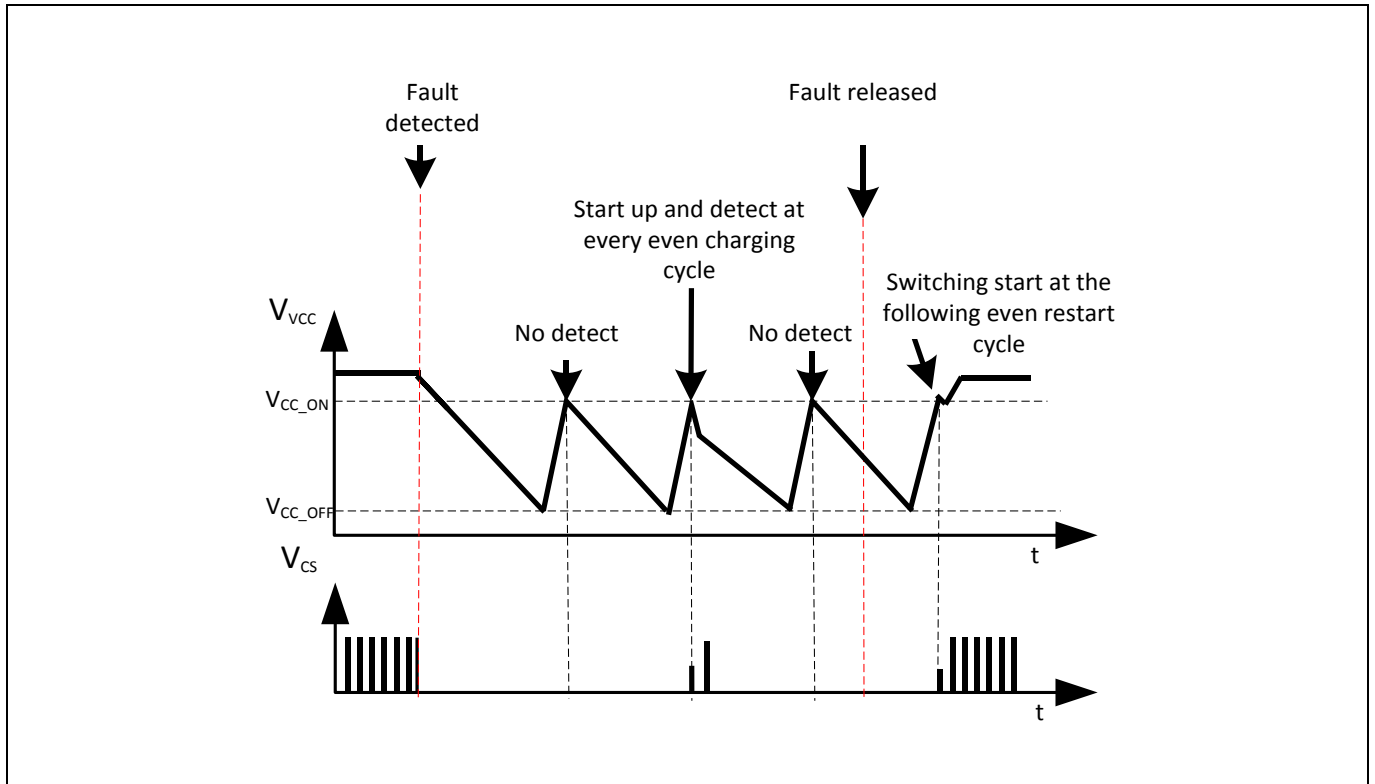


**Figure 13    Odd skip Auto Restart Mode**

# 4 Electrical Characteristics

**Attention:** *All voltages are measured with respect to ground (Pin 8 for DIP-7 and Pin12 for DSO-12). The voltage levels are valid if other ratings are not violated.*

## 4.1 Absolute Maximum Ratings

**Attention:** *Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. System design needs to ensure not to exceed the maximum limit. Ta=25°C unless otherwise specified.*

**Table 6        Absolute Maximum Ratings**

| Parameter | Symbol | Limit Values | | Unit | Note / Test Condition |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Drain Source Voltage (CoolMOS™) ICE5QRxx70Ax | $V_{DS}$ | - | 700 | V | $T_j$ = 25 °C |
| Drain Source Voltage (CoolMOS™) ICE5QRxx80Ax | $V_{DS}$ | - | 800 | V | $T_j$ = 25 °C |
| Pulse drain current | $I_{D\_Pulse}$ | | | A | |
| ICE5QR4770AZ[1] | | - | 2.2 | | |
| ICE5QR4780AZ[1] | | - | 2.6 | | |
| ICE5QR2270AZ[2] | | - | 5.8 | | |
| ICE5QR2280AZ[2] | | - | 5.8 | | |
| ICE5QR1070AZ[2] | | - | 5.8 | | |
| ICE5QR0680AZ[2] | | - | 5.8 | | |
| ICE5QR4770AG[1] | | - | 2.2 | | |
| ICE5QR1680AG[2] | | - | 5.8 | | |
| ICE5QR0680AG[2] | | - | 5.8 | | |
| Avalanche energy, repetitive, $t_{AR}$ limited by max. $T_J$=150°C with $T_{J,Start}$=25°C | $E_{AR}$ | | | mJ | |
| ICE5QR4770AZ | | - | 0.02 | | $I_D$=0.14 A, $V_{DD}$=50 V |
| ICE5QR4780AZ | | - | 0.02 | | $I_D$=0.2 A, $V_{DD}$=50 V |
| ICE5QR2270AZ | | - | 0.07 | | $I_D$=0.4 A, $V_{DD}$=50 V |
| ICE5QR2280AZ | | - | 0.05 | | $I_D$=0.4 A, $V_{DD}$=50 V |
| ICE5QR1070AZ | | - | 0.06 | | $I_D$=0.38 A, $V_{DD}$=50 V |
| ICE5QR0680AZ | | - | 0.22 | | $I_D$=1.8 A, $V_{DD}$=50 V |
| ICE5QR4770AG | | - | 0.02 | | $I_D$=0.14 A, $V_{DD}$=50 V |
| ICE5QR1680AG | | - | 0.07 | | $I_D$=0.6 A, $V_{DD}$=50 V |

[1] Pulse width $t_P$ limited by $T_{j,Max}$

[2] Pulse width $t_P$=20 µs and limited by $T_{j,Max}$

**Electrical Characteristics**

| | | | | | |
|---|---|---|---|---|---|
| ICE5QR0680AG | | - | 0.22 | | $I_D$=1.8 A, $V_{DD}$=50 V |
| Avalanche current, repetitive, $t_{AR}$ limited by max. $T_J$=150°C with $T_{J,Start}$=25°C | $I_{AR}$ | | | A | |
| ICE5QR4770AZ | | - | 0.14 | | |
| ICE5QR4780AZ | | - | 0.2 | | |
| ICE5QR2270AZ | | - | 0.4 | | |
| ICE5QR2280AZ | | - | 0.4 | | |
| ICE5QR1070AZ | | - | 0.82 | | |
| ICE5QR0680AZ | | - | 1.8 | | |
| ICE5QR4770AG | | - | 0.14 | | |
| ICE5QR1680AG | | - | 0.6 | | |
| ICE5QR0680AG | | - | 1.8 | | |
| VCC Supply Voltage | $V_{CC}$ | -0.3 | 27.0 | V | |
| FB Voltage | $V_{FB}$ | -0.3 | 3.6 | V | |
| ZCD Voltage | $V_{ZCD}$ | -0.3 | 27 | V | |
| CS Voltage | $V_{CS}$ | -0.3 | 3.6 | V | |
| VIN Voltage | $V_{IN}$ | -0.3 | 3.6 | V | |
| Maximum DC current on any pin except DRAIN & CS pins | | -10.0 | 10.0 | mA | |
| ESD robustness HBM | $V_{ESD\_HBM}$ | - | 2000 | V | According to EIA/JESD22 |
| ESD robustness CDM | $V_{ESD\_CDM}$ | - | 500 | V | |
| Junction temperature range | $T_J$ | -40 | 150 | °C | Controller & CoolMOS |
| Storage Temperature | $T_{STORE}$ | -55 | 150 | °C | |
| Thermal Resistance (Junction-Ambient) | $R_{thJA}$ | | | K/W | Setup according to the JESD51 standard and using minimum drain pin copper area in a 2 oz copper single sided PCB |
| ICE5QR4770AZ | | - | 106 | | |
| ICE5QR4780AZ | | - | 107 | | |
| ICE5QR2270AZ | | - | 103 | | |
| ICE5QR2280AZ | | - | 104 | | |
| ICE5QR1070AZ | | - | 100 | | |
| ICE5QR0680AZ | | - | 100 | | |
| ICE5QR4770AG | | - | 104 | | |
| ICE5QR1680AG | | - | 95 | | |
| ICE5QR0680AG | | - | 94 | | |

**Electrical Characteristics**

## 4.2 Operating Range

*Note : Within the operating range the IC operates as described in the functional description.*

**Table 7     Operating Range**

| Parameter | Symbol | Limit Values | | Unit | Remark |
|---|---|---|---|---|---|
| | | **Min.** | **Max.** | | |
| VCC Supply Voltage | $V_{VCC}$ | $V_{VCC\_OFF}$ | $V_{VCC\_OVP}$ | | |
| Junction Temperature of controller | $T_{jCon\_op}$ | -40 | $T_{jCon\_OTP}$ | °C | Max value limited due to OTP of controller chip |
| Junction Temperature of CoolMOS | $T_{jCoolMOS\_op}$ | -40 | 150 | °C | |

## 4.3 Operating Conditions

*Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range $T_J$ from – 40 °C to 125 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of $V_{CC}$ = 18 V is assumed.*

**Table 8     Operating Conditions**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | |
| VCC Charge Current | $I_{VCC\_Charge1}$ | -0.35 | -0.2 | -0.09 | mA | $V_{VCC}$=0V, $R_{StartUp}$=50MΩ and $V_{DRAIN}$=90V |
| | $I_{VCC\_Charge2}$ | - | -3.2 | - | mA | $V_{VCC}$=3V, $R_{StartUp}$=50MΩ and $V_{DRAIN}$=90V |
| | $I_{VCC\_Charge3}$ | -5 | -3 | -1 | mA | $V_{VCC}$=15V, $R_{StartUp}$=50MΩ and $V_{DRAIN}$=90V |
| Current Consumption, Startup Current | $I_{VCC\_Startup}$ | - | 0.19 | - | mA | $V_{VCC}$=15V |
| Current Consumption, Normal | $I_{VCC\_Normal}$ | - | 0.9 | - | mA | $I_{FB}$=0A (No gate switching) |
| Current Consumption, Auto Restart | $I_{VCC\_AR}$ | - | 320 | - | µA | |
| Current Consumption, Burst Mode | $I_{VCC\_Burst\ Mode}$ | - | 0.5 | - | mA | $V_{FB}$=1.8V |
| VCC Turn-on Threshold Voltage | $V_{VCC\_ON}$ | 15.3 | 16 | 16.5 | V | |
| VCC Turn-off Threshold Voltage | $V_{VCC\_OFF}$ | 9.5 | 10 | 10.5 | V | |
| VCC Short Circuit Protection | $V_{VCC\_SCP}$ | - | 1.1 | 1.9 | V | |
| VCC Turn-off blanking | $t_{VCC\_OFF\_B}$ | - | 50 | - | µs | |

**Electrical Characteristics**

# 4.4 Internal Voltage Reference

**Table 9**      **Internal Voltage Reference**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Internal Reference Voltage | $V_{REF}$ | 3.2 | 3.3 | 3.39 | V | Measured at pin FB $I_{FB}$=0 |

# 4.5 PWM Section

**Table 10**      **PWM Section**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Feedback Pull-Up Resistor | $R_{FB}$ | 11 | 15 | 20 | kΩ | |
| PWM-OP Gain | $G_{PWM}$ | 1.95 | 2.05 | 2.15 | - | |
| Offset for Voltage Ramp | $V_{PWM}$ | 0.42 | 0.5 | 0.58 | V | |
| Maximum on time in normal operation | $t_{OnMax}$ | 20 | 35 | 60 | µs | |
| Maximum off time in normal operation | $t_{OffMax}$ | 24 | 42.5 | 71 | µs | |

# 4.6 Current Sense

**Table 11**      **Current Sense**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Peak current limitation in normal operation | $V_{CS\_N}$ | 0.94 | 1.00 | 1.06 | V | |
| Leading Edge Blanking time | $t_{CS\_LEB}$ | 118 | 220 | 462 | ns | |
| Peak Current Limitation in Active Burst Mode – Level 1 | $V_{CS\_BL1}$ | 0.26 | 0.31 | 0.36 | V | |
| Peak Current Limitation in Active Burst Mode – Level 2 | $V_{CS\_BL2}$ | 0.3 | 0.35 | 0.4 | V | |

**Electrical Characteristics**

## 4.7 Soft Start

**Table 12 Soft Start**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Soft-Start time | $t_{SS}$ | 8.5 | 12 | - | ms | |
| Soft-start time step | $t_{SS\_s}$[1] | - | 3 | - | ms | |
| Internal regulation voltage at first step | $V_{SS1}$[1] | - | 0.30 | - | V | CS peak voltage |
| Internal regulation voltage step at soft start | $V_{SS\_s}$[1] | - | 0.15 | - | V | CS peak voltage |

## 4.8 Digital Zero Crossing

**Table 13 Digital Zero Crossing**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Zero crossing threshold voltage | $V_{ZCD\_CT}$ | 60 | 100 | 150 | mV | |
| Zero crossing Ringing suppression threshold | $V_{ZCD\_RS}$ | - | 0.45 | - | V | |
| Minimum ringing suppression time | $t_{ZCD\_RS1}$ | 1.5 | 2.5 | 4.1 | µs | $V_{ZCD} > V_{ZCD,RS}$ |
| Maximum ringing suppression time | $t_{ZCD\_RS2}$ | - | 25.00 | - | µs | $V_{ZCD} < V_{ZCD,RS}$ |
| Threshold to reset Up/Down Counter | $V_{FB\_R}$ | - | 2.80 | - | V | |
| Threshold for downward counting | $V_{FB\_HLC}$ | - | 2.05 | - | V | |
| Threshold for upward counting | $V_{FB\_LHC}$ | - | 1.55 | - | V | |
| Counter Time | $t_{COUNT}$ | - | 48 | - | ms | |
| ZCD resistance | $R_{ZCD}$ | 2.5 | 3.0 | 3.5 | kΩ | Internal resistor at ZCD pin |
| VIN voltage threshold for line selection | $V_{VIN\_REF}$ | 1.48 | 1.52 | 1.58 | V | |
| Blanking time for VIN voltage threshold for line selection | $t_{VIN\_REF}$ | - | 16.00 | - | ms | |

---

[1] The parameter is not subjected to production test - verified by design/characterization

**Electrical Characteristics**

## 4.9     Active Burst Mode

Table 14     Active Burst Mode

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Charging current to select burst mode | $I_{sel}$ | 2.1 | 3 | 3.9 | µA | |
| Burst mode selection reference voltage | $V_{REF\_B}$ | 2.65 | 2.75 | 2.85 | V | |
| Feedback voltage for entering Active Burst Mode for level 1 | $V_{FB\_EBL1}$ | 0.86 | 0.90 | 0.94 | V | |
| Feedback voltage for entering Active Burst Mode for level 2 | $V_{FB\_EBL2}$ | 1.0 | 1.05 | 1.1 | V | |
| Blanking time for entering Active Burst Mode | $t_{FB\_BEB}$ | - | 20 | - | ms | |
| Feedback voltage for leaving Active Burst Mode | $V_{FB\_LB}$ | 2.65 | 2.75 | 2.85 | V | |
| Feedback voltage for burst-on | $V_{FB\_BOn}$ | 2.3 | 2.40 | 2.5 | V | |
| Feedback voltage for burst-off | $V_{FB\_BOff}$ | 1.9 | 2.00 | 2.1 | V | |

## 4.10     Line Over Voltage Protection

Table 15     Line OVP

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Line Over Voltage threshold | $V_{VIN\_LOVP}$ | 2.8 | 2.9 | 3.0 | V | |
| Line Over Voltage Blanking | $t_{VIN\_LOVP\_B}$ | - | 250 | - | µs | |

## 4.11     Brownout Protection

Table 16     Brownout Protection

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| BrownIn threshold | $V_{VIN\_BI}$ | 0.63 | 0.66 | 0.69 | V | |
| BrownIn Blanking | $t_{VIN\_BI\_B}$ | - | 250 | - | µs | |
| BrownOut threshold | $V_{VIN\_BO}$ | 0.37 | 0.40 | 0.43 | V | |
| BrownOut Blanking | $t_{VIN\_BO\_B}$ | - | 250 | - | µs | |

**Electrical Characteristics**

## 4.12  $V_{CC}$ Over Voltage Protection

Table 17    Vcc Over Voltage Protection

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| VCC Over Voltage threshold | $V_{VCC\_OVP}$ | 24 | 25.50 | 27 | V | |
| VCC Over Voltage blanking | $t_{VCC\_OVP\_B}$ | - | 50.00 | - | µs | |

## 4.13    Over Load Protection

Table 18    Overload Protection

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Over Load Detection threshold for OLP protection at FB pin | $V_{FB\_OLP}$ | 2.65 | 2.75 | 2.85 | V | |
| Over Load Protection Blanking Time | $t_{FB\_OLP\_B}$ | - | 30 | - | ms | |

## 4.14    Output Over Voltage Protection

Table 19    Output OVP

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output Over Voltage threshold | $V_{ZCD\_OVP}$ | 1.9 | 2.0 | 2.1 | V | |
| Output Over Voltage Blanking Pulse | $P_{ZCD\_OVP\_B}$ | - | 10 | - | pulse | Consecutive Pulse |

## 4.15    Thermal Protection

Table 20    Thermal Protection

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Over temperature protection[1] | $T_{jcon\_OTP}$ | 129 | 140 | 150 | ℃ | Junction temperature of the controller chip (not the CoolMOS™ chip) |
| Over temperature Hysteresis | $T_{jHYS\_OTP}$ | - | 40 | - | ℃ | |
| Over temperature Blanking Time | $t_{jcon\_OTP\_B}$ | - | 50 | - | µs | |

---

[1] The parameter is not subjected to production test - verified by design/characterization

## 4.16    CS Short to GND Protection

**Table 21       CS Short to GND Protection**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|-----------|--------|------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| CS Short to Gnd Protection | $V_{CS\_STG}$ | 0.06 | 0.10 | 0.15 | V | |
| CS Short to Gnd Consecutive Trigger | $P_{CS\_STG}$ | - | 3 | - | cycle | |
| CS Short to Gnd Sample period | $t_{CS\_STG\_SAM}$ | 2.3 | 5 | - | µs | |

## 4.17    CoolMOS™ Section

**Table 22       ICE5QRxxxxAx**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|-----------|--------|------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Drain Source Breakdown Voltage | $V_{(BR)DSS}$ | | | | V | $T_j = 25°C$ |
| ICE5QRxx70Ax | | 700 | - | - | | |
| ICE5QRxx80Ax | | 800 | - | - | | |
| Drain to CS On-Resistance (inclusive of low side MOSFET) | $R_{DSon}$ | | | | Ω | |
| ICE5QR4770AZ | | - | 4.73 | 5.18 | | $Tj = 25°C$ |
| | | - | 8.73 | - | | $Tj=125°C[1]$, $I_D =0.4A$ |
| ICE5QR4780AZ | | - | 4.13 | 4.85 | | $Tj = 25°C$ |
| | | - | 8.69 | - | | $Tj=125°C[1]$, $I_D =0.4A$ |
| ICE5QR2270AZ | | - | 2.13 | 2.33 | | $Tj = 25°C$ |
| | | - | 4.31 | - | | $Tj=125°C[1]$, $I_D =1A$ |
| ICE5QR2280AZ | | - | 2.13 | 2.35 | | $Tj = 25°C$ |
| | | - | 4.31 | - | | $Tj=125°C[1]$, $I_D =1A$ |
| ICE5QR1070AZ | | - | 1.15 | 1.25 | | $Tj = 25°C$ |
| | | - | 1.85 | | | $Tj=125°C[1]$, $I_D =1.1A$ |
| ICE5QR0680AZ | | - | 0.71 | 0.80 | | $Tj = 25°C$ |
| | | - | 1.27 | - | | $Tj=125°C[1]$, $I_D =2A$ |
| ICE5QR4770AG | | - | 4.73 | 5.18 | | $Tj = 25°C$ |
| | | - | 8.73 | - | | $Tj=125°C[1]$, $I_D =0.4A$ |
| ICE5QR1680AG | | - | 1.53 | 1.75 | | $Tj = 25°C$ |
| | | - | 3.01 | - | | $Tj=125°C[1]$, $I_D =1.4A$ |
| ICE5QR0680AG | | - | 0.71 | 0.80 | | $Tj = 25°C$ |
| | | - | 1.27 | - | | $Tj=125°C[1]$, $I_D =2A$ |

## Electrical Characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| Effective output capacitance, energy related[1] | $C_{o(er)}$ | | | | pF | |
| ICE5QR4770AZ | | - | 3.4 | - | | $V_{GS}$=0V,$V_{DS}$=0~480V |
| ICE5QR4780AZ | | - | 3 | - | | $V_{GS}$=0V,$V_{DS}$=0~500V |
| ICE5QR2270AZ | | - | 10 | - | | $V_{GS}$=0V,$V_{DS}$=0~480V |
| ICE5QR2280AZ | | - | 7 | - | | $V_{GS}$=0V,$V_{DS}$=0~500V |
| ICE5QR1070AZ | | - | 13 | - | | $V_{GS}$=0V,$V_{DS}$=0~400V |
| ICE5QR0680AZ | | - | 24 | - | | $V_{GS}$=0V,$V_{DS}$=0~500V |
| ICE5QR4770AG | | - | 3.4 | - | | $V_{GS}$=0V,$V_{DS}$=0~480V |
| ICE5QR1680AG | | - | 8 | - | | $V_{GS}$=0V,$V_{DS}$=0~500V |
| ICE5QR0680AG | | - | 24 | - | | $V_{GS}$=0V,$V_{DS}$=0~500V |
| Rise Time[2] | $t_{rise}$ | - | 30 | - | ns | |
| Fall Time[2] | $t_{fall}$ | - | 30 | - | ns | |

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[1]The parameter is not subjected to production test - verified by design/characterization

[2]Measured in a Typical Flyback Converter Application

# 5 CoolMOS™ Performance Characteristics
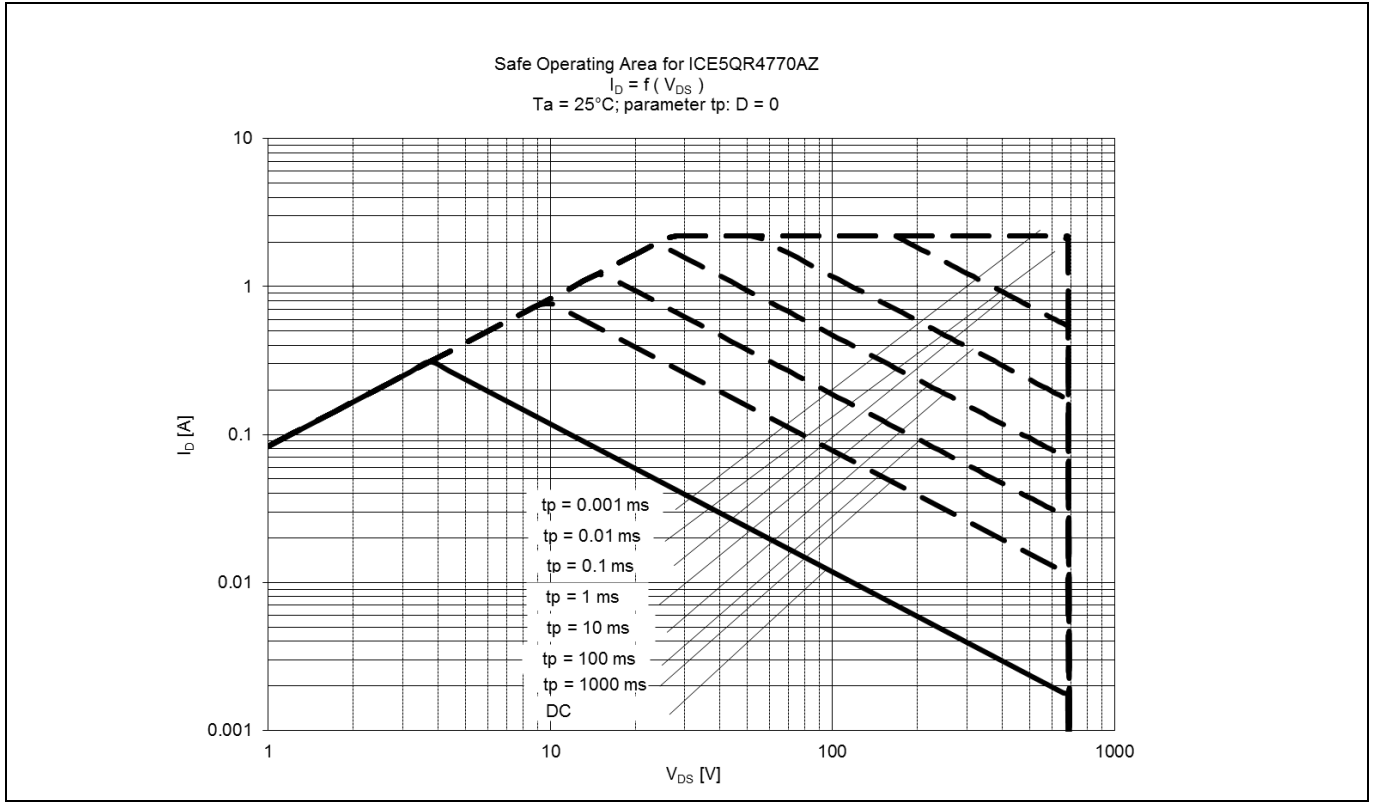


**Figure 14    Safe Operating Area (SOA) curve for ICE5QR4770AZ**
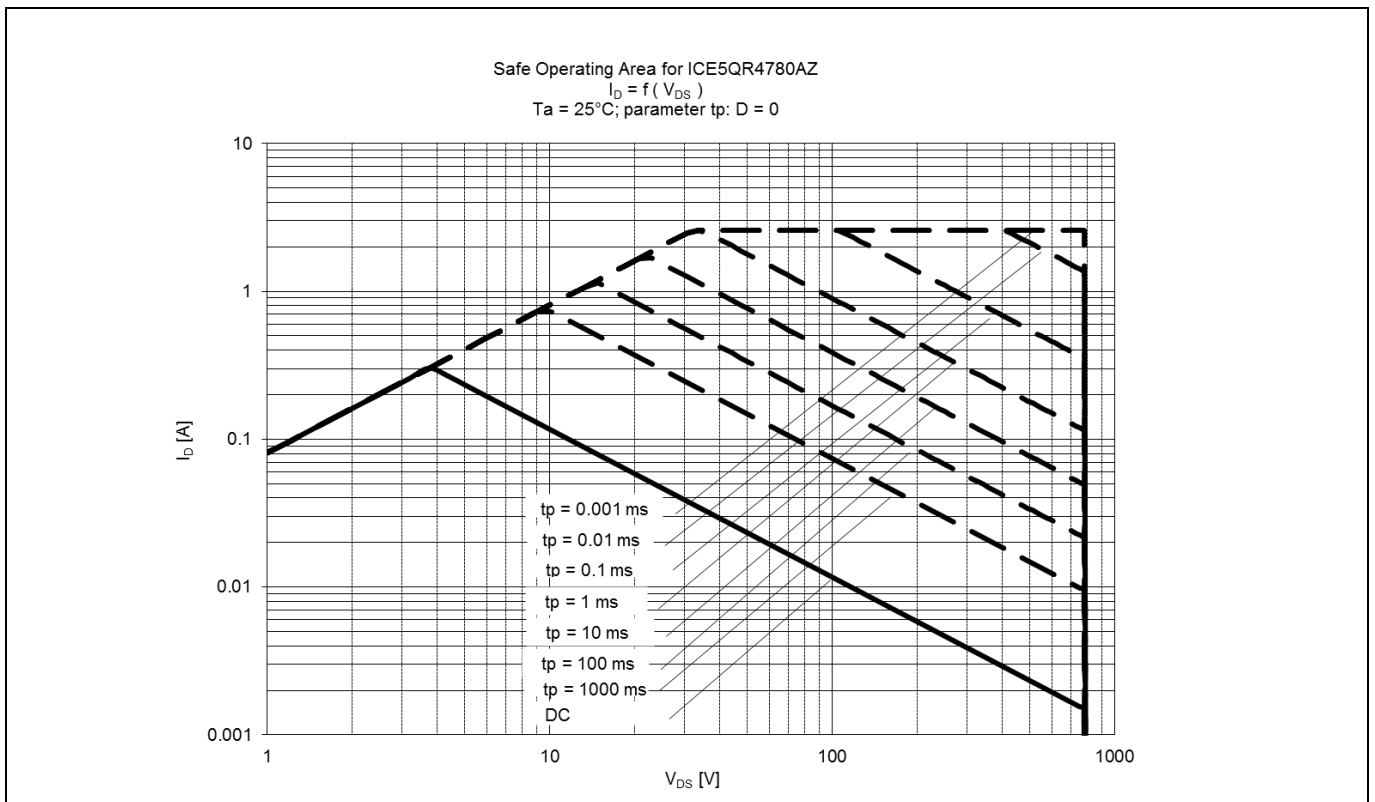


**Figure 15    Safe Operating Area (SOA) curve for ICE5QR4780AZ**

**CoolMOS™ Performance Characteristics**
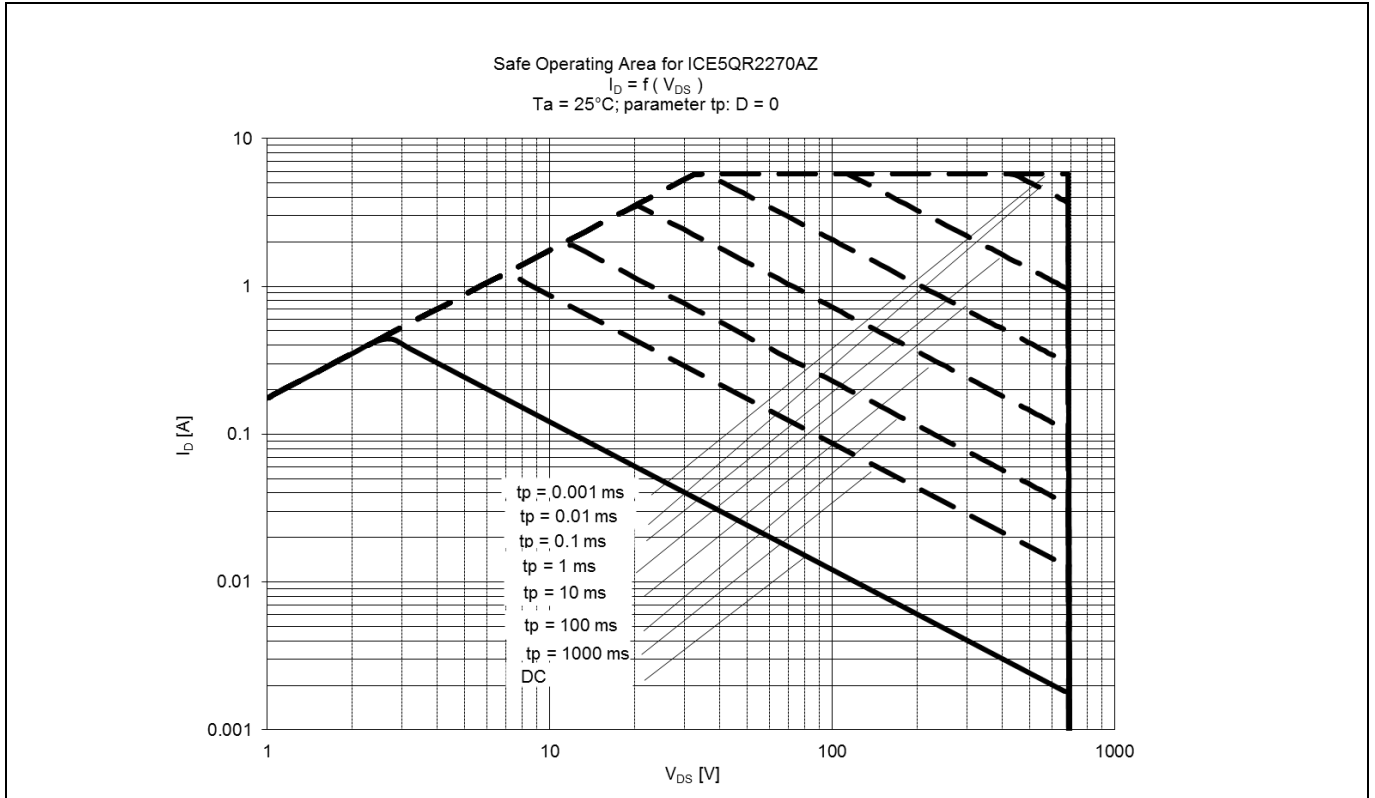


**Figure 16    Safe Operating Area (SOA) curve for ICE5QR2270AZ**
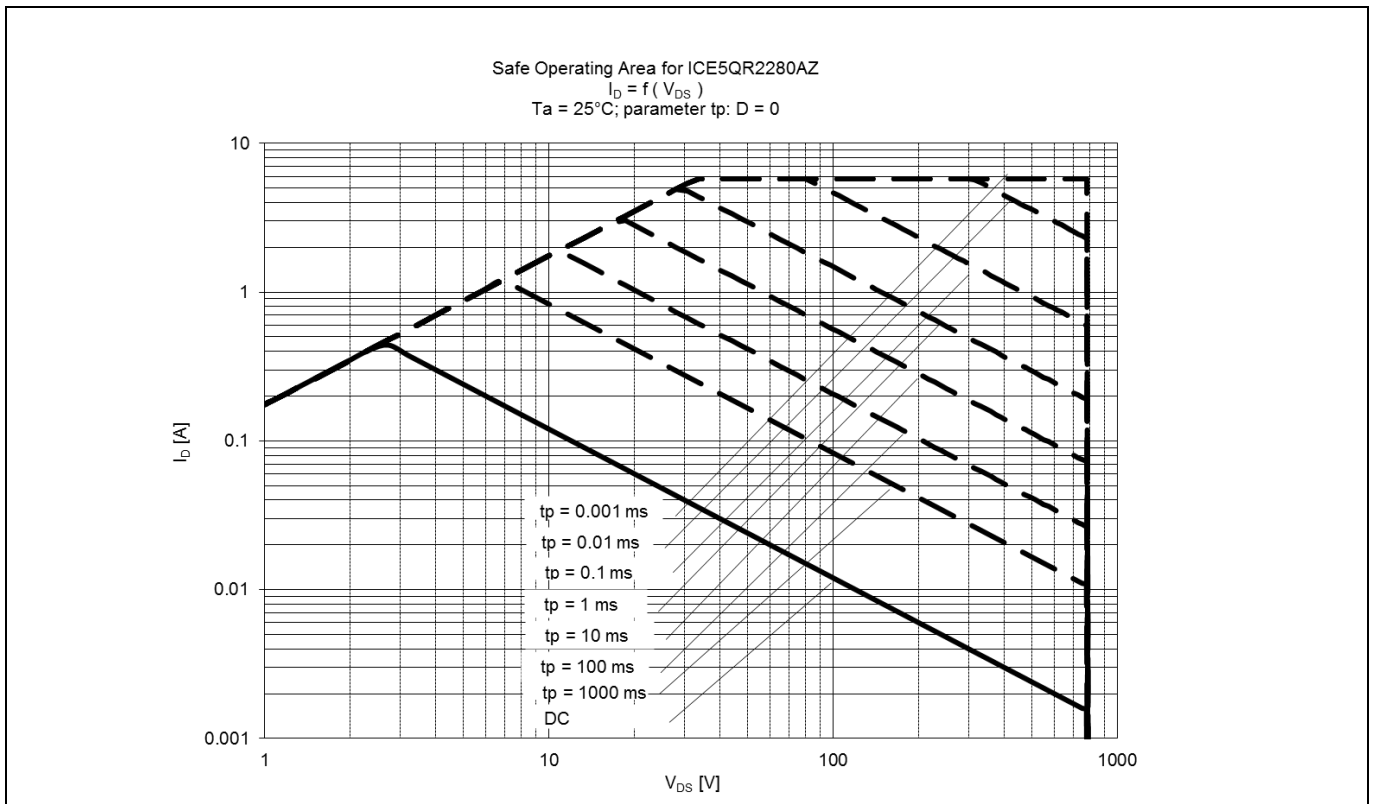


**Figure 17    Safe Operating Area (SOA) curve for ICE5QR2280AZ**

**CoolMOS™ Performance Characteristics**
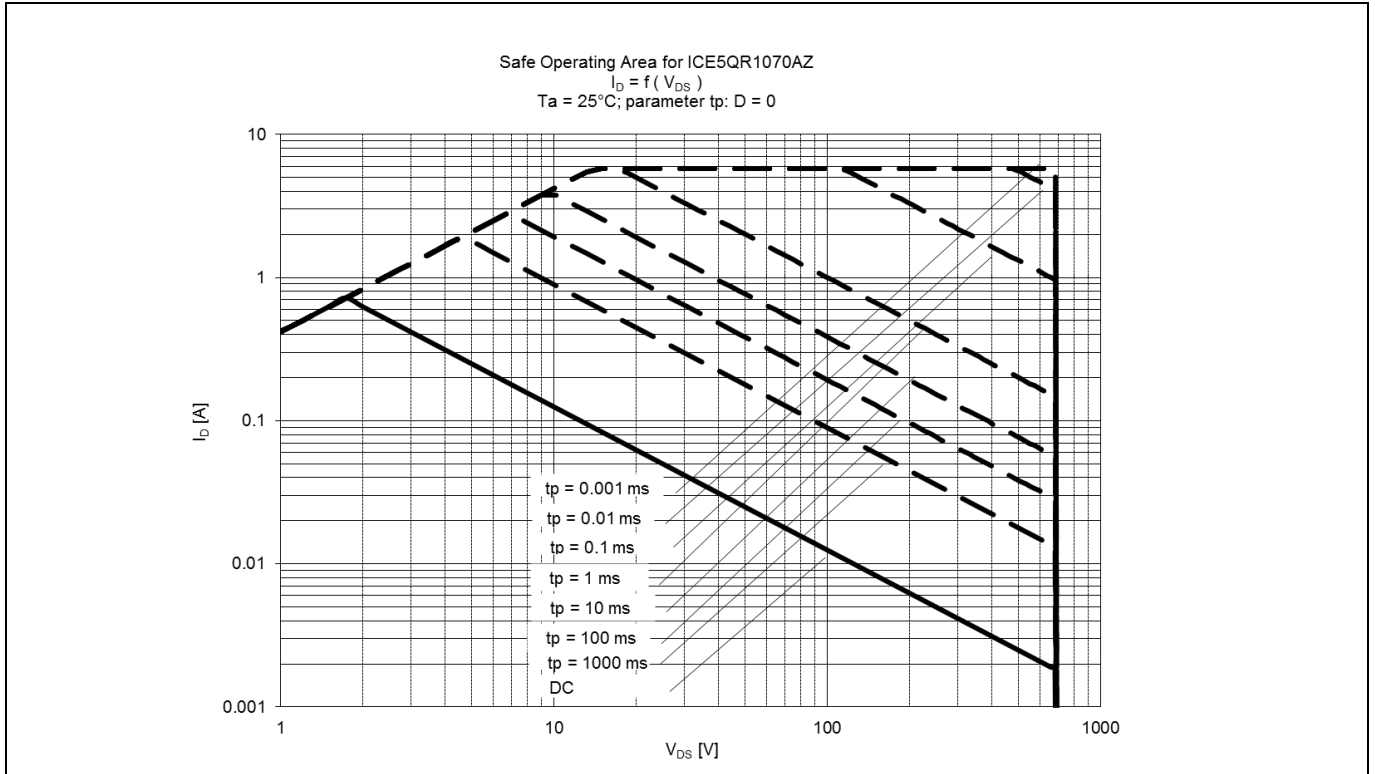


**Figure 18    Safe Operating Area (SOA) curve for ICE5QR1070AZ**
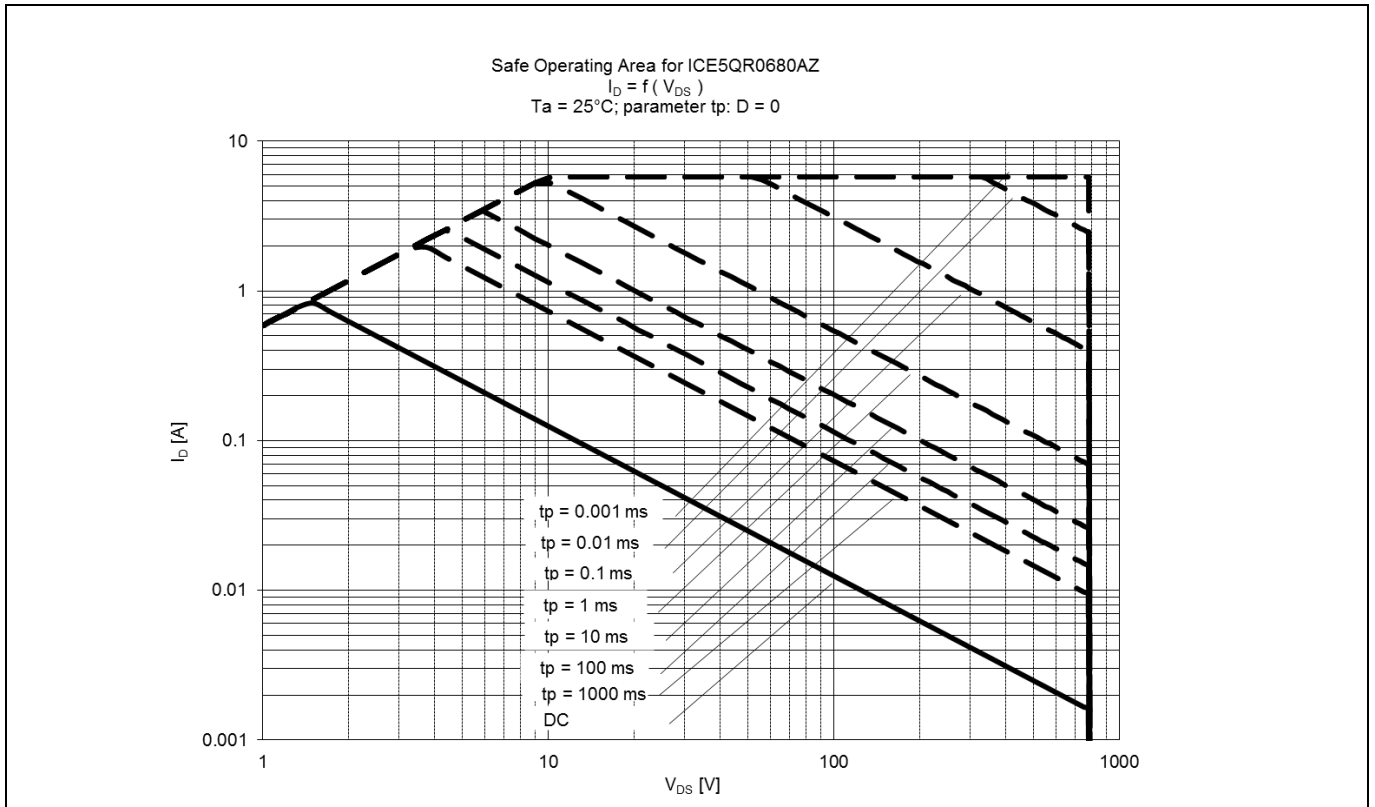


**Figure 19    Safe Operating Area (SOA) curve for ICE5QR0680AZ**

**CoolMOS™ Performance Characteristics**

Safe Operating Area for ICE5QR4770AG
$I_D = f ( V_{DS} )$
Ta = 25°C; parameter tp: D = 0

tp = 0.001 ms
tp = 0.01 ms
tp = 0.1 ms
tp = 1 ms
tp = 10 ms
tp = 100 ms
tp = 1000 ms
DC
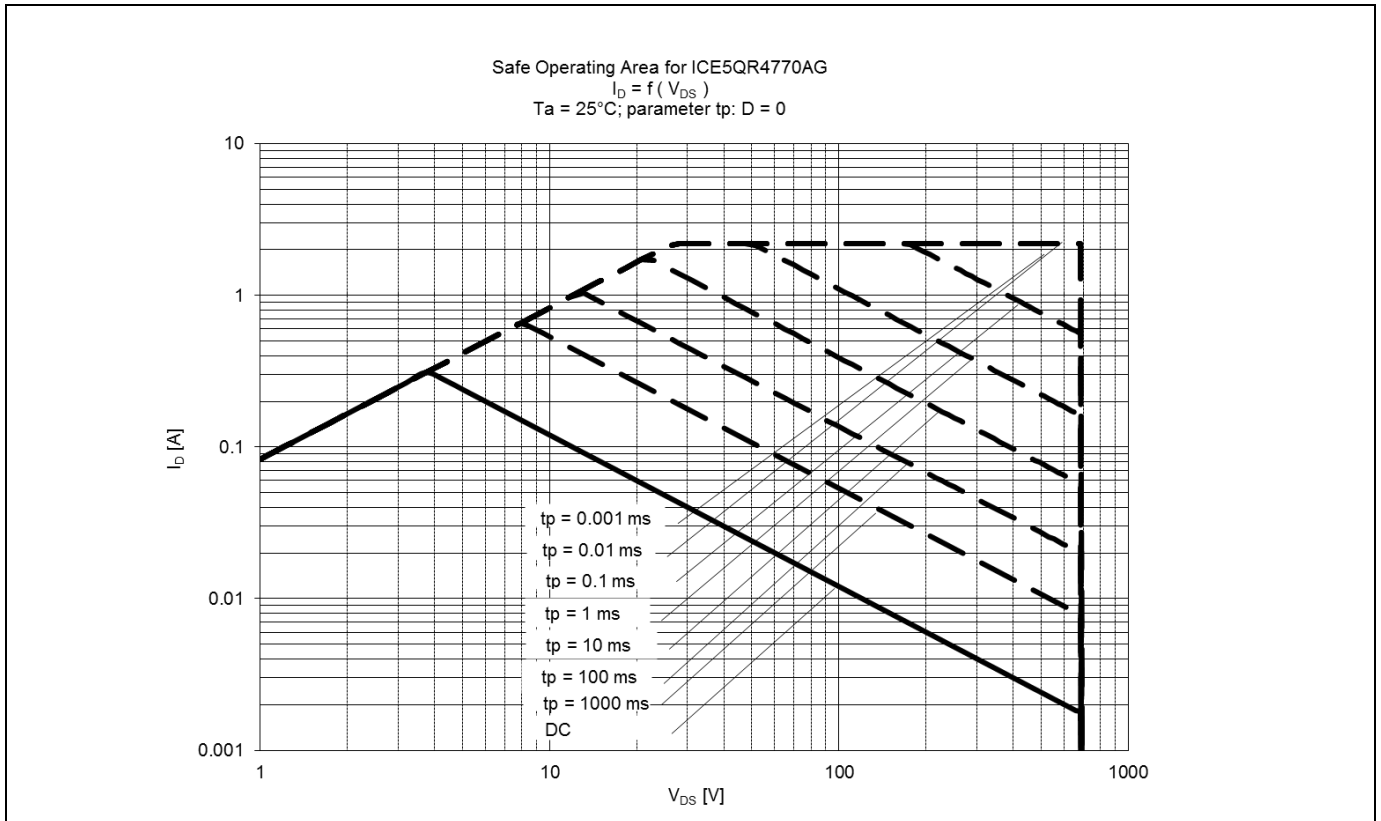
**Figure 20    Safe Operating Area (SOA) curve for ICE5QR4770AG**

Safe Operating Area for ICE5QR1680AG
$I_D = f ( V_{DS} )$
Ta = 25°C; parameter tp: D = 0

tp = 0.001 ms
tp = 0.01 ms
tp = 0.1 ms
tp = 1 ms
tp = 10 ms
tp = 100 ms
tp = 1000 ms
DC
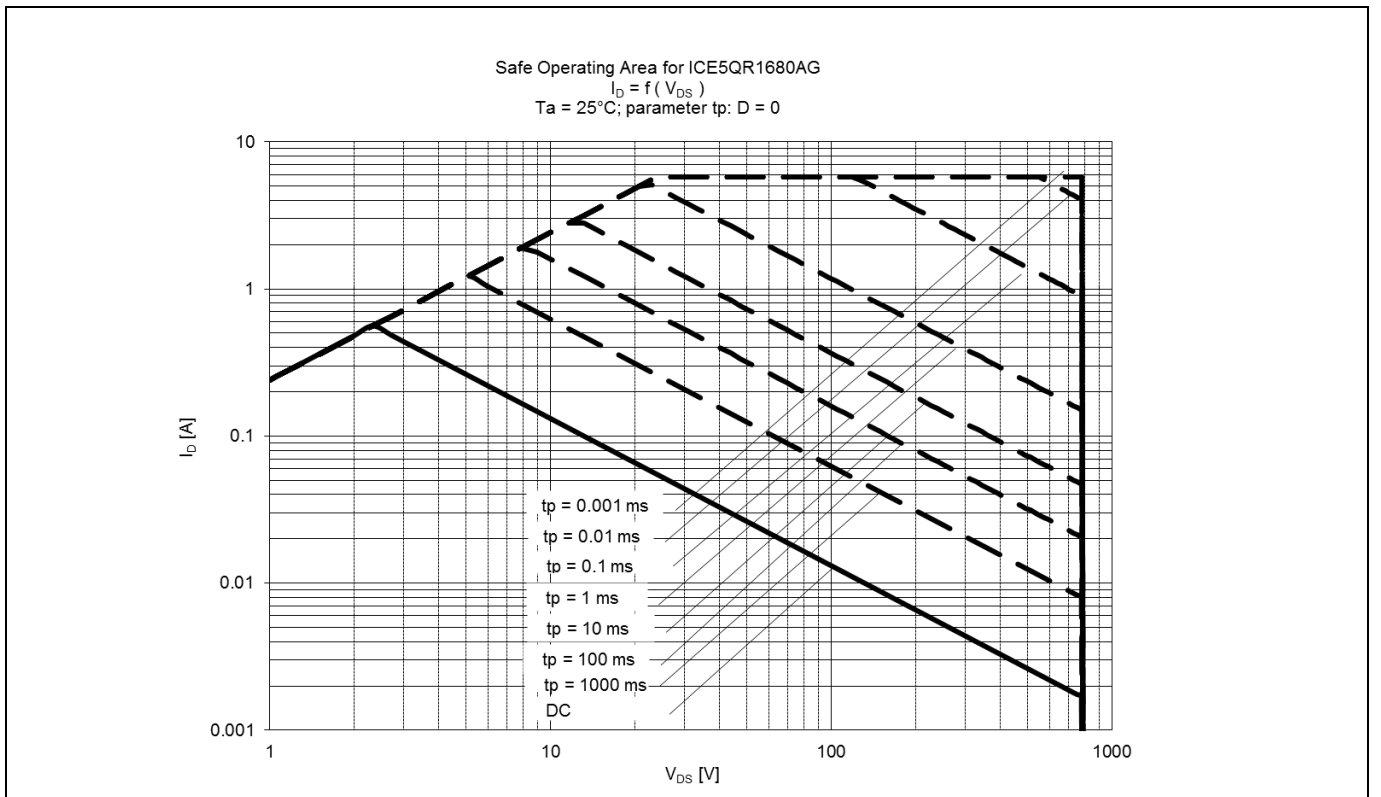
**Figure 21    Safe Operating Area (SOA) curve for ICE5QR1680AG**

**CoolMOS™ Performance Characteristics**



Safe Operating Area for ICE5QR0680AG
$I_D = f(V_{DS})$
Ta = 25°C; parameter tp: D = 0

tp = 0.001 ms
tp = 0.01 ms
tp = 0.1 ms
tp = 1 ms
tp = 10 ms
tp = 100 ms
tp = 1000 ms
DC
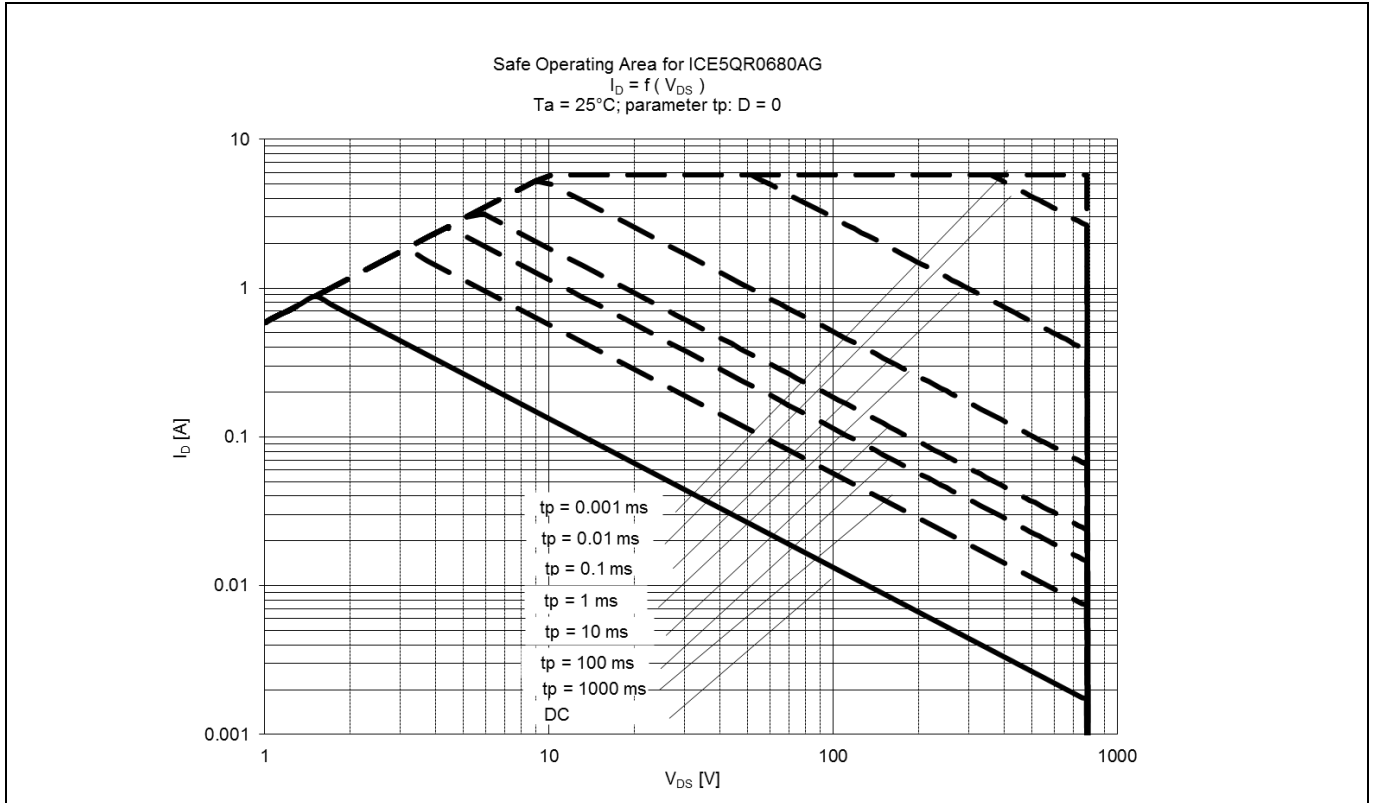
**Figure 22    Safe Operating Area (SOA) curve for ICE5QR0680AG**



Allowable Power Dissipation for ICE5QR4770AZ in DIP-7 package
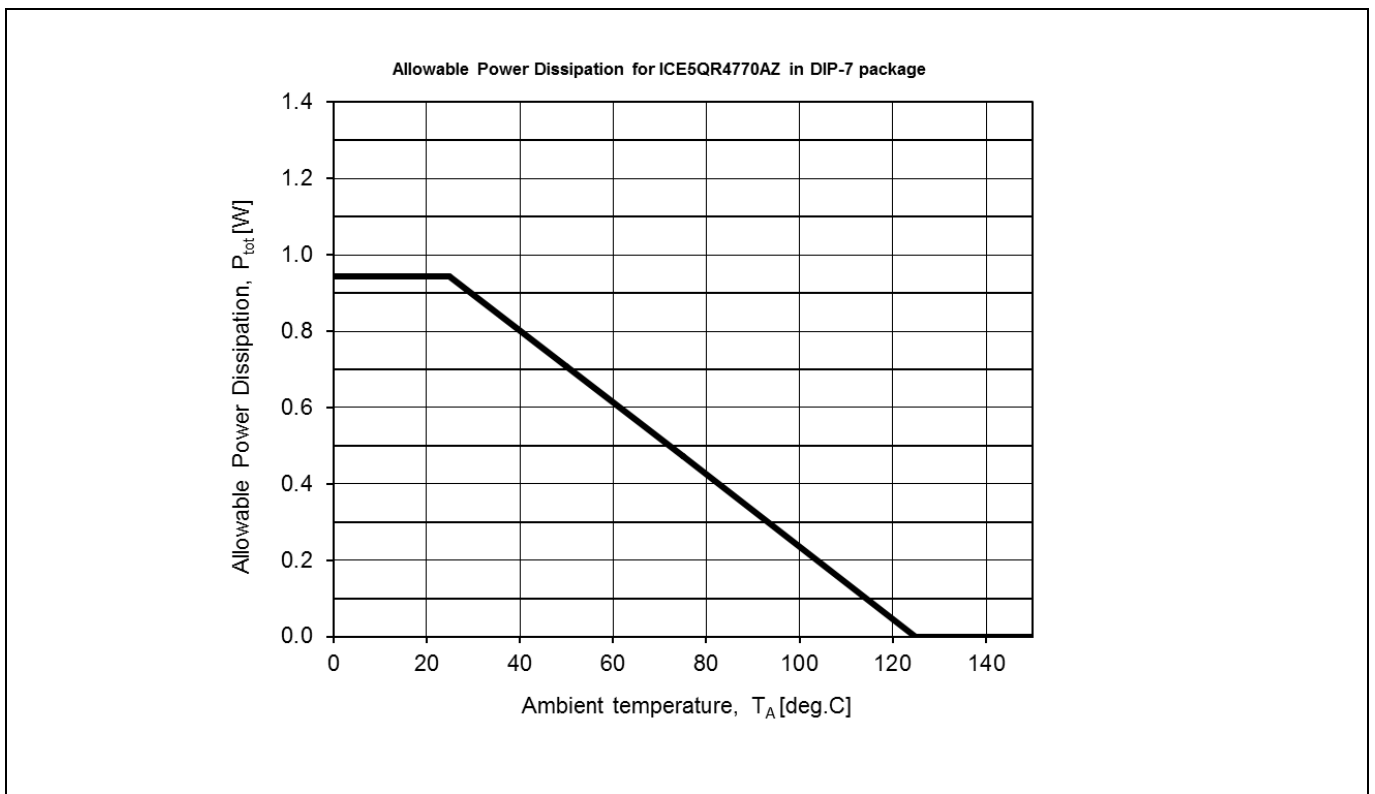
**Figure 23    Power dissipation of ICE5QR4770AZ, DIP-7 package; $P_{tot}$=f($T_a$), (Maximum ratings as given in section 4.1 must not be exceeded)**

**CoolMOS™ Performance Characteristics**
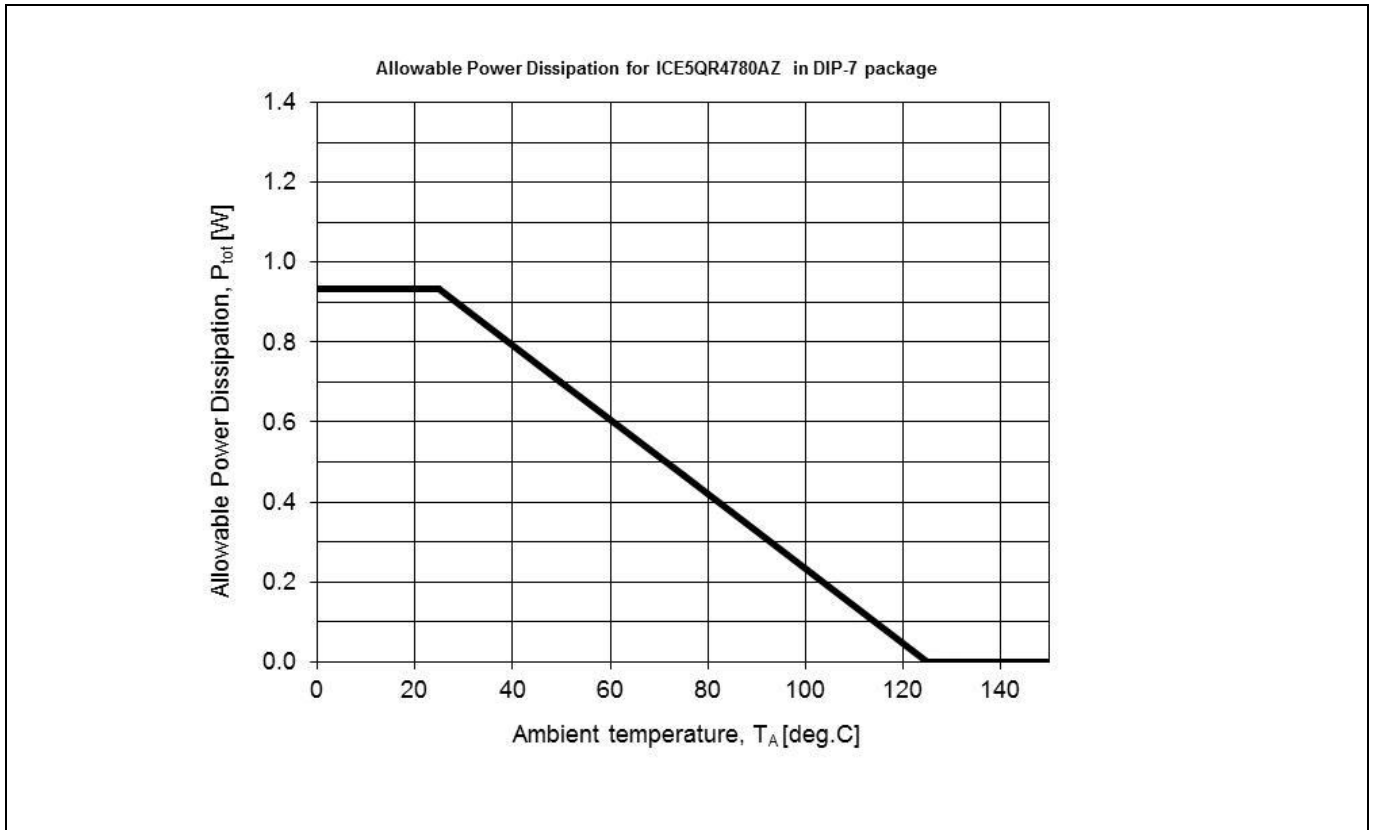


**Figure 24    Power dissipation of ICE5QR4780AZ, DIP-7 package; $P_{tot}$=f($T_a$), (Maximum ratings as given in section 4.1 must not be exceeded)**
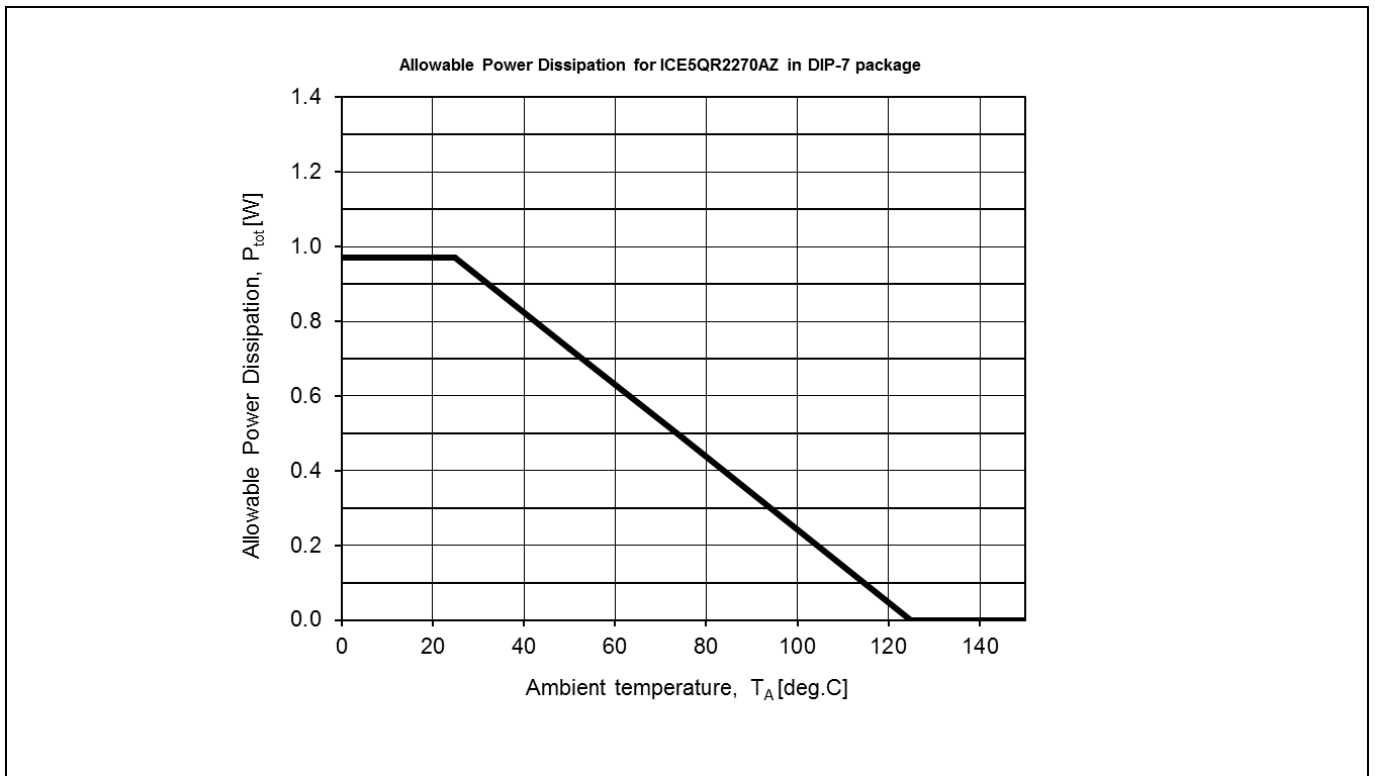


**Figure 25    Power dissipation of ICE5QR2270AZ, DIP-7 package; $P_{tot}$=f($T_a$), (Maximum ratings as given in section 4.1 must not be exceeded)**

**CoolMOS™ Performance Characteristics**
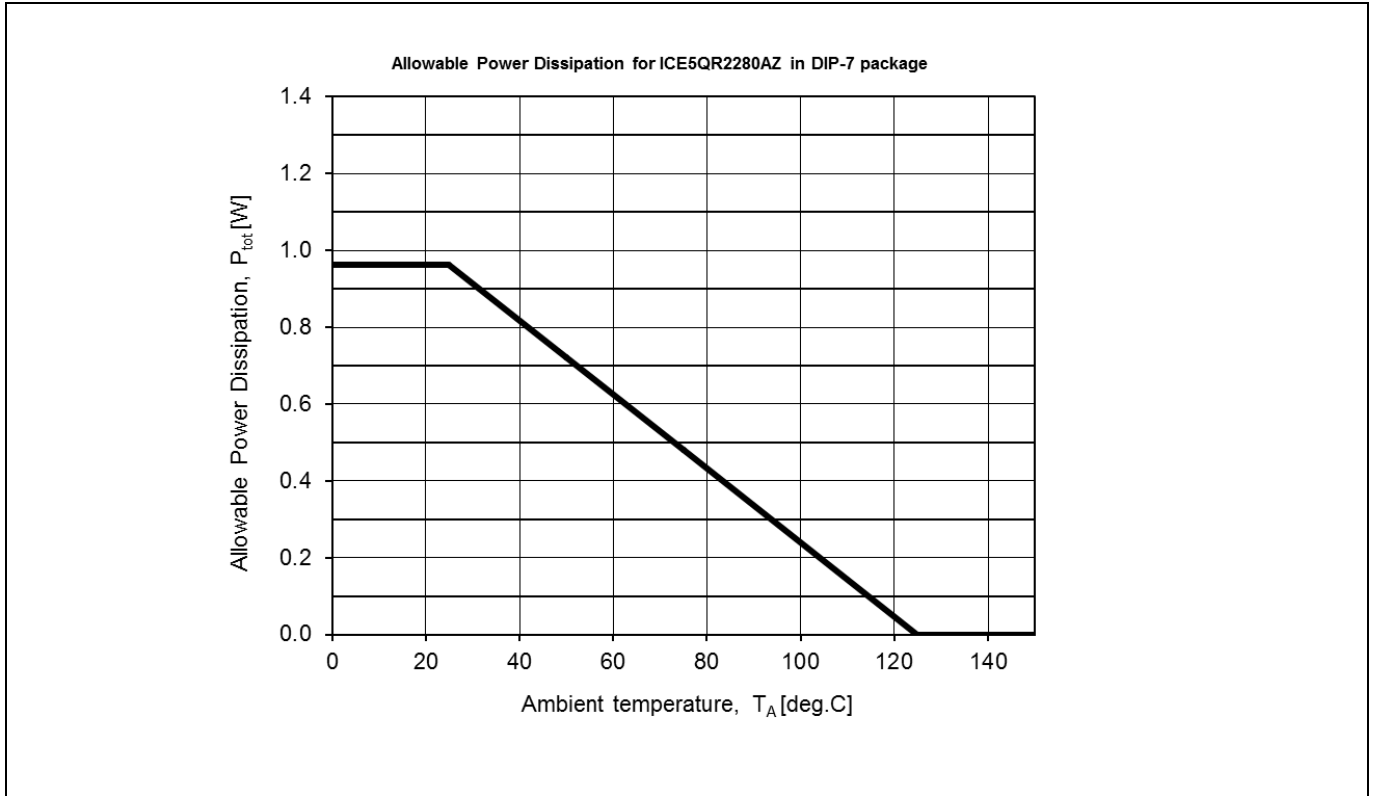


**Figure 26** **Power dissipation of ICE5QR2280AZ, DIP-7 package; $P_{tot}$=f($T_a$), (Maximum ratings as given in section 4.1 must not be exceeded)**
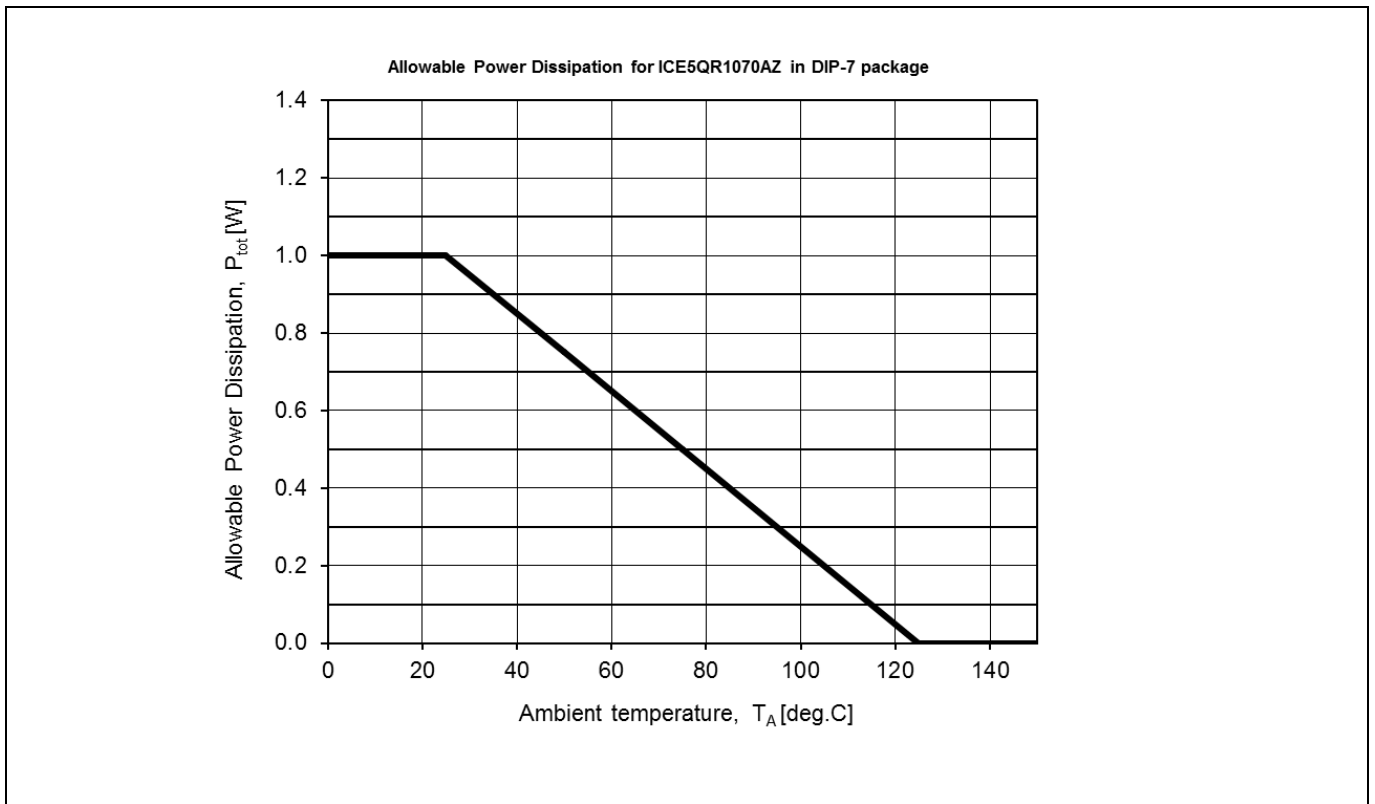


**Figure 27** **Power dissipation of ICE5QR1070AZ, DIP-7 package; $P_{tot}$=f($T_a$), (Maximum ratings as given in section 4.1 must not be exceeded)**

**CoolMOS™ Performance Characteristics**
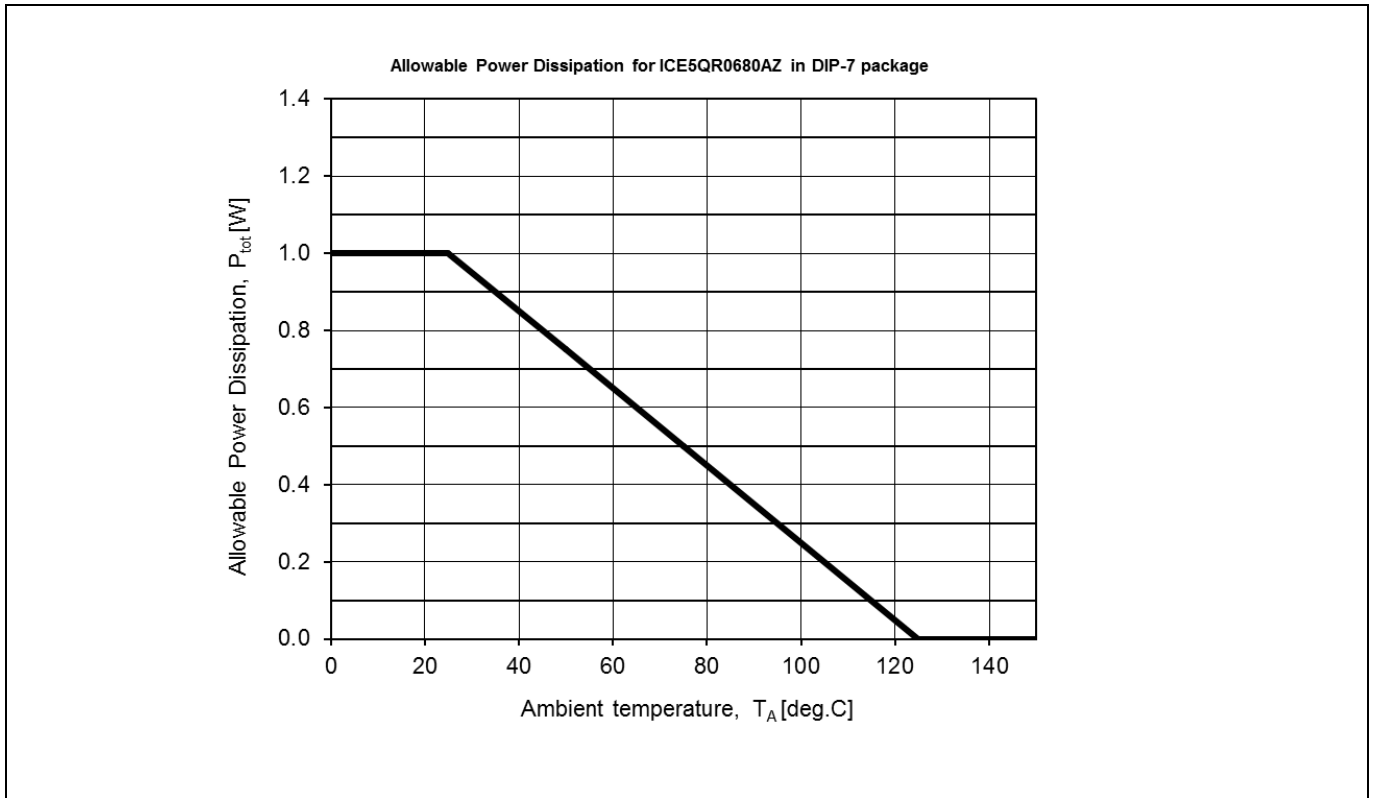


**Figure 28    Power dissipation of ICE5QR0680AZ, DIP-7 package; $P_{tot}=f(T_a)$, (Maximum ratings as given in section 4.1 must not be exceeded)**
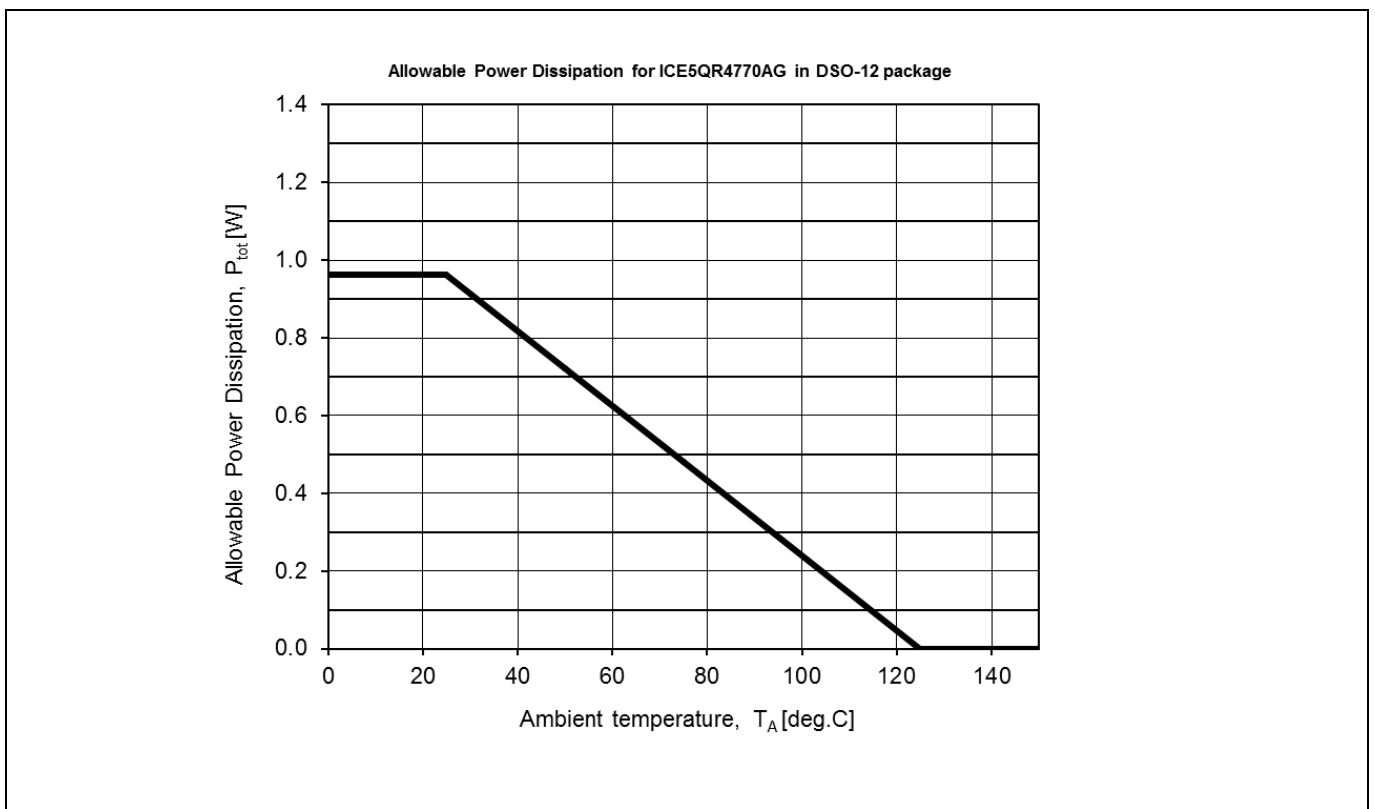


**Figure 29    Power dissipation of ICE5QR4770AG, DSO-12 package; $P_{tot}=f(T_a)$, (Maximum ratings as given in section 4.1 must not be exceeded)**

**CoolMOS™ Performance Characteristics**
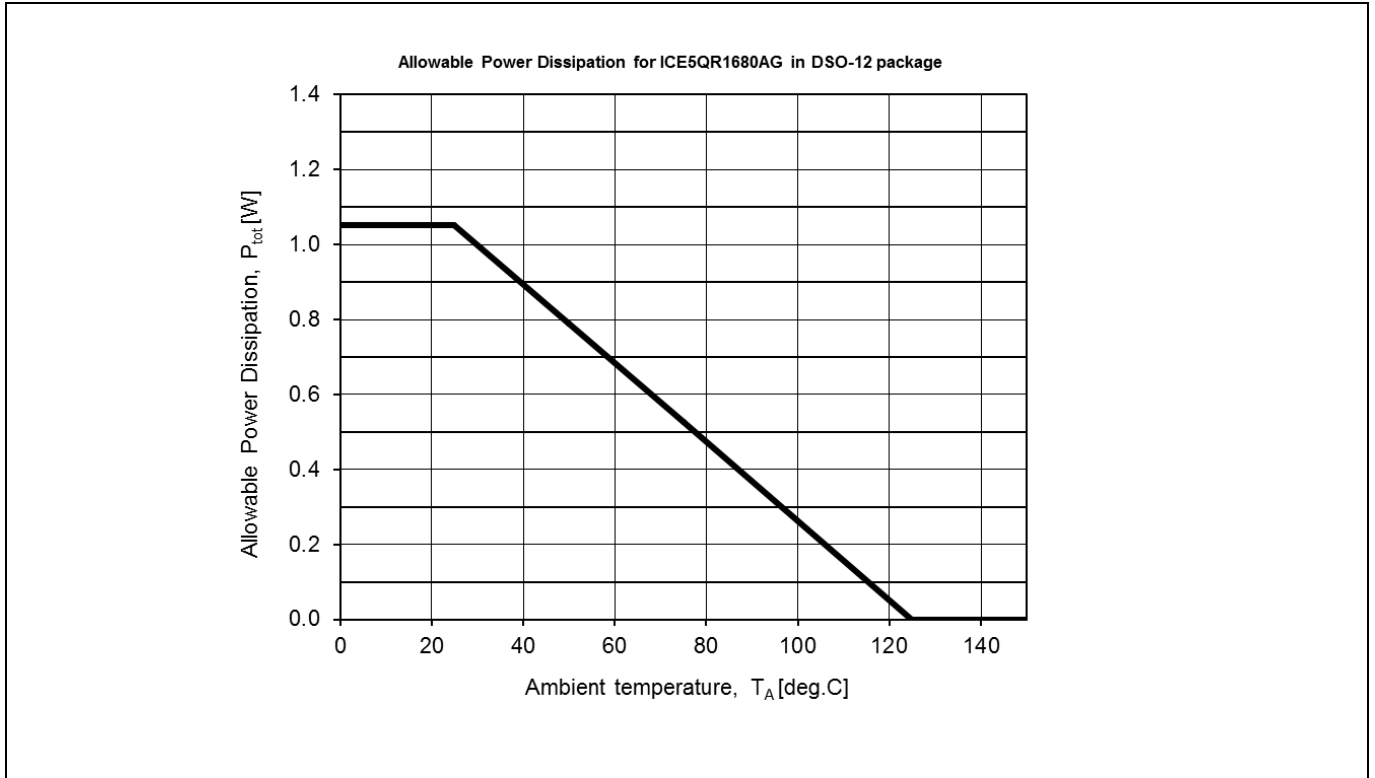


**Figure 30    Power dissipation of ICE5QR1680AG, DSO-12 package; P$_{tot}$=f(T$_a$), (Maximum ratings as given in section 4.1 must not be exceeded)**
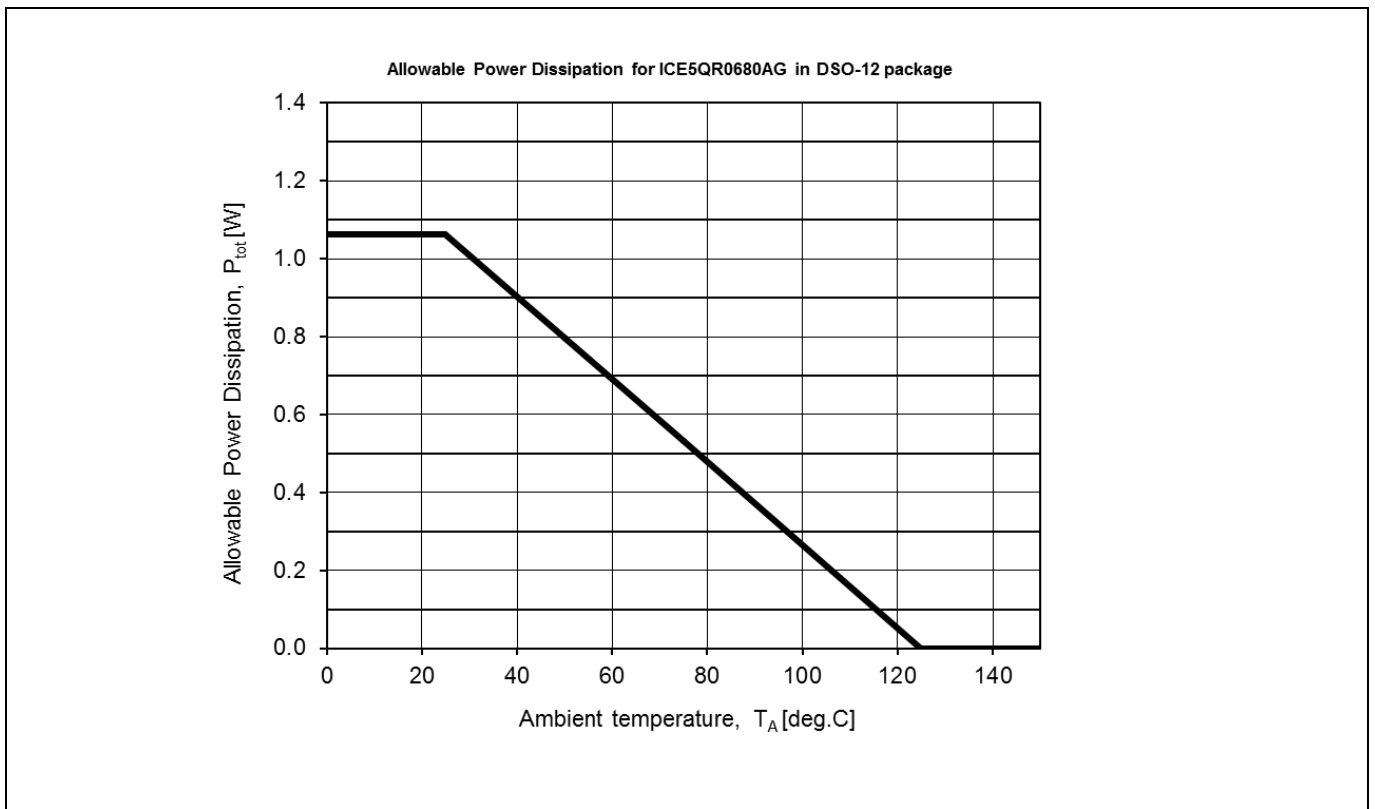


**Figure 31    Power dissipation of ICE5QR0680AG, DSO-12 package; P$_{tot}$=f(T$_a$), (Maximum ratings as given in section 4.1 must not be exceeded)**

**CoolMOS™ Performance Characteristics**
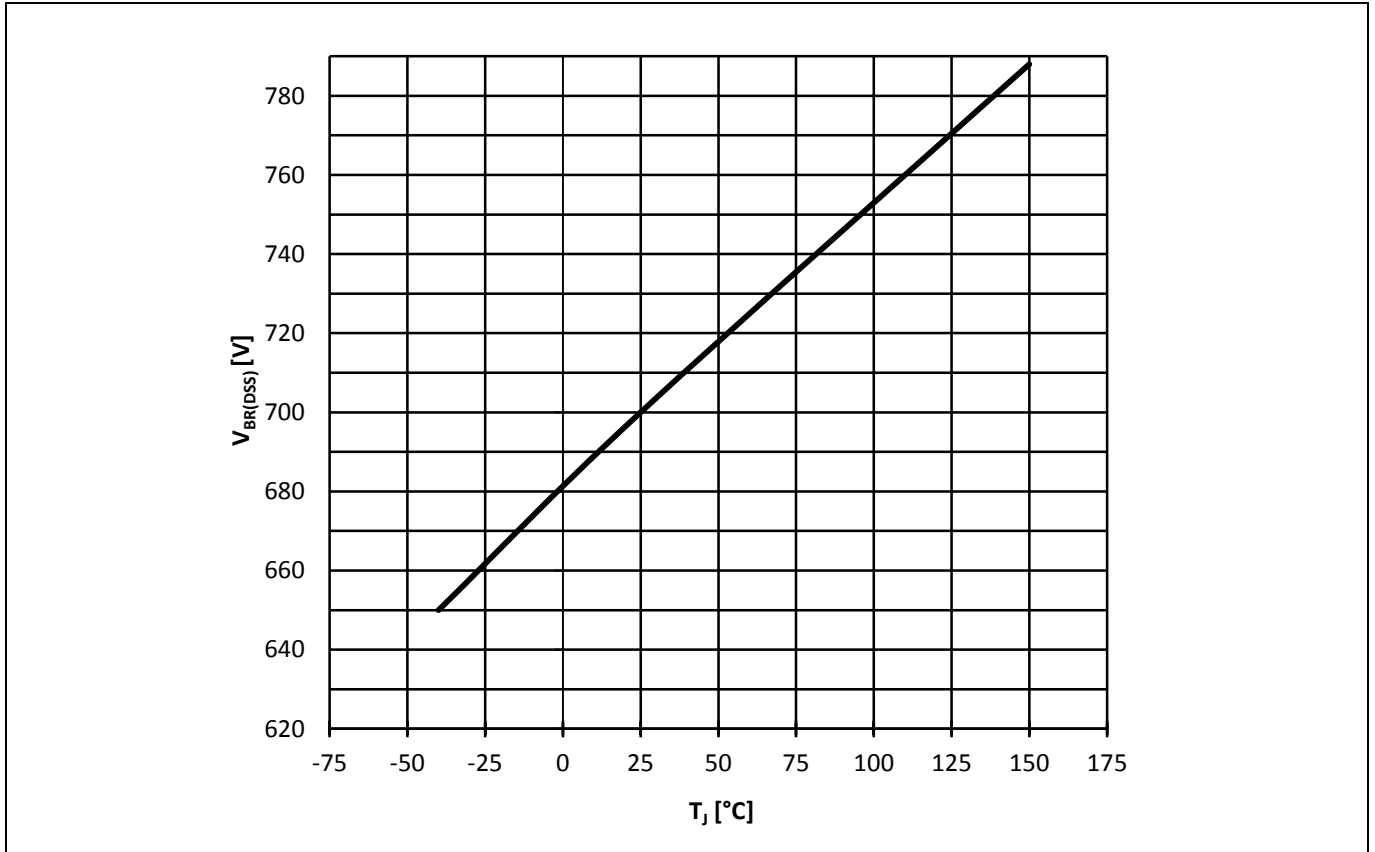


**Figure 32    Drain-source breakdown voltage ICE5QRxx70Ax; $V_{BR(DSS)}=f(T_J)$, $I_D$=1 mA**
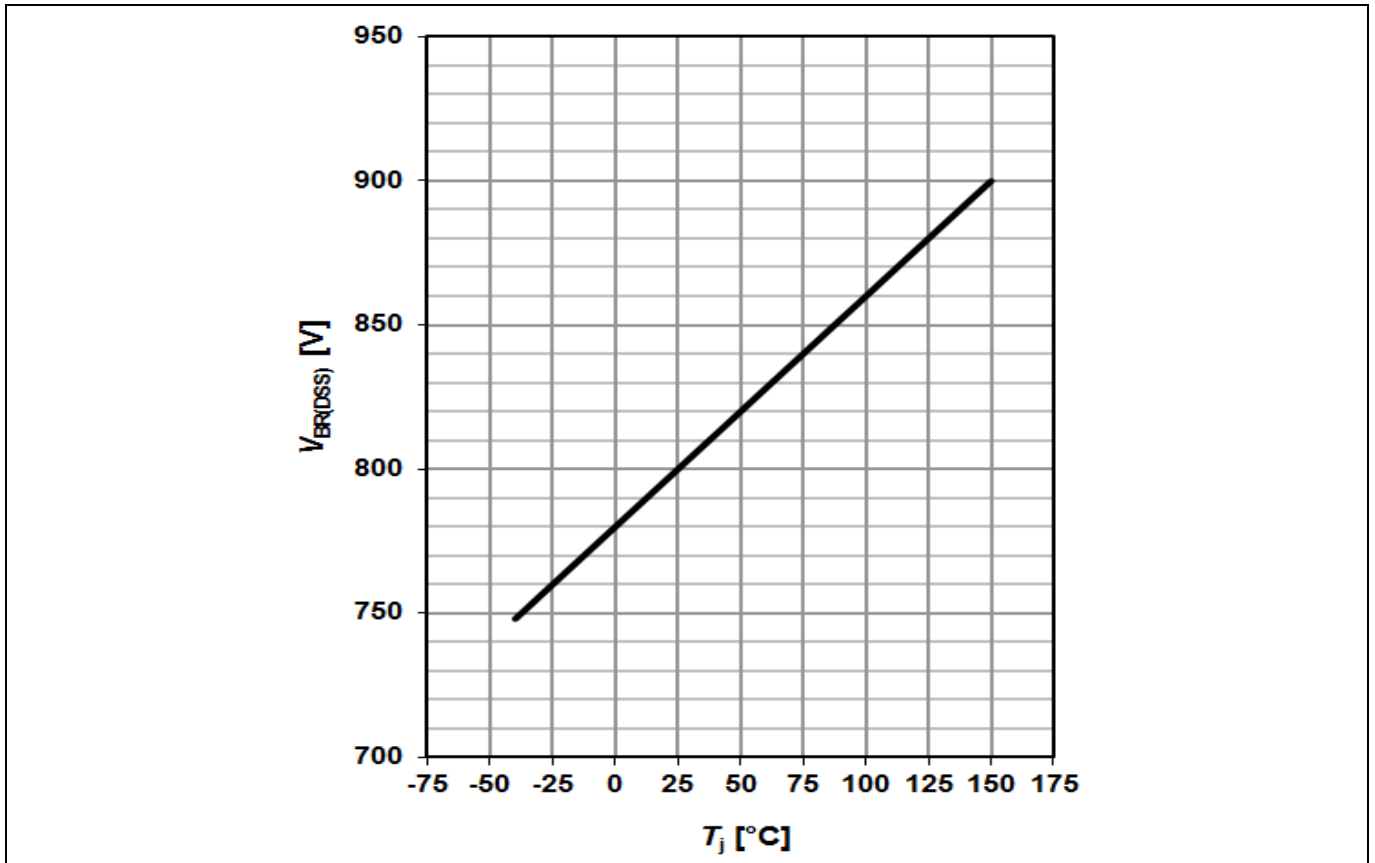


**Figure 33    Drain-source breakdown voltage ICE5QRxx80Ax; $V_{BR(DSS)}=f(T_J)$, $I_D$=1 mA**

**CoolMOS™ Performance Characteristics**
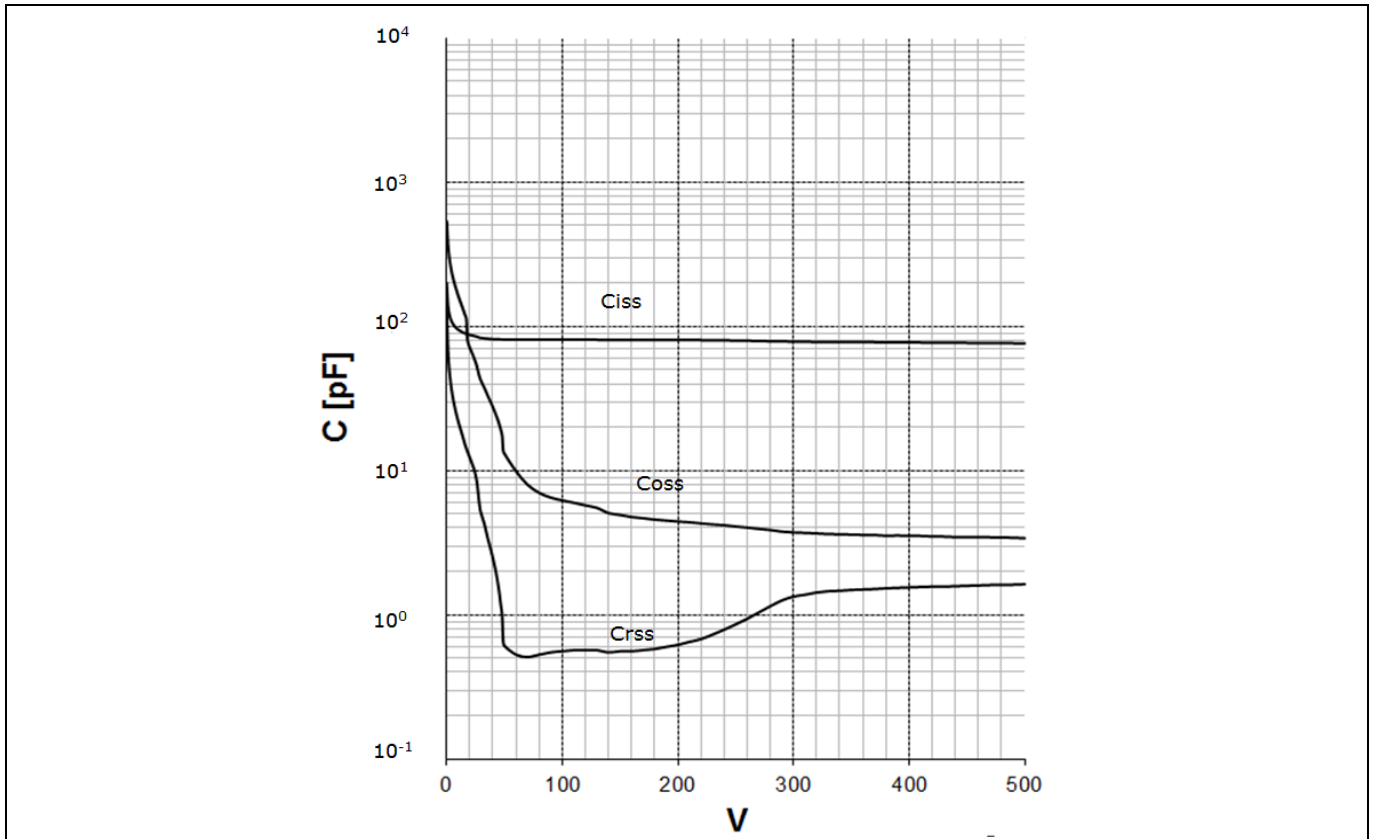


**Figure 34    Typical CoolMOS™ capacitances of ICE5QR4770Ax (C=f($V_{DS}$);$V_{GS}$=0 V; f=1 MHz)**
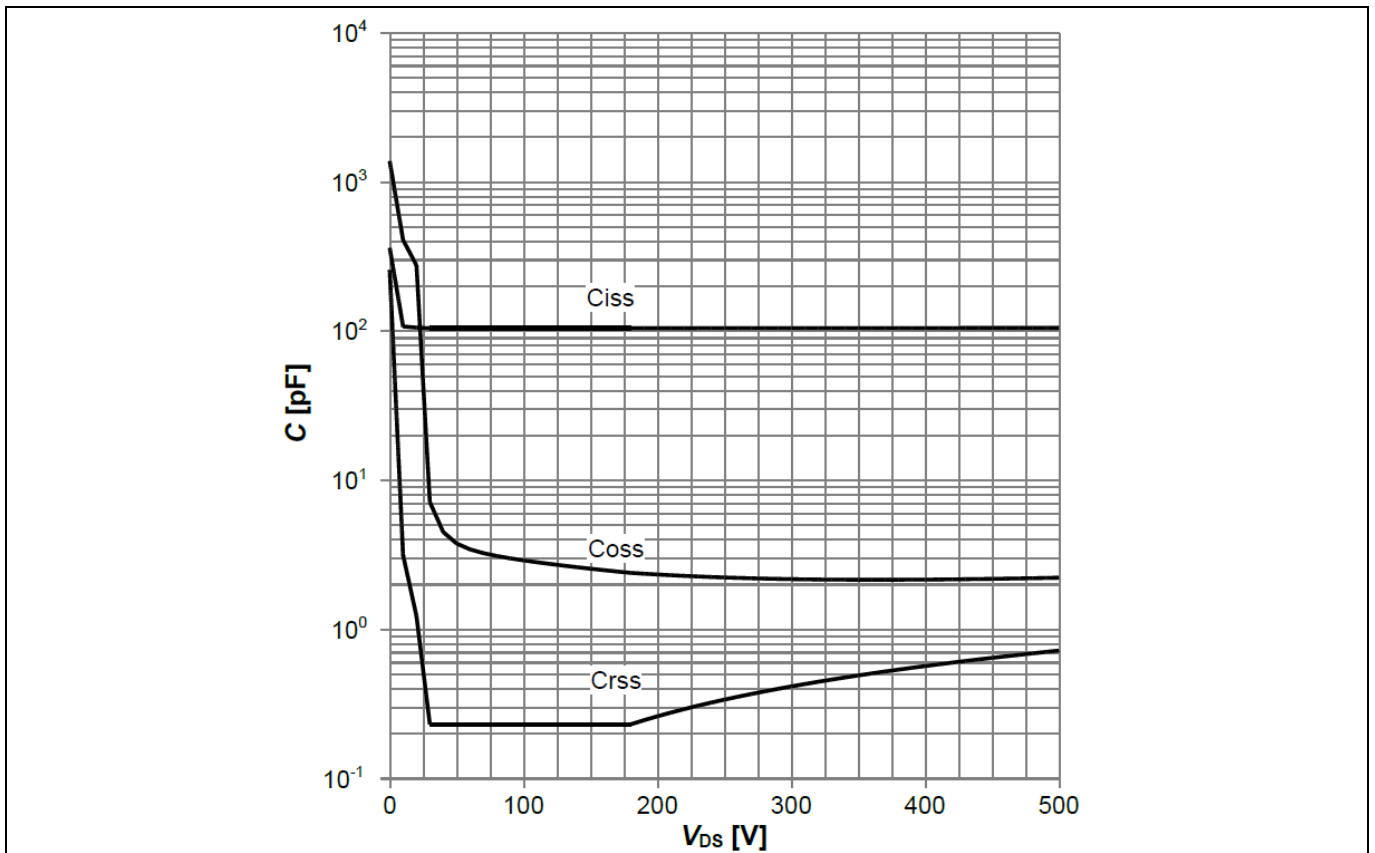


**Figure 35    Typical CoolMOS™ capacitances of ICE5QR4780AZ (C=f($V_{DS}$);$V_{GS}$=0 V; f=250 kHz)**

**CoolMOS™ Performance Characteristics**
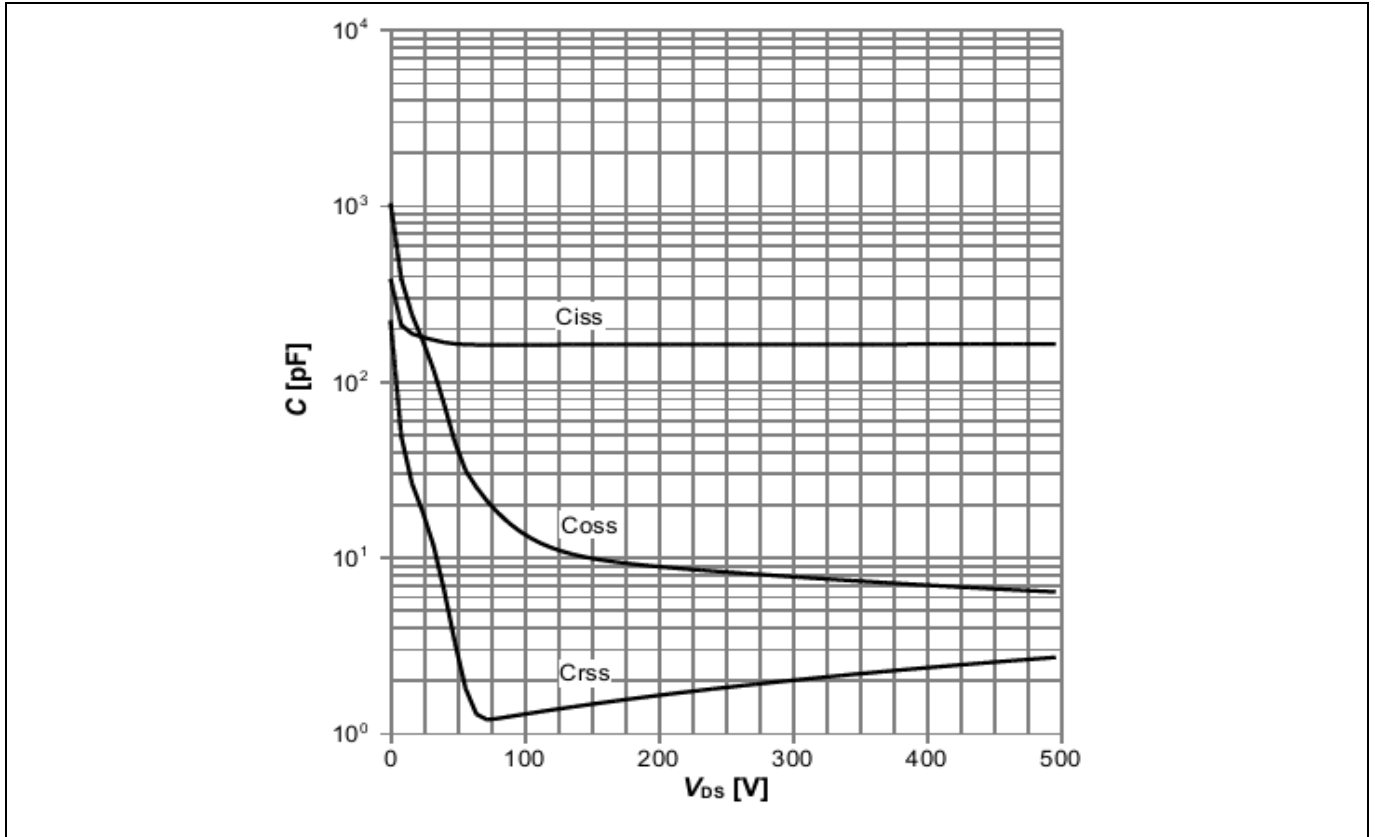


**Figure 36    Typical CoolMOS™ capacitances of ICE5QR2270AZ (C=f($V_{DS}$);$V_{GS}$=0 V; f=1 MHz)**
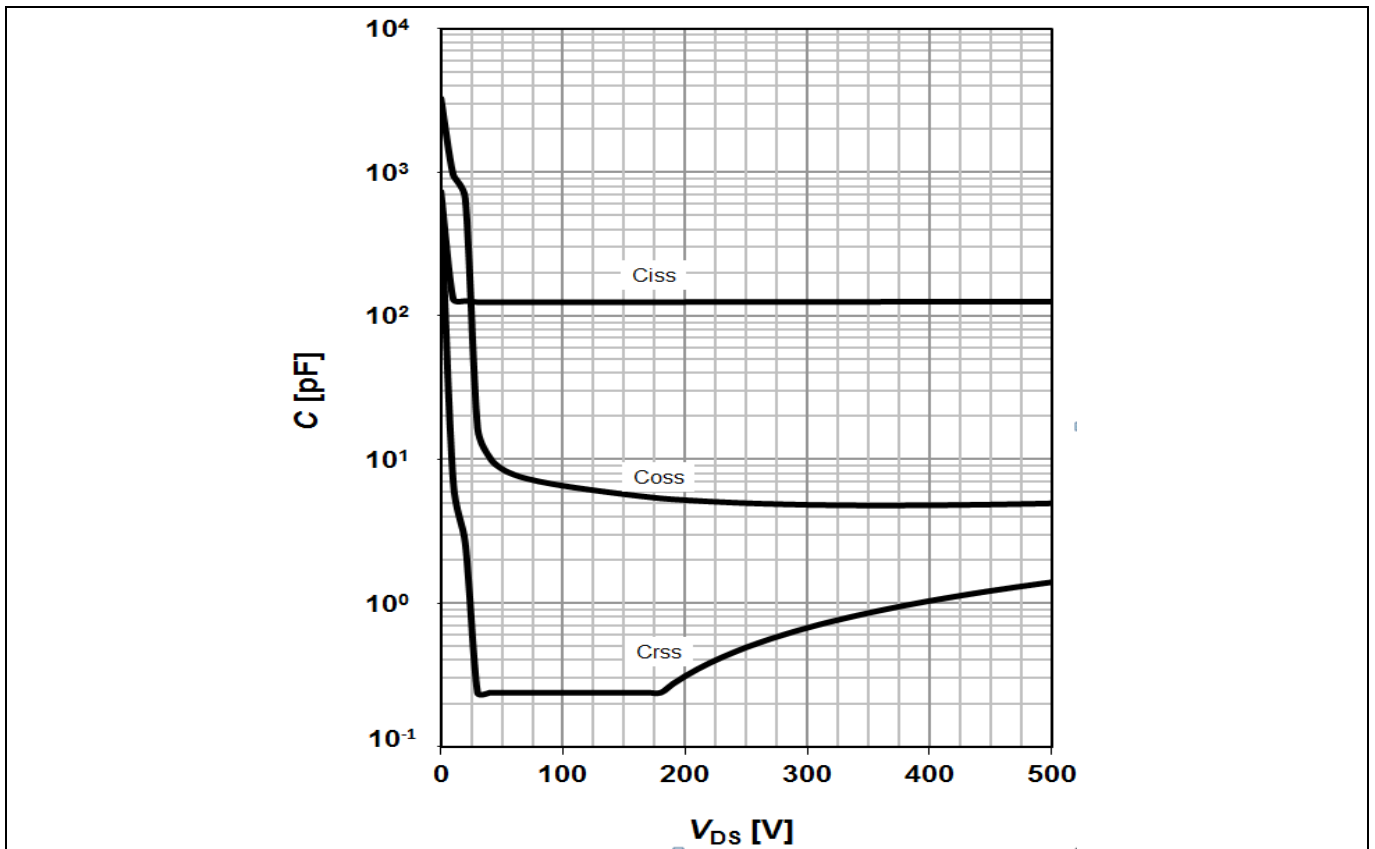


**Figure 37    Typical CoolMOS™ capacitances of ICE5QR2280AZ (C=f($V_{DS}$);$V_{GS}$=0 V; f=250 kHz)**

**CoolMOS™ Performance Characteristics**
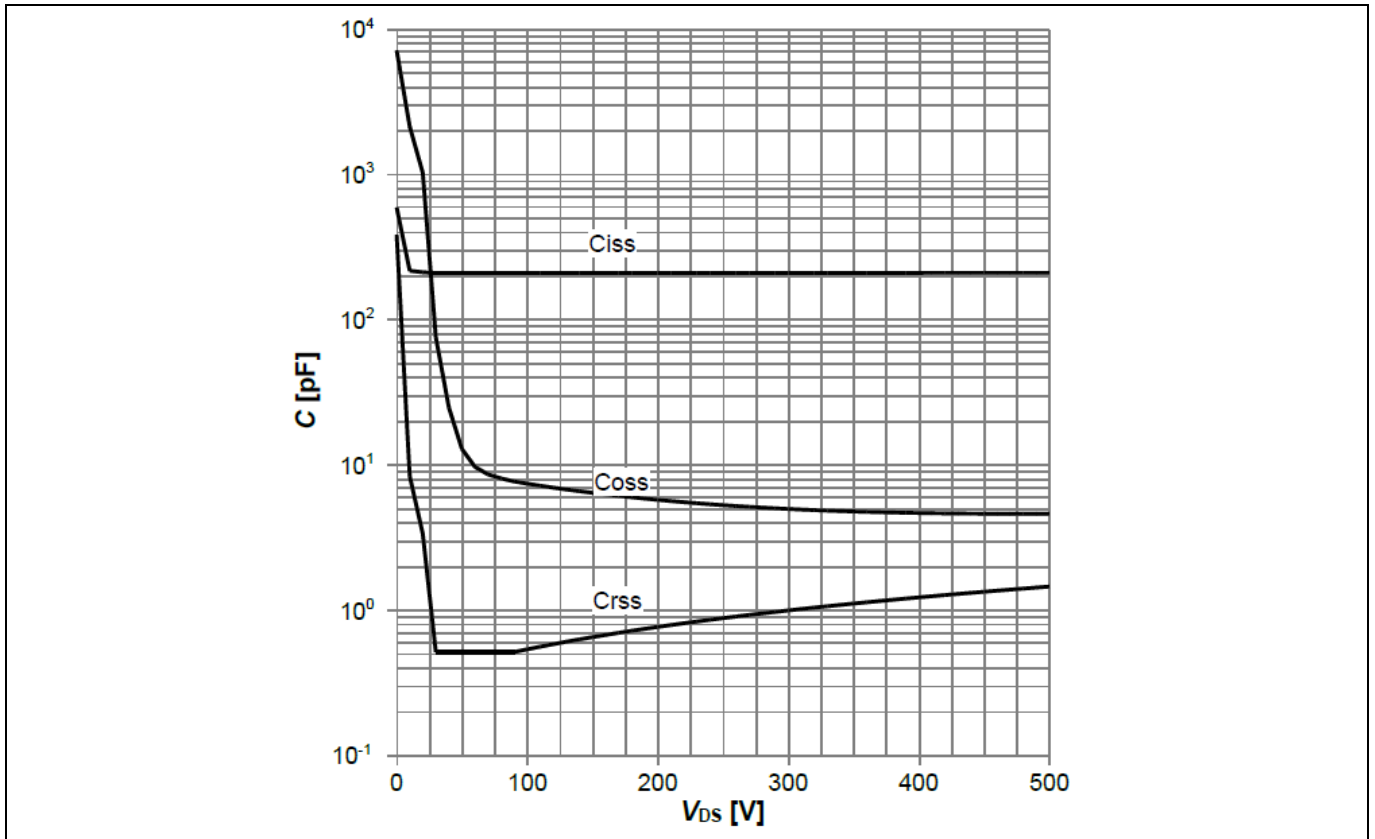


**Figure 38    Typical CoolMOS™ capacitances of ICE5QR1070AZ (C=f($V_{DS}$);$V_{GS}$=0 V; f=250 kHz)**
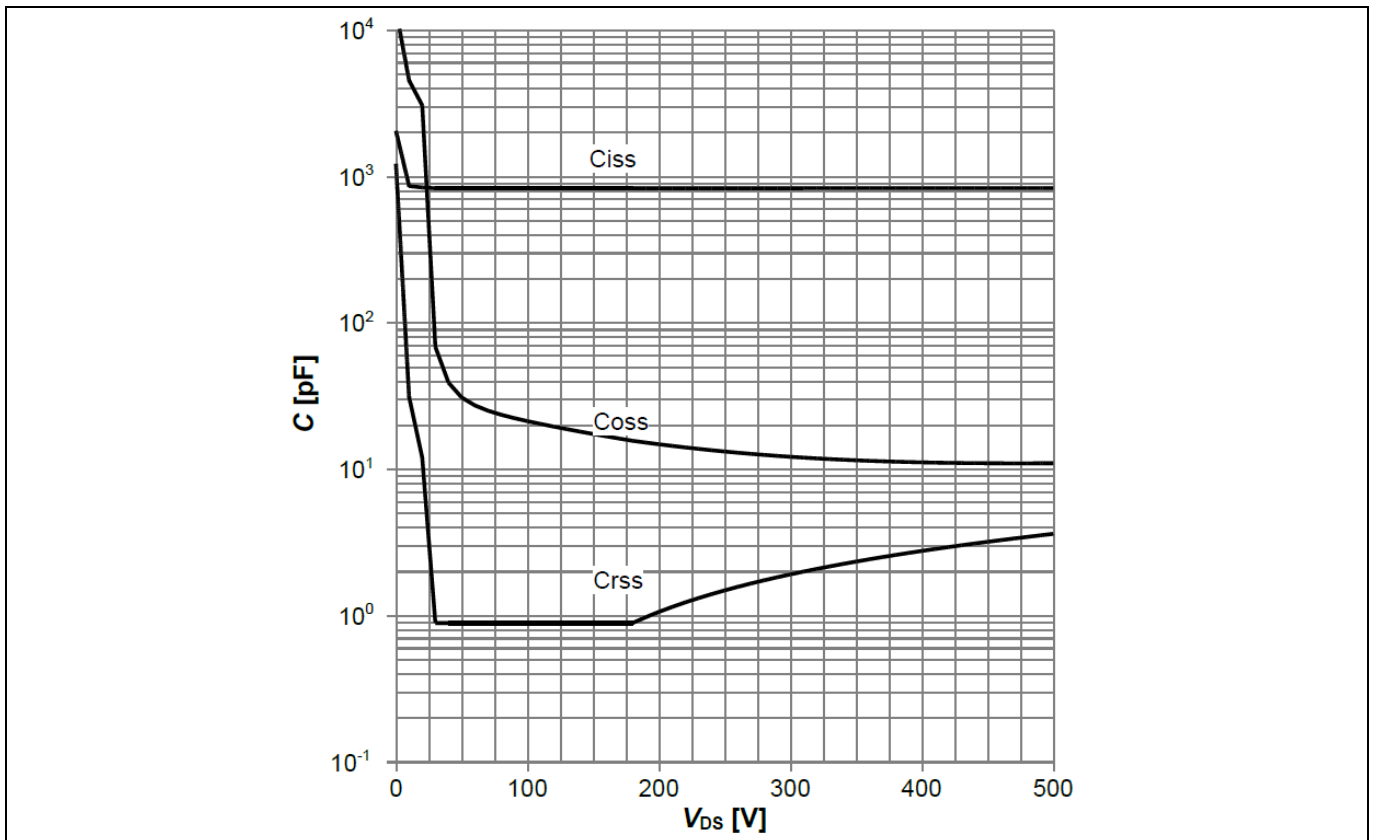


**Figure 39    Typical CoolMOS™ capacitances of ICE5QR0680Ax (C=f($V_{DS}$);$V_{GS}$=0 V; f=250 kHz)**

**CoolMOS™ Performance Characteristics**
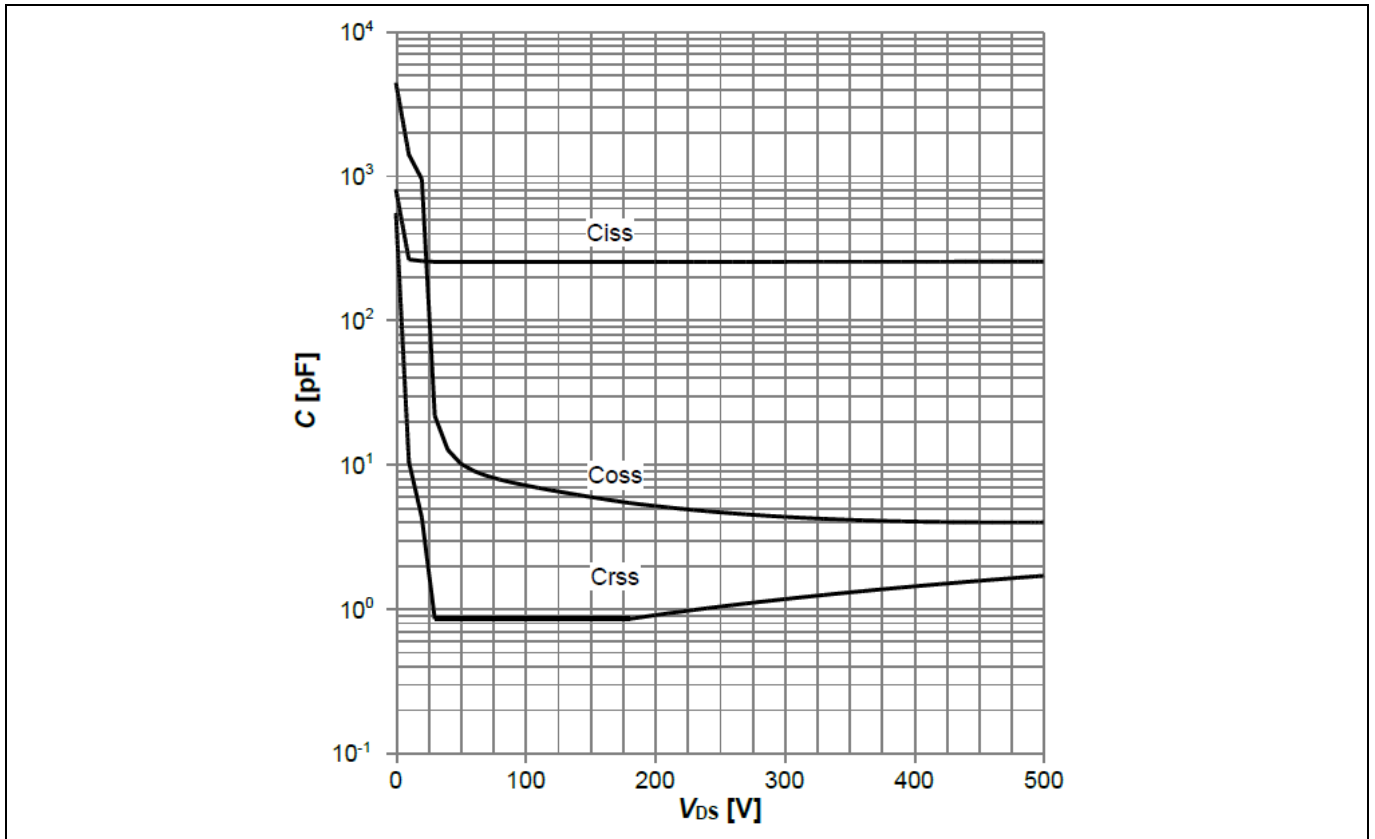


**Figure 40    Typical CoolMOS™ capacitances of ICE5QR1680AG(C=f($V_{DS}$);$V_{GS}$=0 V; f=250 kHz)**

# 6 Output Power Curve

The calculated output power curves giving the typical output power versus ambient temperature are shown below. The curves are derived based on a typical discontinuous mode flyback in an open frame design at $T_a$=50°C, $T_J$=125°C (integrated high voltage MOSFET), using minimum drain pin copper area in a 2 oz copper single sided PCB and steady state operation only (no design margins for abnormal operation modes are included). The output power figure is for selection purpose only. The actual power can vary depending on particular designs. In a power supply system, appropriate thermal design margins must be applied to make sure that the maximum ratings given in section 4.1are respected at all times.
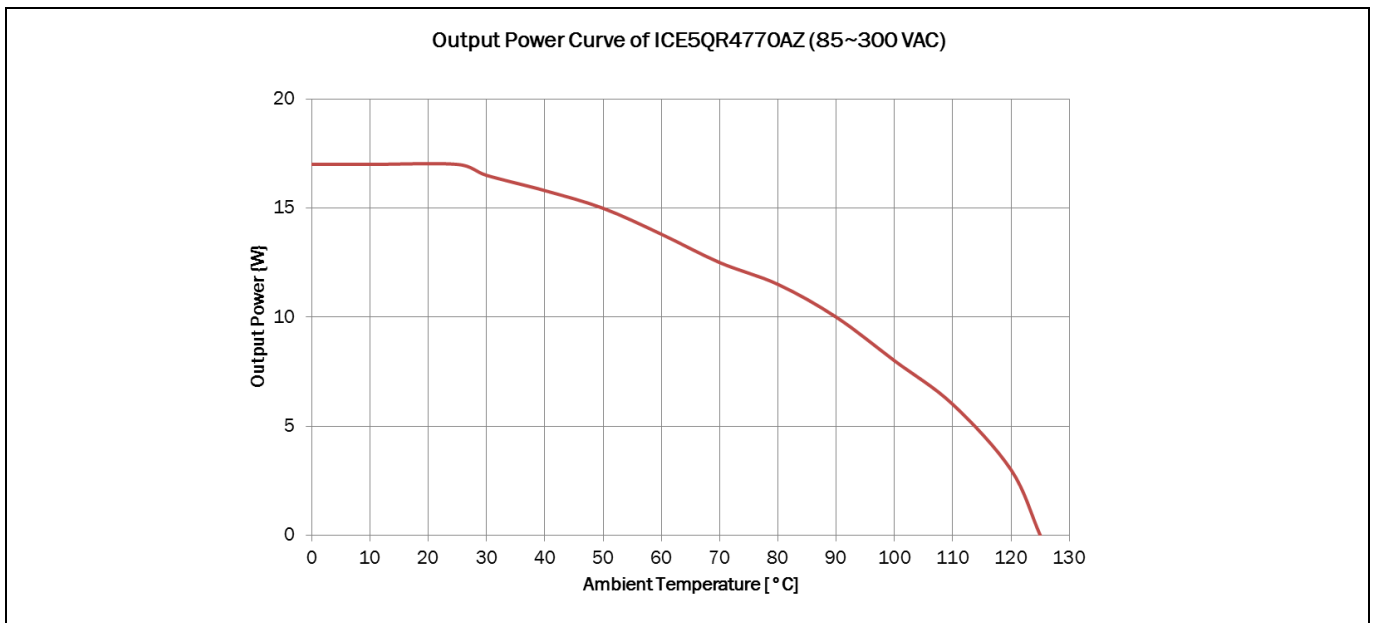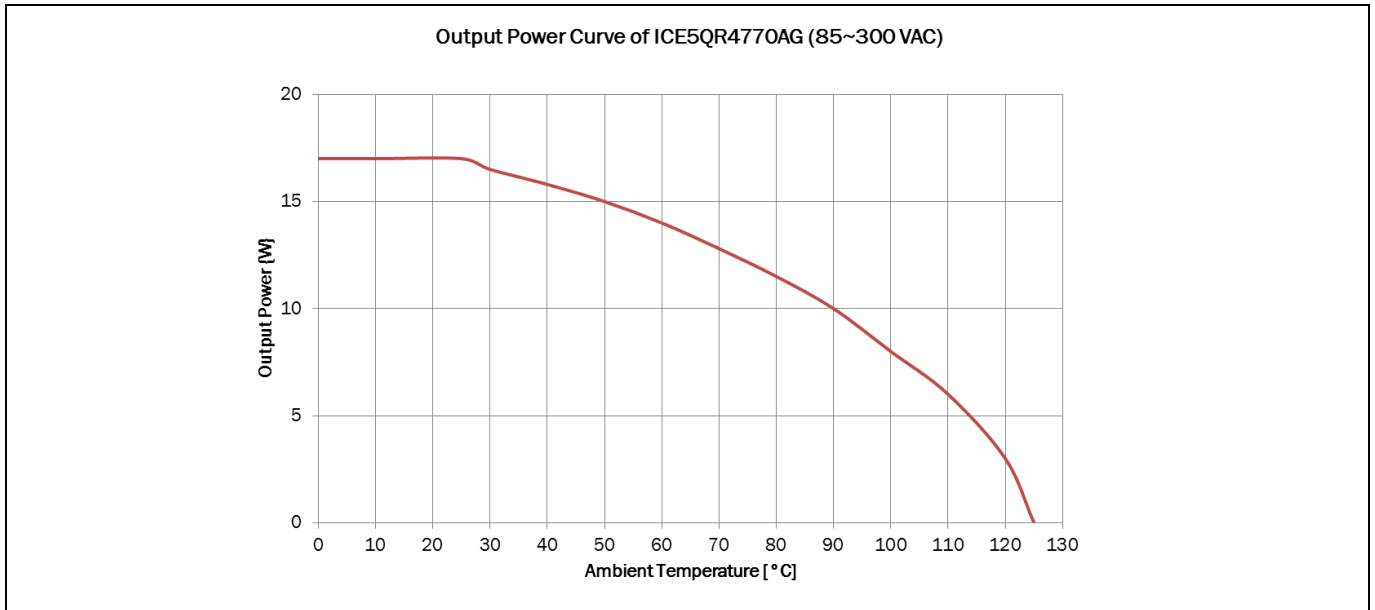


**Figure 41    Output power curve of ICE5QR4770AZ, $V_{IN}$=85~300 $V_{AC}$; $P_{Out}$=f($T_a$)**
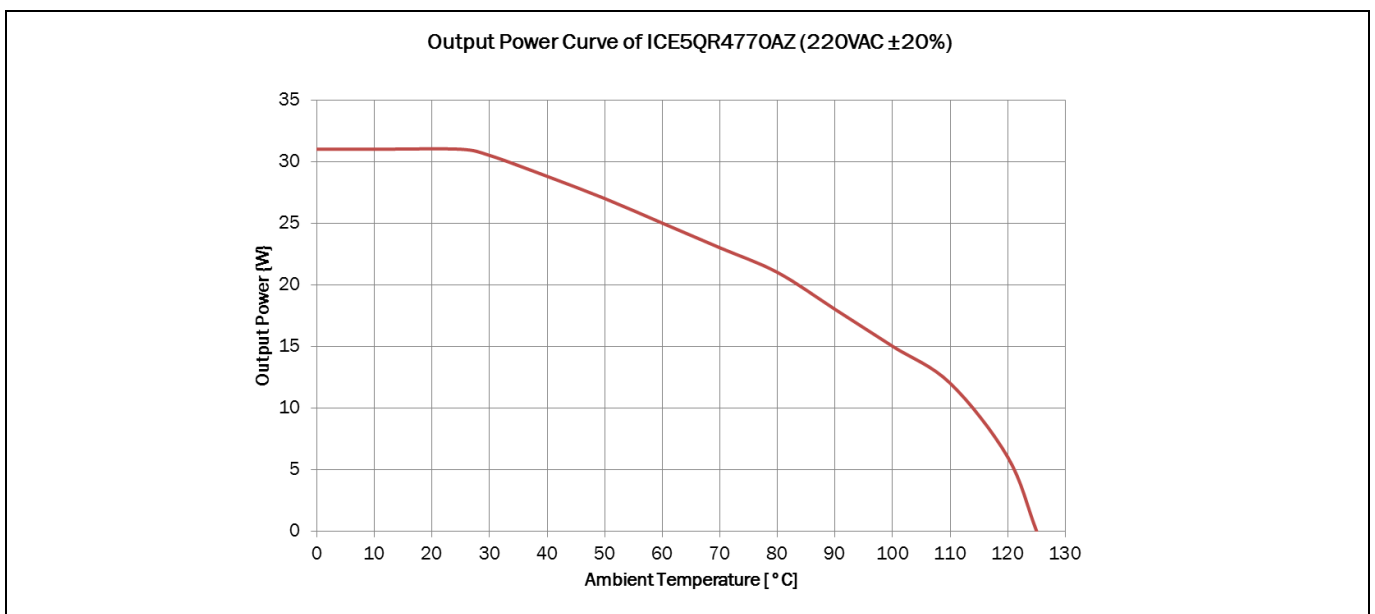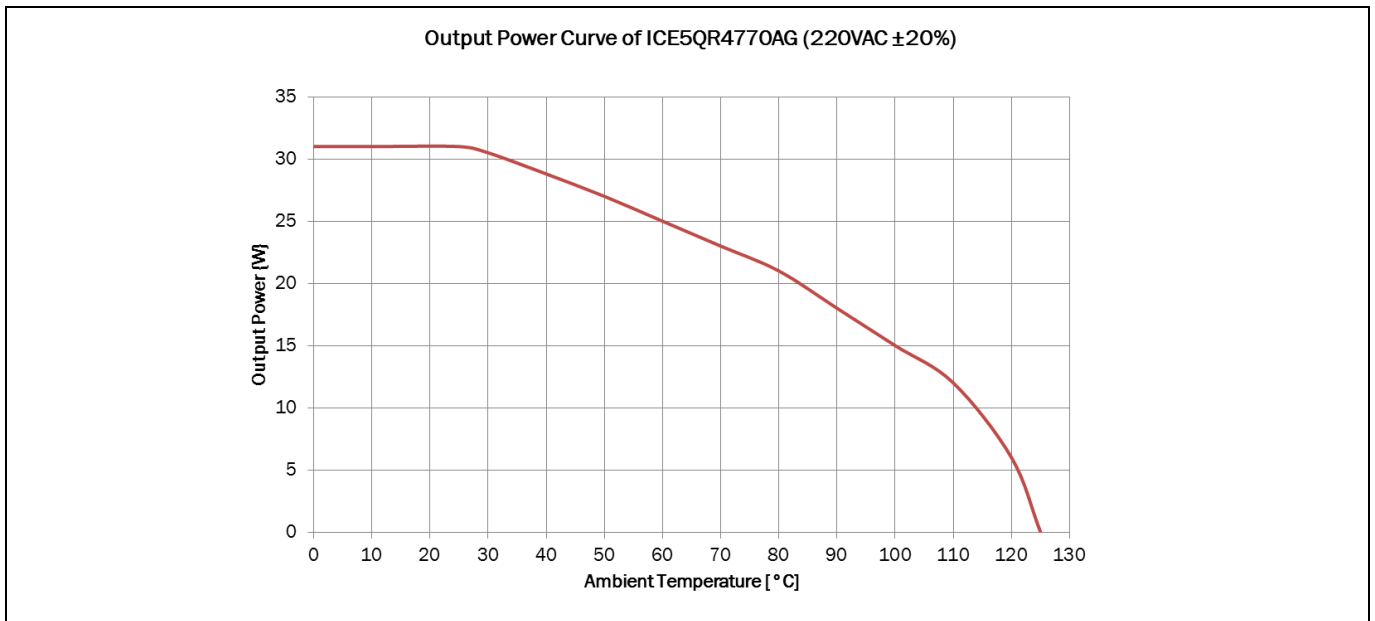


**Figure 42    Output power curve of ICE5QR4770AZ, $V_{IN}$=220 $V_{AC}$; $P_{Out}$=f($T_a$)**
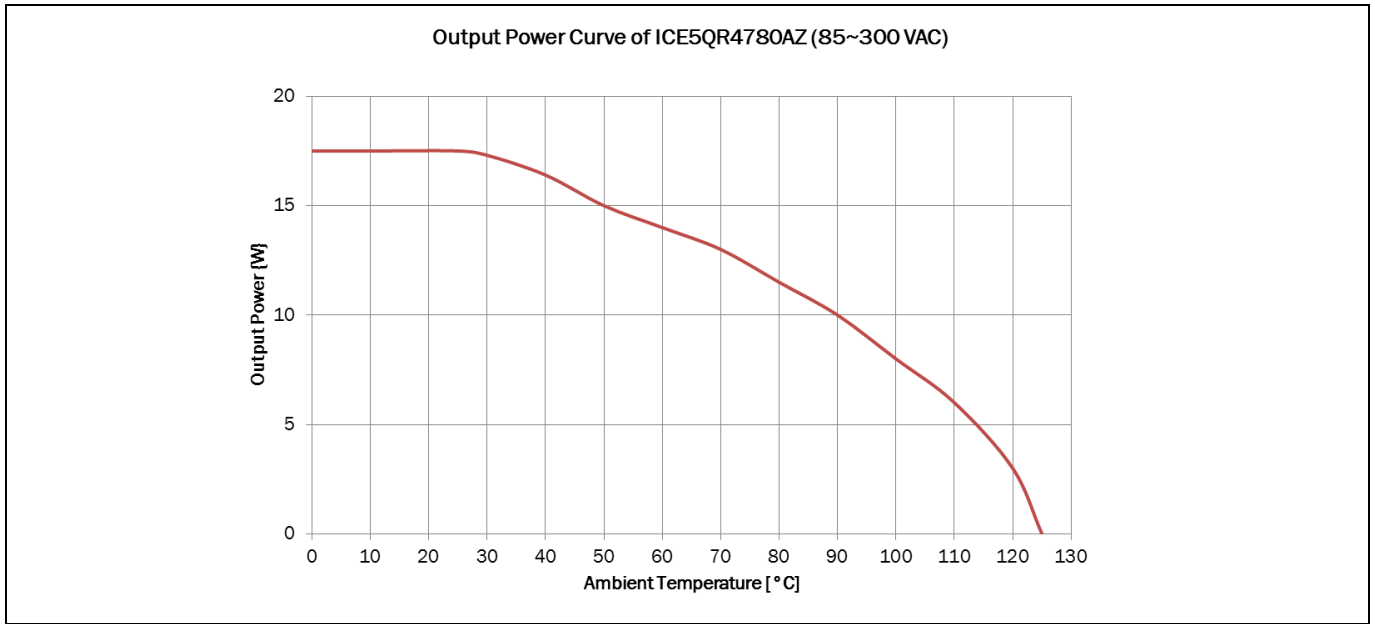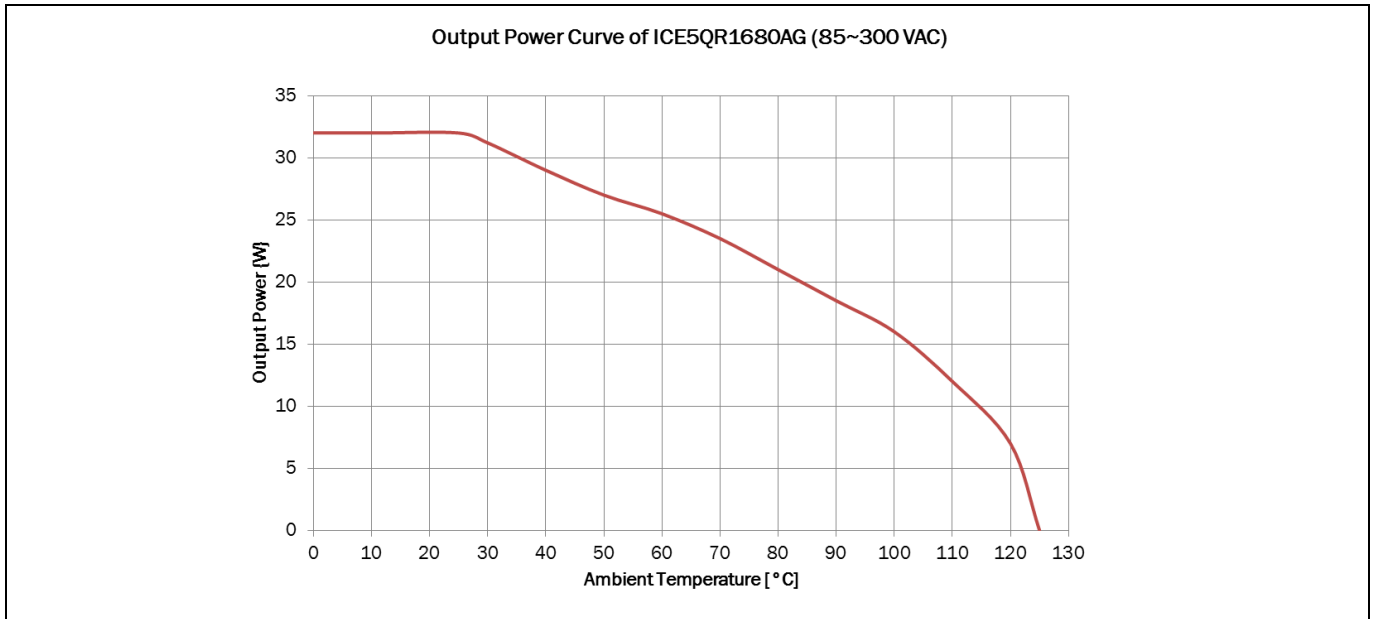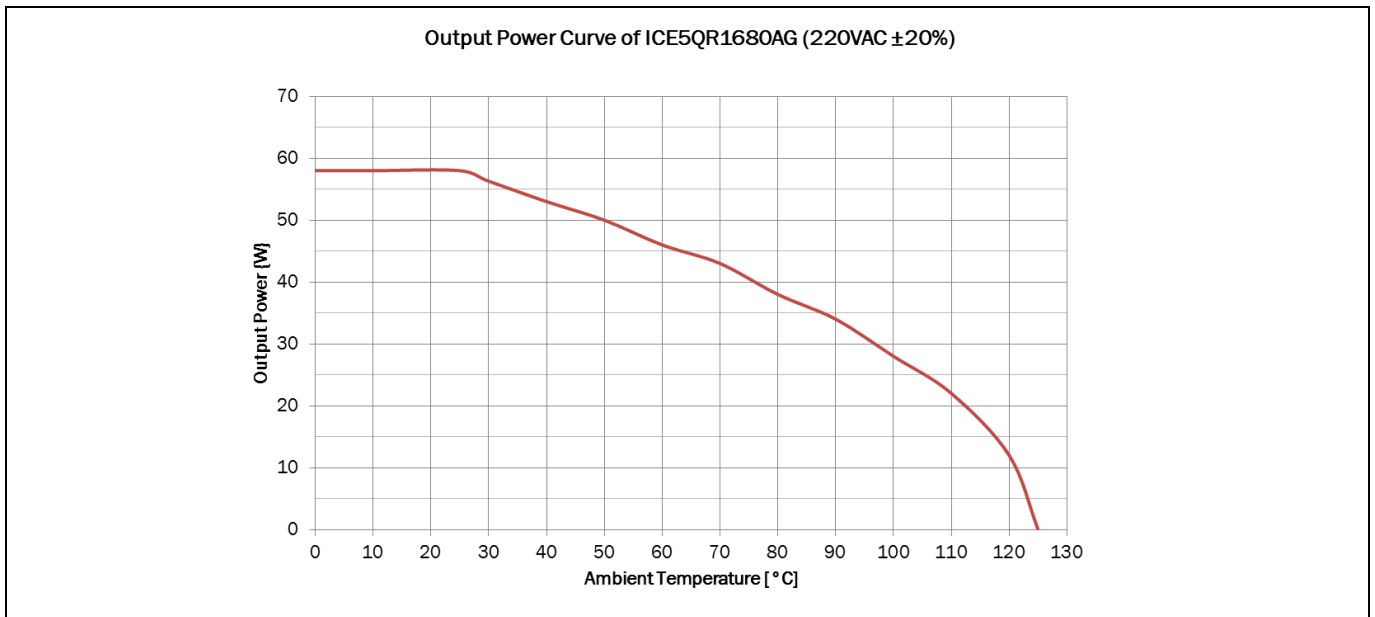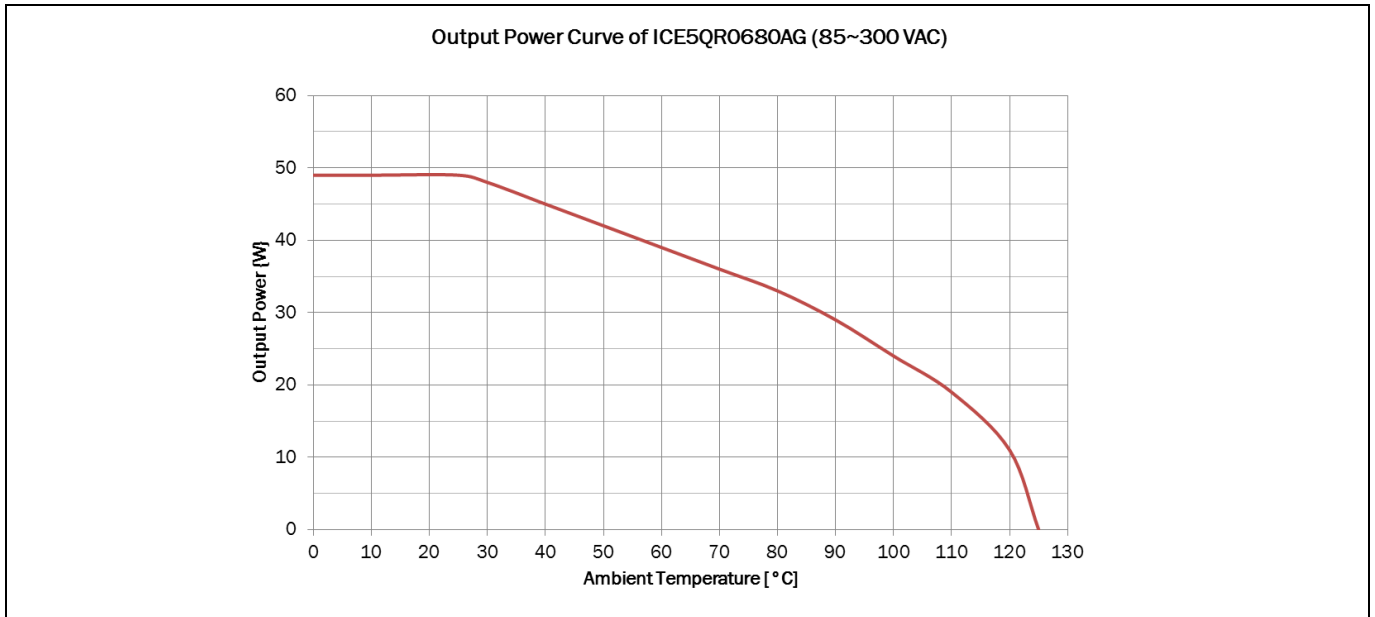
**Output Power Curve**



**Figure 43      Output power curve of ICE5QR4780AZ, $V_{IN}$=85~300 $V_{AC}$; $P_{Out}$=f($T_a$)**
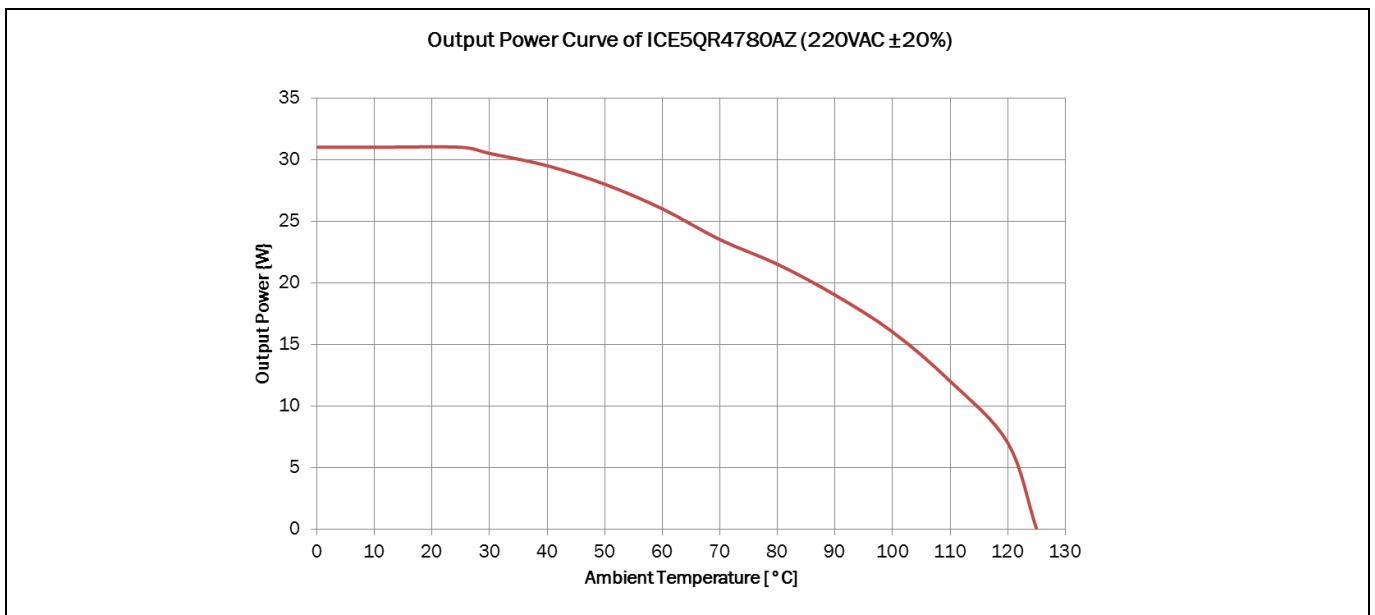


**Figure 44      Output power curve of ICE5QR4780AZ, $V_{IN}$=220 $V_{AC}$; $P_{Out}$=f($T_a$)**
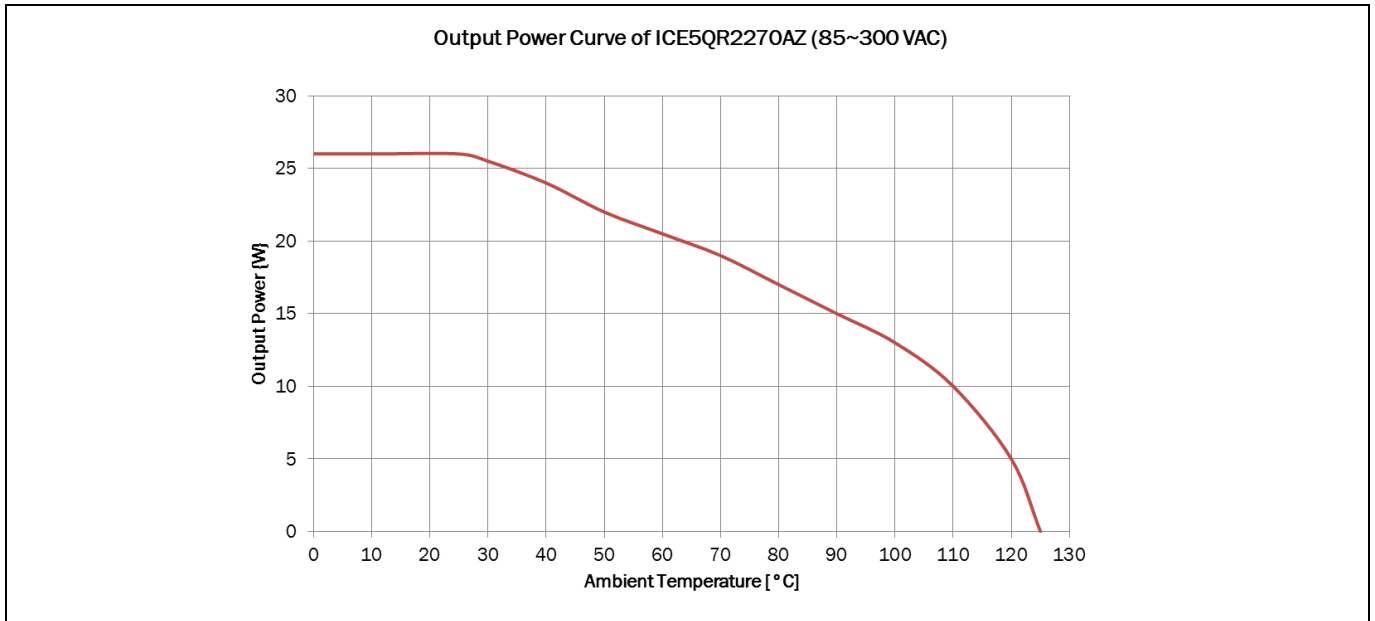
**Output Power Curve**



**Figure 45    Output power curve of ICE5QR2270AZ, $V_{IN}$=85~300 $V_{AC}$; $P_{Out}$=f($T_a$)**
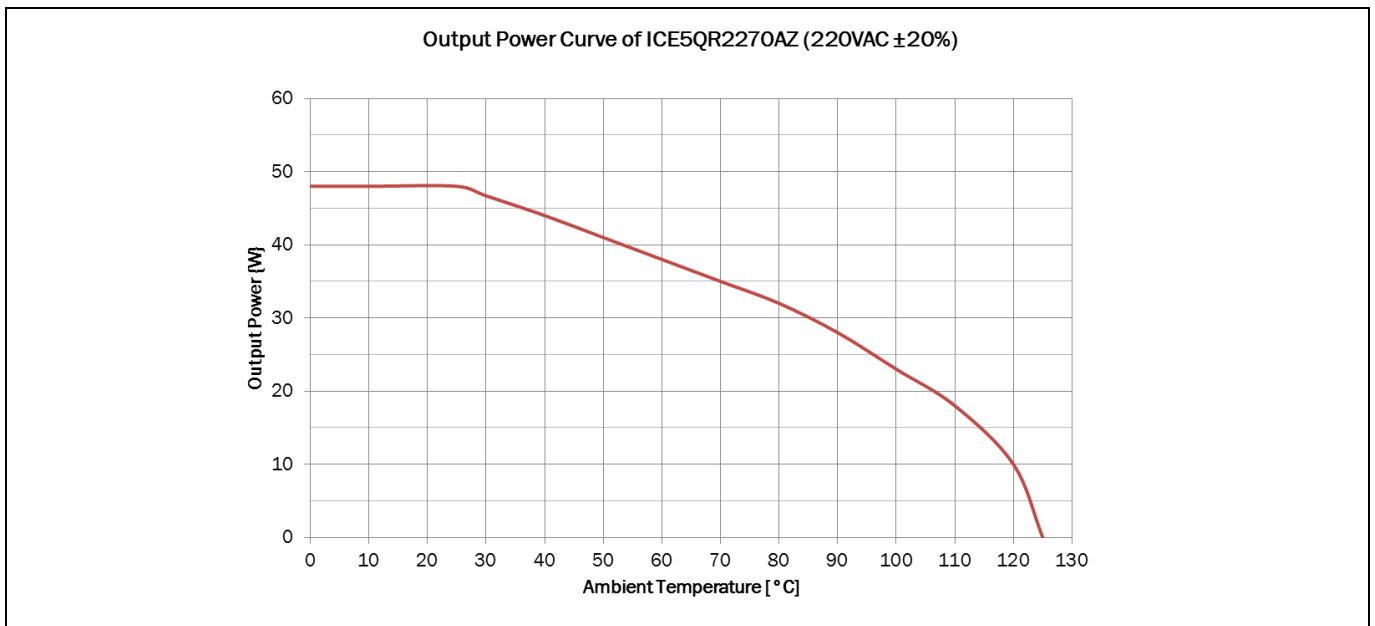


**Figure 46    Output power curve of ICE5QR2270AZ, $V_{IN}$=220 $V_{AC}$; $P_{Out}$=f($T_a$)**
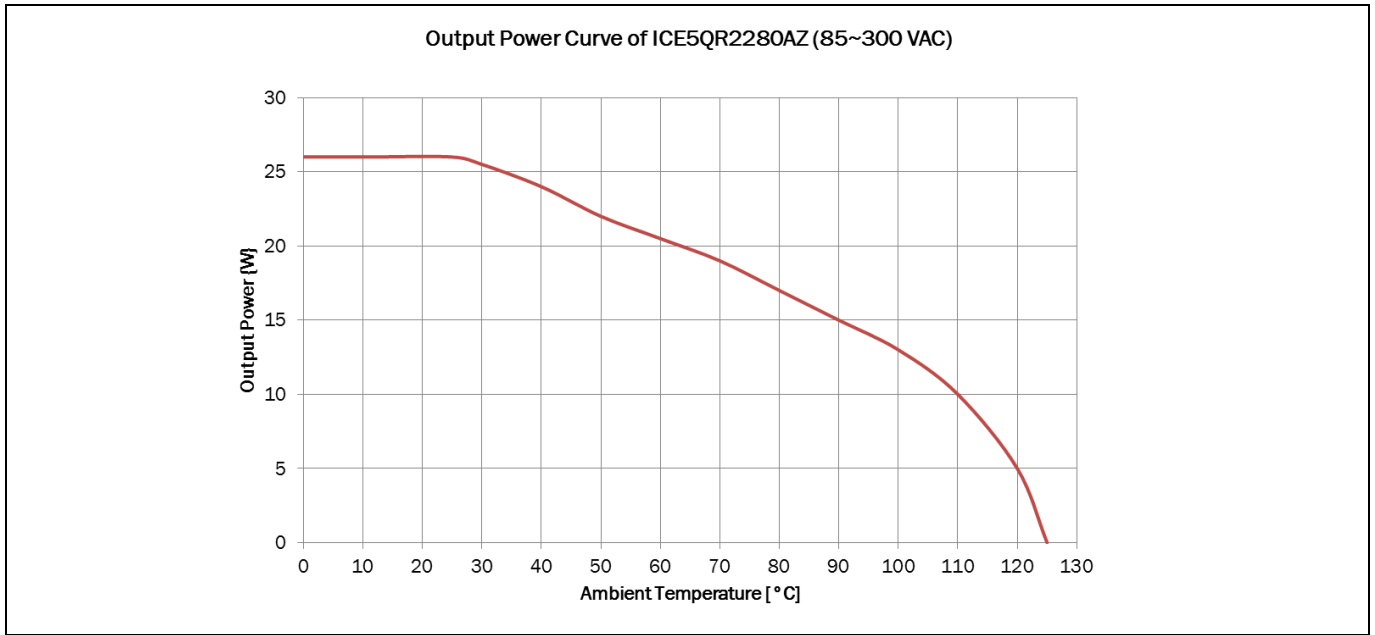
**Output Power Curve**



**Figure 47** Output power curve of ICE5QR2280AZ, $V_{IN}$=85~300 $V_{AC}$; $P_{Out}$=f($T_a$)
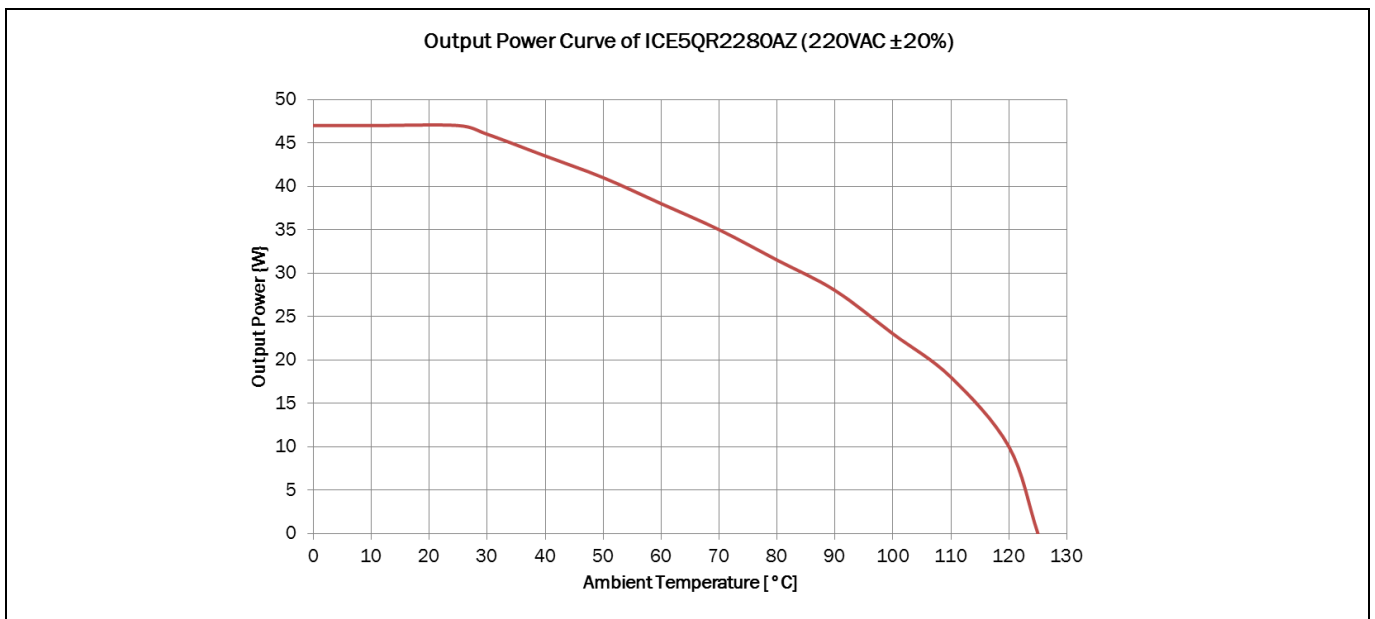


**Figure 48** Output power curve of ICE5QR2280AZ, $V_{IN}$=220 $V_{AC}$; $P_{Out}$=f($T_a$)
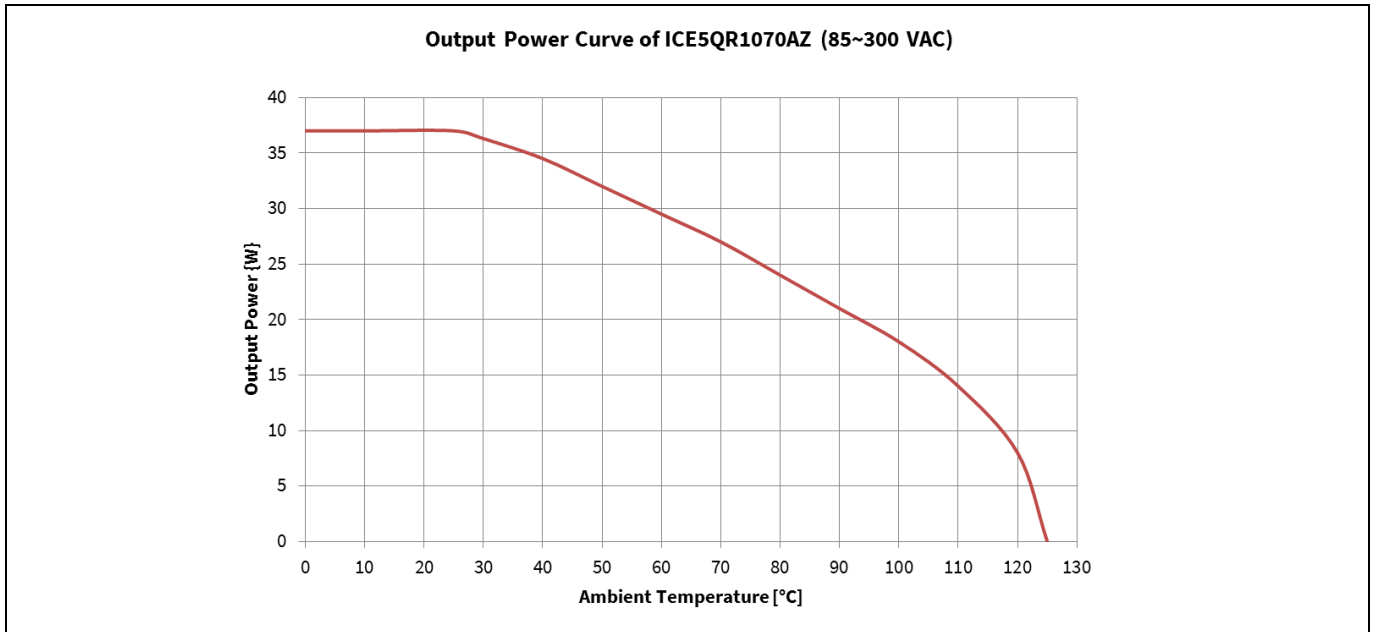
**Output Power Curve**



**Figure 49** Output power curve of ICE5QR1070AZ, $V_{IN}$=85~300 $V_{AC}$; $P_{Out}$=f($T_a$)
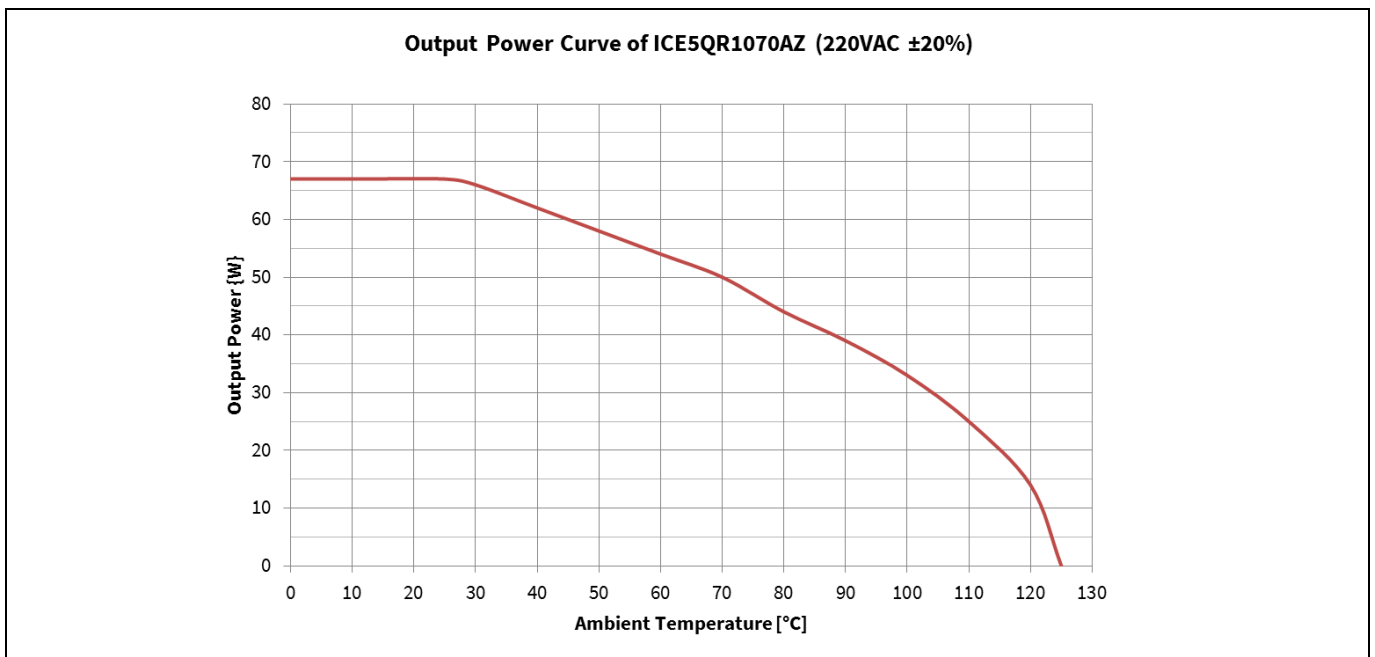


**Figure 50** Output power curve of ICE5QR1070AZ, $V_{IN}$=220 $V_{AC}$; $P_{Out}$=f($T_a$)
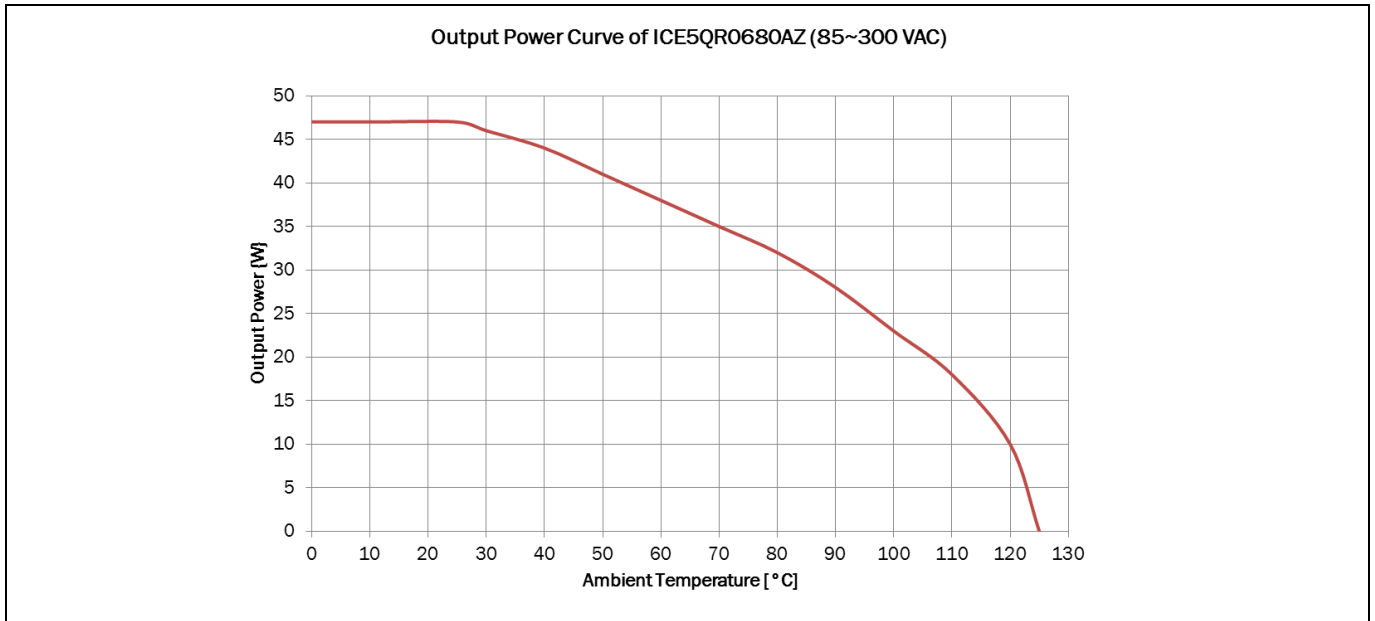
**Output Power Curve**



**Figure 51    Output power curve of ICE5QR0680AZ, $V_{IN}$=85~300 $V_{AC}$; $P_{Out}$=f($T_a$)**
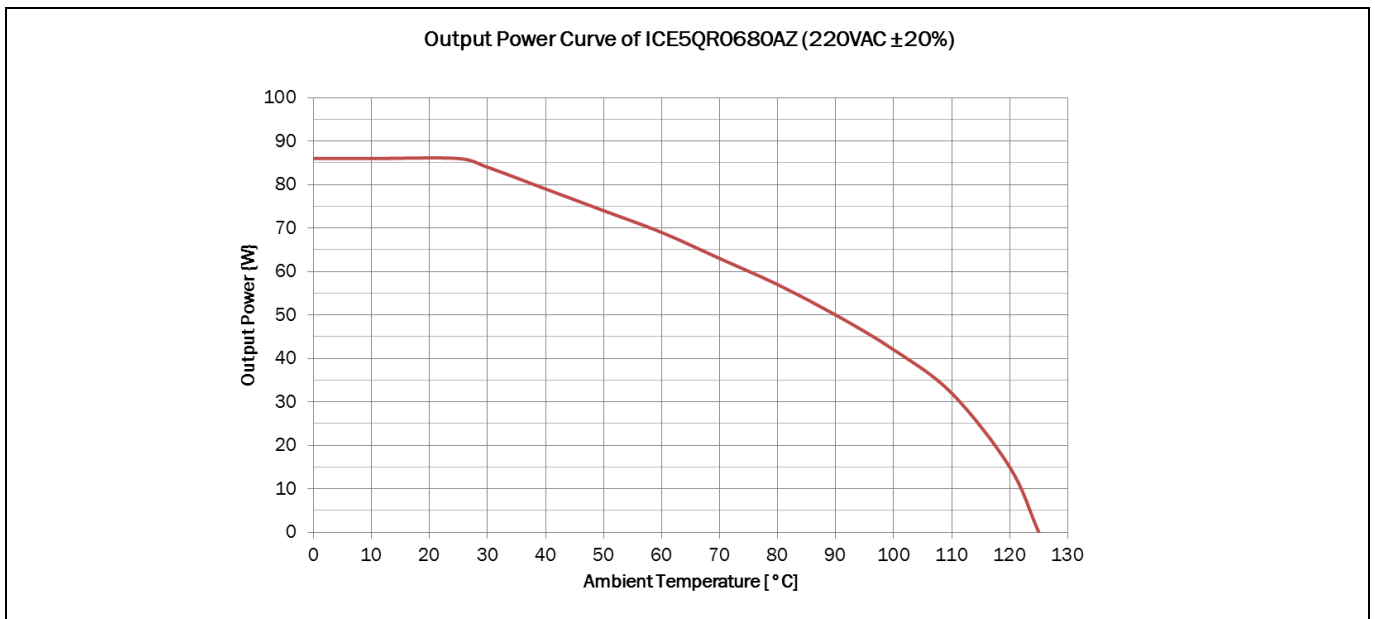


**Figure 52    Output power curve of ICE5QR0680AZ, $V_{IN}$=220 $V_{AC}$; $P_{Out}$=f($T_a$)**

**Output Power Curve**



**Figure 53**    Output power curve of ICE5QR4770AG, $V_{IN}$=85~300 $V_{AC}$; $P_{Out}$=f($T_a$)



**Figure 54**    Output power curve of ICE5QR4770AG, $V_{IN}$=220 $V_{AC}$; $P_{Out}$=f($T_a$)

**Output Power Curve**



**Figure 55** Output power curve of ICE5QR1680AG, $V_{IN}$=85~300 $V_{AC}$; $P_{Out}$=f($T_a$)



**Figure 56** Output power curve of ICE5QR1680AG, $V_{IN}$=220 $V_{AC}$; $P_{Out}$=f($T_a$)

**Output Power Curve**



**Figure 57** Output power curve of ICE5QR0680AG, $V_{IN}$=85~300 $V_{AC}$; $P_{Out}$=f($T_a$)
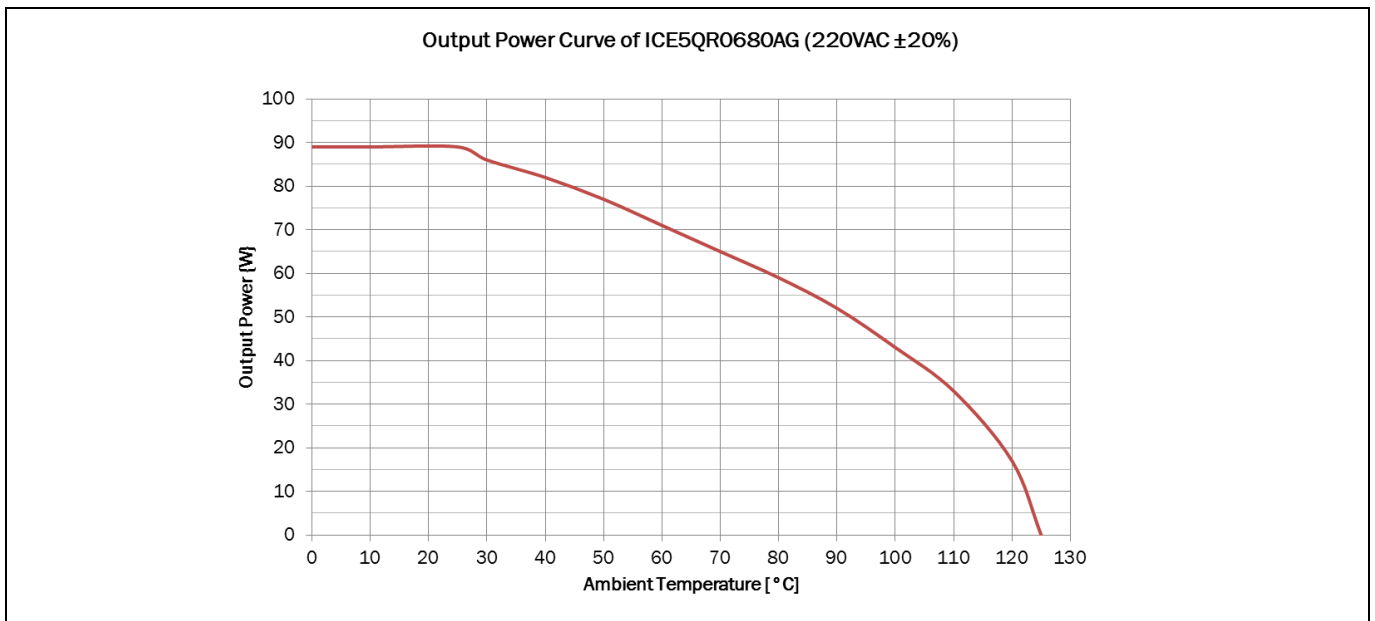


**Figure 58** Output power curve of ICE5QR0680AG, $V_{IN}$=220 $V_{AC}$; $P_{Out}$=f($T_a$)

# 7  Outline Dimension



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

| DIM | MILLIMETERS | | INCHES | |
|-----|------|------|------|------|
|     | MIN | MAX | MIN | MAX |
| A   | -    | 4.57 | -    | 0.180 |
| A1  | 0.38 | -    | 0.015 | -    |
| b   | 0.36 | 0.56 | 0.014 | 0.022 |
| b2  | -    | 1.70 | -    | 0.067 |
| c   | 0.20 | 0.36 | 0.008 | 0.014 |
| D   | 9.10 | 9.77 | 0.358 | 0.385 |
| E   | 7.49 | 8.26 | 0.295 | 0.325 |
| E1  | 6.10 | 6.60 | 0.240 | 0.260 |
| e   | 2.54 BSC | | 0.1 BSC | |
| N   | 7 | | 7 | |
| eB  | 7.90 | 10.90 | 0.311 | 0.429 |
| L   | 2.92 | -    | 0.115 | -    |

DOCUMENT NO.
Z8B00155542

SCALE

EUROPEAN PROJECTION

ISSUE DATE
22.07.2011

REVISION
02
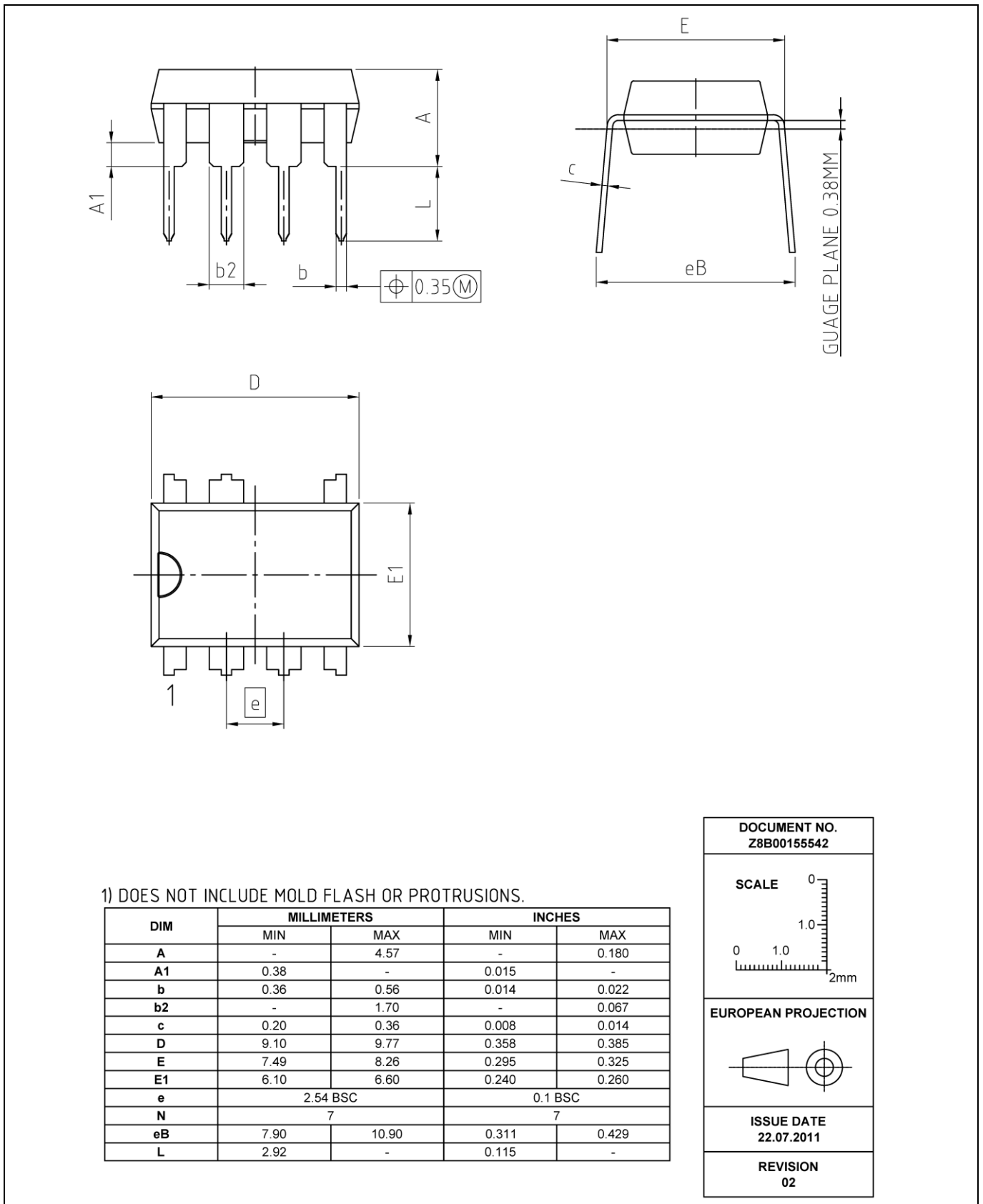
**Figure 59  PG-DIP-7**

**Outline Dimension**
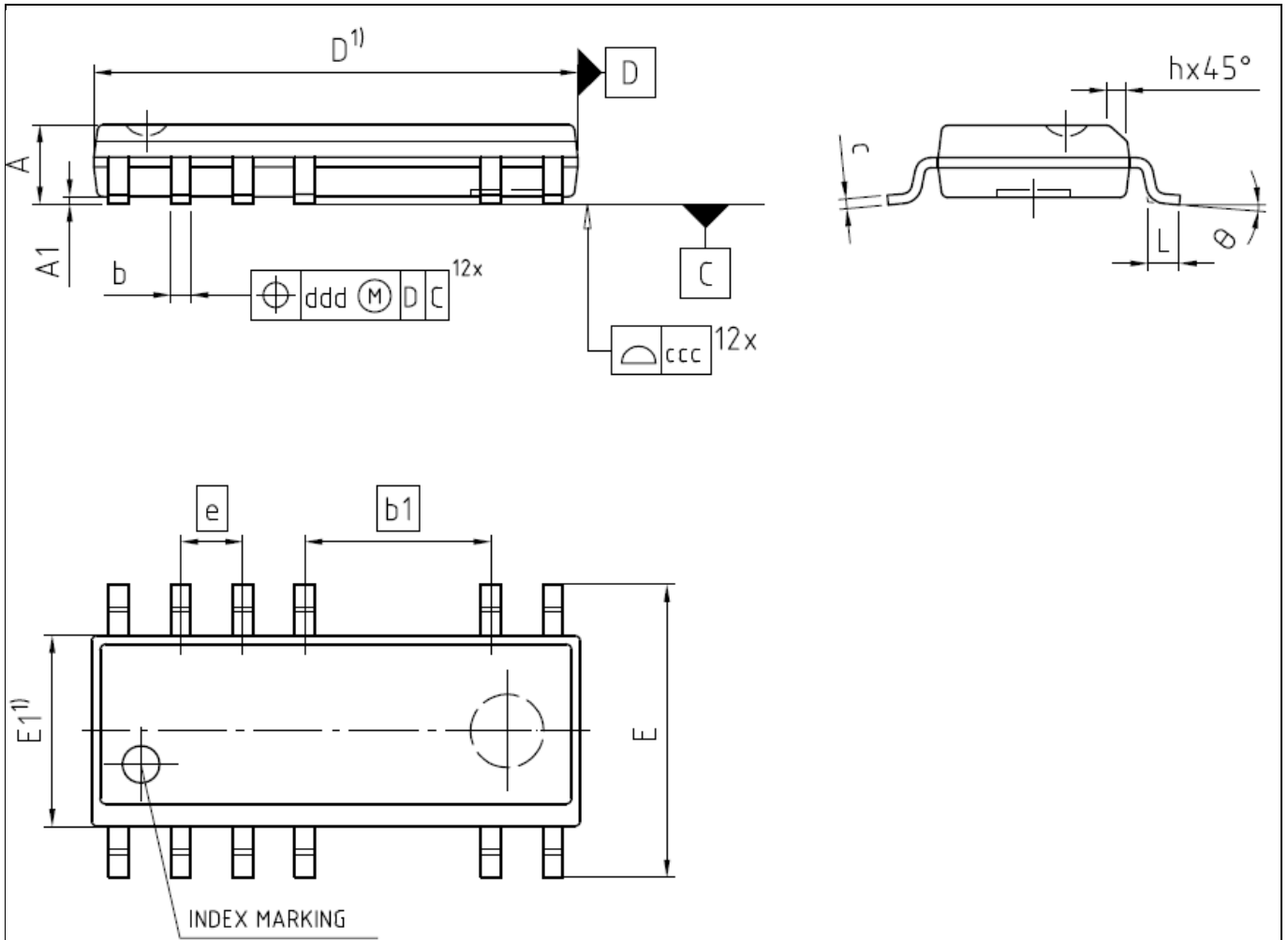


1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | - | 1.75 | - | 0.069 |
| A1 | 0.10 | - | 0.004 | - |
| b | 0.35 | 0.51 | 0.014 | 0.020 |
| b1 | 3.81 (BSC) | | 0.150 (BSC) | |
| c | 0.19 | 0.25 | 0.007 | 0.010 |
| D | 9.80 | 10.00 | 0.386 | 0.394 |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 (BSC) | | 0.050 (BSC) | |
| N | 12 | | 12 | |
| L | 0.39 | 0.89 | 0.015 | 0.035 |
| h | 0.23 | 0.50 | 0.009 | 0.020 |
| Θ | - | 8° | - | 8° |
| ccc | 0.10 | | 0.004 | |
| ddd | 0.20 | | 0.008 | |

DOCUMENT NO.
Z8B00168485

SCALE

EUROPEAN PROJECTION

ISSUE DATE
03.04.2014

REVISION
02

**Figure 60    PG-DSO-12**
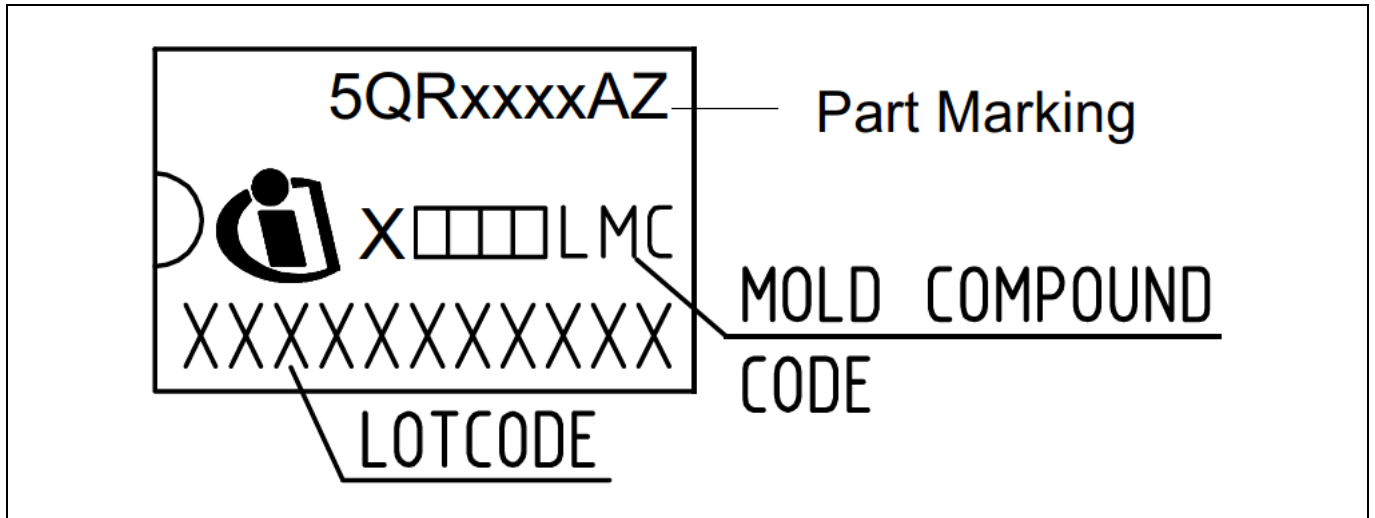
# 8 Marking



**Figure 61    Marking of DIP-7**
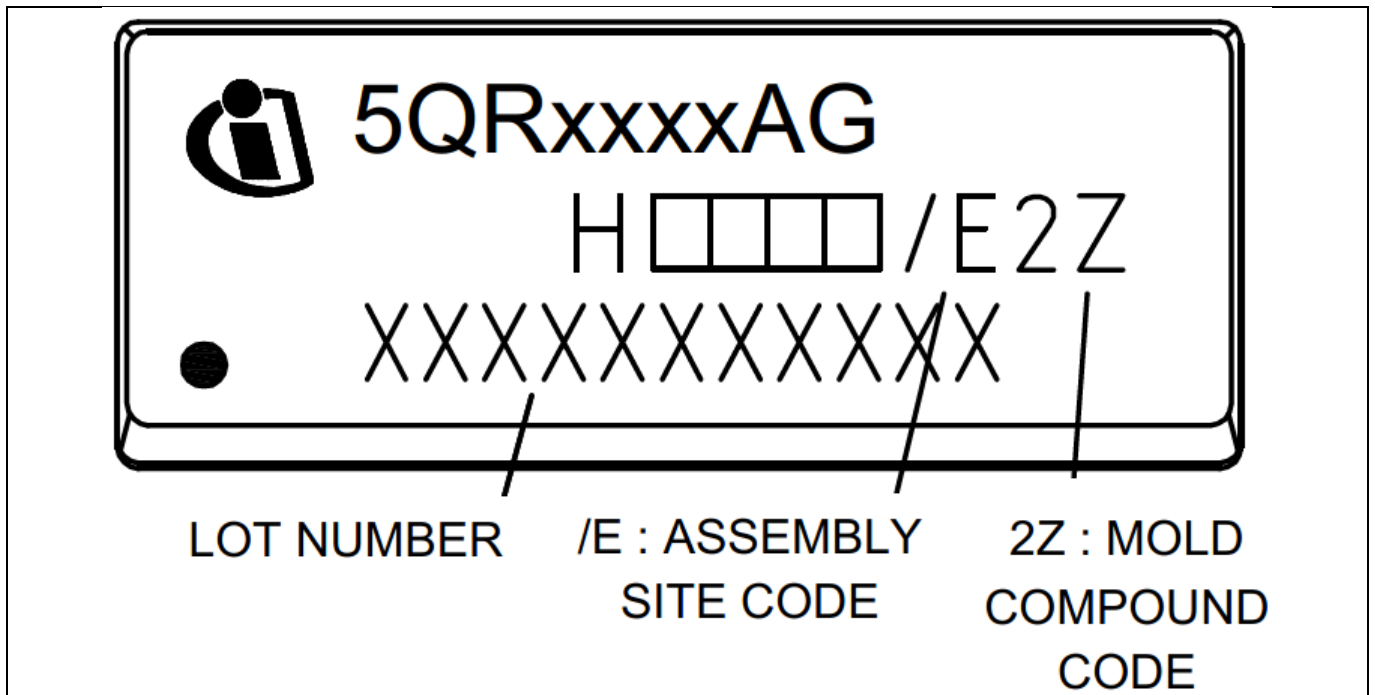


**Figure 62    Marking of DSO-12**

## Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| V2.1 | 11 Aug 2017 | Page 8 ~14<br>    Text content revised<br>Page 17, 18 and 19 (reference to errata sheet 10160AERRA)<br>    Table 6, the limit values for $V_{DS}$ shall be at the maximum column<br>    Table 8, the polarity for maximum limit on $I_{VCC\_Charge1}$ shall be negative<br>    Additional text content revised |
| V2.0 | 4 Jul 2017 | Page 2, 17, 18, 24~44<br>    Addition of ICE5QR1070AZ<br>Page 35<br>    Update of 700V CoolSET™ Drain-source breakdown voltage as shown in Figure 32 reference to errata sheet #10157AERRA |
| | | |

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