ICL7600/ICL7601
High Reliability Commutating Auto-Zero (CAZ) Operational Amplifier

GENERAL DESCRIPTION

The ICL7600/ICL7601 commutating auto-zero (CAZ) operational amplifiers are designed to replace almost any of today's hybrid or monolithic ultra-low offset op amps, and will provide almost three orders of magnitude reduction in input offset voltage compared with conventional device designs. This is achieved through Intersil's CAZ amp principle, an entirely new approach to low-frequency operational amplifier design.

The key feature of the CAZ principle is automatic compensation for long-term drift phenomena and temperature effects. Two internal op amps are connected so that when one amplifier is processing an input signal the other is maintained in an "auto-zero" mode. The ICL7600/ICL7601 contains all of the circuitry required for system operation, including an oscillator, a counter, level translators, analog switches and operational amplifiers. Only two auto-zero capacitors are needed for complete operational amplifier function. Control of the oscillator and counter section is provided through the OSC and DR (division ratio) terminals. Internal biasing of the two on-chip op amps is programmable through a three-voltage-level terminal designated BIAS.

The ICL7600 is internally-compensated and is intended for applications which require voltage gains from unity through 20. The uncompensated ICL7601 is intended for those situations which require voltage gains of greater than 20. Major advantage of the ICL7601 over the ICL7600 at high gain settings is the reduction in commutation noise and subsequent greater accuracy.

Minimum periodic adjustments and extremely low offset voltage and temperature coefficients make the CAZ operational amplifiers very desirable for operation in adverse environments (temperature, humidity, toxic or radioactive) where equipment service is difficult. Since the device will auto-zero its internal offset errors, no adjustment is required other than that of gain, which is established by the external resistors.

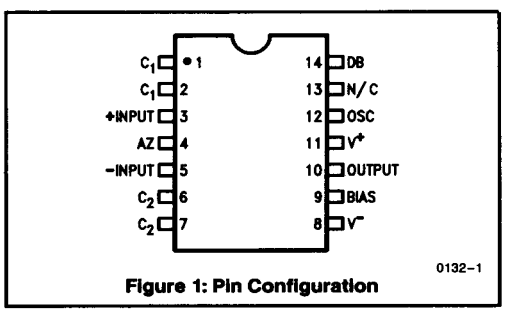

Figure 1: Pin Configuration

FEATURES

- **Exceptionally low input offset voltage—5 μV**
- **Low long-term input offset voltage drift—0.2 μV/year**
- **Low input offset voltage temperature drift—0.005 μV/°C**
- **Low DC input bias current—300 pA**
- **Low DC input offset bias current—150 pA**
- **Wide common mode and differential input voltage ranges**
- **Excellent low supply voltage operation—Down to ±2V**
- **Static-protected inputs—no special handling required**
- **Fabricated using proprietary MAXCMOS™ technology**
- **Compensated (ICL7600) or uncompensated (ICL7601) versions**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7600MJD	−55°C to +125°C	14 Lead CERDIP
ICL7601MJD	−55°C to +125°C	14 Lead CERDIP

ICL7600/ICL7601

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (sum of both positive and negative supply voltages, V^+ and V^-) .....18 Volts

DR Input Voltage .....(V^+ +0.3) to (V^+ −8) Volts

Input Voltage (C_1, C_2, +INPUT, −INPUT, BIAS, OSC (Note 1).....(V^+ +0.3) to (V^- −0.3) Volts

Differential Input Voltage (Note 1) ±(V^+ +0.3) to (V^- −0.3)

Duration of Output Short Circuit (Note 2).....Unlimited

Continuous Total Power Dissipation at or below +25°C free air temperature (Note 3)
CERDIP Package.....500 mW

Operating Temperature Range
ICL760XM.....−55°C to +125°C

Storage Temperature Range.....−55°C to +150°C

Lead Temperature (soldering, 60 seconds) .....+300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1: An SCR structure is inherent in the CMOS process used in the fabrication of these devices. If voltages in excess of (V^+ +0.3) to (V^- −0.3) volts are connected to either inputs or outputs, destructive latchup can occur. For this reason it is recommended that no inputs from sources not on the same power supply or supplies be applied before the ICL7600/ICL7601 supplies are established, and that if multiple supplies are used the ICL7600/ICL7601 supplies be activated first. No restrictions are placed on the differential input voltages on either the inverting or non-inverting inputs, so long as these voltages do not exceed the power supply voltages by more than 0.3V.

2: Outputs may be shorted to ground (GND) or to either supply (V^+, V^-). Temperature and/or supply voltages must be limited to insure that the dissipation rating is not exceeded.

3: For operation above 25°C free-air temperature, derate 4mW/°C from 500mW for CERDIP and 3mW/°C from 375mW for plastic.

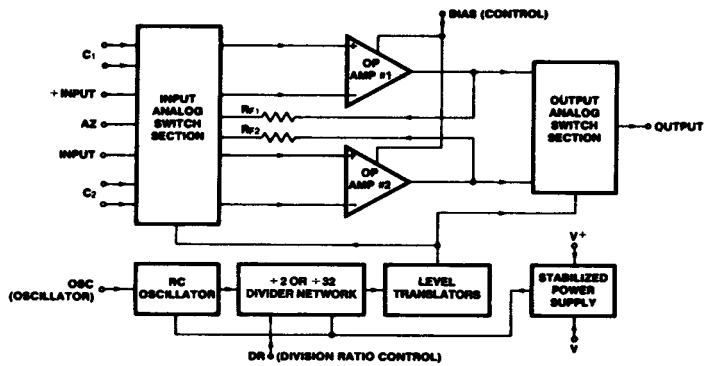

Figure 2: Functional Diagram

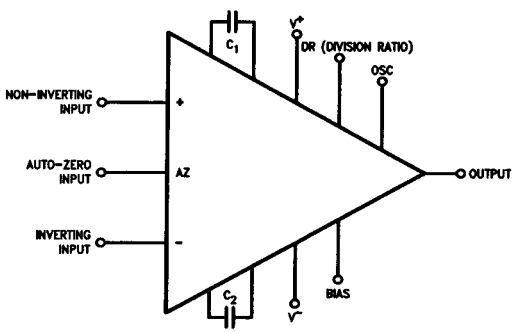

Figure 3: Symbol

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$), $C_1 = C_2 = 1\mu F$, Test Circuit 1, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$R_S \leq 1k\Omega$ $C_1 = C_2 = 1\mu F$ MIL version over temp.	Low Bias Setting Med Bias Setting High Bias Setting Med Bias Setting		±2 ±5 ±7	 ±10 ±40	μV μV μV μV
V_{OS} Time	Long Term Input Offset Voltage Stability	Low or Med Bias Settings			0.2		μV/year
TCV_{OS}	Average Input Offset Voltage Temperature Coefficient (Note 1)	Low or Med Bias Settings	$-55°C > T_A > +25°C$ $+25°C > T_A > +125°C$		0.005 0.05	0.2 0.2	μV/°C μV/°C
e_n	Noise Voltage (RMS)	Band Width 0.1 to 10Hz $R_S \leq 1k\Omega$	Low Bias Med Bias High Bias		0.8 0.8 1.0		μV μV μV
e_{np-p}	Equivalent Input Noise Voltage Peak-to-peak	Band Width 0.1 to 10Hz $R_S \leq 1k\Omega$	Low Bias Med Bias High Bias		4.0 4.0 5.0		μV μV μV
e_{n10}	Spot equivalent Noise voltage	f = 10Hz Band Width 1Hz				700	nV/√Hz
i_{n10}	Spot equivalent Noise Current	f = 10Hz Band Width 1Hz				0.1	pA/√Hz
DIF V_{IN}	Differential Input Voltage Range			$V^- -0.3$	to	$V^+ +0.3$	V
CMVR	Common Mode Input Range	Low Bias Med Bias High Bias		−4.2 −4.0 −3.5		+4.2 +4.0 +3.5	V V V
CMRR	Common Mode Rejection Ratio	Any Bias Setting			88		dB
PSRR	Power Supply Rejection Ratio	Any Bias Setting			110		dB
I_{NIB}	Non Inverting Input Bias Current	Any Bias Setting, (Includes charge injection currents)			0.300	3	nA
I_{IB}	Inverting Input Bias Current	Any Bias Setting, (Includes charge injection currents)			0.150	1.5	nA
A_V	Voltage Gain	$R_L = 100k\Omega$	Low Bias Med Bias High Bias	90 90 80	105 105 100		dB dB dB
V_{OUT}	Maximum Output Voltage Swing	$R_L = 1M\Omega$ $R_L = 100k\Omega$ $R_L = 10k\Omega$	 Positive Swing Negative Swing	 +4.4	±4.9 ±4.8	 −4.5	V V V V V V

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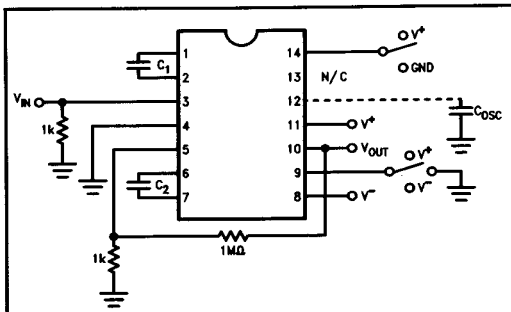
ELECTRICAL CHARACTERISTICS (Continued)

Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$), $C_1 = C_2 = 1\mu F$, Test Circuit 1, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
SR	Large Signal Slew Rate	Unity	High Bias Setting		1.8		V/μs
		Gain	Med Bias Setting		0.5		V/μs
		ICL7600	Low Bias Setting		0.2		V/μs
GBW	Unity Gain Band Width		High Bias Setting		1.2		MHz
		ICL7600	Med Bias Setting		0.3		MHz
		Test Circuit 2	Low Bias Setting		0.12		MHz
GBW	Extrapolated Unity Gain Band Width		High Bias Setting		1.8		MHz
		ICL7601	Med Bias Setting		0.4		MHz
			Low Bias Setting		0.2		MHz
I_{BIAS}	BIAS Terminal Input Current	$V^- - 0.3 \leq V_{BIAS} \leq V^+ + 0.3$ volt			±30		pA
V_{BH}	BIAS Voltage to Define Current Modes	Low Bias Setting		$V^+ - 0.3$	V^+	$V^+ + 0.3$	V
V_{BM}		Med Bias Setting		$V^- + 1.4$	GND	$V^+ - 1.4$	V
V_{BL}		High Bias Setting		$V^- - 0.3$	V^-	$V^- + 0.3$	V
I_{DR}	DR (Division Ratio) Input Current	$V^+ - 8.0V \leq V_{DR} \leq V^+ + 0.3V$			±30		pA
V_{DRH}	DR Voltage to define oscillator division ratio	Internal oscillator division ratio 32		$V^+ - 0.3$		$V^+ + 0.3$	V
V_{DRL}		Internal oscillator division ratio 2		$V^+ - 8$		$V^+ - 1.4$	V
f_{COM}	Nominal Commutation Frequency	$C_{OSC} = 0$ pF	DR Connected to V^+		160		Hz
			DR Connected to GND		2560		Hz
I_S	Supply Current	High Bias Setting			7	15	mA
		Medium Bias Setting			1.7	5	mA
		Low Bias Setting			0.6	1.5	mA
$V^+ - V^-$	Operating Supply Voltage Range	High Bias Setting		5		16	V
		Medium or Low Bias Setting		4		16	V

NOTE 1: For design only, not tested.



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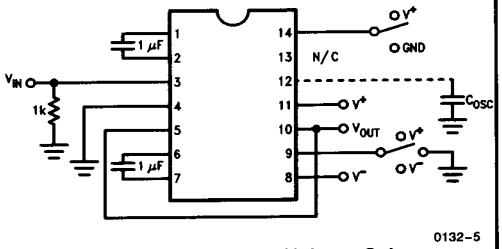
Test Circuit 1: Voltage Gain = 1000



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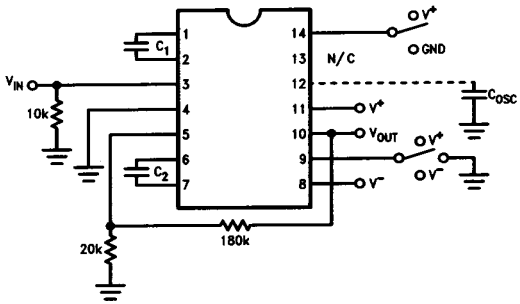
Test Circuit 2: Unity Voltage Gain



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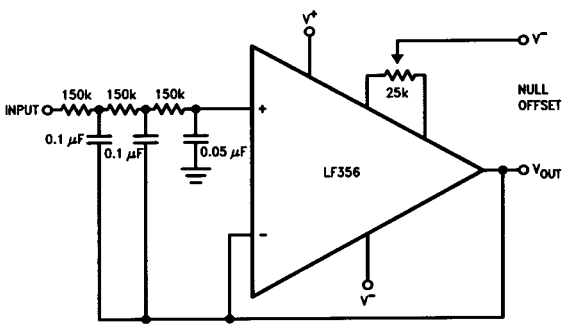
Test Circuit 3: Voltage Gain = 10



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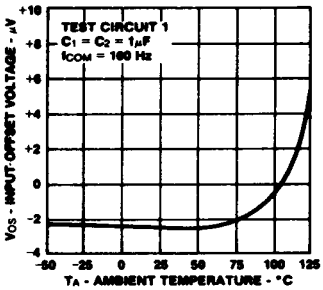
Test Circuit 4: DC to 10Hz Unity Gain Low Pass Filter

Figure 4: Test Circuits

ICL7600/ICL7601

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



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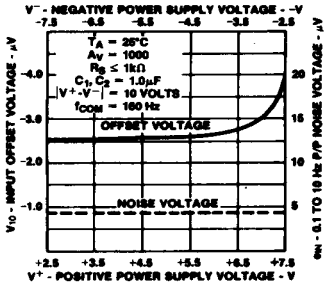
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



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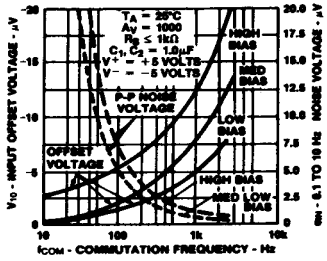
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF COMMUNTATION FREQUENCY (C_1, C_2 = 1µF)



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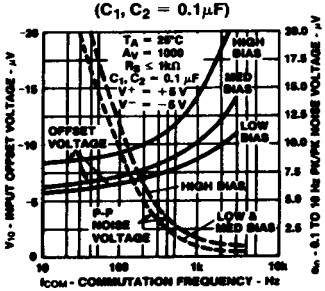
INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 0.1µF)



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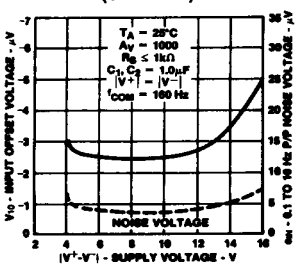
INPUT OFFSET VOLTAGE AND PK TO PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE ($V^+ - V^-$)



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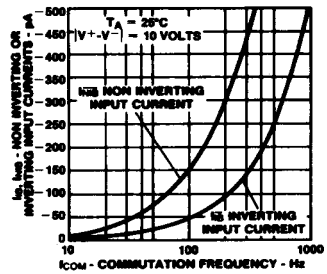
INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



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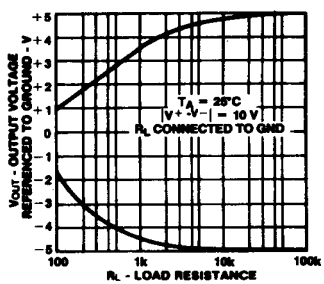
MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



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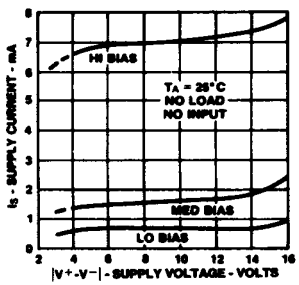
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



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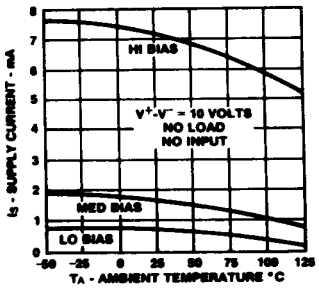
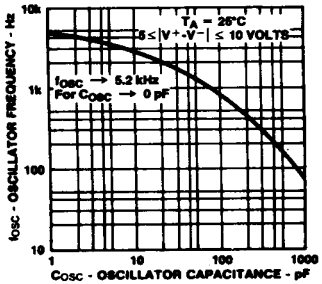
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



0132-16

OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING



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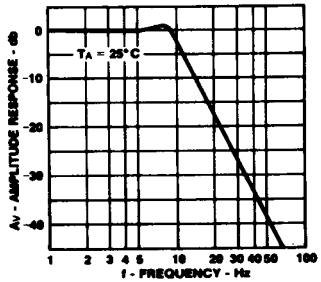
FREQUENCY RESPONSE OF THE 10 Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 4).



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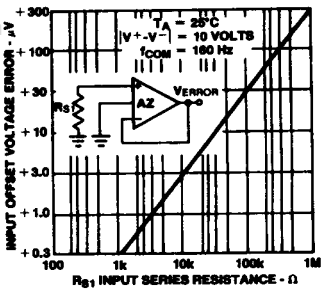
TOTAL EQUIVALENT INPUT OFFSET VOLTAGE AS A FUNCTION OF SOURCE IMPEDANCE—+ INPUT



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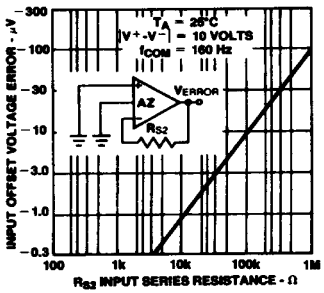
TOTAL EQUIVALENT INPUT OFFSET VOLTAGE AS A FUNCTION OF SOURCE IMPEDANCE—− INPUT



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DETAILED DESCRIPTION

CAZ Operational Amplifier Operation

The CAZ operational amplifier functions on principles which are very different from those encountered in conventional op amp types. An important advantage of the ICL7600/ICL7601 devices is the ability to self-compensate for internal error voltages, whether they are steady-state, related to temperature or supply voltage, or variable in nature over a long term.

Operation of the ICL7600/ICL7601 CAZ operational amplifier is demonstrated in Figure 5. The basic amplifier configuration represented by the large triangles has one more input than does a regular op amp–the AZ, or auto-zero input. The voltage at the AZ input is that to which each of the internal op amps will be auto-zeroed. In Mode A, op amp #2 is connected into a unity gain mode through on-chip analog switches, and charges the external capacitor C_2 to a voltage equal to the DC offset voltage of that amplifier and the instantaneous low frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps in the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which was charged to a voltage equal to its offset and noise voltage) connected in series to its non-inverting (+) input and nulls out the input offset and noise voltage of the amplifier. While one of the op amps is processing the input signal, the other is placed in the auto-zero mode and charges its capacitor to a voltage equal to its equivalent DC and low-frequency error voltage. The internal op amps are reconnected at a rate designated as the commutation frequency, f_{COM}.

The CAZ amp concept offers a number of other advantages to the designer, as compared to standard bipolar or FET-input op amps:

ICL7600/ICL7601

- Effective input offset voltages can be made between 1000x and 10,000x less without trimming.
- Long-term drift phenomena are compensated for and dramatically reduced.
- Temperature effects are compensated for over a wide range. Reductions can be as high as 100 times or higher.
- Supply voltage sensitivity is reduced.

The on-chip op amps are connected internally to the external input and output terminals via CMOS analog switches, as shown in Figure 6. The analog switch structure shown in Figure 6 is arranged so that at any time three switches are open and three switches are conducting. Each analog switch includes a P-channel transistor in parallel with an N-channel transistor.

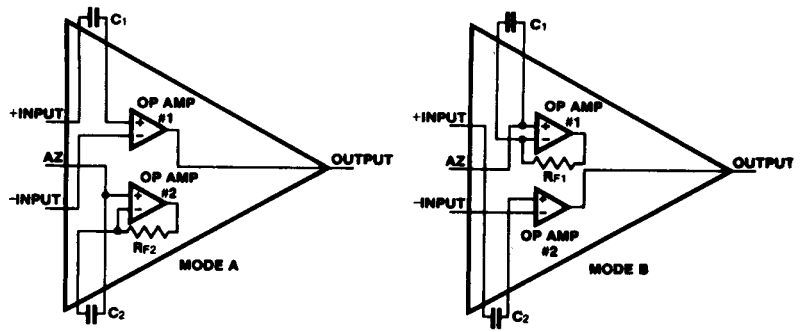

Figure 5: Diagramatic Representation of the 2 Half Cycles of Operation of the CAZ OP AMP

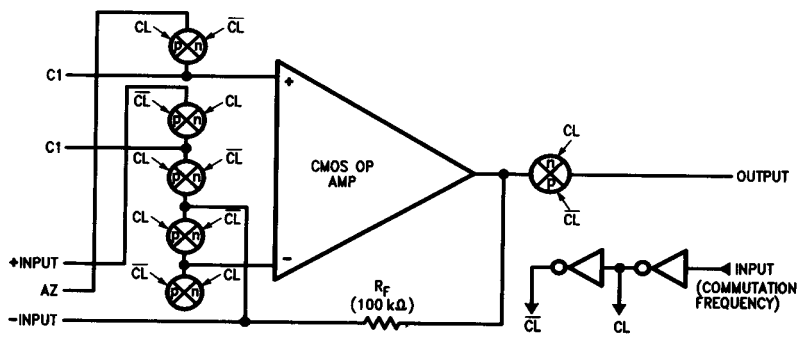

Figure 6: Schematic of Analog Switches Connecting Each Internal OP AMP to the External Inputs and Output

APPLICATIONS

The ICL7600/ICL7601 CAZ op amp is ideal for use as a front-end preamplifier for dual-slope A/D converters which require high sensitivity for single-ended input sources such as thermocouples.

A typical high-sensitivity A/D converter system is shown in Figure 7. The system uses an Intersil ICL7109 12-bit monolithic A/D binary converter, and is intended for direct interface with microprocessors. Both the ICL7600/ICL7601 and the ICL7109 use power supply voltages of ±5V, and the entire system consumes typically 2.5 mA of current.

The input signal is applied through a low-pass filter (150 Hz) to the CAZ op amp, which is connected in a non-inverting gain configuration of either 10 or 100. The internal oscillator of the CAZ amp is allowed to run free at about 5,200 Hz, resulting in a commutation frequency of 160 Hz, with the DR terminal connected to V+. The error-storage capacitors C_1 and C_2 are each 1 μF value, and provide a good compromise between the minimum equivalent input offset voltage and the lowest value of low-frequency noise.

The output signal is then passed through a low-pass filter (1 MΩ and 0.1 μF), with a bandwidth of 1.5 Hz. This results in an equivalent DC offset voltage of 1 μV to 2 μV, and a peak-to-peak noise voltage of 1.7 μV, referred to the input of the CAZ amp. The output from the low-pass filter feeds directly into the input of the ICL7109.

In a system such as that shown in Figure 7 there is a degree of flexibility possible in assigning various gains to the ICL7600/ICL7601 pre-amplifier, and to various sensitivities for the ICL7109. For optimum performance, the CAZ op amp must amplify the input signal so that the equivalent, 15 μV input noise voltage of the A/D converter is masked. This implies a gain of at least 10 for the CAZ op amp preamplifier.

On the other hand, if the gain of the CAZ op amp is increased too much, its output swing will be limited by the ±5V supplies. This condition imposes a maximum gain of 200 to produce an output of ±0.000005 times 4,096 times 200, or ±4,096V, for a 5 μV per count sensitivity. Use of an ICL7600 is recommended for low gains (<20) and the ICL7601 for gains of more than 20.

The values of the integrating resistor and the reference voltage must be chosen to suit the overall sensitivity of the system. For example, in a system requiring a sensitivity of 5 μV per count, use a CAZ amp in a gain configuration of 50 (with ICL7601). Thus for a full scale count of 4096 (12 bits), the input voltage to the ICL7109 would be 5 μV times 50 times 4096 or 1.024 volts. Since the ratio of input to reference is 2:1, the value of the reference voltage becomes 0.512 and a 50 kΩ integrating resistor is recommended. A system such as that shown in Figure 7 will allow a resolution of 1°C for low sensitivity platinum/rhodium junctions. For 0.1°C resolution, use high sensitivity thermocouples having copper/constantan junctions.

The low-pass filter between the output of the CAZ op amp and the input of the ICL7109 A/D converter can be used to improve the signal-to-noise ratio of the system by reducing bandwidth. A 10 Hz filter will result in an equivalent peak-to-peak noise voltage figure of 4 μV. If the bandwidth is reduced to 1.5 Hz, the peak-to-peak noise voltage will be reduced to about 1.7 μV, a reduction by a factor of three. The penalty for this reduction will be a longer system response time; however in most cases this will not be a major consideration, because of the large thermal inertia of many thermocouple probes.

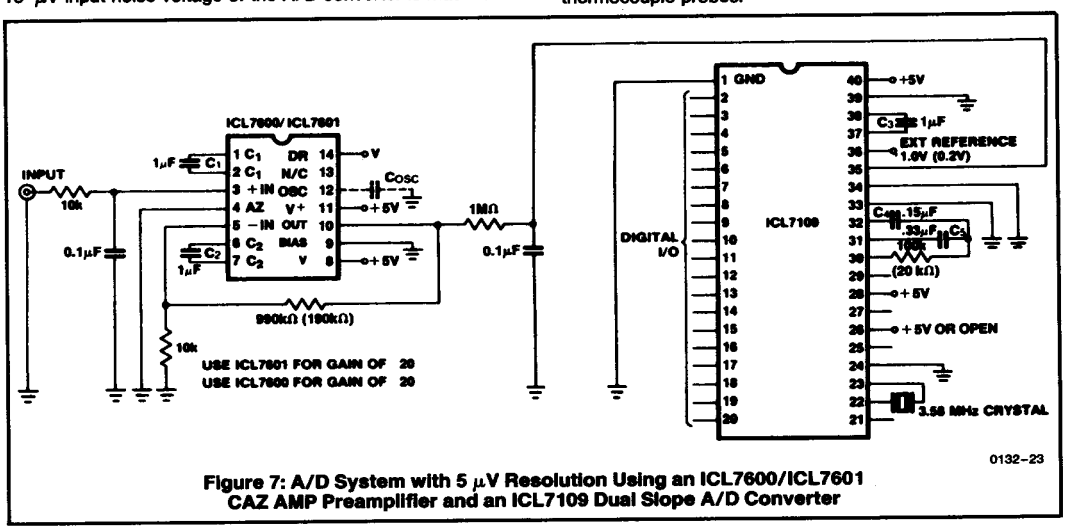

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Figure 7: A/D System with 5 μV Resolution Using an ICL7600/ICL7601 CAZ AMP Preamplifier and an ICL7109 Dual Slope A/D Converter

ICL7600/ICL7601

SOME HELPFUL HINTS

Testing the ICL7600/ICL7601 CAZ Operational Amplifier

A simple and relatively accurate means of testing the CAZ op amp is to use a Tektronix Type 577 curve tracer, with the CAZ op amp inserted in a special 14-lead socket which plugs into a Tektronix 178, and which contains two soldered-in auto-zero capacitors of 1 μF each. This simple and convenient tester will provide most of the information needed for low-frequency parameters. The test setup will allow resolution of input offset voltages to about 10 μV.

For greater accuracy, it is suggested that a breadboard be built which minimizes thermoelectric effects and which includes an output low-pass filter of the type shown in Test Circuit #4. The output from the CAZ amp can be connected to a dual-slope A/D converter as shown in Figure 7. The low-frequency noise can then be displayed on a storage scope or on a strip chart recorder.

Bias Control

The on-chip op amps consume over 90% of the power required for the ICL7600/ICL7601. Three externally-programmable bias levels are provided. These levels are set by connecting the BIAS terminal to V^+, GND or V^-, for LOW, MED of HIGH BIAS levels, respectively. The difference between each bias setting is approximately a factor of three, which allows a 9:1 ratio between supply current and the bias setting. The reason for this current programmability is to provide the user with a choice of device power dissipation levels, slew rate values (the higher the slew rate the better the recovery from commutation spikes), and offset errors due to chip "voltage drop" and thermoelectric effects (the higher the power dissipation the higher the input offset error). In most cases, the medium (MED BIAS) setting will be the best choice.

Output Loading (Resistive)

With a 10 kΩ load the output swing can cover nearly the entire supply voltage range, and the device can be used with loads as low as 2 kΩ. However, with loads of less than 50 kΩ, the on-chip op amps become transconductance amplifiers, since their output impedances are about 50 kΩ each. Thus the open-loop gain is 20 dB less with a 2 kΩ load than it would be with a 20 kΩ load. For high gain configurations requiring high accuracy, output loads of 100 kΩ or more are suggested.

Another consideration which must not be overlooked is the additional power dissipation of the chip which results from a large output swing into a low value load. This added variable can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output to reduce high-frequency noise outside the signal passband of interest. With conventional op amps, the obvious solution would be to place a capacitor across the external feedback resistor to provide the low pass filter.

However, with the CAZ op amp, this is not feasible because of the nature of commutation voltage spikes. The voltage spikes show a low impedance characteristic in the direction of the auto-zero voltage, and a high impedance on the recovery edge, as shown in Figure 8. It can be seen that the effect of the large load capacitor is to produce an area error in the output waveform, and hence an effective gain error. The output low pass filter must be a high impedance type to avoid output voltage area errors. For example, a 1.5 Hz filter should use a 100 kΩ resistor and a 1.0 μF capacitor, or a 1.0 MΩ resistor and an 0.1 μF capacitor. This effect also causes problems with integrator circuits.

Oscillator and Digital Considerations

The oscillator has been designed to run free at about 5.2 kHz when the OSC terminal is open-circuited. If the full divider network is used, this will result in a commutation frequency of about 160 Hz nominal. The commutation frequency is the frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160 Hz commutation frequency represents approximately the optimum frequency at which the input offset voltage is close to minimum, where the low-frequency noise is acceptable, and where errors derived from noise spikes will be low. Other commutation frequencies may provide optimization of other parameters, but always to the detriment of major characteristics.

The oscillator is of a high impedance type, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the desired frequency of the oscillation is 5.2 kHz, the terminal should be left unattached and open. In other instances, it may be desirable to lock the oscillator to a clock or to run it at another frequency. The ICL7600/ICL7601 provides two degrees of flexibility. First, the DR (division ratio) terminal permits the user to choose between dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND), to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and V^+, or system ground terminals. For situations which require the commutation frequency to be locked onto a master clock, the OSC terminal can be driven from TTL logic (with resistive pull-up) or from CMOS logic, provided that the V^+ supply (with respect to ground) is $+5V$ ($\pm 10\%$) and the logic driver also operates from a similar supply voltage. This is because the logic section—including the oscillator—operates from an internal $-5V$ supply referenced to V^+ generated on-chip, and is not accessible externally.

Thermoelectric Effects

The ultimate limitations to ultra-high-precision DC amplifiers are thermoelectric, Peltier or thermocouple effects in junctions consisting of various metals, alloys, silicon, etc. Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1 μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

In order to realize the extremely low offset voltages which the CAZ op amp can provide, it is essential to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. In addition, the supply voltages and power dissipation should be kept to a minimum. Use the medium bias mode as well as a high impedance load, and keep well away from heat dissipated by surrounding equipment.

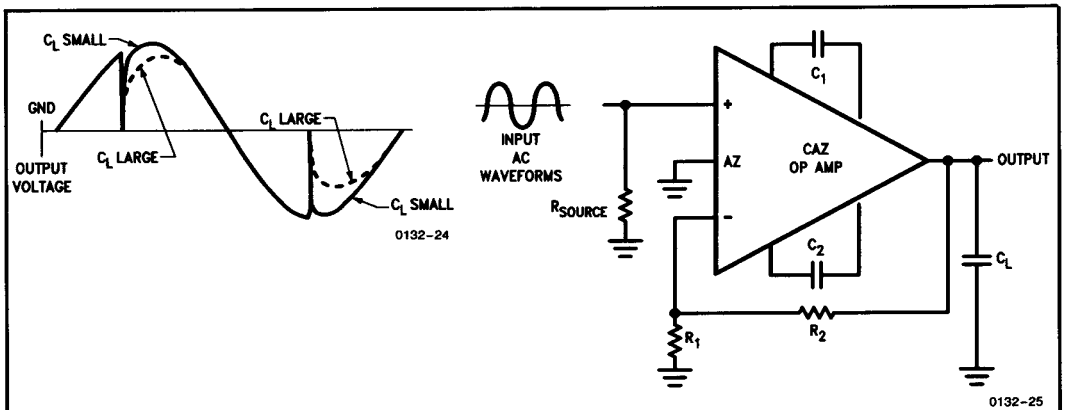

Figure 8: Effect of a Load Capacitor on Output Voltage Waveforms

Component Selection

The two required auto-zero capacitors, C_1 and C_2, should each be of 1.0 μF value. These are large values for non-electrolytic capacitors, but since the voltages impressed on them do not change significantly, problems of dielectric absorption and the like are not important.

Excellent results have been obtained in operation at commercial temperature ranges using several of the smaller-size and more economical capacitors, since the absolute values of the capacitors is not critical. Even polarized electrolytic capacitors rated at 1.0 μF/50V, though not recommended, have been used with success.

Commutating Voltage Transient Effects

While in most respects the CAZ op amp behaves like a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 100 Hz. This is because of the finite switching transients which occur in the input and output terminals due to commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and include all of the higher harmonics. If the commutation frequency is higher than the highest in-band frequency, these transients can be effectively blanked with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage equal to the input offset voltage(about 5–10 mV) which occurs during the transition to the signal processing mode from the auto-zero mode. Since the input capacitances of the on-chip op amps are typically in the 10 pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must be at least 10,000 x 10 pF, or 0.1 μF each.

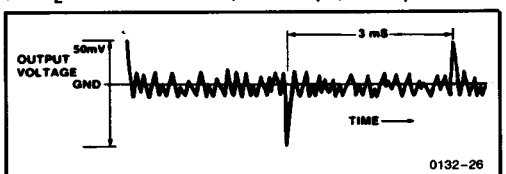

Figure 9: Output waveform from Test Circuit 1.

The charge which is injected into the op amp when it is switched into the signal-processing mode produces a rapidly-decaying voltage spike at the input, in addition to an equivalent DC bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically about 1.0 pA at ambient temperature of 25°C.

The output waveform of Test Circuit #1 (with no input) is shown in Figure 9. Note that the equivalent noise voltage shown is amplified 1000 times, and that because of the finite slew rate of the on-chip op amps the 7 mV input transients are *not* amplified by 1000.

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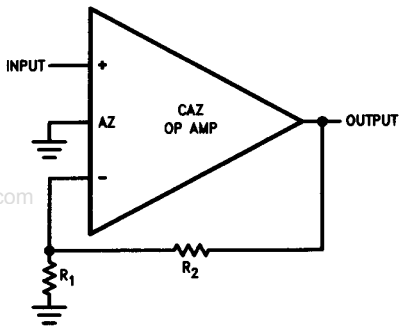
The output transient voltage effects (as distinct from the input effects which are propagated through the on-chip op amps) will occur if there is a difference in the output voltage of the internal op amps between the auto-zero modes and the signal-processing modes. The output stage of the on-chip op amp must slew from its auto-zero output voltage to the desired signal-processing output voltage. This is shown in Figure 10, where the system is auto-zeroed to ground.

The duration of the output transients is greatly affected by the gain configuration and the bias setting, since these two parameters have an effect on system slew rate. At low gains and high bias settings, the output transient durations are very short. For this reason there are two versions of the CAZ op amp, the ICL7600 which is compensated for unity gain and which can be used for gain configurations up to 20, and the ICL7601, which is uncompensated and recommended for operation in gain configurations greater than 20. Thus, when a signal is being processed in a high gain configuration, the effective output signal error is greater for the ICL7600 than it is for the ICL7601.

Non-Amplifier Applications

In principle, this is one of the few "chopper-stabilized" type amplifiers that could be used as a comparator; the transient effects on the output will normally require careful synchronism of output strobes with oscillator drive.



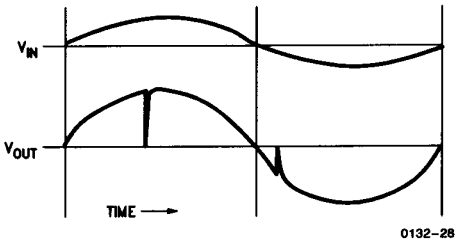


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Figure 10: Simple CAZ OP AMP Circuit and the Output Voltage Waveform