ICL8049

OBSOLETE PRODUCT
NO RECOMMENDED REPLACEMENT
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Antilog Amplifier

Features

- **Full Scale Accuracy 0.5%**
- **Temperature Compensated Operation . . . . 0°C to 70°C**
- **Scale Factor, Adjustable 1V/Decade**
- **Dynamic Voltage Range 60dB**
- **Dual JFET Input Op Amps**

Description

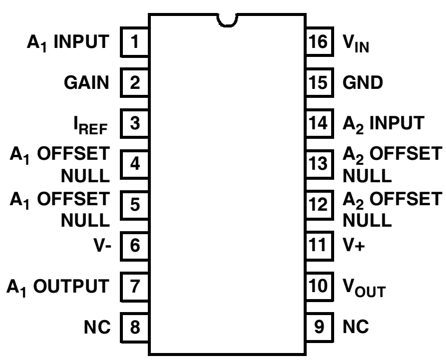
The ICL8049 is a monolithic antilogarithmic amplifier that is fully temperature compensated and is nominally designed to provide 1 decade of output voltage for each 1V change of input voltage. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

Part Number Information

PART NUMBER	ERROR (25°C)	TEMPERATURE RANGE (°C)	PACKAGE
ICL8049BCJE	10mV	0 to 70	16 Ld CERDIP
ICL8049CCJE	25mV	0 to 70	16 Ld CERDIP

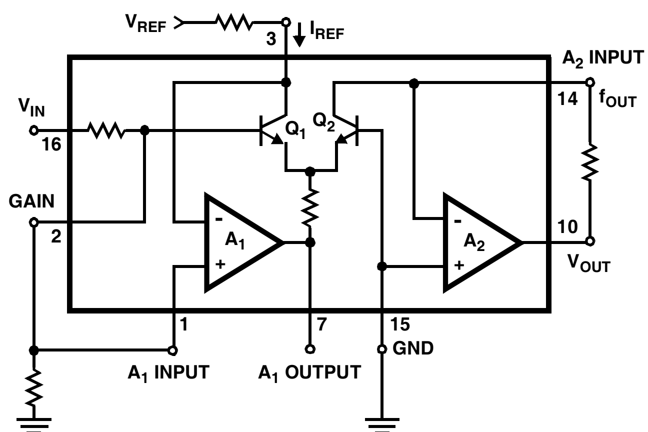
Pinout

ICL8049 (CERDIP)
TOP VIEW



Functional Diagram

ICL8049



Absolute Maximum Ratings

Supply Voltage . . . . ±18V
V_{IN} (Input Current) . . . . ±15V
I_{REF} (Reference Current) 2mA
Voltage Between Offset Null and V+ . . . . ±0.5V
Output Short Circuit Duration . . . . Indefinite
Power Dissipation. 750mW
Lead Temperature (Soldering 10 Sec.) . . . . 300°C

Operating Conditions

Operating Temperature Range . . . . 0°C to 70°C
Storage Temperature Range . . . . -65°C to 150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_S = ±15V, T_A = 25°C, I_{REF} = 1mA, Scale Factor Adjusted for 1 Decade (Out) per Volt (In), Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS	ICL4049BC			ICL8049CC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic Range (V_{OUT})	V_{OUT} = 10mV to 10V	60	-	-	60	-	-	dB
Error, Absolute Value	0V ≤ V_{IN} ≤ 2V	-	3	15	-	5	25	mV
	T_A = 0°C to 70°C, 0V ≤ V_{IN} ≤ 3V	-	20	75	-	30	150	mV
Temperature Coefficient, Referred to V_{IN}	V_{IN} = 3V	-	0.38	-	-	0.55	-	mV/°C
Power Supply Rejection Ratio	Referred to Input, for V_{IN} = 0V	-	2.0	-	-	2.0	-	μV/V
Offset Voltage (A_1 and A_2)	Before Nulling	-	15	25	-	15	50	mV
Wideband Noise	Referred to Input, for V_{IN} = 0V	-	26	-	-	26	-	μV_{RMS}
Output Voltage Swing	R_L = 10kΩ	±12	±14	-	±12	±14	-	V
	R_L = 2kΩ	±10	±13	-	±10	±13	-	V
Power Consumption		-	150	200	-	150	200	mW
Supply Current		-	5	6.7	-	5	6.7	mA

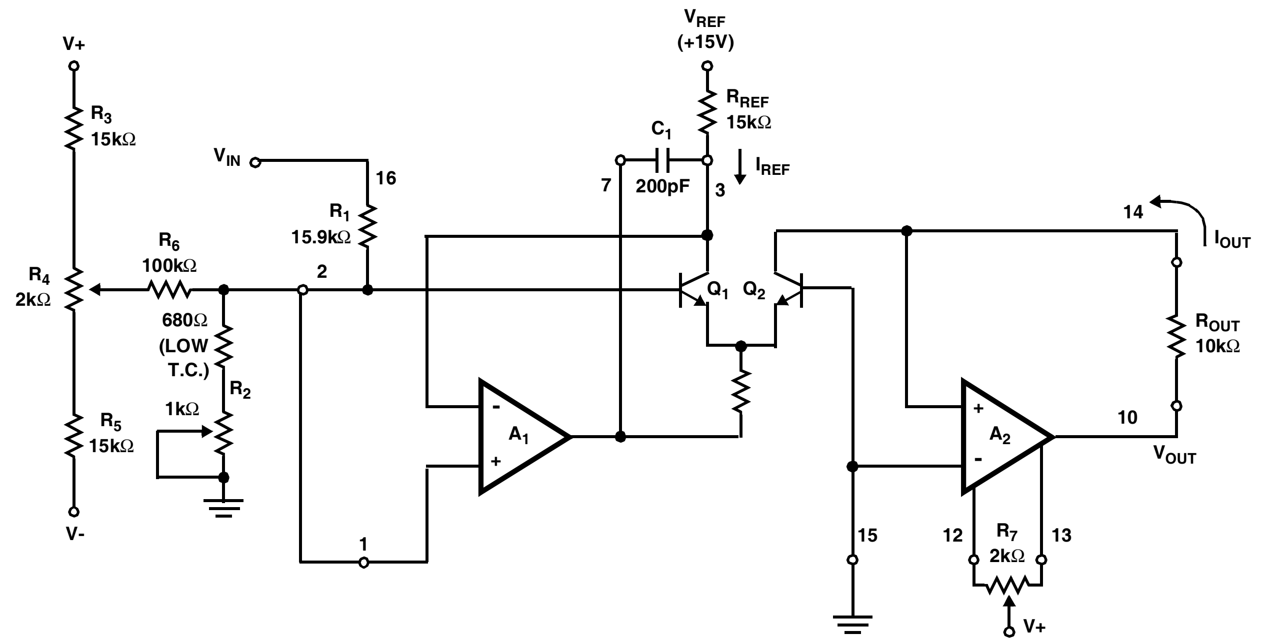


FIGURE 1. ICL8049 OFFSET AND SCALE FACTOR ADJUSTMENT

ICL8049 Detailed Description

The ICL8049 relies on the same logarithmic properties of the transistor as the ICL8048. The input voltage forces a specific ΔV_{BE} between Q_1 and Q_2 (Figure 1). This V_{BE} difference is converted into a difference of collector currents by the transistor pair. The equation governing the behavior of the transistor pair is derived from (2) on the previous page and is as follows:

$$\frac{I_{C1}}{I_{C2}} = \exp\left[\frac{q\Delta V_{BE}}{kT}\right] \quad (1)$$

When numerical values for q/kT are put into this equation, it is found that a ΔV_{BE} of 59mV (at +25°C) is required to change the collector current ratio by a factor of ten. But for ease of application, it is desirable that a 1V change at the input generate a tenfold change at the output. The required input attenuation is achieved by the network comprising R_1 and R_2. In order that scale factors other than one decade per volt may be selected, R_2 is external to the chip. It should have a value of 1kΩ, adjustable ±20%, for one decade per volt. R_1 is a thin film resistor deposited on the monolithic chip; its temperature characteristics are chosen to compensate the temperature dependence of Equation 1, as explained on the previous page.

The overall transfer function is as follows:

$$\frac{I_{OUT}}{I_{REF}} = \exp\left[\frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (2)$$

Substituting $V_{OUT} = I_{OUT} \times R_{OUT}$ gives:

$$V_{OUT} = R_{OUT}\, I_{REF} \exp\left[\frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (3)$$

For voltage references Equation 3 becomes

$$V_{OUT} = V_{REF} \times \frac{R_{OUT}}{R_{REF}} \exp\left[\frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (4)$$

ICL8049 Offset and Scale Factor Adjustment

As with the log amplifier, the antilog amplifier requires three adjustments. The first step is to null out the offset voltage of A_2. This is accomplished by reverse biasing the base-emitter of Q_2. A_2 then operates as a unity gain buffer with a grounded input. The second step forces $V_{IN} = 0$; the output is adjusted for $V_{OUT} = 10V$. This step essentially “anchors” one point on the transfer function. The third step applies a specific input and adjusts the output to the correct voltage. This sets the scale factor. Referring to Figure 1 the exact procedure for 1 decade/volt is as follows:

1. Connect the input (pin #16) to +15V. This reverse biases the base-emitter of Q_2. Adjust R_7 for $V_{OUT} = 0V$. Disconnect the input from +15V.
2. Connect the input to Ground. Adjust R_4 for $V_{OUT} = 10V$. Disconnect the input from Ground.
3. Connect the input to a precise 2V supply and adjust R_2 for $V_{OUT} = 100mV$.

The procedure outlined above optimizes the performance over a 3 decade range at the output (i.e., V_{OUT} from 10mV) to 10V). For a more limited range of output voltages, for example 1V to 10V, it would be better to use a precise 1V supply and adjust for $V_{OUT} = 1V$. For other scale factors and/ or starting points, different values for R_2 and R_{REF} will be needed, but the same basic procedure applies.