ICM-20648 Datasheet
Revision 1.0

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1 Document Information

1.1 Revision History

Revision Date	Revision	Description
05/01/2015	1.0	Initial Release

1.2 Purpose and Scope

This document is a preliminary product specification, providing a description, specifications, and design related information on the ICM-20648 MotionTracking device.

Specifications are subject to change without notice. Final specifications will be updated based upon characterization of production silicon. For references to register map and descriptions of individual registers, please refer to the ICM-20648 Register Map and Register Descriptions document.

1.3 Product Overview

The ICM-20648 is a MotionTracking device that combines a 3-axis gyroscope, 3-axis accelerometer, and a Digital Motion Processor™ (DMP) all in a small 3.0x3.0x0.9mm QFN package. The device supports the following features:

- Android Lollipop support
- FIFO of size 512 bytes (FIFO size will vary depending on DMP feature-set)
- Runtime Calibration
- Enhanced FSYNC functionality to improve timing for applications like EIS

ICM-20648 devices, with their 6-axis integration, on-chip DMP, and run-time calibration firmware, enable manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope has a programmable full-scale range of ±250, ±500, ±1000, and ±2000 degrees/sec. The accelerometer has a user-programmable accelerometer full-scale range of ±2*g*, ±4*g*, ±8*g*, and ±16*g*. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other key features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71 to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

Communication with all registers of the device is performed using I^2C at up to 100kHz (standard-mode) or up to 400kHz (fast-mode), or SPI at up to 7MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 3.0x3.0x0.9mm (24-pin QFN), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

1.4 Applications

- Mobile phones and tablets
- Portable gaming
- Motion-based game controllers
- 3D remote controls for Internet connected DTVs and set top boxes, 3D mice
- Wearable sensors for health, fitness and sports

2 Features

2.1 Gyroscope Features

The triple-axis MEMS gyroscope in the ICM-20648 includes the following features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±250, ±500, ±1000, and ±2000°/sec and integrated 16-bit ADCs
- User-selectable ODR; User-selectable low pass filters
- Self-test

2.2 Accelerometer Features

The triple-axis MEMS accelerometer in ICM-20648 includes the following features:

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full scale range of ±2*g*, ±4*g*, ±8*g* and ±16*g* and integrated 16-bit ADCs
- User-selectable ODR; User-selectable low pass filters
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 DMP Features

The DMP in ICM-20648 includes the following capabilities:

- Offloads computation of motion processing algorithms from the host processor. The DMP can be used to minimize power, simplify timing, simplify the software architecture, and save valuable MIPS on the host processor for use in applications.
- Optimized for Android Lollipop for low power features (AP suspended) including SMD, Step Count, Step Detect, Activity Classification, Rotation Vector, and Gaming Rotation Vector
- Optimized for Android Lollipop batching, both while the AP is active and suspended. The DMP will also batch data from externally connected sensors such as a compass, or pressure sensor.
- The DMP enables ultra-low power run-time and background calibration of the accelerometer, gyroscope, and compass, maintaining optimal performance of the sensor data for both physical and virtual sensors generated through sensor fusion. This enables the best user experience for all sensor enabled applications for the lifetime of the device.
- DMP features simplify the software architecture resulting in quicker time to market.
- DMP features are OS, Platform, and Architecture independent, supporting virtually any AP, MCU, or other embedded architecture.

2.4 Additional Features

The ICM-20648 includes the following additional features:

- I^2C at up to 100kHz (standard-mode) or up to 400kHz (fast-mode) or SPI at up to 7MHz for communication with registers
- Auxiliary master I^2C bus for reading data from external sensors (e.g. magnetometer)
- Digital-output temperature sensor
- 10,000 *g* shock tolerant
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 Electrical Characteristics

3.1 Gyroscope Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Note: All specifications apply to Standard (Duty-Cycled) Mode and Low-Noise Mode, unless noted otherwise

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	GYRO_FS_SEL=0		±250		º/s	1
	GYRO_FS_SEL=1		±500		º/s	1
	GYRO_FS_SEL=2		±1000		º/s	1
	GYRO_FS_SEL=3		±2000		º/s	1
Gyroscope ADC Word Length			16		bits	1
Sensitivity Scale Factor	GYRO_FS_SEL=0		131		LSB/(º/s)	1
	GYRO_FS_SEL=1		65.5		LSB/(º/s)	1
	GYRO_FS_SEL=2		32.8		LSB/(º/s)	1
	GYRO_FS_SEL=3		16.4		LSB/(º/s)	1
Sensitivity Scale Factor Tolerance	25°C		±3		%	2
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C		±0.02		%/ºC	2
Nonlinearity	Best fit straight line; 25°C		±0.2		%	2, 3
Cross-Axis Sensitivity			±2		%	2, 3
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C (Component-level)	-20		+20	º/s	2
ZRO Variation Over Temperature	-40°C to +85°C		±0.24		º/s/°C	2
GYROSCOPE NOISE PERFORMANCE (GYRO_FS_SEL=0)						
Noise Spectral Density	Based on Noise Bandwidth = 10Hz		0.011		º/s/√Hz	2
GYROSCOPE MECHANICAL FREQUENCIES		25	27	29	kHz	2
LOW PASS FILTER RESPONSE	Programmable Range	5.7		197	Hz	1, 3
GYROSCOPE START-UP TIME	From Full-Chip Sleep mode		35		ms	2, 3
OUTPUT DATA RATE	Standard (duty-cycled) Mode	4.4		562.5	Hz	1
	Low-Noise Mode GYRO_FCHOICE=1; GYRO_DLPFCFG=x	4.4		1.125k	Hz	
	Low-Noise Mode GYRO_FCHOICE=0; GYRO_DLPFCFG=x			9k	Hz	

Table 1 Gyroscope Specifications

Notes:

1. Guaranteed by design
2. Derived from validation or characterization of parts, not guaranteed in production
3. Low-noise mode specification

3.2 Accelerometer Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Note: All specifications apply to Standard (Duty-Cycled) Mode and Low-Noise Mode, unless noted otherwise

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY							
Full-Scale Range	ACCEL_FS=0			±2		*g*	1
	ACCEL_FS=1			±4		*g*	1
	ACCEL_FS=2			±8		*g*	1
	ACCEL_FS=3			±16		*g*	1
ADC Word Length	Output in two's complement format			16		bits	1
Sensitivity Scale Factor	ACCEL_FS=0			16,384		LSB/*g*	1
	ACCEL_FS=1			8,192		LSB/*g*	1
	ACCEL_FS=2			4,096		LSB/*g*	1
	ACCEL_FS=3			2,048		LSB/*g*	1
Initial Tolerance	Component-level			±3		%	2
Sensitivity Change vs. Temperature	-40°C to +85°C ACCEL_FS=0			±0.026		%/ºC	2
Nonlinearity	Best Fit Straight Line			±0.5		%	2, 3
Cross-Axis Sensitivity				±2		%	2, 3
ZERO-G OUTPUT							
Initial Tolerance	Component-level, all axes			±80		m*g*	2
Zero-G Level Change vs. Temperature	-40°C to +85°C	X and Y axes		±0.64		m*g*/°C	2
		Z axis		±1		m*g*/°C	2
ACCELEROMETER NOISE PERFORMANCE							
Noise Spectral Density	Based on Noise Bandwidth = 10Hz			190		µ*g*/√Hz	2
LOW PASS FILTER RESPONSE	Programmable Range		5.7		246	Hz	1, 3
INTELLIGENCE FUNCTION INCREMENT				32		m*g*/LSB	1
ACCELEROMETER STARTUP TIME	From Sleep mode				20	ms	2, 3
	From Cold Start, 1ms V_{DD} ramp				30	ms	2, 3
OUTPUT DATA RATE	Standard (duty-cycled) Mode		0.27		562.5	Hz	1
	Low-Noise Mode ACCEL_FCHOICE=1; ACCEL_DLPFCFG=x		4.5		1.125k	Hz	
	Low-Noise Mode ACCEL_FCHOICE=0; ACCEL_DLPFCFG=x				4.5k	Hz	

Table 2 Accelerometer Specifications

Notes:

1. Guaranteed by design
2. Derived from validation or characterization of parts, not guaranteed in production
3. Low-noise mode specification

3.3 Electrical Specifications

3.3.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	Units	Notes
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.71	1.8	3.6	V	1
SUPPLY CURRENTS						
Gyroscope Only (DMP & Accelerometer disabled)	102.3Hz update rate, 1x averaging filter		1.23		mA	2, 3
Accelerometer Only (DMP & Gyroscope disabled)	102.3Hz update rate, 1x averaging filter		68.9		µA	2, 3
Gyroscope + Accelerometer (DMP disabled)	102.3Hz update rate, 1x averaging filter		1.27		mA	2, 3
Full-Chip Sleep Mode			8		µA	2
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3 D.C. Electrical Characteristics

Notes:

1. Guaranteed by design
2. Derived from validation or characterization of parts, not guaranteed in production
3. The 102.3Hz ODR value shown here is an example, please see the section below for the full list of ODRs supported and corresponding current values

Standard Mode Noise and Power Performance:

The following tables contain Gyroscope and Accelerometer noise and current consumption values for standard mode, for various ODRs and averaging filter settings. Please refer to the ICM-20648 Register Map for further information about the registers referenced in the tables below.

	Averages	1x	2x	4x	8x	16x	32x	64x	128x
	GYRO_FCHOICE	1	1	1	1	1	1	1	1
	GYRO_AVGCFG	0	1	2	3	4	5	6	7
	Ton [ms]	1.15	1.59	2.48	4.26	7.82	14.93	29.15	57.59
	NBW [Hz]	773.5	469.8	257.8	134.8	68.9	34.8	17.5	8.8
	RMS Noise [dps-rms] TYP (based on gyroscope noise: 0.011dps/√Hz)	0.31	0.24	0.18	0.13	0.09	0.06	0.05	0.03
GYRO_SMPLRT_DIV	ODR [Hz]	Current Consumption [mA] TYP							
255	4.4	1.04	1.05	1.05	1.06	1.09	1.14	1.24	1.45
64	17.3	1.07	1.08	1.10	1.15	1.25	1.45	1.85	N/A
63	17.6	1.07	1.08	1.11	1.16	1.26	1.46	1.87	
32	34.1	1.10	1.12	1.17	1.27	1.47	1.86	N/A	
31	35.2	1.10	1.13	1.18	1.28	1.48	1.89		
22	48.9	1.13	1.16	1.23	1.37	1.66	2.22		
16	66.2	1.16	1.21	1.30	1.49	1.88	N/A		
15	70.3	1.17	1.22	1.32	1.52	1.93			
10	102.3	1.23	1.30	1.45	1.74	2.34			
8	125.0	1.27	1.36	1.54	1.90	N/A			
7	140.6	1.30	1.40	1.60	2.01				
5	187.5	1.38	1.52	1.79	2.33				
4	225.0	1.45	1.62	1.94	N/A				
3	281.3	1.56	1.76	2.17					
2	375.0	1.74	2.00	N/A					
1	562.5	2.09	N/A						

Table 4 Gyroscope Noise and Current Consumption

	Averages	1x	4x	8x	16x	32x
	ACCEL_FCHOICE	0	1	1	1	1
	ACCEL_DLPFCFG	x	7	7	7	7
	DEC3_CFG	0	0	1	2	3
	Ton (ms)	0.821	1.488	2.377	4.154	7.71
	NBW (Hz)	1237.5	496.8	264.8	136.5	69.2
	RMS Noise [mg-rms] TYP (based on accelerometer noise: 190µg/√Hz)	6.7	4.2	3.1	2.2	1.6
ACCEL_SMPLRT_DIV	ODR [Hz]	Current Consumption [µA] TYP				
4095	0.27	6.2	6.3	6.5	6.9	7.6
2044	0.55	6.3	6.6	7.0	7.7	9.2
1022	1.1	6.7	7.2	8.0	9.4	12.3
513	2.2	7.3	8.4	9.9	12.8	18.6
255	4.4	8.7	10.9	13.8	19.7	31.4
127	8.8	11.4	15.8	21.6	33.3	56.7
63	17.6	16.8	25.6	37.3	60.7	107.5
31	35.2	27.6	45.2	68.6	115.3	208.9
22	48.9	36.1	60.5	93.0	158.1	288.3
15	70.3	49.2	84.3	131.1	224.7	411.9
10	102.3	68.9	119.9	188.0	324.1	596.3
7	140.6	92.4	162.7	256.3	443.3	N/A
5	187.5	121.2	214.9			
3	281.3	178.9	319.3	N/A		
1	562.5	351.7	N/A			

Table 5 Accelerometer Noise and Current Consumption

3.3.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameter	Conditions	MIN	TYP	MAX	Units	NOTES
SUPPLIES						
Supply Ramp Time (T_{RAMP})	Monotonic ramp. Ramp rate is 10% to 90% of the final value.	0.01	20	100	ms	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
Sensitivity	Untrimmed		333.87		LSB/°C	
Room Temp Offset	21°C		0		LSB	
Power-On RESET						
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01	20	100	ms	1
Start-up time for register read/write	From power-up		11	100	ms	1
I^2C ADDRESS	AD0 = 0 AD0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, AD0, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1MΩ;			0.1*VDDIO	V	
$V_{OL.INT1}$, INT Low-Level Output Voltage	OPEN=1, 0.3mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	
I2C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4V V_{OL}=0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		250	ns	
AUXILLIARY I/O (AUX_CL, AUX_DA)						
V_{IL}, LOW-Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7* VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1* VDDIO		V	
V_{OL1}, LOW-Level Output Voltage	VDDIO > 2V; 1mA sink current	0		0.4	V	

Parameter	Conditions	MIN	TYP	MAX	Units	NOTES
V_{OL3}, LOW-Level Output Voltage	VDDIO < 2V; 1mA sink current	0		0.2* VDDIO	V	
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V V_{OL} = 0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pF	20+0.1C_b		250	ns	
INTERNAL CLOCK SOURCE						
Clock Frequency Initial Tolerance	Accelerometer Only Mode	-5		+5	%	1
	Gyroscope or 6-Axis Mode WITHOUT Timebase Correction	-9		+9	%	1
	Gyroscope or 6-Axis Mode WITH Timebase Correction	-1		+1		
Frequency Variation over Temperature	Accelerometer Only Mode	-10		+10	%	1
	Gyroscope or 6-Axis Mode		±1		%	1

Table 4 A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.3.3 Other Electrical Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	Units	Notes
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low Speed Characterization		100 ±10%		kHz	
	High Speed Characterization		7 ±10%		MHz	
I^2C Operating Frequency	All registers, Fast-mode			400	kHz	
	All registers, Standard-mode			100	kHz	

Table 5 Other Electrical Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.4 I2C Timing Characterization

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency				400	kHz	1, 2
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	1, 2
t_{LOW}, SCL Low Period		1.3			µs	1, 2
t_{HIGH}, SCL High Period		0.6			µs	1, 2
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	1, 2
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1, 2
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1, 2
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	1, 2
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	1, 2
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	1, 2
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	1, 2
C_b, Capacitive Load for each Bus Line			< 400		pF	1, 2
$t_{VD.DAT}$, Data Valid Time				0.9	µs	1, 2
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	1, 2

Table 6 I²C Timing Characteristics

Notes:

1. Timing Characteristics apply to both Primary and Auxiliary I2C Bus
2. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

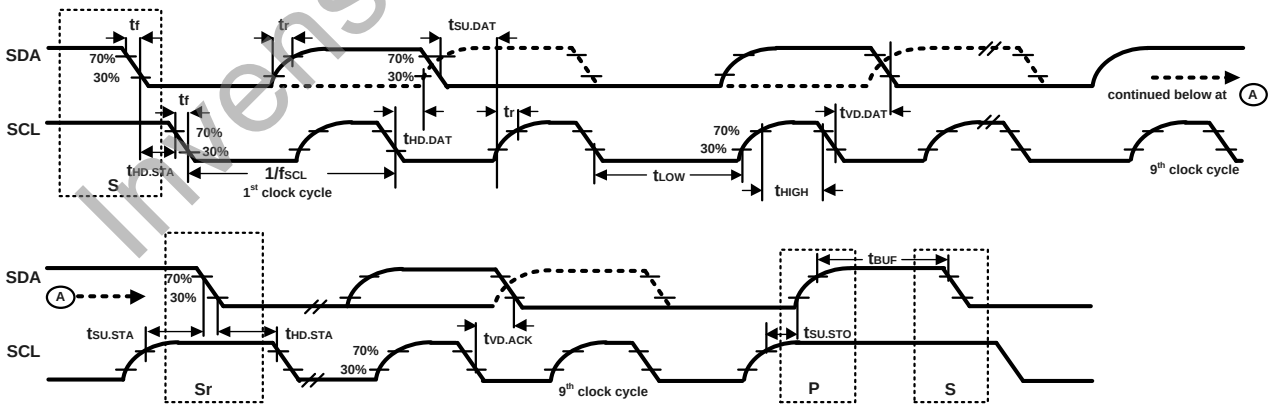


Figure 1 I2C Bus Timing Diagram

3.5 SPI Timing Characterization

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
SPI TIMING						
f_{SCLK}, SCLK Clock Frequency				7	MHz	
t_{LOW}, SCLK Low Period		64			ns	
t_{HIGH}, SCLK High Period		64			ns	
$t_{SU.CS}$, CS Setup Time		8			ns	
$t_{HD.CS}$, CS Hold Time		500			ns	
$t_{SU.SDI}$, SDI Setup Time		5			ns	
$t_{HD.SDI}$, SDI Hold Time		7			ns	
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF			59	ns	
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20pF	6			ns	
$t_{DIS.SDO}$, SDO Output Disable Time				50	ns	

Table 7 SPI Timing Characteristics (7MHz)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

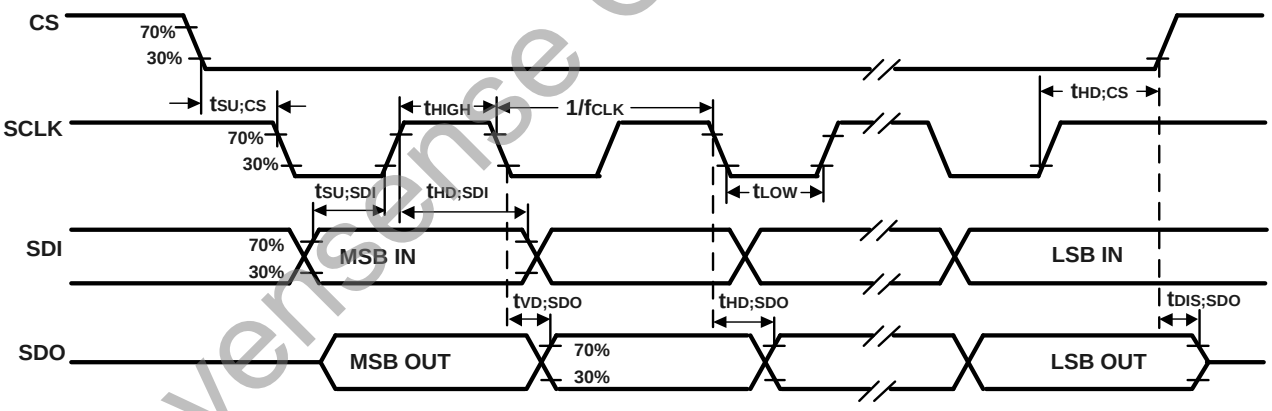


Figure 2 SPI Bus Timing Diagram

3.6 Absolute Maximum Ratings

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5V to +4V
Supply Voltage, VDDIO	-0.5V to +4V
REGOUT	-0.5V to 2V
Input Voltage Level (AUX_DA, AD0, FSYNC, INT, SCL, SDA)	-0.5V to VDD + 0.5V
Acceleration (Any Axis, unpowered)	10,000g for 0.2ms
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2kV (HBM); 200V (MM)
Latch-up	JEDEC Class II (2),125°C ±100mA

Table 8 Absolute Maximum Ratings

4 Applications Information

4.1 Pin Out Diagram and Signal Description

Pin Number	Pin Name	Pin Description
7	AUX_CL	I²C Master serial clock, for connecting to external sensors.
8	VDDIO	Digital I/O supply voltage.
9	AD0 / SDO	I²C Slave Address LSB (AD0); SPI serial data output (SDO).
10	REGOUT	Regulator filter capacitor connection.
11	FSYNC	Frame synchronization digital input. Connect to GND if unused.
12	INT1	Interrupt 1.
13	VDD	Power supply voltage.
18	GND	Power supply ground.
19	INT2	Interrupt 2.
20	RESV	Reserved. Connect to GND.
21	AUX_DA	I²C master serial data, for connecting to external sensors.
22	nCS	Chip select (SPI mode only).
23	SCL / SCLK	I²C serial clock (SCL); SPI serial clock (SCLK).
24	SDA / SDI	I²C serial data (SDA); SPI serial data input (SDI).
1 – 6, 14 - 17	NC	No Connect pins. Do not connect.

Table 9 Signal Descriptions

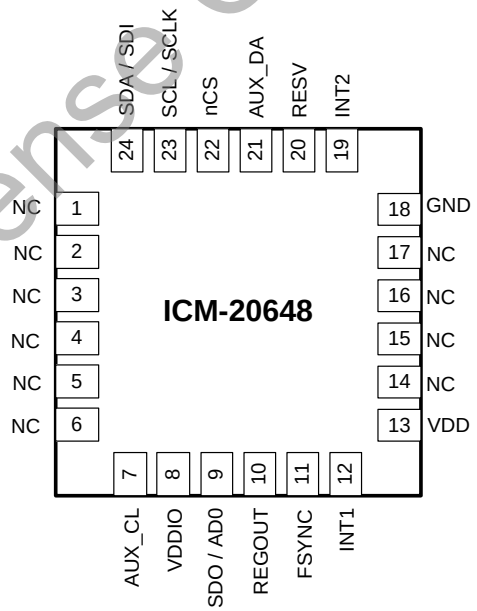


Figure 3 Pin out Diagram for ICM-20648 3.0x3.0x0.9mm QFN

4.2 Typical Operating Circuit

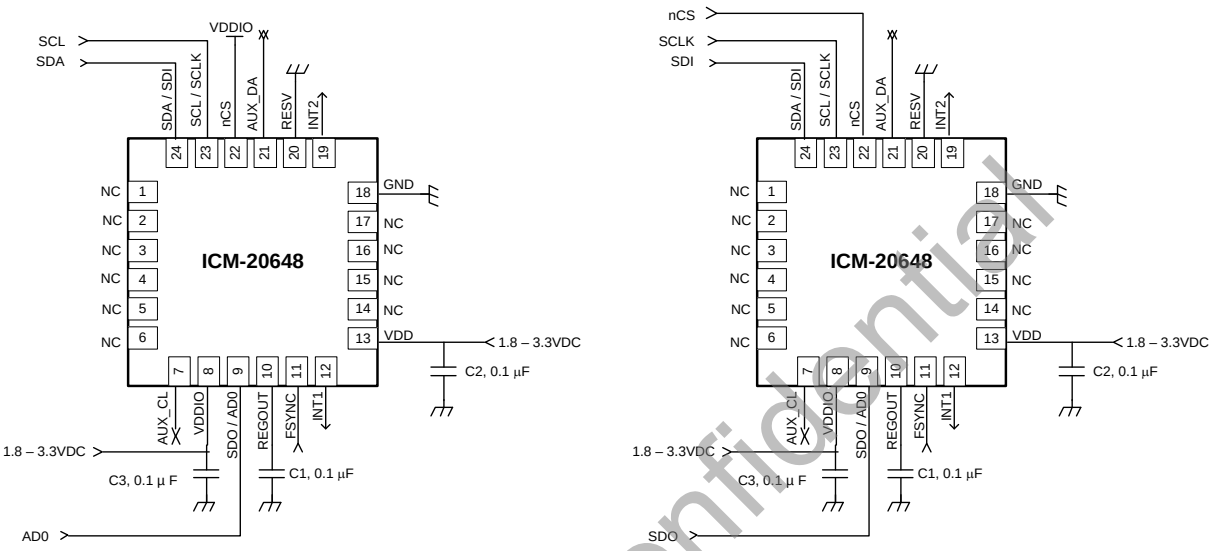


Figure 4 ICM-20648 Application Schematic (a) I2C operation (b) SPI operation

4.3 Bill of Materials for External Components

Component	Label	Specification	Quantity
Regulator Filter Capacitor	C1	Ceramic, X7R, 0.1µF ±10%, 2V	1
VDD Bypass Capacitor	C2	Ceramic, X7R, 0.1µF ±10%, 4V	1
VDDIO Bypass Capacitor	C3	Ceramic, X7R, 0.1µF ±10%, 4V	1

Table 10 Bill of Materials

4.4 Block Diagram

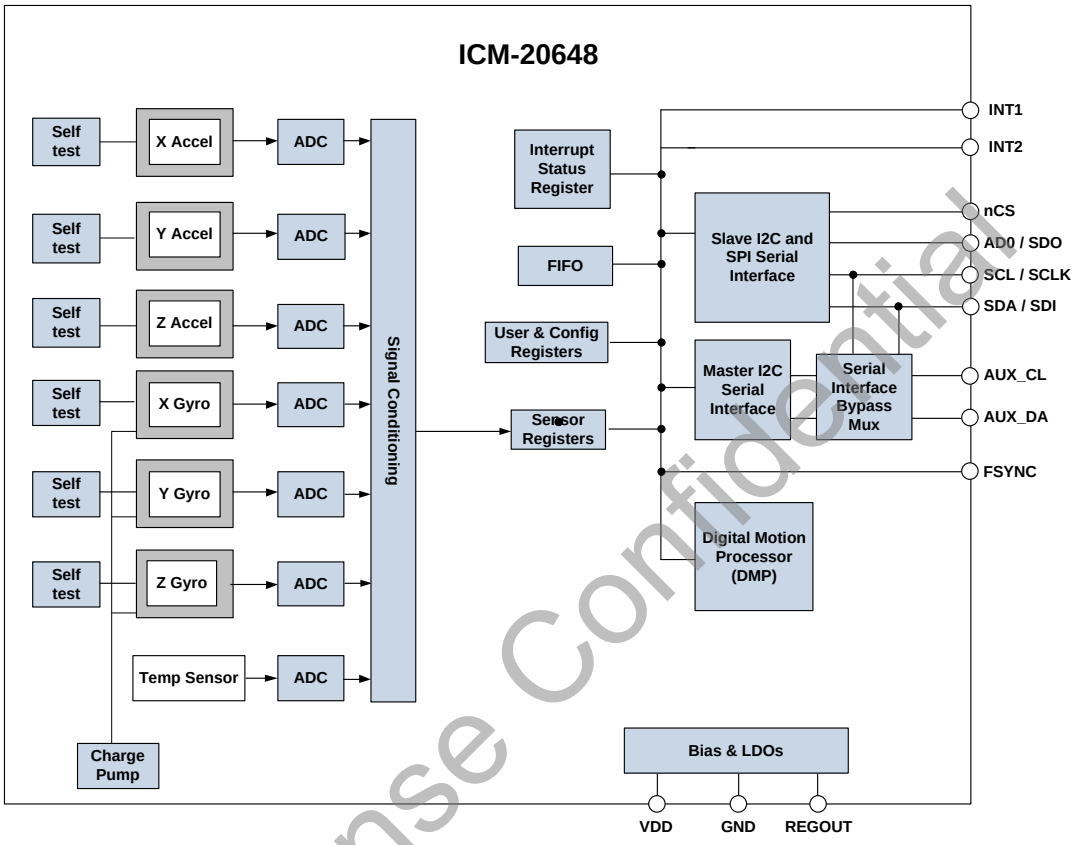


Figure 5 ICM-20648 Block Diagram

4.5 Overview

The ICM-20648 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- Digital Motion Processor (DMP) engine
- Primary I^2C and SPI serial communications interfaces
- Auxiliary I^2C serial interface
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- FSYNC
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Power Modes

4.6 Three-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning

The ICM-20648 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps).

4.7 Three-Axis MEMS Accelerometer with 16-bit ADCs and Signal Conditioning

The ICM-20648's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The ICM-20648's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g*, or ±16*g*.

4.8 Digital Motion Processor

The embedded Digital Motion Processor (DMP) within the ICM-20648 offloads computation of motion processing algorithms from the host processor. The DMP acquires data from accelerometers, gyroscopes, and additional 3rd party sensors such as magnetometers, and processes the data. The resulting data can be read from the FIFO. The DMP has access to the external pins, which can be used for generating interrupts.

The purpose of the DMP is to offload both timing requirements and processing power from the host processor. Typically, motion processing algorithms should be run at a high rate, often around 200Hz, in order to provide accurate results with low latency. This is required even if the application updates at a much lower rate; for example, a low power user interface may update as slowly as 5Hz, but the motion processing should still run at 200Hz. The DMP can be used to minimize power, simplify timing, simplify the software architecture, and save valuable MIPS on the host processor for use in applications.

The DMP is optimized for Android Lollipop support.

4.9 Primary I2C and SPI Serial Communications Interfaces

The ICM-20648 communicates to a system processor using either a SPI or an I²C serial interface. The ICM-20648 always acts as a slave when communicating to the system processor. The LSB of the of the I²C slave address is set by pin 1 (AD0).

4.9.1 ICM-20648 Solution Using I2C Interface

In the figure below, the system processor is an I²C master to the ICM-20648. In addition, the ICM-20648 is an I²C master to the optional external compass sensor. The ICM-20648 has limited capabilities as an I²C Master, and depends on the system processor to manage the initial configuration of any auxiliary sensors. The ICM-20648 has an interface bypass multiplexer, which connects the system processor I²C bus pins 23 and 24 (SCL and SDA) directly to the auxiliary sensor I²C bus pins 7 and 21 (AUX_CL and AUX_DA).

Once the auxiliary sensors have been configured by the system processor, the interface bypass multiplexer should be disabled so that the ICM-20648 auxiliary I²C master can take control of the sensor I²C bus and gather data from the auxiliary sensors.

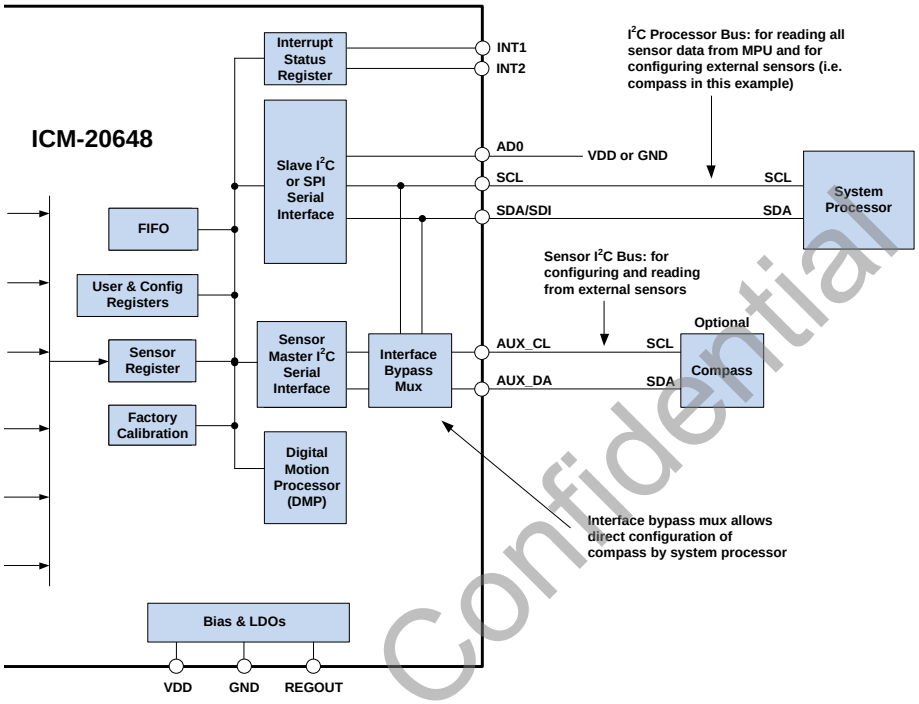


Figure 6 ICM-20648 Solution Using I²C Interface

4.9.2 ICM-20648 Solution Using SPI Interface

In the figure below, the system processor is an SPI master to the ICM-20648. Pins 9, 22, 23, and 24 are used to support the SDO, nCS, SCLK, and SDI signals for SPI communications. Because these SPI pins are shared with the I²C slave pins (9, 23 and 24), the system processor cannot access the auxiliary I²C bus through the interface bypass multiplexer, which connects the processor I²C interface pins to the sensor I²C interface pins. Since the ICM-20648 has limited capabilities as an I²C Master, and depends on the system processor to manage the initial configuration of any auxiliary sensors, another method must be used for programming the sensors on the auxiliary sensor I²C bus pins 7 and 21 (AUX_CL and AUX_DA).

When using SPI communications between the ICM-20648 and the system processor, configuration of devices on the auxiliary I²C sensor bus can be achieved by using I²C Slaves 0-4 to perform read and write transactions on any device and register on the auxiliary I²C bus. The I²C Slave 4 interface can be used to perform only single byte read and write transactions. Once the external sensors have been configured, the ICM-20648 can perform single or multi-byte reads using the sensor I²C bus. The read results from the Slave 0-3 controllers can be written to the FIFO buffer as well as to the external sensor registers.

For further information regarding the control of the ICM-20648's auxiliary I²C interface, please refer to the ICM-20648 Register Map and Register Descriptions document.

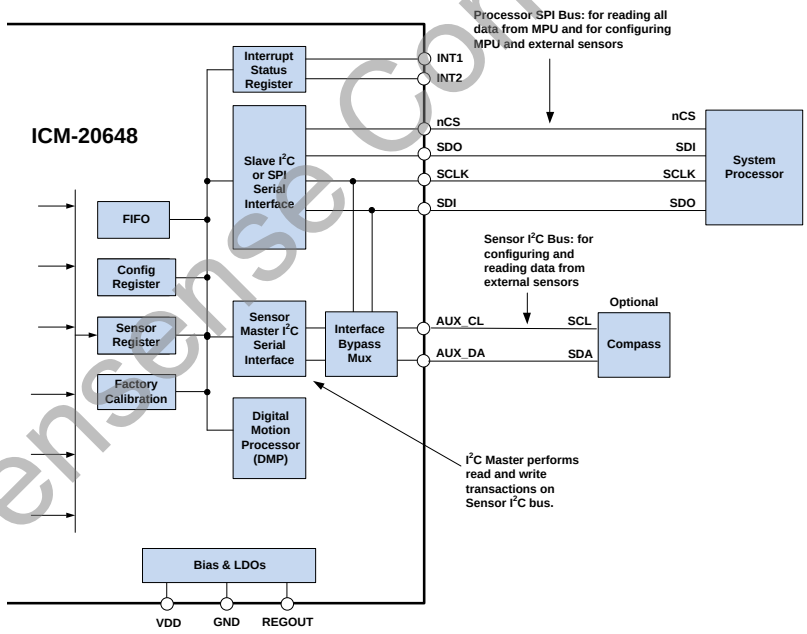


Figure 7 ICM-20648 Solution Using SPI Interface

4.10 Auxiliary I2C Serial Interface

The ICM-20648 has an auxiliary I²C bus for communicating to an off-chip 3-Axis digital output magnetometer or other sensors. This bus has two operating modes:

- I²C Master Mode: The ICM-20648 acts as a master to any external sensors connected to the auxiliary I²C bus
- Pass-Through Mode: The ICM-20648 directly connects the primary and auxiliary I²C buses together, allowing the system processor to directly communicate with any external sensors.

Auxiliary I²C Bus Modes of Operation:

- I²C Master Mode: Allows the ICM-20648 to directly access the data registers of external digital sensors, such as a magnetometer. In this mode, the ICM-20648 directly obtains data from auxiliary sensors without intervention from the system applications processor.

  For example, in I²C Master mode, the ICM-20648 can be configured to perform burst reads, returning the following data from a magnetometer:

  - X magnetometer data (2 bytes)
  - Y magnetometer data (2 bytes)
  - Z magnetometer data (2 bytes)

  The I²C Master can be configured to read up to 24 bytes from up to 4 auxiliary sensors. A fifth sensor can be configured to work single byte read/write mode.

- Pass-Through Mode: Allows an external system processor to act as master and directly communicate to the external sensors connected to the auxiliary I²C bus pins (AUX_DA and AUX_CL). In this mode, the auxiliary I²C bus control logic (3rd party sensor interface block) of the ICM-20648 is disabled, and the auxiliary I²C pins AUX_CL and AUX_DA (pins 7 and 21) are connected to the main I²C bus (Pins 23 and 24) through analog switches internally. Pass-Through mode is useful for configuring the external sensors.

4.11 Self-Test

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers.

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output without self-test enabled

The self-test response for each gyroscope axis is defined in the gyroscope specification table, while that for each accelerometer axis is defined in the accelerometer specification table.

When the value of the self-test response is within the specified min/max limits, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test. It is recommended to use InvenSense MotionApps software for executing self-test.

4.12 Clocking

The internal system clock sources include: (1) an internal relaxation oscillator, and (2) a PLL with MEMS gyroscope oscillator as the reference clock. With the recommended clock selection setting (CLKSEL = 1), the best clock source for optimum sensor performance and power consumption will be automatically selected based on the power mode. Specifically, the internal relaxation oscillator will be selected when operating in accelerometer only mode, while the PLL will be selected whenever gyroscope is on, which includes gyroscope and 6-axis modes.

As clock accuracy is critical to the preciseness of distance and angle calculations performed by DMP, it should be noted that the internal relaxation oscillator and PLL show different performances in some aspects. The internal relaxation oscillator is trimmed to have a consistent operating frequency at room temperature, while the PLL clock frequency varies from part to part. The PLL frequency deviation from the nominal value in percentage is captured in register TIMEBASE_CORRECTION_PLL (detailed in section 12.5), and users can

factor it in during distance and angle calculations to not sacrifice accuracy. Other than that, PLL has better frequency stability and lower frequency variation over temperature than the internal relaxation oscillator.

4.13 Sensor Data Registers

The sensor data registers contain the latest gyro, accelerometer, auxiliary sensor, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.14 FIFO

The ICM-20648 contains a FIFO of size 512 bytes (FIFO size will vary depending on DMP feature-set) that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, accelerometer data, temperature readings, auxiliary sensor readings, and FSYNC input.

A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

For further information regarding the FIFO, please refer to the ICM-20648 Register Map and Register Descriptions document.

4.15 FSYNC

The FSYNC pin can be used from an external interrupt source to wake up the device from sleep. It is particularly useful in EIS applications to synchronize the gyroscope ODR with external inputs from an imaging sensor. Connecting the VSYNC or HSYNC pin of the image sensor subsystem to FSYNC on ICM-20648 allows timing synchronization between the two otherwise unconnected subsystems.

An FSYNC_ODR delay time register is used to capture the delay between an FSYNC pulse and the very next gyroscope data ready pulse.

4.16 Interrupts

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pins configuration, the interrupt latching and clearing method, and triggers for the interrupt. Section 5 provides a summary of interrupt sources. The ICM-20648 includes two interrupt pins, INT1 and INT2. Certain DMP based interrupts are mapped to INT2 while all other interrupts are mapped to INT1. The interrupt status can be read from the Interrupt Status register.

For further information regarding interrupts, please refer to the ICM-20648 Register Map and Register Descriptions document.

4.17 Digital-Output Temperature Sensor

An on-chip temperature sensor and ADC are used to measure the ICM-20648 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.18 Bias and LDOs

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-20648. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.19 Charge Pump

An on-chip charge pump generates the high voltage required for the MEMS oscillators.

4.20 Power Modes

The following table lists the user-accessible power modes for ICM-20648.

Mode	Name	Gyro	Accel	DMP
1	Sleep Mode	Off	Off	Off
2	Accelerometer Mode	Off	Low-Noise or Duty-Cycled	Duty-Cycled or Off
3	Gyroscope Mode	Low-Noise or Duty-Cycled	Off	Duty-Cycled or Off
4	6-Axis Mode	Low-Noise or Duty-Cycled	Low-Noise or Duty-Cycled	Duty-Cycled or Off
5	DMP only mode	Off	Off	Duty-Cycled

Table 11 Power Modes for ICM-20648

Notes:

1. The standard mode of gyroscope and accelerometer operation is duty-cycled

5 Programmable Interrupts

The ICM-20648 has a programmable interrupt system which can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually. The following table lists the interrupt sources and which interrupt may propagate to which pin.

Interrupt Source	Interrupt Pin
DMP Interrupt	INT1/INT2
Wake on Motion Interrupt	INT1
PLL RDY Interrupt	INT1
I2C Master Interrupt	INT1
Raw Data Ready Interrupt	INT1
FIFO Overflow Interrupt	INT1
FIFO Watermark Interrupt	INT1

Table 12 Table of Interrupt Sources

For information regarding interrupt registers, please refer to the ICM-20648 Register Map and Register Descriptions document.

6 Digital Interface

6.1 I2C and SPI Serial Interfaces

The internal registers and memory of the ICM-20648 can be accessed using either I²C at 400 kHz or SPI at 7MHz. SPI operates in four-wire mode.

Pin Number	Pin Name	Pin Description
9	AD0 / SDO	I²C Slave Address LSB (AD0); SPI serial data output (SDO)
22	nCS	Chip select (SPI mode only)
23	SCL / SCLK	I²C serial clock (SCL); SPI serial clock (SCLK)
24	SDA / SDI	I²C serial data (SDA); SPI serial data input (SDI)

Table 13 Serial Interface

Note:

To prevent switching into I²C mode when using SPI, the I²C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in Section 6.3.

For further information regarding the *I2C_IF_DIS* bit, please refer to the ICM-20648 Register Map and Register Descriptions document.

6.2 I2C Interface

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-20648 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the ICM-20648 is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin AD0. This allows two ICM-20648s to be connected to the same I²C bus. When used in this configuration, the address of the one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high).

6.3 I2C Communications Protocol

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

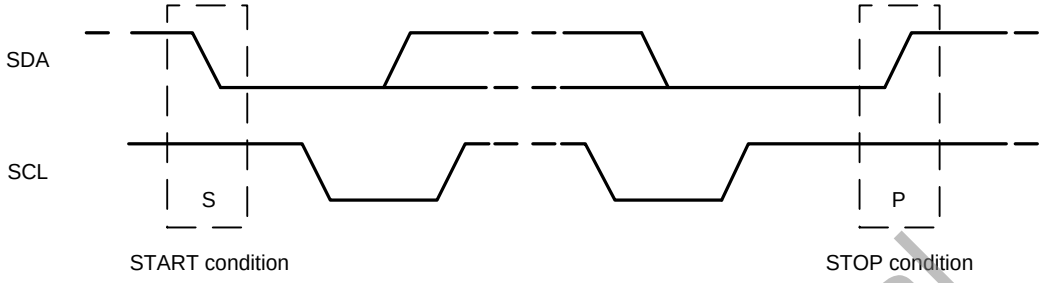


Figure 8 START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

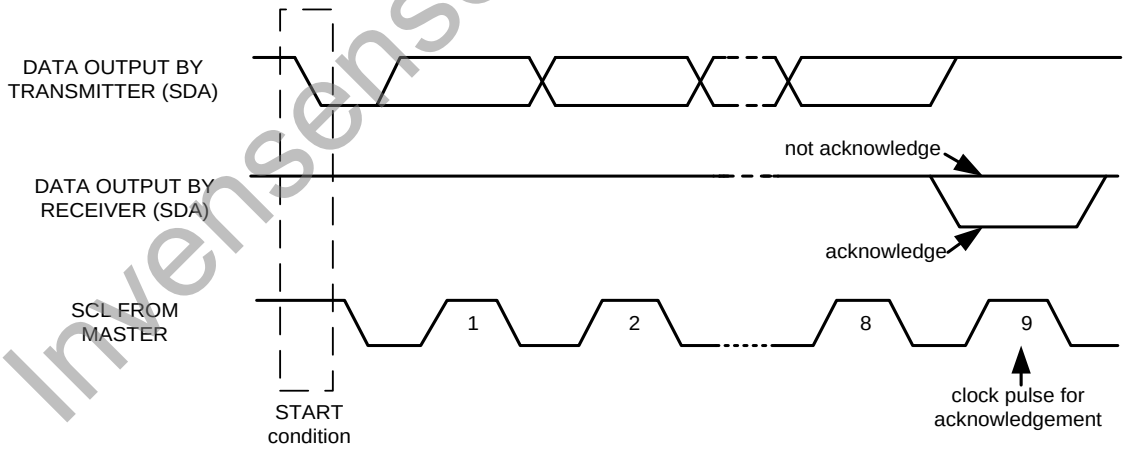


Figure 9 Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

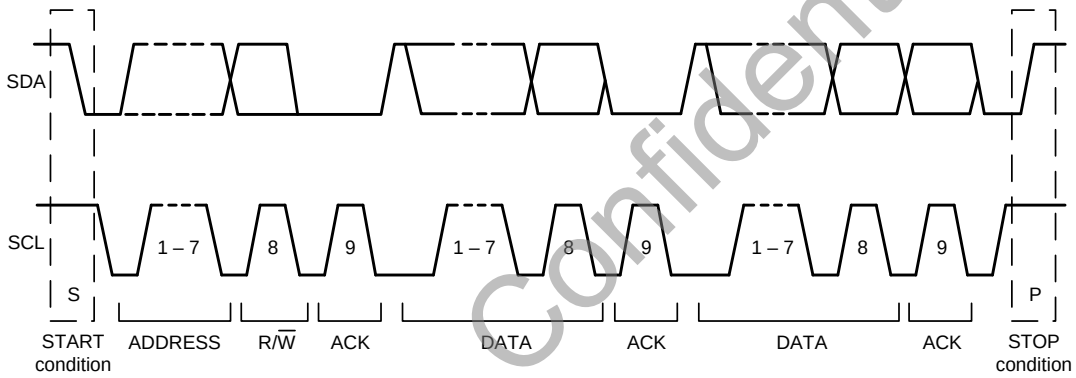


Figure 10 Complete I²C Data Transfer

To write the internal ICM-20648 registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICM-20648 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICM-20648 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICM-20648 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ICM-20648 registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICM-20648, the master transmits a start signal followed by the slave address and read bit. As a result, the ICM-20648 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

6.4 I²C Terms

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	ICM-20648 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 14 I²C Terms

6.5 SPI Interface

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The ICM-20648 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO) and the Serial Data Input (SDI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 7MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

SPI Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

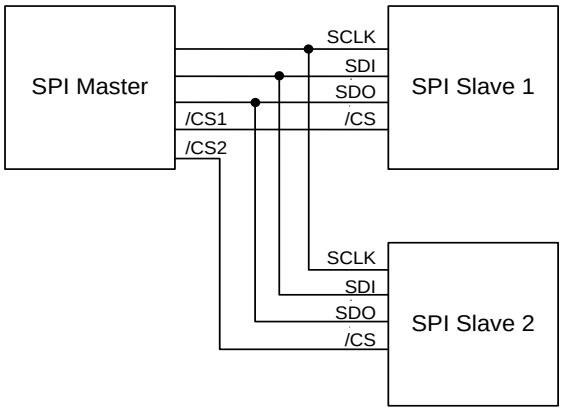


Figure 11 Typical SPI Master / Slave Configuration

7 Orientation of Axes

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (⍰) in the figure.

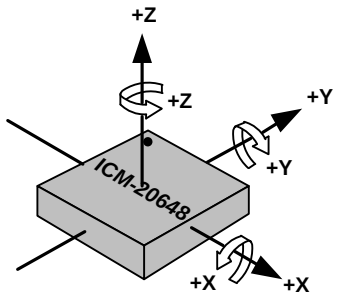
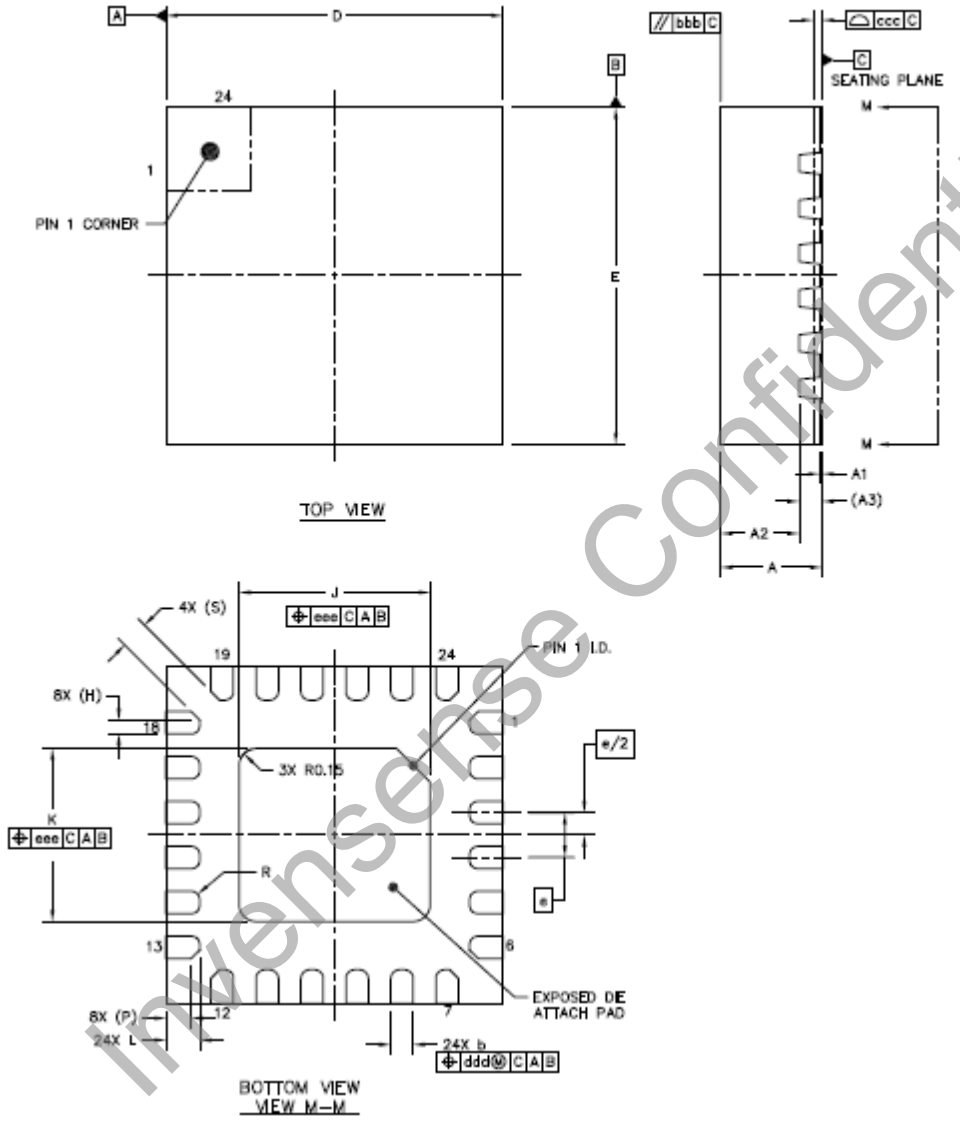


Figure 12 Orientation of Axes of Sensitivity and Polarity of Rotation

8 Package Dimensions

This section provides package dimensions for the device. Information for the 24 Lead QFN 3.0x3.0x0.9 package is below.

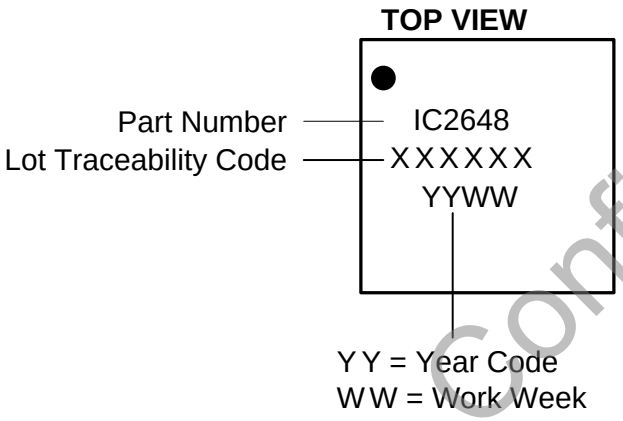


	Symbol	MIN.	NOM.	MAX.
Total Thickness	A	0.85	0.90	0.95
Stand Off	A1	0.00	0.02	0.05
Mold Thickness	A2	---	0.70	---
L/F Thickness	A3		0.203 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D	2.90	3.00	3.10
	E	2.90	3.00	3.10
Lead Pitch	e		0.40 BSC	
EP Size	J	1.65	1.70	1.75
	K	1.49	1.54	1.59
Lead Length	L	0.25	0.30	0.35
	S		0.25 REF	
	R	0.075	---	---
	H		0.12 REF	
	P		0.22 REF	
Mold Flatness	bbb		0.10	
Coplanarity	ccc		0.075	
Lead Offset	ddd		0.10	
Exposed Pad Offset	eee		0.10	

9 Part Number Part Markings

The part number part markings for ICM-20648 devices are summarized below:

Part Number	Part Number Part Marking
ICM-20648	IC2648



10 Use Notes

10.1 Gyroscope Mode Transition

When gyroscope is transitioning from standard to low-noise mode, several unsettled output samples will be observed at the gyroscope output due to filter switching and settling. The number of unsettled gyroscope output samples depends on the filter and ODR settings.

10.2 Power Management 1 Register Setting

CLKSEL[2:0] has to be set to 001 to achieve the datasheet performance.

10.3 DMP Memory Access

Reading/writing DMP memory and FIFO through I2C in a multithreaded environment can cause wrong data being read. To avoid the issue, one may use SPI instead of I2C, or use I2C with mutexes.

10.4 Time Base Correction

The system clock frequency at room temperature in gyroscope mode and 6-Axis mode varies from part to part, and the clock rates specified in datasheet are the nominal values. The percentage of frequency deviation from the nominal values for each part is logged in register TIMEBASE_CORRECTION_PLL, and the range of the code is +/- 10% with each LSB representing a step of 0.079%. For example, if on one part TIMEBASE_CORRECTION_PLL = 0x0C = d'12, it means the clock frequency in gyroscope mode and 6-Axis mode is ~0.94% faster than the nominal value.

When operating in accelerometer-only mode, the system clock frequency at room temperature is the nominal frequency over parts, and it is independent of the value stored in TIMEBASE_CORRECTION_PLL register.

10.5 I²C Master Clock Frequency

I²C master clock frequency can be set by register I2C_MST_CLK as shown in the table below. Due to temperature variation and part to part variation of system clock frequency in different power modes, I2C_MST_CLK should be set such that in all conditions the clock frequency will not exceed what a slave device can support. To achieve a targeted clock frequency of 400 kHz, MAX, it is recommended to set I2C_MST_CLK = 7 (345.6 kHz / 46.67% duty cycle).

I2C_MST_CLK	Nominal CLK Frequency [kHz]	Duty Cycle
0	370.29	50.00%
1	-	-
2	370.29	50.00%
3	432.00	50.00%
4	370.29	42.86%
5	370.29	50.00%

6	345.60	40.00%
7	345.60	46.67%
8	304.94	47.06%
9	432.00	50.00%
10	432.00	41.67%
11	432.00	41.67%
12	471.27	45.45%
13	432.00	50.00%
14	345.60	46.67%
15	345.60	46.67%

10.6 Clocking

The internal system clock sources include: (1) an internal relaxation oscillator, and (2) a PLL with MEMS gyroscope oscillator as the reference clock. With the recommended clock selection setting (CLKSEL = 1), the best clock source for optimum sensor performance and power consumption will be automatically selected based on the power mode. Specifically, the internal relaxation oscillator will be selected when operating in accelerometer only mode, while the PLL will be selected whenever gyroscope is on, which includes gyroscope and 6-axis modes.

As clock accuracy is critical to the preciseness of distance and angle calculations performed by DMP, it should be noted that the internal relaxation oscillator and PLL show different performances in some aspects. The internal relaxation oscillator is trimmed to have a consistent operating frequency at room temperature, while the PLL clock frequency varies from part to part. The PLL frequency deviation from the nominal value in percentage is captured in register TIMEBASE_CORRECTION_PLL, and users can factor it in during distance and angle calculations to not sacrifice accuracy. Other than that, PLL has better frequency stability and lower frequency variation over temperature than the internal relaxation oscillator.

10.7 LP_EN Bit-Field Usage

The LP_EN bit-field (User Bank 0, PWR_MGMT_1 register, bit [5] helps to reduce the digital current. The recommended setting for this bit-field is 1 to achieve the lowest possible current. However when LP_EN is set to 1, user may not be able to write to the following registers. If it is desired to write to registers in this list, it is recommended to first set LP_EN=0, write the desired register(s), then set LP_EN=1 again:

- USER BANK 0: All registers except LP_CONFIG, PWR_MGMT_1, PWR_MGMT_2, INT_PIN_CFG, INT_ENABLE, FIFO_COUNTH, FIFO_COUNTL, FIFO_R_W, FIFO_CFG, REG_BANK_SEL
- USER BANK 1: All registers except REG_BANK_SEL
- USER BANK 2: All registers except REG_BANK_SEL
- USER BANK 3: All registers except REG_BANK_SEL

10.8 Register Access Using SPI Interface

Using the SPI interface, when the AP/user disables the gyroscope sensor (User Bank 0, PWR_MGMT_2 register, bits [2:0]=111) as part of a sequence of register read or write commands, the AP/user will be required to subsequently wait 22µs prior to any of the following operations:

(1) Writing to any of the following registers:
- USER BANK 0: All registers except LP_CONFIG, PWR_MGMT_1, PWR_MGMT_2, INT_PIN_CFG, INT_ENABLE, FIFO_COUNTH, FIFO_COUNTL, FIFO_R_W, FIFO_CFG, REG_BANK_SEL
- USER BANK 1: All registers except REG_BANK_SEL
- USER BANK 2: All registers except REG_BANK_SEL
- USER BANK 3: All registers except REG_BANK_SEL

(2) Reading data from FIFO
(3) Reading from memory

11 References

Please refer to "InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)" for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Tape & Reel Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

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